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Sønderskov, Simon Dyhr; Jørgensen, Asger Bjørn; Maarbjerg, Anders Eggert ; Frederiksen, Kristian Linding; Munk-Nielsen, Stig; Beczkowski, Szymon; Uhrenfeldt, Christian

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Test Bench for Thermal Cycling of 10 kV Silicon Carbide Power Modules

S. D. Sønderskov[(1)], A. B. Jørgensen[(1)], A. E. Maarbjerg[(1)], K. L. Frederiksen[(1)], S. Munk-Nielsen[(2)], S. Bęczkowski[(2)], C. Uhrenfeldt[(2)]

[(1)]School of Engineering and Science
Aalborg University
9100 Aalborg, Denmark
Email: sdsa11@student.aau.dk
URL: http://www.ses.aau.dk

[(2)]Department of Energy Technology
Aalborg University
9100 Aalborg, Denmark
Email: smn@et.aau.dk
URL: http://www.et.aau.dk

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Keywords

≪Silicon Carbide (SiC)≫, ≪Power cycling≫, ≪Reliability≫

Abstract

This paper presents a test bench for lifetime investigation of 10 kV silicon carbide power modules. The test bench subjects high voltage switching operation to the modules while power cycling. Thus both a thermal and electrical operating point is emulated. The power cycling setup features offline measurement of on-state voltages and direct real-time measurement of die surface temperatures, enabled by fiber optical sensors, which are built into the power modules. A thermal model of the module prototypes, based on the temperature measurements, is established. Independent verification steps have been made to validate the performance of the on-state voltage measurement and the thermal model. Issues are revealed in the form of common mode currents in gate drive supply, which should be remedied. Finally a new operating point for power cycling is suggested to better stress the power modules.

Introduction

Silicon carbide (SiC) devices present a number of advantages in high power converter applications compared to conventional silicon (Si) technology. Some inherent properties are higher blocking voltage and faster switching transients. However the research in SiC reliability is limited compared to the well studied Si technology. For example the failure mechanisms of Si power modules are well known and the most common failure mechanisms are bond wire lift-off and solder degradation [1]. The failure mechanisms of SiC is, on the other hand, still an unknown. The high voltage and fast switching properties of the material might cause different failure mechanisms in the power modules. [2], [3], [4]

This paper presents the construction of a test bench, which can power cycle 10 kV SiC power modules at realistic operating voltages and currents, i.e. thermal cycling is obtained through both conduction and switching loss in the semiconductor devices. The test bench features a gate driver, designed for high isolation and low capacitive paracitics and an on-state voltage measurement circuit for state of health monitoring.

Power Modules

The power modules, that are treated in this paper are half bridge modules containing 10 kV, 10 A CREE MOSFETs and anti-parallel JBS diodes. The power modules are packaged at Aalborg university, which means that there is access to every step of the packaging process. This has allowed for mounting a fiber optic temperature probe on the surface of the die inside the power module. This probe is used in the verification of the test bench and when constructing the thermal model. The power module is shown in Fig. 1.

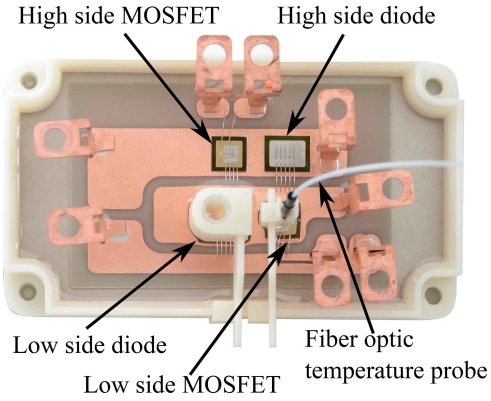

Fig. 1: Half bridge power module prototype.

Test Bench

The concept of the test bench is depicted in Fig. 2. Power cycling is obtained by generating PWM sinusoidal voltage waveforms on each of the converter leg outputs, which are connected through an inductive load. The voltage of the left module is controlled in open loop. The voltage reference of the right module is generated by a PI controller which uses a feedback measurement of the load current, i_{L}. This configuration means that the voltage and current can be controlled to a desired amplitude and phase.

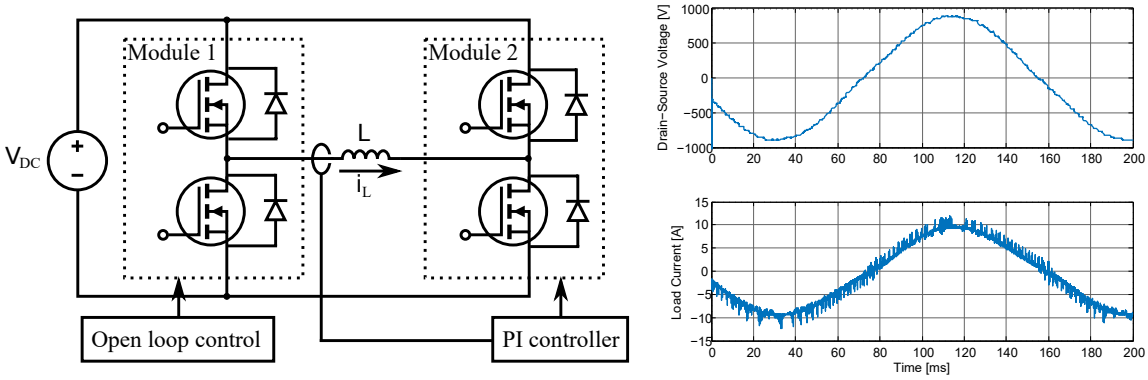

Fig. 2: Back-to-back converter used for power cycling. The displayed waveforms are the output voltage and current of module 1. The PWM voltage has been filtered digitally.

The initial operating conditions for accelerated testing of the power modules are given in Table I. The chosen fundamental frequency and load current parameters are based on earlier studies on accelerated testing [5],[6]. For the preliminary tests presented in this paper, the DC-link voltage has been derated compared to the expected nominal voltage of the power modules.

The spikes which are detectable in the load current depicted in Fig. 2 are present due to the capacitive parasitics in the load. For the same reason, the load inductor has been designed for small stray capacitance. The stray capacitance has been measured to be approximately 2 pF.

Table I: Initial power cycling test conditions.

Parameter	Value
DC-link voltage	4000 V
Peak output voltage	920 V
Peak output current	10 A
Output frequency	6 Hz
Switching frequency	20 kHz
Mean temperature of low side MOSFET	89°C

Gate Drive

The design of the gate drive circuit is based on the findings in [7]. The design has been carried out with a high level of electric insulation. Thus, the gate signals are sent optically to the gate drive PCB and power is supplied through DC/DC converters with reinforced insulation. The power supplies are chosen from the commercially available Recom REC3.5-S-DRW/R10 series which is able to isolate DC voltages of up to 10 kV (5 kV continuous) with an isolation capacitance of 20 pF.

This paracitic capacitance leads to unwanted common mode currents from the laboratory power supply to the gate drive as shown in Fig. 4. Therefore a common mode filter (LC) is connected on each of the laboratory supply lines to the ground. The effect of the filter is shown in Fig. 4. Some of the current spikes are attenuated but the common mode currents are still an issue. One solution would be to build a custom switch mode power supply with low capacitive coupling.

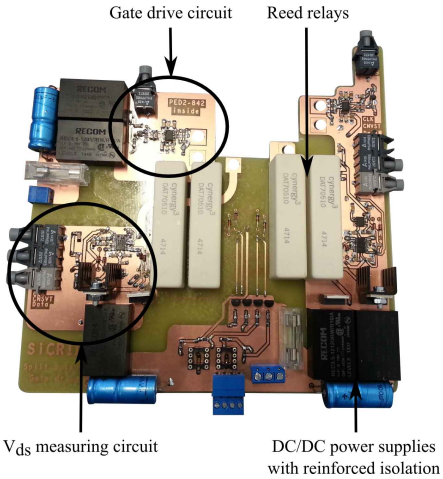

Fig. 3: Gate driver PCB.

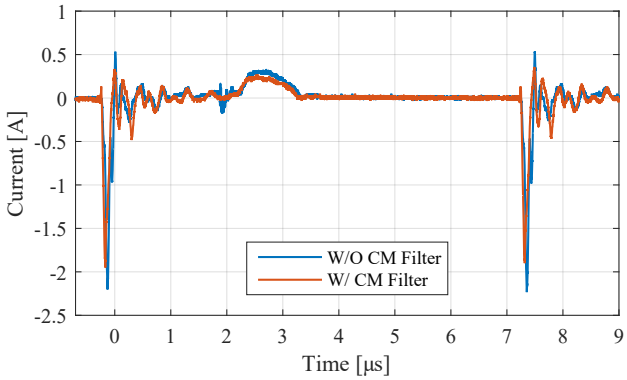

Fig. 4: Common mode current with and without common mode filter

On-State Voltage Measurement

Previous studies show that the on-state resistance of SiC MOSFETs is continuously increasing over time when subjected to thermal cycling [6], [8]. Therefore, a measuring system is needed to monitor the on-state voltage during power cycling of the power modules. The measuring circuit should be capable of blocking the off-state voltage and of measuring the on-state voltage with high accuracy. It is chosen to use an off-line measuring method as presented in [5]. As shown in Fig. 5, the circuit consists of an analog to digital converter (ADC) connected to the positive and negative terminal of the half bridge module through two reed relays. The relays have a blocking voltage of 10 kV. To achieve high measurement accuracy, a 14-bit ADC with an input range of ±10 V is used, corresponding to a resolution of 1.2 mV.

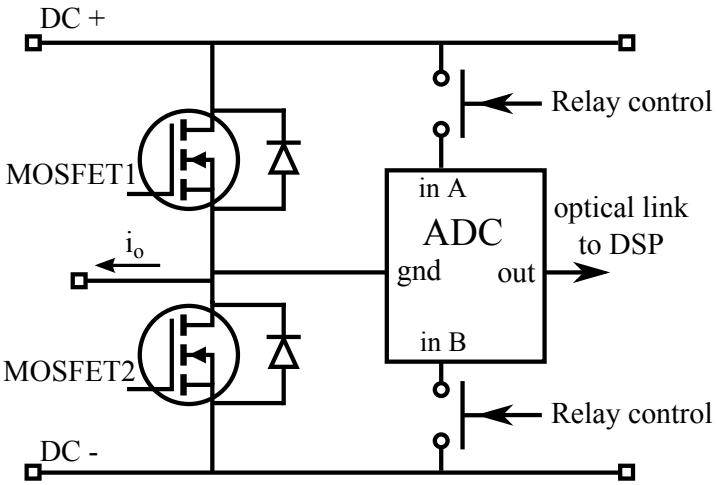

Fig. 5: V_{ds} measuring circuit proposed by [5]

When the MOSFETs or anti parallel diodes are in the conducting state, their corresponding relay is turned on and the on-state voltage is acquired by the ADC. The turn-on time of the reed relays is 3 ms, which is why the power cycling has to be terminated while the measurements are taken.

A measuring routine is conducted while the power cycling is stopped, consisting of three steps. 1) the inductor current is ramped up by turning on the high side MOSFET of one module and the low side MOSFET of the other module, depending on the desired current direction. 2) One MOSFET is turned off while the other remains on. The inductor current is now freewheeling through the MOSFET which is on and the diode in the other module. The on-state voltages are measured for each of the conducting devices. 3) The inductor current is ramped down by turning off all MOSFETs. These steps are repeated for each of the MOSFET and diode pairs.

Temperature Measurement

On each power module, the surface temperatures, T_s of the low side MOSFET and diode are monitored. T_s is measured directly using fiber optic temperature sensors which are positioned on the surface of the bottom SiC die as shown in Fig. 1. The sensors are OTG-M280 from Opsens which are customized for this project and have a response time of approximately 10 ms. A temperature measurement is shown in Fig. 6 which has been conducted under the test conditions stated in Table I.

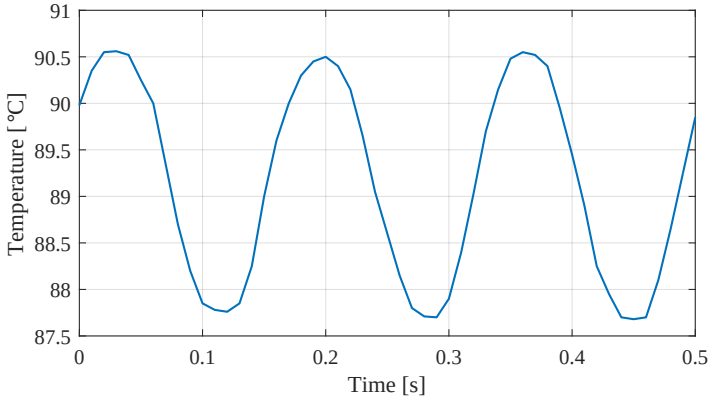

Fig. 6: Surface temperature measurement using OTG-M280

The temperature profile is approximately sinusoidal with an amplitude of 2.9°C and an average value of 89.2°C. The response time of the probe might hide fast fluctuations in the temperature profile.

Thermal Model

A Foster model of the dynamic response of the thermal impedance from the die through the heat sink to the ambient surroundings is made.

A method for obtaining the thermal impedance response of a semiconductor device is suggested in [9]. The method applies DC power dissipation to the device which causes the device to self heat to a steady state temperature. This is followed by a low power state where thermo-sensitive electrical parameters (TSEPs) are measured during cool down. By knowing the DC power level (P_{loss}) and relating the TSEPs to the device surface temperature (T_{s}), the thermal impedance is obtained through

$$Z_{\text{th}}(t) = \frac{T_{\text{s}}(t) - T_{\text{amb}}}{P_{\text{loss}}(t)} \tag{1}$$

where T_{amb} is the ambient temperature.

The temperature probe, which is incorporated into the power module allows for direct measurement of the surface temperature. Therefore this temperature measurement is used instead of the TSEP based junction temperature estimation. This also means that the low power measuring phase of [9] is replaced by an off phase where the MOSFETs are turned off.

A tests was conducted on the low side MOSFET. The current conducted through the device in the first phase of the test was 6 A. The thermal impedance response is depicted in Fig. 7. During the tests the power module was mounted on a heat sink, which is therefore included in the thermal impedance. A fourth order Foster model is fitted data and the parameters are listed in Table II.

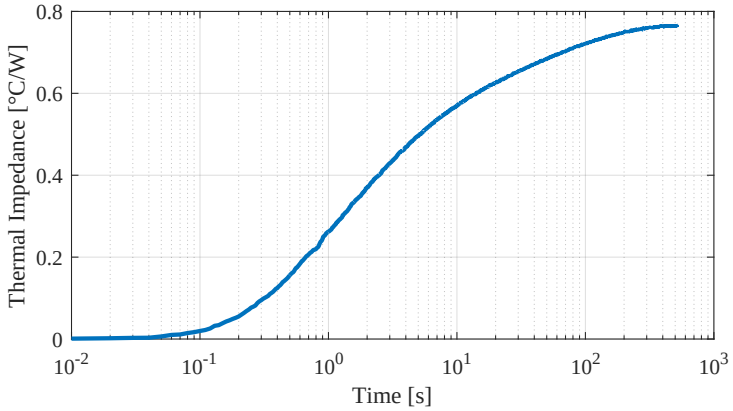

Fig. 7: Thermal impedance response of the low side MOSFET

Table II: Foster model.

	$i=1$	$i=2$	$i=3$	$i=4$
R_i	0.0033	0.3514	0.2383	0.1616
τ_i	0.0100	1.0523	6.1249	56.4831

Test Bench Verification

A number of independent verification steps have been taken to verify the principles and the operation of the test bench.

On-State Voltage Measurement

The on-state voltage measurement accuracy is verified on Si IGBTs in order to spare the SiC prototypes. One purpose of the V_{ds} measurements is to monitor the state of health of the module.

This property is verified by imposing bond wire failures on the IGBT module. Each of the IGBT and diode dies in the module are interconnected by four bond wires. During power cycling the bond wires are cut one after another. The measuring routine is executed with a fixed time interval. The measurements of on-state voltage are shown in Fig. 8. The measurements fluctuate with 10 mV when no bond wires are cut (between 0 and 11,000 cycles), which is more than the measuring accuracy of 1.2 mV. An increase in the average on-state voltage of approximately 3.4 mV is observed when the first bond wire is cut, 25.6 mV for the second bond wire and 47.6 mV for the third bond wire.

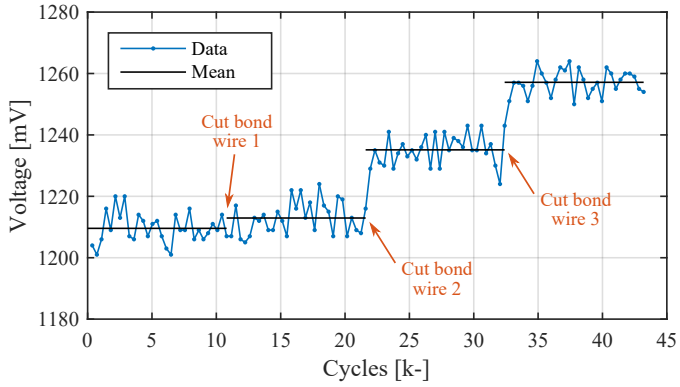

Fig. 8: On-state voltages of low side IGBT for imposed bondwire failuers.

Verification of Thermal Model

The junction temperature is simulated by applying a power input to the thermal model. To verify the model the operating point of Table I is simulated, to make the simulated temperature comparable to Fig. 6. This implies that the power dissipation in this operating point should be known.

One method of deriving these losses are by evaluating the system in steady state. Two assumptions are made to create the model: The average surface temperature is 89.2°C and the ambient temperature is 25°C. These assumptions are based on the power cycling test using the working point given in Table I. The thermal impedance in Fig. 7 approaches steady state at approximately 0.78 $\frac{\mathrm{K}}{\mathrm{W}}$.

From (1) the total power is found to be 82 W, which makes up both the conduction loss and the switching loss, which are given by (2) and (3), respectively.

$$P_{cond} = I^2 R_{\mathrm{ds,on}}(T_{\mathrm{s}}) \tag{2}$$

$$P_{\mathrm{sw}} = (E_{\mathrm{on}} + E_{\mathrm{off}}) f_{\mathrm{s}} \tag{3}$$

Conduction losses

The conduction losses depend on the current and $R_{\mathrm{ds,on}}$. The RMS current during power cycling is $\frac{10}{\sqrt{2}}$ A as shown in Table I. Since $R_{\mathrm{ds,on}}$ depends on the MOSFET surface temperature, a test is conducted to find the $R_{\mathrm{ds,on}} - T_{\mathrm{s}}$ relationship. This is done by placing the module on a heat plate and measuring the on-state voltage and current at different steady state temperatures (Fig. 9). From the results, $R_{\mathrm{ds,on}}$ is estimated to be 0.8 Ω at 89.2°C. Thus the power loss at 89.2°C is calculated from (2) to be 40 W. It is assumed that the two MOSFETs in a half bridge shares the conduction losses equally thus the conduction loss for the lower MOSFET is assumed to be 20 W.

Switching losses

By subtracting the conduction losses from the total power loss the switching losses are estimated to be 62 W. However, to have a more realistic simulation the energy dissipated in each period

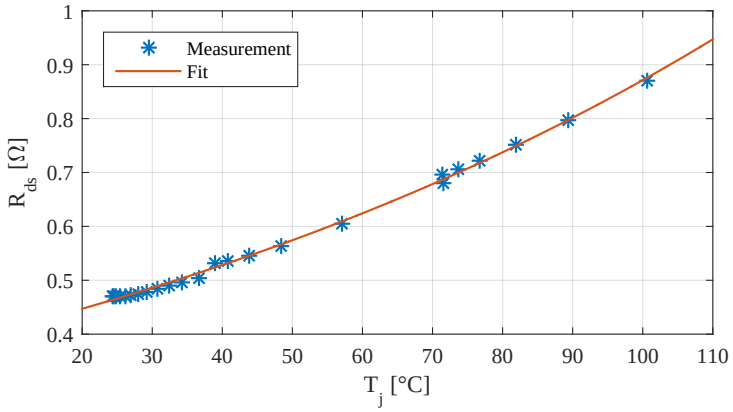

Fig. 9: On-state resistance of low side MOSFET as a function of the surface temperature.

is needed. By using the initial working point frequency of 20 kHz and by rearranging (3) $E_{\text{on}} + E_{\text{off}} = 3.1$ mJ.

Simulation results

By using the derived conduction and switching losses as inputs to the thermal model, the junction temperature response is simulated and compared with the measurements in Fig. 10. The simulated temperature profile is not identical to the measured temperature profile. One explanation is that the temperature probe used for measurements has a response time of 10 ms, hence it can not capture the fast transients of the temperature profile. Also the OTG-M280 probe datasheet states a measuring accuracy of 0.8°C, which might explain the offset between the temperatures.

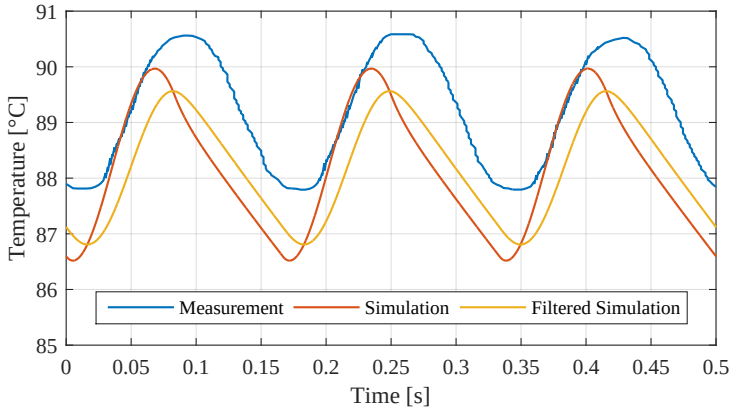

Fig. 10: T_{s} comparison of simulation and measurements.

The system which relates the simulation result to the measured data is estimated to a first order transfer function. The estimated time constant is 17 ms. A low pass filter with this time constant has been applied to the simulation and is included in Fig. 10.

Suggested Operating Point

The initial operating point of Table I causes an average temperature of around 89 °C with swings of approximately 3 °C. The small temperature swings are not suitable for life time testing and a new operating point should be chosen. Simulations show that lowering the fundamental frequency to 1 Hz while maintaining the remaining parameters, increases the temperature swings to 18°C. Reducing the frequency further to 0.5 Hz would result in temperature swings of approximately 34°C. The average temperature in this case is 89°C. The suggested operating point is listed in Table III.

Table III: Suggested power cycling operating point.

Parameter	**Value**
DC-link voltage	4000 V
Peak output voltage	920 V
Peak output current	10 A
Output frequency	0.5 Hz
Switching frequency	20 kHz
Mean temperature of low side MOSFET	89°C

Conclusion

A power cycling setup for 10 kV, 10 A silicon carbide power modules, capable of stress testing the modules at realistic voltage and current levels is constructed. The setup features die surface temperature and on-state voltage measurements. The direct temperature measurement allows for validation and the voltage measurement serves as a state of health indicator.

Test bench verification reveals obstacles in the form of common mode currents, which, which might be solved with a custom made gate drive supply. A thermal model, based on temperature measurements, is used to obtain a suitable operating point for power cycling stress testing.

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