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High Step-Up Y-Source Inverter With Reduced DC-Link Voltage Spikes

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Abstract—Impedance-source inverters using coupled inductors have been investigated as alternatives for providing high step-up voltages. However, leakage inductances of the coupled inductors have commonly led to lower overall effectiveness, in addition to generating high dc-link voltage spikes. The latter raises voltage stresses of switches, which in turn, may reduce the power levels of the inverters. A high step-up Y-source inverter (HS-YSI) has therefore been proposed in this paper to provide a high boost with a smooth dc-link voltage ensured by proper recycling of the leakage energy. These features have been verified by comparing simulation and experimental results of an existing Y-source and the proposed inverters. Factors compared are their respective boost ratios, voltage stresses, current stresses and dc-link voltage spikes.

Index Terms—Impedance-source inverter, Y-source inverters, voltage spikes, leakage and coupled inductances.

I. INTRODUCTION

Traditional voltage-source inverters (VSIs) and current-source inverters (CSIs) have some drawbacks, such as their limited load voltage and/or current ranges, and output distortions due to dead-times or overlap delays. These issues have subsequently led to the development of impedance-source inverters, which can both buck and boost voltages without demanding for dead-times or overlap delays. The most representative of which is the Z-source voltage-type inverter [1], whose two switches from the same phase-leg can be turned on simultaneously for a short shoot-through (ST) duration. It is thus less affected by unintentional short-circuit and waveform distortions, while providing the necessary voltage boost and buck.

Some improvements can however still be introduced to the Z-source inverter, which gradually lead to other developments. One of them is the quasi-Z-source inverter, proposed in [2], for realizing continuous input current. Others can be found in [3]-[7], where the switched-inductor and switched-capacitor techniques have been added for achieving higher gains with the same specified ST duration or duty ratio. However, more inductors or capacitors, and diodes are needed, and hence not so appealing in practice. The same applies to the extended-boost Z-source inverters found in [8]-[11], where more stages have been added for even higher gains.

An attempt to reduce components without compromising gains has then been started, leading to various impedance-source networks with coupled inductors, rather than numerous discrete components [12]-[17]. High voltage gains can now be achieved by altering turns ratios of the coupled inductors, even with only small ST duty ratios used. Despite that, some problems remain, like the sourcing of pulsed input currents, which can obviously be solved by adding inductors and/or capacitors for filtering. An example can be found in Fig. 1, where $L_{in}$ and $C_z$ have been added to the original Y-source inverter with a three-winding coupled inductor ($N_1$, $N_2$ and $N_3$). A gradual start-up and a smoother input current can then be enforced by $L_{esr}$, whose current will continue to flow through $C_z$ whenever $D_1$ blocks. The resulting inverter has hence been referred to as the improved Y-source inverter (I-YSI) [18], [19].

It should however be clarified that pulsed input current is not uniquely related to the coupled inductor, since it has also been experienced by the original Z-source inverter. Rather, the coupled inductor may cause large voltage spikes at the dc-link when currents through its leakage inductances undergo rapid interruptions. This may happen when the inverter switches from ST to non-shoot-through (NST) state and may undesirably lead to higher rated switches needed for realization. It is thus not practical to consider most existing impedance-source inverters with coupled inductors, unless appropriate absorbing circuits are introduced to them for preventing the voltage spikes.

To date, absorbing circuits can either be active or passive,
whose common purpose is to provide a path for the leakage energy to flow. This is important, since regardless of the cores and winding techniques adopted, leakage inductances cannot be nullified completely. An absorbing circuit for continuously recycling the leakage energy to the source or capacitor is thus necessary, which in [20], is implemented by an extra DC-DC buck converter. This solution may however be complex and costly, because of the extra switch, and its accompanied control and driving circuits. Passive absorbing circuits without extra switches have therefore been introduced. Some possible circuits with different types and numbers of extra components are shown in Fig. 2 (in red), where their coupled inductors $L_{couple}$ can have either two or three windings. Their respective operating principles vary slightly, even though their common purpose is to suppress the dc-link voltage spikes.

For instance, the circuit in Fig. 2(a) relies on capacitors and diode for clamping the dc-link voltage [20], but may experience damaging large current drawn from the power source at the instant of entering the ST state. This large current will, in fact, flow through diode $D_S$, capacitor $C_S$, and the shorted phase-leg, before returning to the power source with no limiting inductance in the loop. The current is thus momentarily large and may sometimes damage semiconductor devices unintentionally. A better alternative may then be the second passive absorbing circuit shown in Fig. 2(b) [21], where diode $D_{S2}$ conducts only when voltage of capacitor $C_S$ becomes greater than that of $C_2$. On the other hand, diode $D_{S3}$ conducts only during the transfer from ST to NST state, which together with $C_{S1}$ and $C_1$, will clamp the otherwise spiky dc-link voltage.

The same effect may also be achieved by the simplified absorbing circuit shown in Fig. 2(c) [22], where the conduction of diode $D_3$ connects $C_1$ and $C_2$ in series across the dc-link for limiting its voltage. The main drawback with Fig. 2(c), and also Fig. 2(b), is that their absorbing circuits can only be used with the I-YSI in Fig. 1 or other inverters with the same configuration but different number of coupled windings. Such restriction of usage is even more severe with the absorbing circuit shown in Fig. 2(d), comprising diode $D_S$ and capacitor $C_S$. No doubt, this absorbing circuit has earlier been used with a popular high-efficiency high-step-up converter [23], but its extension to an impedance-source inverter with a coupled inductor is generally not so viable. It is therefore not an option for consideration.

Another technique investigated in [24] is to reorient the three coupled windings shown in Fig. 1 from Y to Δ without introducing an absorbing circuit. The purpose is to lower the equivalent leakage inductances and equivalent series resistances (ESRs) of the windings, but by doing so, the number of turns of the third winding can no longer be decided independently. It is thus no different from a coupled inductor with only two windings, in terms of achievable voltage gains. Moreover, since some leakage inductances still remain, a Δ-connected coupled inductor may not help greatly with the subduing of dc-link voltage spikes, if an absorbing circuit has not been added.

Therefore, in this paper, a more effective absorbing circuit has been proposed for eliminating dc-link voltage spikes and improving the overall boost ability. The proposed circuit consists of two capacitors, one diode and one inductor, which when merged with the I-YSI in Fig. 1, yield a high step-up Y-source inverter (HS-YSI) with low dc-link voltage spikes.

### II. Leakage Effects from Coupled Inductor

In most impedance-source inverters with coupled inductors, leakage inductances may reduce gain, lower efficiency and generate dc-link voltage spikes. The generated voltage spikes may sometimes be larger than the normal dc-link voltage, which certainly, is a critical concern. How and when these spikes are generated should hence be explained first, before describing the proposed HS-YSI. For the explanation, the I-YSI in Fig. 1 is considered. Its equivalent circuits in both ST and NST states are shown in Fig. 3, where leakage inductances (in

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Fig. 2. Illustration of passive absorbing (a) Circuit 1 [20], (b) Circuit 2 [21], (c) Circuit 3 [22], and (d) Circuit 4 [23].

Fig. 3. Equivalent circuits of I-YSI when in (a) ST and (b) NST states.

Fig. 4. High step-up Y-source inverter (HS-YSI).
red) of three windings have been marked as $L_{K3}$, $L_{K2}$ and $L_{K3}$.

Assuming now that the I-YSI is initially in its ST state in Fig.
3(a), its large ST current $i_{K1}$ is then supplied mostly through $N_3$
with $L_{K3}$ in series, since the current through $C_2$ has been limited
by $L_{o3}$ to the filtered input current $I_{in}$. Respective winding currents
through $N_1$, $N_2$ and $N_3$ in the state can also be determined as:

$$i_1 = 0$$

$$i_3 = -i_2 = K \frac{P}{V_{in}}$$

where $K = \frac{N_2 + N_3}{N_1 - N_2}$, and $P$ is the power.

Subsequently, at the instant of crossover to the NST state in
Fig. 3(b), $L_{K3}$ and $C_2$ must instantaneously change to supply the
predetermined inductive load current $I_o$. Unfortunately, both
$L_{K3}$ and $C_2$ do not permit instantaneous changes, since current
through $C_2$ comes from $L_{o3}$ and $L_{K3}$. A mismatch thus occurs,
which will abnormally force the currents through $L_{K1}$ and $L_{K3}$
($L_{K2}$ too according to circuit laws) to change abruptly during the
ST to NST crossover. These give rise to high voltage spikes
throughout the I-YSI, including at its dc-link. Eventually, the
winding currents stabilize to values expressed below in the
NST state.

$$i_3 = \frac{P}{(1-d)V_{in}}$$

$$i_2 = \frac{K d P}{(1-d) V_{in}}$$

where $d$ is the ST duty ratio.

Clearly, a method to solve the problem is to provide an
alternative capacitive path across the dc-link only during the ST
to NST crossover. This method has smoothly been realized by
the proposed HS-YSI, as demonstrated in subsequent sections.

### III. HIGH-STEP-UP Y-SOURCE INVERTER

Fig. 4 shows the proposed HS-YSI with its absorbing circuit
comprising $C_1$, $C_2$, $D_2$ and $L_o$ (in red). Like all impedance-source inverters, it has two board operational modes,
notated as ST and NST, respectively. But, due to leakage
influences from its coupled inductor and the non-ideal of
semiconductor devices, these two operational modes can be
further divided, as explained below.

#### A. Operational Modes

Fig. 5 shows operational modes of the HS-YSI, where the
inverter bridge and ac load have been simplified as a switch $SW$
and a current source $I_o$ in parallel. Response times of the
switches and diodes have also been assumed to be much shorter
than consequential inductive and / or capacitive transitional
times. This is especially true, if $C_1$, $C_2$, $C_3$, and $C_o$ and $L_{o3}$

![Fig. 5. Operational modes of HS-YSI when in (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, (d) $[t_3, t_4]$, (e) $[t_4, t_5]$, and (f) $[t_5, t_6]$.](image-url)
and \( L_M \) are chosen large enough, so that their respective voltages and currents are almost constant during one switching period. It should however be noted that, unlike the others, \( L_M \) does not represent a discrete inductor. Rather, it represents the equivalent magnetizing inductance of the three-winding coupled inductor, which in practice, also has a small leakage inductance in series with each winding. There are therefore three small leakage inductances, drawn with red wavy lines in Fig. 5, whose currents are not constant over a switching period. Key waveforms for illustrating them are summarized in Fig. 6, where each switching period has been divided into six intervals to be described next.

1) ST states

\([t_0, t_t]\): Switch \( SW \) begins to turn on at \( t_0 \), but because of leakage inductance of winding \( N_t \), diode \( D_1 \) continues to conduct, while diode \( D_2 \) remains reverse-biased. Voltage across \( SW \), which is also the dc-link voltage, then begins to drop. This causes voltages across the three leakage inductances to change. Moreover, by tracing through the circuit, it has been found that components of current flowing through \( SW \) are all limited by inductances. The turning on of \( SW \) is therefore realized with zero current at \( t_0 \), over this very short semiconductor-switching subinterval.

\([t_t, t_3]\): Voltage across \( SW \) drops to zero, while its current increases significantly. Windings \( N_2 \) and \( N_3 \) are now clamped by voltages of \( C_1 \) and \( C_4 \) in series, while \( N_1 \) and \( N_5 \) are clamped by \( C_2 \), since \( D_1 \) is still conducting. Current through \( D_1 \) is, in fact, falling at a rate mostly determined by its parasitic capacitance resonating with leakage inductance of \( N_1 \).

\([t_3, t_2]\): The final ST state has been entered with both \( D_1 \) and \( D_2 \) reverse-biased. It is the longest among the three ST subintervals, during which, \( L_{11}, L_0 \) and \( L_M \) charge linearly, while \( C_1 \) to \( C_4 \) discharge linearly.

2) NST states

\([t_0, t_3]\): Diodes \( D_1 \) and \( D_2 \) start to conduct. The three leakage inductances can then form resonating meshes with capacitances in the circuit. In total, three meshes can be drawn with windings of the coupled inductor included. They are mesh 1 formed by \( N_2, N_3, C_1 \) and \( C_3 \), mesh 2 formed by \( N_1, N_5 \) and \( C_2 \), and mesh 3 formed by \( N_1, N_2, C_1, L_{in} \) and the input dc source. During this subinterval, the conduction of \( D_2 \) also permits \( C_3 \) and \( C_4 \) to be connected in series for clamping the dc-link voltage across \( SW \). Voltage spikes have hence been intentionally suppressed at ST to NST crossovers.

\([t_3, t_0]\): This is the final NST state entered, after current of \( D_2 \) drops to zero and it begins to block. Meanwhile, \( D_1 \) continues to conduct, which hence permits \( C_2 \) to be connected across \( N_1 \) and \( N_5 \) for clamping their total voltage. Additionally, the dc-link voltage across \( SW \) is no longer solely equal to the combined voltage of \( C_1 \) and \( C_4 \) in series, since it now includes the reverse voltage of \( D_2 \). There will hence be a very small dc-link voltage drop (proven later), after entering this subinterval at \( t_3 \).

B. Current Analysis

To avoid complex current expressions that may not have any analytical value, the equivalent circuits in Fig. 5 have been simplified to those in Fig. 7, where all leakage inductances have been reflected and summed as \( L_K \) in series with \( N_t \). Additionally, since Fig. 5(a) and (d) for representing very short semiconductor-switching subintervals are similar to Fig. 5(f) and (c), they can be ignored, and hence not included in Fig. 7. Fig. 8 then shows simplified key waveforms with only four distinct subintervals and winding currents \( i_1, i_2 \) and \( i_3 \) assumed to change linearly during \([t_s, t_3]\). This figure, like Fig. 6, again shows that the state in Fig. 7(a) is much shorter in duration than the other three states. It is nonetheless included for showing influences caused by leakage inductances. Its circuit expressions have however been omitted from the mathematical analysis, since energies of passive components have hardly changed during such short interval between \([t_0, t_3]\).

Therefore, beginning with Fig. 7(b), where both \( D_1 \) and \( D_2 \)
are blocking, and $SW$ is conducting from $t_2$ to $t_a$, their related current expressions can be obtained as:

$$i_{c1} = -i_3$$  \hspace{1cm} (6)  \\
$$i_{c2} = -I_{o3}$$  \hspace{1cm} (7)  \\
$$i_{c3} = -I_{o4}$$  \hspace{1cm} (8)  \\
$$i_{c4} = -(I_{o1} + i_3)$$  \hspace{1cm} (9)  \\
$$N_3i_1 + (N_3 - N_2)i_3 = 0$$  \hspace{1cm} (10)  \\
i_{03} = -I_{o2}$$  \hspace{1cm} (11)

where (10) and (11) are for relating currents within the coupled inductor. Substituting them into (6) and (9) then yields the following current expressions for $C_1$ and $C_4$.

$$i_{c1} = -\frac{N_1}{N_3 - N_2}I_{o3}$$  \hspace{1cm} (12)  \\
i_{c4} = -I_{o1} - \frac{N_1}{N_3 - N_2}I_{o4}$$  \hspace{1cm} (13)

The capacitor currents will change, after progressing to Fig. 7(c), where both $D_1$ and $D_2$ are conducting, while $SW$ is blocking from $t_4$ to $t_5$. Collectively, they cause currents $i_2$ and $i_4$ to increase linearly without any abrupt step at $t_a$. In contrast, $i_{c4}$ and $i_{c3}$ change abruptly at $t_a$ to:

$$i_{c4} = I_{o3} - I_{o4}$$  \hspace{1cm} (14)  \\
i_{c3} = I_{o1} - I_{o2} + \frac{N_1}{N_3 - N_2}I_{o4}$$  \hspace{1cm} (15)

These capacitor currents will again change, after entering the state in Fig. 7(d), where $D_2$ has stopped conduction, and hence leads to the following new set of current expressions.

$$i_{c3} = -I_{o2}$$  \hspace{1cm} (16)  \\
i_{c4} = I_{o3} - I_{o4}$$  \hspace{1cm} (17)  \\
i_{c1} = i_{c2}$$  \hspace{1cm} (18)  \\
i_1 = I_{o1} + i_{c2}$$  \hspace{1cm} (19)  \\
i_3 = I_{o1} - I_{o2} + i_{c2}$$  \hspace{1cm} (20)  \\
i_5 = I_{o1} + I_{o2} - I_{o4}$$  \hspace{1cm} (21)  \\
N_3i_1 + N_2i_5 + N_3i_3 = 0$$  \hspace{1cm} (22)  \\
i_1 = i_{03} + I_{o2}$$  \hspace{1cm} (23)
where (22) and (23) are for the coupled inductor. These new expressions then yield the following currents through $C_1$ and $C_2$.

\[
i_{c_1} = I_m + I_{L_0} - I_o \quad (24)
\]

\[
i_{c_2} = \frac{(N_5 - N_2)(I_m + I_{L_0} - I_o) + N_1 I_m}{N_3 + N_1} - I_m \quad (25)
\]

Related current expressions for each capacitor can now be current-second integrated over a switching period, as expressed below.

\[
\int_{t_1}^{t} i_{c_1} dt + \int_{t_1}^{t} i_{c_2} dt + \int_{t_1}^{T} i_{c_3} dt = \int_{0}^{t} i_{c_1} dt + \int_{0}^{t} i_{c_2} dt + \int_{0}^{T} i_{c_3} dt + \int_{(t_{a}+\delta t)}^{t_{a}+\delta t} i_{c_3} dt
\]

\[
= 0
\]

where $\alpha \frac{t_{a} - t_5}{T}$ is the proportionality coefficient, $x = 1, 2, 3$ or $4$ is an index for the capacitors, and interval $[t_6, t_7]$ has been omitted.

Eventually, the following current expressions can be derived, from which currents through all components of the impedance network can be computed.

\[
\alpha = \frac{2}{1 + K} (1 - d) \quad (27)
\]

\[
I_{L_0} = \alpha I_o \quad (28)
\]

\[
I_m = \frac{(N_1 + N_3)}{N_1} I_m \quad (29)
\]

\[
I_o = \frac{1 - (2 + K)d}{1 - d} I_o \quad (30)
\]

### C. Voltage Analysis

In terms of voltages, equivalent circuits in Fig. 7(a) and (b) can be analyzed as a single ST state with $SW$ conducting from $t_0$ to $t_6$. The conduction of $SW$, in turn, causes $C_1$ and $C_4$ to be connected in series for clamping $N_2$ and $N_3$ of the coupled inductor. Relevant voltage expressions can thus be written as:

\[
v_{L_0} = (V_{C_1} + V_{C_2}) \frac{N_3}{N_3 - N_2} \quad (31)
\]

\[
v_{L_m} = -V_{C_3} \quad (32)
\]

\[
v_{L_o} = -(V_{C_m} + V_{C_2} + V_{C_4}) \quad (33)
\]

where $V_{C_1}, V_{C_2}, V_{C_3}$ and $V_{C_4}$ are voltages across $C_1, C_2, C_3$ and $C_4$, and $v_{L_0}, v_{L_m}$ and $v_{L_o}$ are voltages across $L_0, L_m$ and $L_o$, respectively.

Upon turning off $SW$, the first NST state entered is shown in Fig. 7(c), where leakage current through $L_k$ starts to increase linearly from $t_4$ to $t_5$. During this time, $N_2$ and $N_3$ are also clamped by $C_1$ and $C_3$ in series, which together with other circuit features, permit voltages across various inductances to be derived as:

\[
v_{L_M} = (V_{C_1} - V_{C_3}) \frac{N_1}{N_1 - N_2} \quad (34)
\]

\[
v_{L_o} = V_{C_4} \quad (35)
\]

\[
v_{L_m} = V_{C_3} - V_{C_2} - V_{m} \quad (36)
\]

\[
v_{L_k} = -(V_{C_1} - V_{C_3}) \frac{N_1 + N_1}{N_1 - N_2} - V_{C_2} \quad (37)
\]

Moreover, since leakage current through $L_k$ increases linearly from zero at $t_4$, its current $i(t_5)$ at $t_5$ can be expressed as:

\[
i(t_5) = 0 + \frac{1}{L_k} \int_{t_4}^{t_{(a+\delta t)}} v_{L_k} dt \quad (38)
\]

which together with (20), (25), (27), (28), (29) and (30), permits voltage across $L_k$ to be derived as:

\[
v_{L_k} = \frac{(1 + K)^2}{(2(1 - d)^2)} I_o L_k \quad (39)
\]

The NST state then changes to Fig. 7(d), in which $N_1, N_3$ and $L_k$ are clamped by $C_2$ during $[t_3, t_4]$, as leakage $L_k$ and magnetizing $L_M$ will hence share $V_{C_2}$ proportionally. These observations permit voltages across various inductances to be expressed as:

\[
v_{L_M} = (V_{C_1} - V_{C_3} + v_{D_2}) \frac{N_1}{N_1 - N_2} \quad (40)
\]

\[
v_{L_o} = V_{C_4} - v_{D_2} \quad (41)
\]

\[
v_{L_m} = V_{C_3} - V_{C_2} - v_{D_2} \quad (42)
\]

\[
v_{L_k} = -V_{C_2} \quad (43)
\]

\[
v_{L_k} = -(V_{C_1} - V_{C_3} + v_{D_2}) \frac{N_1 + N_1}{N_1 - N_2} - V_{C_2} \quad (43)
\]

Moreover, since $L_k \ll L_M, v_{L_k}$ in (43) can be approximated as zero from $t_3$ to $t_4$, and by substituting (37) and (39) into it, voltage across the reverse-biased $D_2$ can be derived as:

\[
v_{D_2} = \frac{(1 + K)^2}{2(1 - d)^2} \frac{K}{T} I_o L_k \quad (44)
\]

Later, by substituting numerical values to it, $v_{D_2}$ can be proven to be very small, and can hence be safely omitted during $[t_3, t_4]$ to simplify the final derived expressions. That causes the voltages across various inductances in Fig. 7(c) and (d) to the same, which can then be applied to derive the following voltage relationship.

\[
(V_{C_3} - V_{C_1}) \frac{N_1 + N_1}{N_1 - N_2} - V_{C_2} = v_{D_2} \frac{N_1 + N_1}{N_1 - N_2} \approx 0 \quad (45)
\]

All derived voltage expressions for each inductor can follow-up to be volt-second integrated over a switching period $T$, in accordance to:

\[
\int_{t_4}^{t_5} v_{L_k} dt + \int_{t_5}^{t_{(a+\delta t)}} v_{L_k} dt = \int_{0}^{t} v_{L_k} dt + \int_{0}^{T} v_{L_k} dt = 0 \quad (46)
\]

where $L_k$ represents $L_M, L_o$ or $L_m$. Performing the integration finally leads to the following voltages across $C_1, C_2, C_3$ and $C_4$.

\[
V_{C_1} = (1 - 2d) B V_{m} \quad (47)
\]

\[
V_{C_2} = d B V_{m} \quad (48)
\]

\[
V_{C_3} = (1 - d) B V_{m} \quad (49)
\]

\[
V_{C_4} = d B V_{m} \quad (50)
\]

where $B = \frac{1}{1 - (2 + K)d}$ is the voltage gain, and $K$ is the
turns ratio of the coupled inductor. A gain higher than that of the original Z-source inverter can thus be obtained by setting $K$ equal or greater than one.

Regardless of that, the dc-link voltage $V_{dc}$ and peak ac output voltage $\hat{v}_o$ of the inverter are always expressed as:

$$V_{dc} = BV_{in}$$ (51)

$$\hat{v}_o = BMV_{in}$$ (52)

where $M$ is the modulation index, which together with $d$, must satisfy:

$$M < 1 - d$$ (53)

$$1 - (2 + K)d > 0$$ (54)

A larger $d$ to obtain a bigger gain will hence limit the maximum of $M$, together with some deterioration of output waveform quality. One method to lower $M$ and raise $V_{dc}$ without compromising gain is to introduce a larger $K$. Alternatively, multiple cascaded absorbing circuits can be introduced. Fig. 9 shows two possible topologies, whose cascaded absorbing circuits (in red) are placed at different locations. Despite that, they can both eliminate dc-link voltage spikes at instants of ST crossovers. In Fig. 9(a), it is ensured by the conduction of $D_n$, which in turn, causes $C_{2n-1}$ and $C_{2n}$ to be in series across the dc-link of the inverter bridge. The same conduction of $D_n$ in Fig. 9(b) also permits $C_1$, $C_{2n}$ and $C_{2n-1}$ to clamp the dc-link voltage. Both inverters in Fig. 9 are therefore effective, and have a common gain, expressed as:

$$B = \frac{1}{1 - (1 + n + K)d}$$ (55)

where $n$ is the number of absorbing circuits cascaded together, which unquestionably, is an additional parameter for tuning the gain of the inverter.

The main disadvantage here is more discrete components, which in practice, should be avoided, if varying $K$ of the coupled inductor can produce the same effect. Thus, the number of cascaded absorbing circuits should be limited. Nonetheless, the gain in (55) is summarized in Table I for comparison with those of the existing impedance-source inverters. In case of HS-YSI, $n$ equals one, which still gives a higher gain than existing impedance-source inverters, if they use the same $K$ and $d$. The same $K$ can, in turn, be realized with different $N_1$: $N_2$: $N_3$ ratios for a three-winding coupled inductor, as seen from Table II. Voltage gains of a few inverters in Table I, namely the YSI, I-YSI and HS-YSI, can be plotted in Fig. 10, where it can be seen that if the three inverters have the same duty cycle, output voltage of the HS-YSI is higher than those of the YSI and I-YSI.

### TABLE I

<table>
<thead>
<tr>
<th>Impedance Network</th>
<th>Gain $B=V_{dc}/V_{in}$</th>
<th>Turns ratio $K$</th>
</tr>
</thead>
<tbody>
<tr>
<td>T- or Trans-Z-source [12][20]</td>
<td>$(N_1+N_2)/N_2$</td>
<td>$(N_1+N_2)/N_2$</td>
</tr>
<tr>
<td>Γ-Z-Source [15]</td>
<td>$(N_1+N_2)/N_2$</td>
<td>$(N_1+N_2)/N_2$</td>
</tr>
<tr>
<td>Y-Source [17]</td>
<td>$(N_1+N_2)/N_2$</td>
<td>$(N_1+N_2)/N_2$</td>
</tr>
<tr>
<td>LCCT-Z-Source [14]</td>
<td>$N_1/N_2$</td>
<td>$N_1/N_2$</td>
</tr>
<tr>
<td>Improved-Trans-Z-source [21]</td>
<td>$(N_1+N_2)/N_2$</td>
<td>$(N_1+N_2)/N_2$</td>
</tr>
<tr>
<td>Improved-Y-source [18]</td>
<td>$(N_1+N_2)/N_2$</td>
<td>$(N_1+N_2)/N_2$</td>
</tr>
<tr>
<td>HS-YSI $(n=1)$</td>
<td>$1/(1-(1+K)d)$</td>
<td>$(N_1+N_2)/N_2$</td>
</tr>
</tbody>
</table>

### TABLE II

<table>
<thead>
<tr>
<th>$K$</th>
<th>Voltage gain $B$</th>
<th>$N_1/N_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>$1/4$ ($1-4d$)</td>
<td>$(1:3)$</td>
</tr>
<tr>
<td>3</td>
<td>$1/5$ ($1-5d$)</td>
<td>$(1:3.7)$</td>
</tr>
<tr>
<td>4</td>
<td>$1/6$ ($1-6d$)</td>
<td>$(2:1.2)$</td>
</tr>
<tr>
<td>5</td>
<td>$1/7$ ($1-7d$)</td>
<td>$(3:1.2)$</td>
</tr>
<tr>
<td>6</td>
<td>$1/8$ ($1-8d$)</td>
<td>$(4:1.2)$</td>
</tr>
<tr>
<td>7</td>
<td>$1/9$ ($1-9d$)</td>
<td>$(5:1.2)$</td>
</tr>
</tbody>
</table>

![Fig. 10. Voltage gains of different YSIs versus duty cycle.](image)

**D. Stresses and Lifetime**

From earlier derivations, expressions for calculating voltage and current stresses experienced by components of the HS-YSI can be extracted and summarized in Table III. Also added to the table are corresponding expressions for the I-YSI in Fig. 1. Both inverters can then be compared under various conditions. For instance, if they have the same gain $B$ and duty ratio $d$, their respective turns ratios must satisfy $K_{I} = 1 + K$, where subscript $c$ has been added for representing the I-YSI. More turns are thus needed by the I-YSI, whose voltage stresses across $C_2$, $C_2$ and $D_i$ are also higher than those of the HS-YSI. The HS-YSI however experiences a high voltage stress across $D_n$, which must hence be sized appropriately.

As for their coupled inductors, maximum currents flowing through $N_1$ and $N_3$ of the HS-YSI are larger than those of the I-YSI, while its current through $N_2$ may either be less than or equal to that of the I-YSI, depending on the values of $K$ and $d$. 

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Despite that, ST current stresses experienced by the switches of the inverter bridges are quite close for both inverters, according to entries for $i_{st}$ in Table III.

As for their lifetimes, a simple comparison may be provided, based on the understanding that lifetime of a system is mainly determined by the component with the shortest lifetime. This component is likely a capacitor in the HS-YSI, since the lifetime of its added diode is always several times higher. Therefore, only the lifetime of the deciding capacitor is assessed, which from [25], may be computed using:

$$LT = L_{T0} \times \left( \frac{V}{V_0} \right)^{-n} \times 2^{\frac{t_0-T}{10}}$$

where $n$ is an exponential index, and $LT$ and $L_{T0}$ are lifetimes under normal usage and testing conditions, respectively. For both conditions, $V$ and $V_0$ represent voltages across the capacitor, and $T$ and $T_0$ represent their temperatures in Kelvin.

By next comparing expressions in Table III, it can be determined that for the I-YSI and HS-YSI, their shoot-through ratios must satisfy $d < d_c$, if their parameters are set as $K = K_c$ and $B = B_c$, where subscript $c$ has been added for notating the 1-YSI. This then leads to capacitor $C_1$ in the HS-YSI shouldering a higher voltage stress and a shorter lifetime according to (56).

The outcome will however change, if parameters of the two inverters are alternatively set to $d = d_c$ and $B = B_c$. Their winding factors must then satisfy $K = K_c - 1$, or in other words, winding factor of the HS-YSI is smaller than that of the I-YSI to attain the same performance. That setting causes capacitor $C_1$ in the I-YSI and capacitor $C_1$ in the HS-YSI to have similarly high voltage stresses. Their lifetimes are therefore comparable. Besides, because the higher voltage stress in the post-stage, the HS-YSIs with multiple cascaded absorbing circuits have shorter lifetimes.

### IV. Extra Power Losses

Additional components found in the HS-YSI will undeniably introduce extra losses. It may thus be necessary to quantify these losses, which are mostly contributed by diode $D_2$ and inductor $L_0$ (losses from capacitors $C_1$ and $C_2$ are comparably less significant). Expressions for computing these losses are hence derived, as presented below.

#### A. Losses from $L_0$

Fig. 11 shows key waveforms of $L_0$, whose losses include hysteresis loss $P_H$ and copper loss $P_{Cu}$. The latter can be calculated using:

$$P_{Cu} = i_{st, rms}^2 R$$

where $R$ is the winding resistance and $i_{st, rms}$ is the root-mean-square current through $L_0$.

Further, since current ripple $\Delta L_0$ of $L_0$ is relatively small, it can be ignored, resulting in $i_{st, rms} \approx I_{Lo}$, where $I_{Lo}$ is the DC component of $I_{Lo}$. Therefore, (57) can be rewritten as:

$$P_{Cu} = I_{Lo}^2 R$$

On the other hand, $P_H$ is caused by the ac component of $I_{Lo}$, which in theory, can be determined using:

$$P_H = a_1 B_{\phi m}^b f^c$$

where $a_1$, $b$, and $c$ are constants determined by curve-fitting of the recorded core losses [26], and $f$ is the applied frequency. The flux density $B_{\phi m}$ may then be calculated from:

$$B_{\phi m} = \frac{\Delta B}{2} + \frac{B_{AC,max} - B_{AC,min}}{2}$$

where $\Delta B$ is the AC flux swing between maximum $B_{AC,max}$ and minimum $B_{AC,min}$.

Since the flux density can further be expressed in terms of magnetizing field $H$, related maximum and minimum of $H$ can preliminarily be obtained from:

$$H_{AC,max} = \frac{N}{I_{Lo}} (I_{Lo} + \Delta I_{Lo})$$

$$H_{AC,min} = \frac{N}{I_{Lo}} (I_{Lo} - \Delta I_{Lo})$$

From (61) and (62), $B_{AC,max}$ and $B_{AC,min}$ can eventually be expressed as:

$$B_{AC,max} = \left[ a_2 + b_1 H_{AC,max} + c_2 H_{AC,max}^2 \right]$$

$$B_{AC,min} = \left[ a_2 + b_1 H_{AC,min} + c_2 H_{AC,min}^2 \right]$$

where $a_2$, $b_2$, $c_2$, $d_2$, $e_2$ and $x$ are magnetization constants determined from appropriate curve-fitting [26].

#### B. Losses from $D_2$

Losses from $D_2$ include conduction loss $P_D$ and reverse recovery loss $P_r$. However, from Fig. 8, it can be seen that current through $D_2$ slowly drops to zero at $t_{sp}$, which
HS-YSI have occurred gradually from all winding current changes through leakage inductances of the drawn in Fig. 8. Most importantly, they have demonstrated that 12 have been found to match well with theoretical waveforms instantaneously at C.

In contrast, $P_t$ is not zero, and can be computed using:

$$P_t = I_R V_{D_s} d$$  \hspace{1cm} (65)

where $I_R$ is the reverse current taken from [27].

Conduction loss $P_f$ can also be calculated using:

$$P_f = \frac{1}{T} \int_{t_1}^{t_2} i_{D_s} V_f dt$$  \hspace{1cm} (66)

where $V_f$ is the forward voltage drop across $D_2$, whose value can be obtained from [27].

**C. Total extra loss from HS-YSI**

With a nominal output power of 200 W, the total extra loss contributed by additional components $L_o$ and $C_4$ of the HS-YSI is:

$$P_{total} = P_{C_4} + P_{D_2} + P_{D_1} + P_f \approx 5.62 \text{ W}$$  \hspace{1cm} (67)

This extra loss cannot be avoided, but by recycling energy from the leakage inductances, energy wasted in switches can be lowered considerably. Moreover, since voltage spikes are fully eliminated at the dc-link, a lower voltage-rated switch with a lower on-resistance can be chosen for lowering the overall power loss.

**V. SIMULATION AND EXPERIMENTAL RESULTS**

Simulations and experiments have been performed with the I-YSI in Fig. 1 and HS-YSI in Fig. 4 using the same parameters listed in Table IV. To boost an input voltage of 80 V to an output voltage of 160 V, ST duty ratios of the I-YSI and HS-YSI have been set 0.15 and 0.12, respectively, since they use the same parameters from Table IV and same modulation index of $M = 0.8$. Their respective theoretical voltages can then be determined as $V_{C1} = 170$ V and $V_{C2} = 90$ V for the I-YSI, and $V_{C1} = 152$ V, $V_{C2} = 72$ V, $V_{C3} = 176$ V and $V_{C4} = 24$ V for the HS-YSI. Their dc-link voltages are however the same at $V_{dc} = 200$ V. Their respectively obtained results are described next.

**A. Simulation Results**

The key current waveforms of the two inverters shown in Fig. 12 have been found to match well with theoretical waveforms drawn in Fig. 8. Most importantly, they have demonstrated that all winding current changes through leakage inductances of the HS-YSI have occurred gradually from $i_s$ to $i_s$, rather than instantaneously at $i_s$, after each ST to NST crossover. Voltage spikes are hence not generated by the proposed HS-YSI.

![Image](image-url)

**B. Experimental Results**

A 200 W prototype controlled by a TMS320F2812 digital signal processor has been built and shown in Fig. 13. It can be configured as either the I-YSI in Fig. 1 or HS-YSI in Fig. 4, using the same parameters provided in Table IV. Its coupled inductor has also been loosely wound to better demonstrate the effects from leakage inductances, as seen from Fig. 14, where dc-link voltages, voltages and currents of diodes are plotted.

![Image](image-url)

**Table IV**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value/Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>80 V</td>
</tr>
<tr>
<td>Load resistance</td>
<td>60 Ω (200 W)</td>
</tr>
<tr>
<td>Capacitances $C_i$ and $C_j$</td>
<td>470 μF</td>
</tr>
<tr>
<td>Capacitances $C_3$ and $C_4$</td>
<td>100 μF</td>
</tr>
<tr>
<td>Inductances $L_o$ and $L_c$</td>
<td>4.3 mH</td>
</tr>
<tr>
<td>Switching frequency $f_{sw}$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>Turns ratio $N_i/N_s/N_t$</td>
<td>40:40:80</td>
</tr>
<tr>
<td>Core</td>
<td>C055863A2</td>
</tr>
<tr>
<td>Switches</td>
<td>IRGP4062DPbF</td>
</tr>
<tr>
<td>Diodes $D_1$ and $D_2$</td>
<td>30EP060PBF</td>
</tr>
<tr>
<td>Filter inductance $L_f$</td>
<td>5.6 mH</td>
</tr>
<tr>
<td>Filter capacitance $C_f$</td>
<td>4.7 μF</td>
</tr>
</tbody>
</table>

![Image](image-url)
Clearly, the dc-link voltage spikes of the I-YSI can reach 530 V, even though its stabilized value is only 194 V. It is thus inferior, as compared to the HS-YSI, whose dc-link voltage of 195 V is nearly free of spikes.

Other key features from waveforms of the HS-YSI in Fig. 14(b) have also been found to match well with those from the theoretical waveforms drawn in Fig. 5. For example, the time duration from $t_4$ to $t_5$ in Fig. 14(b) has been measured as 0.4387, while that in Fig. 8 or from (27) is 0.447, where $T$ is the switching period. Furthermore, from (44) and using parameters from Table IV, $v_{D2}$ has been determined as $2.87 \times 10^4 L_K$ from $t_5$ to $t_0$. Its value is thus only a few mV, since the leakage $L_K$ is usually from 10 nH to 10 μH. It is thus expected to be unnoticeable, as verified by the third trace in Fig. 14(b).

Corresponding dc input and ac output waveforms are then shown in Fig. 15, where double-line-frequency ripples can noticeably be seen from input currents of both inverters [28], [29]. The ripples are however slightly smaller in the HS-YSI, where more passive components are used for filtering. Their peak ac output voltages have also been read as 155 V for both
the I-YSI and the HS-YSI. Both values are smaller than their common theoretical value of 160 V, because of reduction of effective ST duty ratio caused by leakage inductances and ESRs [24]. Other than these, most theoretical and experimental values have been found to match closely, like $V_{C1} = 169$ V and $V_{C2} = 86$ V measured in Fig. 16(a) for the I-YSI, and $V_{C1} = 150$ V, $V_{C2} = 69$ V, $V_{C3} = 176$ V and $V_{C4} = 20$ V from Fig. 16(b) for the HS-YSI.

Follow-up, Fig. 17 shows the winding currents of the coupled inductor, which for the HS-YSI, change more gradually in the NST state, rather than jump abruptly at the considered ST to NST crossover. However, both I-YSI and HS-YSI exhibit oscillatory currents, which may be due to leakage inductances interacting with parasitic capacitances of the semiconductors. Meanwhile, the HS-YSI operating with a higher gain has been tested by increasing its shoot-through duty ratio $d$ to 0.15 with the other parameters kept unchanged. The new boost ratio $B$, theoretical dc-link voltage $V_{dc}$ and output peak voltage computed are thus 4, 320 V and 256 V, respectively. Obtained experimental results are given in Fig. 18, where the read $V_{dc}$ and output peak voltage are 296 V and 235 V, respectively. The output voltage loss is thus $256 - 235 = 21$ V due mainly to leakage of the coupled inductor and equivalent series resistances (ESRs) in the circuit. Especially with ESRs, their effects increase sharply with gain like most boost converters. They thus cause output voltage loss with $B = 4$ to be greater than that with $B = 2.5$. Despite that, voltage spikes at the dc-link for both cases have been suppressed noticeably, as seen from Fig. 14(b) and Fig. 18.

VI. CONCLUSION

In this paper, a high step-up Y-source inverter with a unique absorbing circuit has been proposed for eliminating dc-link voltage spikes without demanding extra switches and compromising the voltage gain. Its gain has, in fact, been improved, when compared with the improved Y-source inverter published recently in the literature. The same absorbing circuit can also be used with other impedance-source...
inverters realized with coupled inductors. It is therefore a universal circuit for removing dc-link voltage spikes, regardless of the number of coupled windings. Simulation and experimental results have verified its effectiveness, when compared with the improved Y-source inverter.

REFERENCES


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