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A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices

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***Abstract*—New packaging solutions and power module structures are required to fully utilize the benefits of emerging commercially available wide bandgap semiconductor devices. Conventional packaging solutions for power levels of a few kilowatt are bulky, meaning important gate driver and measurement circuitry are not properly integrated. This paper presents a fast-switching integrated power module based on gallium nitride enhancement-mode high-electron-mobility transistors, which is easier to manufacture compared with other hybrid structures. The structure of the proposed power module is presented, and the design of its gate driver circuit and board layout structure is discussed. The thermal characteristics of the designed power module are evaluated using COMSOL Multiphysics. An ANSYS Q3D Extractor is used to extract the parasitics of the designed power module, and is included in simulation models of various complexities. The simulation model includes the SPICE model of the gallium nitride devices, and parasitics of components are included by experimentally characterizing them up to 2 GHz. Finally, the designed power module is tested experimentally, and its switching characteristics cohere with the results of the simulation model. The experimental results show a maximum achieved switching transient of 64 V/ns and verify the power loop inductance of 2.65 nH.**

***Index Terms*—Circuit simulation, power semiconductor switches, semiconductor device packaging.**

I. Introduction

POWER electronics is an ever growing industry, used to handle and treat electrical energy in every aspect from production to consumption. Power electronics are used for all power levels, such as in wind turbines, solar panels, industry motor drives, pumps, kitchen appliances, or artificial lighting. In many cases, the electrical energy is handled by switch mode power supplies, in which the semiconductor die is the core unit. Typically, at lower power levels <1 kW, the semiconductor device is directly integrated with other components to form a power supply as a single unit [1]. For higher power levels or systems of higher complexity, the semiconductor devices are often packaged as a power module, which is then just seen as a component of the total power electronic system. In either case, the performance of the semiconductor device is dependent on the interconnection it has with the critical components of the circuit such as gate driver integrated circuits, capacitors, sensors, and other auxiliary circuitry. Furthermore, to ensure reliable and robust operation, it must be ensured that the device is properly cooled, enclosed, and interconnected with other peripherals. New wide bandgap (WBG) semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), offer potential size, efficiency, and performance improvements of power modules used in switch mode power supplies. These materials offer higher breakdown voltage, faster switching speeds, lowered on-resistance, and increased operating temperatures, when compared to silicon [2], [3]. The fast-switching speed of WBG devices produces high dv/dt and di/dt, which may induce ringings and electromagnetic interference issues due to parasitic elements in the packaging [4]. Current power module packaging design for power levels in the kilowatt range is still bulky, which causes difficulty in integration and minimization of parasitic elements in both power and gate driver loop simultaneously [5], [6]. To harvest the benefits of WBG devices, new designs and integration of parts must be studied and tested.

Silicon power modules with base plates are currently the most dominant design, used in approximately 70–80% of all power modules [7]. A typical sectional view of the conventional power module structure is shown in Fig. 1(a). At the bottom is the baseplate, which is mounted to a heat sink to ensure low thermal resistance. A direct bonded copper (DBC) is soldered to the baseplate. The DBC is a sandwich structure with copper on either side of a ceramic substrate, which is an electrically insulating material yet capable of transferring heat efficiently [8]. Encapsulation such as epoxy or silicone gel is used to ensure high electric breakdown strength and protect the semiconductor dies from humidity and contaminants. The entire assembly is enclosed in a plastic housing to mechanically protect the internal structures of the power module. Terminals are mounted on the copper planes, and used to connect the semiconductor with electrical circuits outside the power module. Typically, this control circuitry is soldered on a printed circuit board (PCB) and connected outside of the power module. The benefits of this structure include its high voltage blocking capabilities and high power dissipation [9]. The conventional structure is challenged

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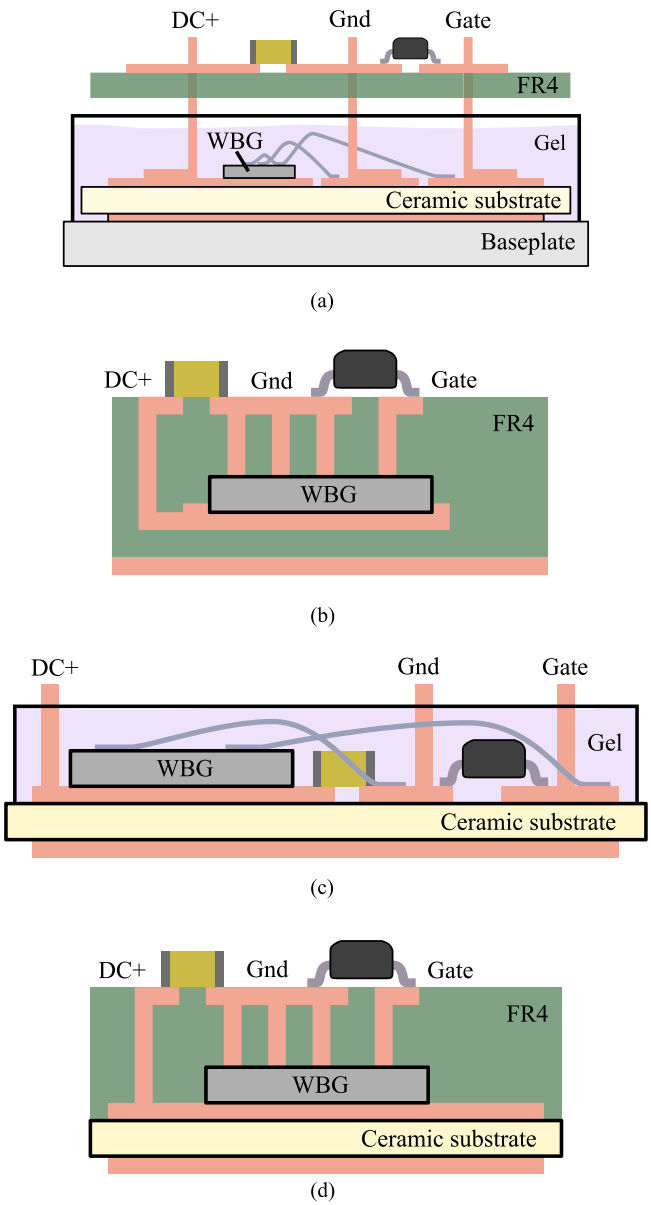

Fig. 1. Packaging technologies. (a) Conventional power module structure. (b) PCB embedded die technology. (c) Integrated DBC power module structure. (d) PCB/DBC hybrid power module structure.

by the emergence of new WBG devices. Due to the terminals and copper planes, a parasitic inductance of typically 10–30 nH [10]–[13] limits the utilization of the increased switching speeds of WBG semiconductors.

A solution is to assemble every part of the switching device into a multilayer PCB, as shown in Fig. 1(b). In this way, the semiconductor die is directly embedded into the PCB, and has copper planes connecting to its peripheral units [14]. This eliminates the use of bond wires. The concept reduces the parasitic inductance in the power loop, reported at 2.8 nH [12]. But, it is hard to achieve both good thermal and electrostatic performance simultaneously [15]. An issue is to dissipate the heat, due to the high thermal resistance of the FR4 material. For high power dissipation levels, larger copper planes and vias reduce thermal impedance by more effectively conducting the heat to the outer layers of the PCB. To further reduce thermal impedance, the FR4 layer is minimized in thickness, which, in turn, causes issues related to high electric field stress. Too high electric field stress causes partial discharges or sparking [16]. Modifications to the geometry allows for some reduction in electric field stress [17], but still restrictions on spacing have to be maintained. In conclusion, embedding everything in a PCB enables low parasitic design, but requires strict compromise between the thermal and electrostatic performance.

TABLE I
COMPARISON OF POWER MODULE STRUCTURES

	Inductance	Thermal	E-field	Manufacture
(a) Conventional	− −	+ +	+ +	+ +
(b) PCB embedded	+ +	−	−	−
(c) DBC integrated	+	+ +	+ +	+
(d) PCB/DBC	+ +	+ +	+	− −

To improve the heat dissipation of the semiconductor device, it is preferred to mount it on a DBC. An idea is to utilize the DBC as much as possible. The most important components such as semiconductor device, gate drivers, and capacitors are soldered directly onto the DBC [6]. The structure is depicted in Fig. 1(c). The power module has good heat dissipation through the ceramic, and high electrostatic performance is maintained by encapsulating the module in silicone gel. The power loop layout is restricted to a single copper layer and achieves loop inductances of 7–11 nH [18]. This technology does not introduce any new steps in terms of manufacturing when compared to the conventional power module. It mainly requires etching of more tracks and soldering of more components. However, as the DBC is limited to only a single layer, it reduces the complexity of circuits that can be incorporated. An attempt to mitigate this issue is to use printed copper thick-film technology on the DBC [13], [19]. This increases the level of integration of the gate driver circuitry, but it is still not as compact as what is achievable using PCB technology.

Power modules using both DBC and PCB technologies reduce the issue of poor heat dissipation, while maintaining the low inductive design. A state-of-the-art power loop inductance of 1.5 nH including current measurement is reported [20]. The solution is to mold the PCB directly on top of the DBC, in which no bond wires are used [21]–[23]. The structure is shown in Fig. 1(d). This structure shows very fast switching speeds of both gate and power loops. However, this solution significantly increases the manufacturing complexity, as the PCB molding is done directly on the DBC. A summary of the four packaging structures shown in Fig. 1 is given in Table I, where positive metrics are given for technologies allowing low inductance, low thermal resistance, high electric field breakdown strength, and low manufacturing complexity.

In this paper, a power module hybrid structure of DBC and PCB is proposed for use with commercially available lateral GaN enhancement-mode high-electron-mobility transistor (eHEMT), which reduces the manufacturing complexity as only

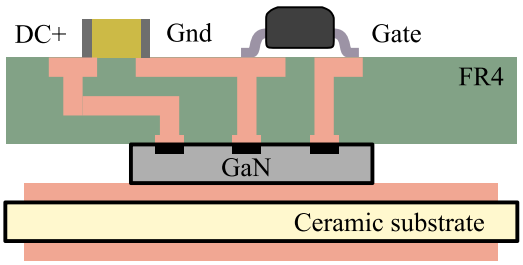

Fig. 2. Proposed DBC/PCB hybrid power module structure for lateral GaN eHEMT devices.

soldering is required for assembly. The structure is used to design a fast-switching integrated GaN eHEMT power module, which focuses on a board layout to simultaneously achieve both fast dv/dt and di/dt switching, as described in Section II. This also requires that the parameters of the gate driver circuit are properly designed. Thermal characteristics of the module are evaluated in Section III. The switching behavior of the designed power module is simulated prior to testing. Due to the compactness of the designed board, it is difficult to measure and verify the operation. Thus, efforts are made to construct a simulation model of high accuracy, to get knowledge of voltages/currents internally on the board. A simulation framework is discussed in Section IV, which includes three different levels of simulation complexity and their influence on the resulting waveforms. Finally, in Section V, the power module is built, and its switching behavior is experimentally validated and compared with the simulation. This paper is concluded in Section VI.

II. Design of Integrated GaN Power Module

New commercially available lateral GaN eHEMT devices have all electrical connections on the top surface, and a solderable bottom surface for heat dissipation [24]. This enables the use of a premanufactured PCB to be stacked on top of the GaN device. A power module structure as shown in Fig. 2 is proposed. This solution offers very low inductance, high power dissipation, and low capacitive coupling. The air gap to the DBC means that traces and planes on the PCB have limited electrical coupling to the DBC and heat sink. A three-dimensional (3-D) model of the stack to be assembled is shown in Fig. 3. At the bottom is an Al_2O_3 DBC substrate. The GaN eHEMT has an exposed metal backside as a heatsink, but is internally connected to source potential. Thus, a pattern is etched on the DBC to isolate each GaN eHEMT device. Additionally, holes are etched underneath each pin for safety, to avoid shorting of the different press-fit pins to DBC. The PCB with all the control and measurement circuitry is soldered on top of the GaN eHEMT. At last, a plastic housing is used to enclose and mechanically protect the power module.

A. Gate Driver

A schematic of the gate driver circuit used for a single half-bridge is shown in Fig. 4. A bootstrap gate driver configuration is used, due to its simplicity and compactness. Using a bootstrap

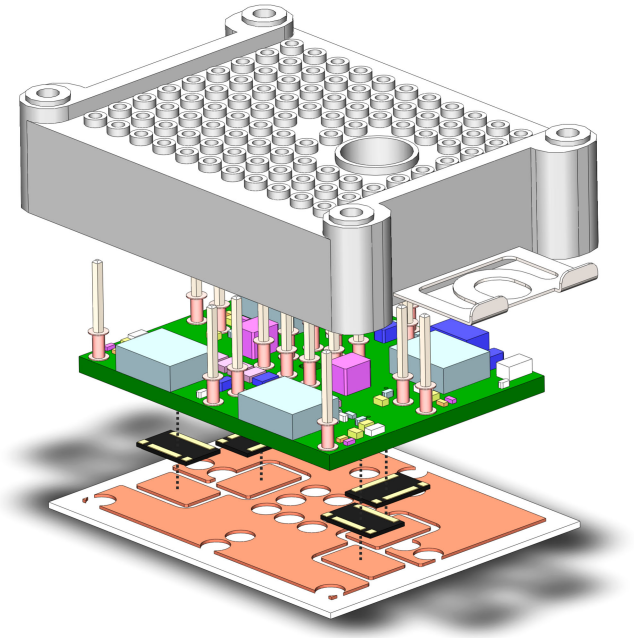

Fig. 3. 3-D rendering of the GaN eHEMT power module stack assembly. DBC dimensions are 36 × 28 mm.

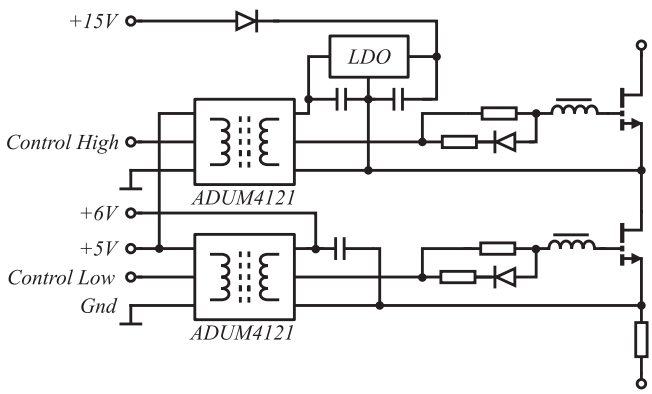

Fig. 4. Schematic of the gate driver and switching circuit for a single half-bridge.

configuration removes the requirement of isolated power supplies, which can be relatively bulky and adds additional parasitic capacitance between the switching output and ground. However, the disadvantage is that there is some limit to the achievable duty cycle range, switching frequency, and it requires a start-up procedure to power the high side gate driver circuitry. The ADUM4121 gate driver is used, which provides 5 kV voltage isolation between the input and output sides. It has a coupling capacitance of 2 pF between the input and output sides. It has a 5-V supply on the input side, and is provided with a 6-V supply on the output side. Thus, the gate–source voltages supplied to the GaN eHEMT are 6 and 0 V for high and low sides, respectively. For the high side, a low dropout linear regulator is used to stabilize the 6 V supply. The ADUM4121 gate driver also has a Miller clamp functionality, but, for the tests shown in this paper, the Miller clamp connection is left unconnected. A 20-nH ferrite bead is inserted in the gate driver path to suppress

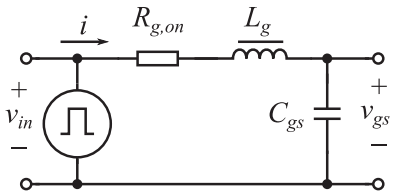

Fig. 5. Schematic used to analyze the dynamics of the gate–source voltage.

high-frequency ringing originating from the source inductance of the power circuit, and it shifts the resonance frequency of the gate driver loop away from the power loop resonance frequency [25]–[27].

There is a small operation margin of the gate–source voltage of the GaN eHEMT, as its recommended drive voltage is 6V and the maximum limit is 7V. Thus, the turn-ON gate resistance is chosen such that gate–source voltage oscillations are kept low, yet without slowing down the switching speed [21]. The gate–source loop schematic shown in Fig. 5 is analyzed to obtain such dynamics, including the gate loop inductance L_g, turn-ON gate resistance $R_{g,\text{on}}$, and gate–source capacitance C_{gs}. By applying Kirchoff's voltage law

$$v_{\text{in}}(t) = i(t)R_{g,\text{on}} + L_g\frac{di(t)}{dt} + v_{gs}(t). \tag{1}$$

The expression $i(t) = C_{gs}\frac{dv_{gs}(t)}{dt}$ is inserted, and the Laplace transform of (1) becomes

$$\frac{V_{gs}(s)}{V_{\text{in}}(s)} = \frac{\frac{1}{L_g C_{gs}}}{s^2 + \frac{R_{g,\text{on}}}{L_g}s + \frac{1}{L_g C_{gs}}}. \tag{2}$$

Equation (2) describes the dynamics from the gate driver to the gate–source voltage on the GaN eHEMT. It is compared with the standard form of a second-order system [28], given by

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3}$$

where ζ is the damping ratio and ω_n is the natural frequency. By comparing (2) with the standard form in (3), an expression for the gate turn-ON resistance is found as

$$R_{g,\text{on}} = 2\cdot\zeta\cdot\sqrt{\frac{L_g}{C_{gs}}} \tag{4}$$

A damping ratio of $\zeta = 0.707$ is chosen to achieve fast rise time, yet limited oscillation of gate–source voltage. Inserting the gate–source capacitance of GS66508T, and assuming that the gate inductance is dominated by the ferrite bead, the required gate resistance is calculated from the following equation:

$$R_{g,\text{on}} = 2\cdot 0.707\cdot\sqrt{\frac{20\text{ nH}}{258\text{ pF}}} = 12.4\ \Omega. \tag{5}$$

The ADUM4121 gate driver and internal gate resistance of the GS66508T GaN device contributes with approximately 1.7–2.7 Ω, and thus, the external gate resistor is chosen as 10 Ω. According to the design guidelines for the GS66508T GaN eHEMT [29], the turn-OFF gate resistance should be 5–10 times lower to avoid Miller latch up. Due to the resistance contributions from the ADUM4121 and GS66508T internal gate, external turn-OFF gate resistance is chosen as 0 Ω. This results in a slight overshoot during turn-OFF, but as the minimum gate–source voltage is rated at −10 V, a slight overshoot during turn-OFF does not pose a threat for safe operation of the module.

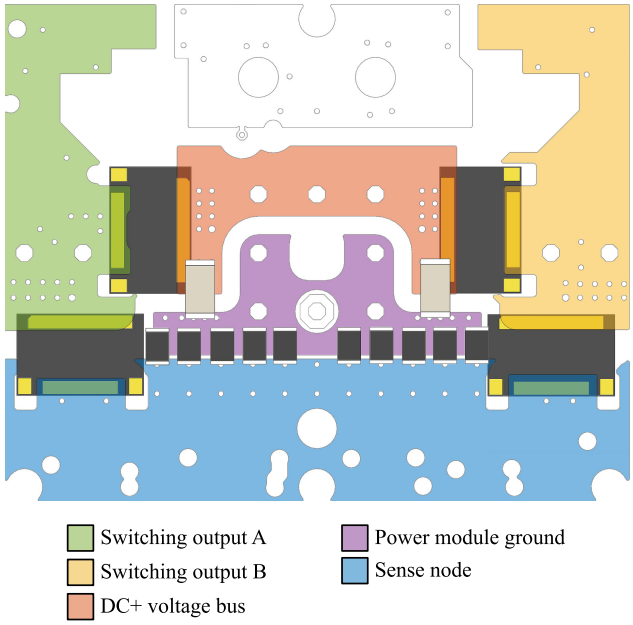

Fig. 6. PCB layout of main power planes, and positioning of GaN eHEMT devices (bottom side), decoupling capacitors (top side), and current shunt resistors (top side).

B. Board Layout

The board layout is designed to have both low parasitic capacitance and low inductance in the power loop, to push the capability of both high dv/dt and di/dt. However, maintaining both low parasitic capacitance and low inductance is often a compromise between the two. For instance, the inductance can be kept small by decreasing the loop area, and using parallel planes on the PCB to cancel the magnetic fields generated. However, parallel planes have a large capacitive coupling, and result in increased common mode current during voltage transients [30]. Likewise, to have low capacitive coupling between planes, they should be spaced far apart, but this will increase the loop area and, thus, increase the inductance. For this board layout, the parasitic capacitance is kept low by ensuring that switching outputs are not overlapping with other planes, as shown in Fig. 6.

Inductance is then kept low by placing the GaN eHEMT devices close to one another, reducing the effective loop area. DC-link capacitors are placed on the top side of the board, directly above the GaN eHEMT devices, and multiple vias are used to connect the top and bottom plane. A current measurement circuit must be integrated for control and safety purposes. For current measurements, Hall effect, Rogowski, or similar are often used, but they all require a winding around a current carrying conductor. The inductance introduced by such a solution could compromise the desired fast switching. Instead, it is

decided to measure the current through the low GaN eHEMT devices by inserting current shunts resistors in the power loop path. The current shunt resistor array has relatively low insertion inductance compared with other current measurement techniques [31]. The current shunt layout is based on the design presented in [32] and [33]. In total, ten current shunt resistors are inserted to minimize the parasitic inductance, which improves measurement bandwidth [34]. The issue of this solution is that the measurement is not isolated, and thus, it is influenced by parasitics in the circuit. Thus, it is important to accurately model the parasitics of the board, as further studied in Section IV, to know their influence on the measured shunt resistor voltage. Two half-bridges are placed in the same power module, and by symmetrical placement they share both the same current shunt resistors and decoupling capacitors.

III. Thermal Characteristics

The chosen GaN eHEMT device is a prepackaged device and has a thermal resistance from junction to case Θ_{jc} of 0.5K/W. In comparison, the CPM2-1200-0040B SiC MOSFET bare die of similar dimensions has $\Theta_{jc} = 0.38$ K/W [35]. However, the additional 0.12 K/W must be compared to the total thermal resistance from junction to heatsink of the final power module. The thermal performance of the power module is analyzed using a steady-state finite element simulation. The 3-D model in Fig. 3 is imported to COMSOL Multiphysics.

The DBC stack has a 0.3-mm thick copper layer with thermal conductivity $k = 380$ W/mK, on either side of 0.63-mm Al_2O_3 ceramic substrate of $k = 25$ W/mK. A thin solder layer of 60 μm thickness having thermal conductivity, $k = 60$ W/mK, is included to the heat pad of the GaN eHEMT device. The backside of the power module is cooled by the heat flux

$$q = h(T_{\text{ext}} - T) \tag{6}$$

where q is the heat flux, h is the heat transfer coefficient, and T_{ext} is the exterior temperature. The heat transfer coefficient changes greatly depending on how the power module is cooled. Typically, the *h*-coefficient is up to 100–300 W/m^{2}K for forced convection of air, 500–2000 W/m^{2}K for modules mounted on heatsink, and 10 000 W/m^{2}K or more for direct water cooling [15], [23], [36]–[38]. Fig. 7 shows the maximum junction temperature of the power module, when subjected to different power inputs per device and heat transfer coefficients. In all cases, the exterior temperature is kept at 40 °C.

A case where each GaN eHEMT device is subjected to a power loss P of 10 W, the exterior temperature $T_{\text{ext}} = 40$ °C, and $h = 1000$ W/m^{2}K is shown in Fig. 8. The thermal resistances from junction to heatsink Θ_{jh} are evaluated as 2.4 and 2.1 K/W for low and high sides, respectively. This is comparable with power modules on a DBC material having similar thickness and semiconductor die area [5], [13]. The difference in thermal resistance between high- and low-side devices is 12%. Compared to other integrated power modules, the difference between devices is found to be 18–19% [15], [23]. It is concluded that the thermal performance, measured in terms of thermal resistance Θ_{jh} and mismatch between devices, is within the range

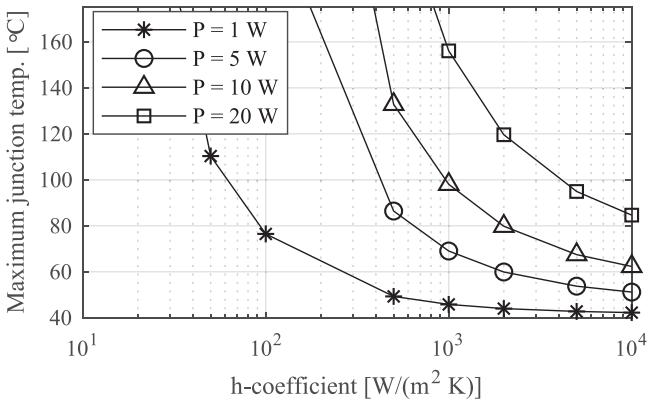

Fig. 7. Maximum junction temperature for different power inputs and heat transfer coefficient. Exterior temperature is $T_{\text{ext}} = 40$ °C.

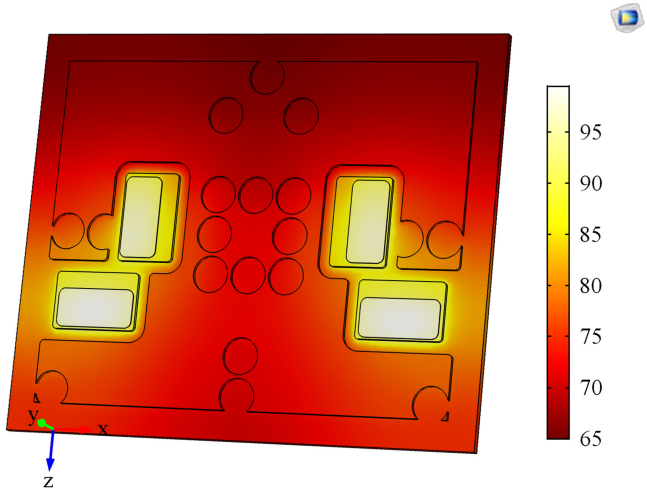

Fig. 8. Temperature distribution simulated in COMSOL Multiphysics, for conditions $P = 10$ W per device, $h = 1000$ W/m^{2}K, and $T_{\text{ext}} = 40$ °C.

of similar integrated solutions. Based on the total thermal resistance of the power module, the prepackaged GaN eHEMT device is not regarded as the bottleneck. It is concluded as suitable for use in the power module without modifications to its proposed structure.

IV. Electrical Simulation Model

Due to the compactness of the design, only a limited number of measurement points are available from the power module, namely, switching output voltages and the current sense measurement. Thus, during development and testing, an accurate simulation model is a necessary tool to gain insight into other nodes of interest, i.e., gate voltages. Second, to further improve the design, it is required to know the contribution different board parasitics have on the switching performance and measurements. A simplified schematic of the parasitics and the components of one half-bridge is shown in Fig. 9. As an example, due to the location of the grounding on the board, and if assuming that trace impedances are mainly inductive, the sense

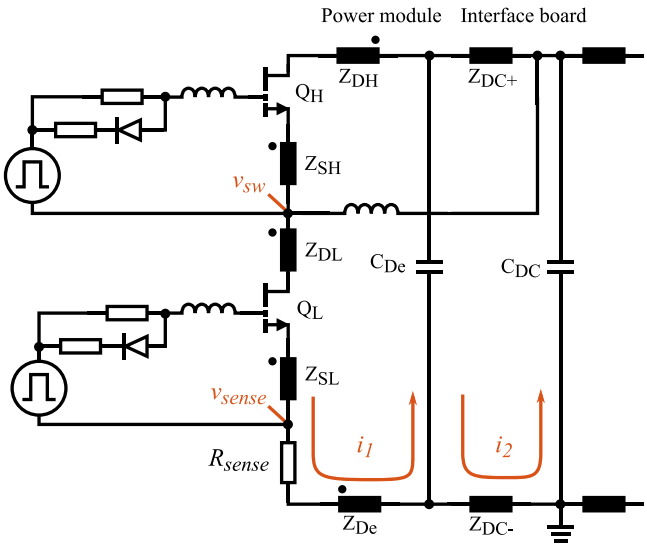

Fig. 9. Simplified schematic of the simulation model.

voltage measured is given by

$$v_{\text{sense}}(t) = i_1(t)R_{\text{sense}} + L_{\text{De}}\frac{di_1(t)}{dt} + L_{\text{DC}-}\frac{di_2(t)}{dt} \quad (7)$$

where i_1 is the power loop current, i_2 is the circulating current between distributed dc-links, R_{sense} is the resistance of the shunt array, and L_{De} and $L_{\text{DC}-}$ are trace self-inductances. When achieving fast-switching speed, there is a significant contribution from the parasitic inductances L_{De} and $L_{\text{DC}-}$, and thus, their values are important to know, to validate that the experimental measurements are correct.

To extract the board parasitics, the ANSYS Q3D Extractor simulation software is used. The ANSYS Q3D Extractor uses a finite element method and methods of moments to solve electromagnetic field simulations [39]. A 3-D model of the board is imported to the software, and inputs/outputs of each net are defined. A literature review reveals that different simulation approaches are used with the ANSYS Q3D Extractor software, which might result in different accuracies, simulation times, and ease of convergence when later implemented in a SPICE solver. In the following section, three different approaches are implemented and the simulation results are compared. The first approach is to replace each impedance of Fig. 9 with the self-inductance of the trace. The parasitic capacitances are designed to be low for this board and, thus, are neglected. The inductances are evaluated using a point-by-point approach, i.e., from the dc-link to the drain of the high device, then from source of high device to drain of low device, and so forth [9], [40], [41]. This model is denoted as a Level 1 model, and self-inductance calculated for each trace is shown in Table II.

A reported issue of this is that the summation of the inductances becomes large, because when evaluating each inductance individually, no mutual inductance effects are included in the model [42]. Thus, often an approach is used at which the full loop is evaluated [30], [43], [44]. In this approach, each device is modeled as a conductor, i.e., the drain and source of a switch are electrically shorted. The effective inductance of a full loop is calculated, and by this approach, the mutual inductance effects are included in the solution. However, to use the extracted inductance in a SPICE simulation, it must be placed accordingly in the circuit diagram, and this is difficult when inductances are calculated for the full loop. Thus, an approach considered for this paper is to use both the self-inductance and mutual inductance [44]–[46]. From the ANSYS Q3D Extractor, an *RLC* matrix is exported, meaning that it models the resistance and self-inductance in each trace, and mutual inductance and parasitic capacitances between nodes. This is denoted as a Level 2 model. It is advantageous during development that electromagnetic fields and couplings are already included in the circuit simulation, which reveals effects of conducted and near-field electromagnetic interference issues related to the board structure.

TABLE II
SELF-INDUCTANCE OF TRACES

Symbol	Value	Symbol	Value
L_{DH}	0.31 nH	L_{De}	0.23 nH
L_{SH}	0.26 nH	$L_{\text{DC}+}$	1.9 nH
L_{DL}	0.35 nH	$L_{\text{DC}-}$	0.3 nH
L_{SL}	0.86 nH		

When exporting the *RLC* matrix, the parameters must be extracted at a certain frequency. Typically, resistance values are extracted for low frequencies, where the skin effect is neglected and the current is assumed to flow equally distributed in the conductor volume. This is done to correctly model steady-state power loss of the board. The inductance values are extracted for high frequencies, at which the current path shifts to reduce the total loop area, and the inductance value decreases. Using this value results in the best approximation of the inductance during fast-switching transients.

A. Measurement of Component Parasitics

In addition to extraction of parasitics of the board, the influence of the parasitics in the components is also of interest. As board parasitics are small, the relative influence of the surface mount device (SMD) packages become larger. Especially, the measurement of voltage across the shunt resistors where the influence of the parasitic inductance can be significant. As resistors are conducting the full current and the voltage across them is just a few hundred millivolts, it requires a good estimation of how they are influenced by parasitics. Measuring the parasitic inductance and capacitance of SMD resistors, capacitors, and ferrite beads down to just a few nanohenry and picofarad requires a large frequency range to capture the cutoff/resonance frequency of the component. A Keysight E5016B impedance analyzer is used, which is capable of measuring the components up to 3 GHz. The Keysight 16192A test fixture has a measurement capability up to 2 GHz and is used to mount the SMD components. The impedance spectrum of an 220-mΩ 0805 shunt resistor, 100-nF 1210 dc-link capacitor, and the 20-nH ferrite

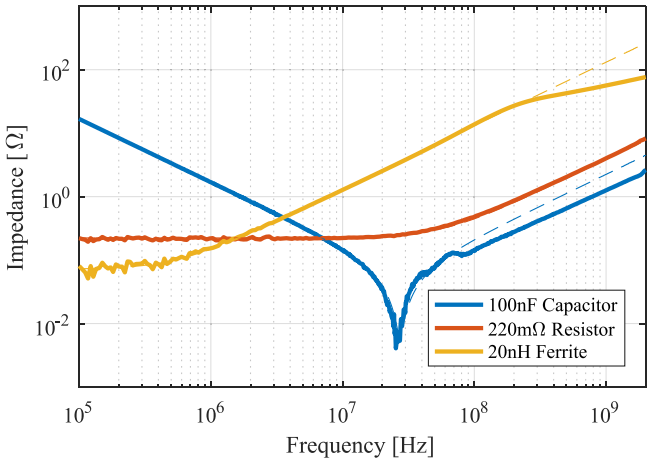

Fig. 10. Impedance as a function of frequency of main components of the half-bridge circuit (including their simulated models in dashed line).

TABLE III
PARASITICS EXTRACTED OF SMD COMPONENTS

Model			
Component	R	L	C
100 nF, 1210 capacitor	6 mΩ	257 pH	95.6 nF
220 mΩ, 0805 resistor	224 mΩ	616 pH	-
20 nH, 0603 ferrite bead	71 mΩ	21 nH	-

TABLE IV
COMPLEXITY IN SIMULATION MODEL

	Board parasitics	Component parasitics
Level 1	L w/o coupling	Ideal R, L or C
Level 2	RLC incl. coupling	Ideal R, L or C
Level 3	RLC incl. coupling	Measured RLC

bead in the gate driver is shown in Fig. 10, which also includes the frequency response of its estimated *RLC* model. The model used for fitting the response is an idealized *RLC* series connection. Table III summarizes the parasitics values extracted from the frequency response. The simulation model that includes both *RLC* board parasitics and *RLC* of SMD components is denoted as a Level 3 model.

B. Simulation Results

The results are compared for three different levels of simulation complexity. A summary of what is included in the three simulation models is given in Table IV.

All simulations use the SPICE model of the GS66508T GaN eHEMT device, and are all solved using the recommended solver settings provided by GaN Systems [47]. The SPICE model used includes a drain–source stray inductance of 0.4 nH originating from the packaging of the device, and its temperature is set to be 25 °C.

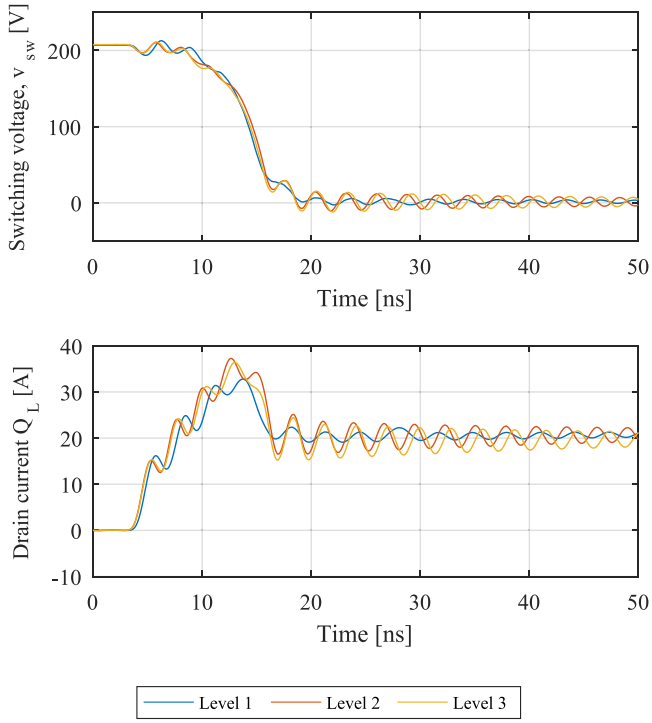

Fig. 11. Simulated waveforms of switching voltage and drain–source current during turn-ON for three different levels of simulation complexity.

A double pulse test is simulated. The dc-link voltage is 200 V, and current is ramped up in a 10-μH load inductor for 1 μs, to achieve a load current of 20 A. Transients of turn ON and turn OFF are investigated, as shown in Figs. 11 and 12, respectively.

The voltage rise time is defined as the time from 10% to 90% of dc-link voltage, and vice versa for voltage fall time. By this definition, both the fall and rise times are 6 ns, equivalent to 27 V/ns. These switching speeds are the same for all three simulation cases. Following turn-ON and turn-OFF oscillations in both voltage and current are visible, due to the resonance frequency of the power loop, shown as i_1 in Fig. 9. The resonance frequency is given by

$$f = \frac{1}{2\pi\sqrt{LC}}. \tag{8}$$

For the Level 1 model, the power loop inductance is calculated as the sum of inductances in the power loop, i_1 in Fig. 9, combined with the 0.4-nH contribution from the packaging of the two GaN devices. The resonance frequency for the Level 1 model is calculated by reading the time period of oscillations in Figs. 11 and 12. The output capacitance of the GaN eHEMT device is estimated for the given test condition by rearranging (8)

$$C = \frac{1}{(2\pi \cdot 325\ \text{MHz})^2 \cdot 2.8\ \text{nH}} = 85\,\text{pF}. \tag{9}$$

As observed from the simulation result, the resonance frequency is slightly higher for Level 2 and 3 models. However, because they include mutual inductance coupling terms, the effective loop inductance is cumbersome to calculate. Instead, the effective loop inductance for Level 2 and 3 models is calculated

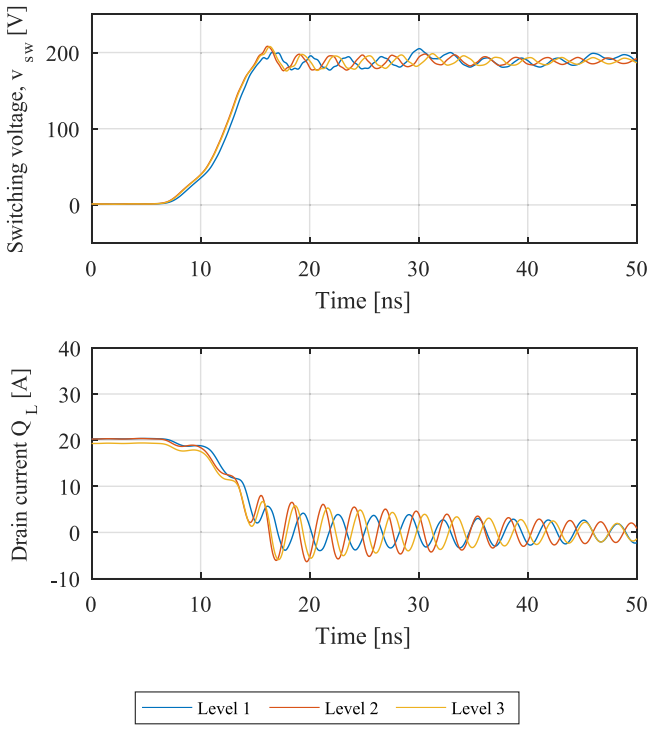

Fig. 12. Simulated waveforms of switching voltage and drain–source current during turn-OFF for three different levels of simulation complexity.

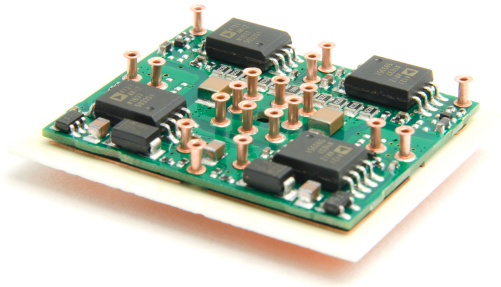

Fig. 13. Photograph of power module after soldering.

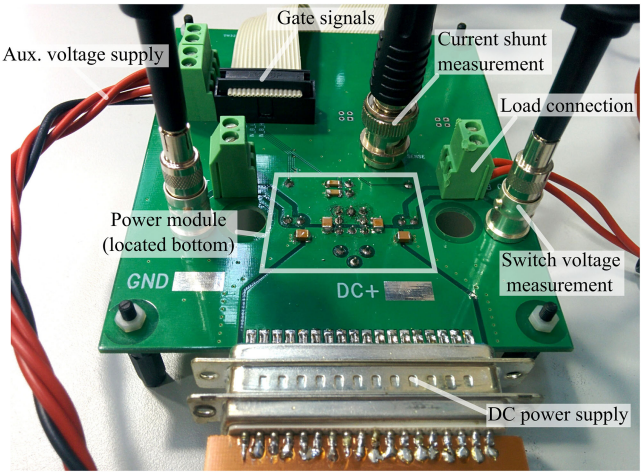

Fig. 14. Test board interfacing auxiliary voltage supply, gate control signals, and BNC connector points for measurements of switching voltage and current shunt. The power module is located below the test board.

by reading the resonance frequency from the simulation results and equals 358 and 338MHz, respectively. By rearranging (8), the effective inductance for the Level 3 model is calculated as follows:

$$L_{L3} = \frac{1}{(2\pi \cdot 338\ \text{MHz})^2 \cdot 85\ \text{pF}} = 2.6\ \text{nH}. \qquad (10)$$

Thus, the effective inductance is 8% higher for the Level 1 model, which only includes self-inductance, compared with the Level 3 case where mutual inductance coupling and component parasitics are included. The slightly higher inductance values of the Level 1 model means it could be more susceptible to false and oscillatory turn ON during simulation, due to increased ringing of the gate–source loop [25], [48]. However, this cannot be concluded because the coupling of the *RLC* matrix introduces new complexity that has not yet been studied in literature. The three models differ in terms of the time required to generate the simulated turn ON/OFF waveforms, which are simulated for a total of 5 μs. The real time required in LTSpice XVII is 5.5, 7.4, and 11.3 s for Level 1, Level 2, and Level 3 models, respectively. Thus, the total simulation time is about two times longer for the increased complexity.

V. Experimental Results

The power module is built for experimental tests on a 0.63-mm thick Al_2O_3 DBC and is etched with the designed pattern. All components are soldered to the PCB board in a multivacuum vapor phase oven. Following this step, the PCB including the GaN eHEMT devices is soldered to the DBC, as shown in Fig. 13. At last, the press-fit pins are inserted in the sockets and the plastic housing is mounted.

For the experimental tests, the power module is connected to a test board, as shown in Fig. 14. The test board interfaces the auxiliary voltages and control signals for the gate drivers. It includes the main dc power supply and switching output terminals for each half-bridge. Bayonet Neill–Concelman (BNC) connectors are used to measure the voltage switching outputs and the current shunt signal. The voltage switching waveforms are measured using 500-MHz LeCroy PP018-1 probes on a LeCroy HDO6104A oscilloscope. All cables of probes, auxiliary power supply, and main power supply are equipped with common mode choke cores.

A. Switching Behavior

The experimental waveforms are compared with the Level 3 simulation model during turn-OFF and turn-ON, as shown in Fig. 15. The voltage switching waveforms show very good coherence with the simulation model. The experimental results show that the GaN eHEMT devices for both voltage fall and rise times switch in 6ns for the tested 200 V/20 A condition, equivalent to a voltage transient of 27 V/ns. The resonance frequency of the experimental results is read as 335 MHz. Assuming that the loop capacitance is the same as observed from

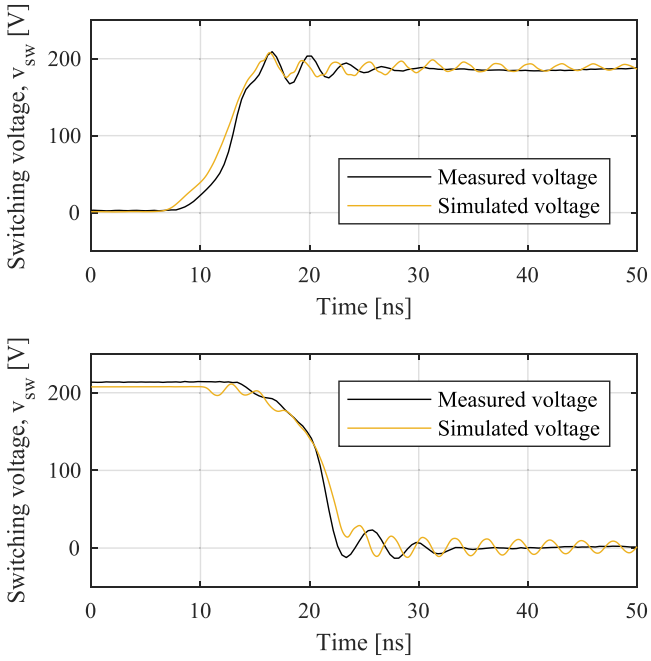

Fig. 15. Comparison of experimental and Level 3 simulated waveforms of switch voltage during turn-OFF and turn-ON at 200 V/20 A.

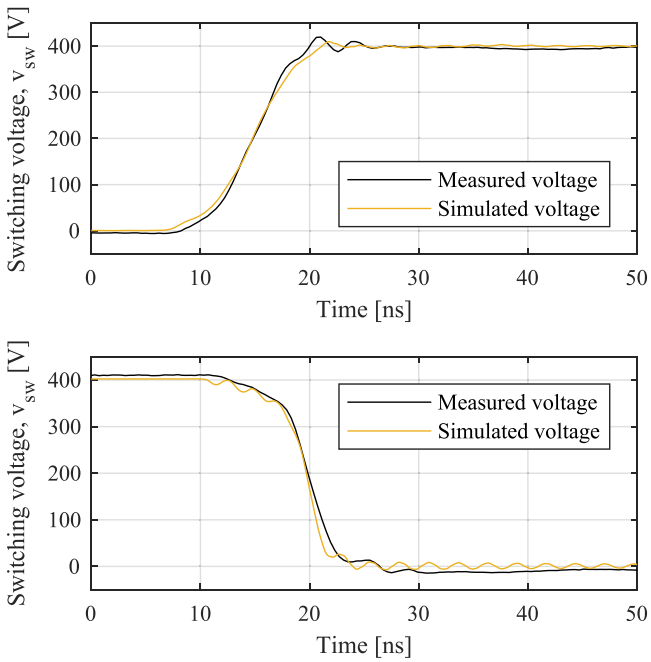

Fig. 16. Comparison of experimental and Level 3 simulated waveforms of switch voltage during turn-OFF and turn-ON at 400 V/15 A.

the simulation model in Section IV, it indicates that the effective power loop inductance is 2.65 nH.

To further verify the simulation model, the operating conditions are modified to 400 V/15 A, as shown in Fig. 16. The simulation model is the same, except for a change in the dc bus voltage and gate timing to achieve the right current value. At 400 V/15 A, the voltage fall and rise times are 5 and 8 ns,

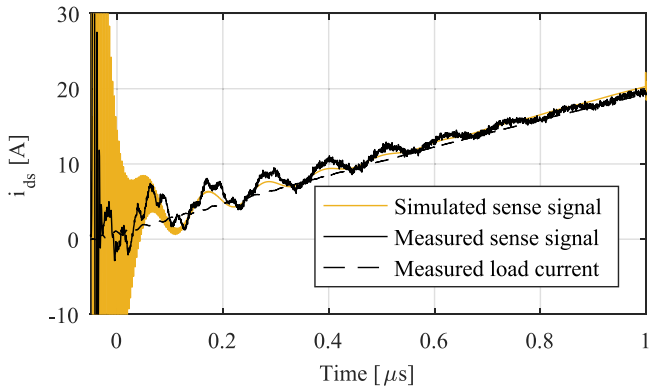

Fig. 17. Measured load current of inductor, measured sense current, and Level 3 simulated sense current.

respectively. This corresponds to voltage transients during the turn-ON and turn-OFF of 64 and 40 V/ns.

In addition to verifying the switching voltage, it is also ensured that the shunt resistor array delivers accurate current measurements for control purposes, preferably without additional measurements and computational expensive compensations. The measured sense voltage is divided by 22 mΩ (now called measured sense signal). As an additional verification, the current through the inductor is measured using a Teledyne LeCroy CP030 current probe, as a reference that is not affected by the high-frequency ringing. The measured sense current, the measured inductor load current, and the simulated sense current are shown in Fig. 17.

The results highlight that due to damping in the circuit, the influence of inductive terms shown (7) are decayed after 1 μs, at which an accurate current measurement can be sampled. The initial high-frequency oscillations are due to the power loop, indicated as i_1 in Fig. 9. The lower frequency ringing is due to the ringing of the decoupling and main dc-link capacitors. As the GaN eHEMTs are switching, power is delivered from the decoupling capacitors C_{De} inside the power module and their voltage drops. Current i_2, as denoted in Fig. 9, conducts to charge the decoupling capacitors. When the two voltages are equal, current is still loaded in inductances and, thus, charges the decoupling capacitors slightly above their initial 200 V. This causes an oscillating current, which experimentally is measured at a frequency of 8.8 MHz. This oscillation is correctly predicted by the simulation model. In general, the oscillations of the simulated response are less damped than the experimental results. This can be explained by the choice of using the dc resistance values in the exported *RLC* matrix from the ANSYS Q3D Extractor. To solve this, a frequency dependent resistance model should be implemented, such that the resistance is higher for increasing frequency due to the skin effect. However, in terms of the switching speed of both turn-ON and turn-OFF voltages as well as its frequency and amplitude of oscillation, this has a minor impact. In conclusion, the use of the ANSYS Q3D Extractor provides a very good simulation result of the switching voltage transient.

VI. Conclusion

A hybrid PCB/DBC structure is proposed, designed for fast-switching and high-power dissipation. In contrast to other hybrid methods, the proposed structure does not require embedding of dies and molding of PCBs on top of a DBC. The DBC, PCB, and semiconductors are available from suppliers and only require vapor phase soldering to assemble the stack, which decreases the manufacturing complexity.

A finite element simulation is used to assess the thermal characteristics of the power module, and the thermal resistance from junction to heatsink is evaluated as 2.4 K/W. An ANSYS Q3D Extractor is used to extract the parasitics of the board, which are implemented in a SPICE solver. Three levels of simulation complexity were investigated. A Level 1 simulation model only includes self-inductance, a Level 2 model has a coupled *RLC* matrix, and a Level 3 model is combined with SMD component parasitics, by using an impedance analyzer up to 2 GHz. The Level 1 simulation case estimates 8% higher loop inductance, when compared to the Level 3 model. The experimental results verified the simulation model for the main switching voltage waveforms, and shows a turn-ON and turn-OFF speed of 6 ns during switching at 200 V/20 A. By analyzing the resonance frequency, it is concluded that the achieved power loop inductance is 2.65 nH including current measurement circuitry. The Level 3 simulation model provides the best approximation of the inductance as can be observed from the experimental results, but the simulation time is two times longer compared to the Level 1 model. The power module is tested at 400V/15A, at which voltage fall and rise times of 5 and 8 ns are achieved, respectively. This equals a maximum dv/dt of 64 V/ns. The measured switching voltage waveform of the GaN eHEMT integrated power module shows low overshoot and ringing, which proves the proposed module structure and its accompanying board layout. Compared with other integrated power module structures, the proposed hybrid DBC/PCB power module structure performs well in terms of thermal performance, has very low commutation loop inductance, and is relatively easy to manufacture.

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