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Impact of Power Module Parasitic Capacitances on Medium Voltage SiC MOSFETs Switching Transients

Dipen Narendra Dalal, Nicklas Christensen, Asger Bjørn Jørgensen, Jannick Kjær Jørgensen, Szymon Bęczkowski, Stig Munk-Nielsen and Christian Uhrenfeldt

***Abstract*—Increased switching speeds of WBG semiconductors result in a significant magnitude of the displacement currents through power module parasitic capacitances which are inherent in packaging design. This is of increasing concern particularly in case of newly emerging medium voltage SiC MOSFETs since the magnitude of the displacement currents can be several order higher due to the fast switching transients and increased voltage magnitudes of the SiC MOSFETs compared to their Si counter parts. The severity intensifies when the magnitude of the displacement current become comparable to a significant fraction of SiC MOSFETs rated current, leading to the worsened impact on the converter EMI as well as performance in terms of switching losses. The key objective of the paper is to provide a detail insight into the impact of the module parasitic capacitances on the SiC MOSFET switching dynamics and losses. To realize this, a well defined approach to dissect the switching energy dissipation is proposed, based on which the detail analysis and quantitative measurements of the module parasitic capacitance impact in terms of added switching energy losses and common mode currents is investigated using a custom packaged 10 kV half bridge SiC MOSFET power modules. The theoretical analysis and experimental results obtained from dynamic as well as static characterization reveals that the impact of the module parasitic capacitance on the switching energy dissipation is two-fold and substantially adverse such that it can not be overlooked considering its intended application in the high power medium voltage power electronic converters.**

***Index Terms*—Silicon Carbide, 10 kV SiC MOSFETs, parasitic capacitance, switching losses, EMI/EMC**

I. Introduction

THE medium voltage (MV) Silicon Carbide (SiC) MOSFETs are evolving as a mature technology due to continuous refinements and technological advancement in the SiC device fabrication technology over the past few years. In particular, the modern MV SiC MOSFETs technology in 6.5 kV or higher voltage class has gained increased interest in the medium voltage and high power conversion applications such as solid state transformers, renewable, traction, MV motor drives and grid support [1]–[6]. Recently, these devices have been demonstrated in a multi-chip half-bridge power module packages that are specially tailored to be utilized in such applications [7]–[9]. In a typical power module, the parasitic capacitances are inevitably present due to the capacitive coupling between the top copper traces on direct bonded copper (DBC) and mounting baseplate as shown in Fig. 1. Some of these parasitic capacitances get charged or discharged during every switching transient which introduces displacement currents and give rise to the switching losses as well as electromagnetic interference (EMI) issues. The

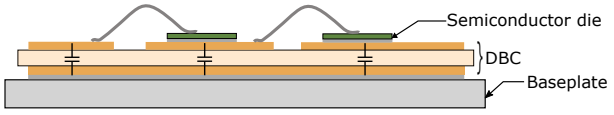

Fig. 1. Schematic showing the parasitic capacitances in a power module.

magnitude of these displacement currents is governed by the dv/dt appearing across the capacitance, the values of module parasitic capacitances and the heatsink grounding impedance [10]. The dv/dt in the wide band gap (WBG) devices are significantly higher compared to the Si devices which increases the magnitude of the displacement currents to an extent, where accurate quantification and prediction capability of the module parasitic capacitances is key in order to design modules that qualify for the electromagnetic compatibility (EMC) standards [6], [11]–[17]. Apart from its impact on worsening the electromagnetic interference (EMI) performance, the displacement currents due to module parasitic capacitances result in the diminished switching performance in terms of losses. Therefore it is desired to minimize the module parasitic capacitances, however the area occupied by the semiconductor dies, lower stray inductance requirements, thermal performance and cost are the key factors that limits the power module designer in regards to which extent the coupling capacitances can be reduced.

An EMI investigation performed on SiC based power electronics converter for a range of applications in [11], [18]–[23], identified module parasitic capacitances as one of the dominant contributors to the conducted EMI. For example, the simulation based parametric study performed by [24] to investigate the impact of module parasitic capacitance on the switching transients and energy loss for MV SiC MOSFET show that understanding the high dv/dt induced displacement currents due to module packaging is very important to accurately model the device switching behaviour and switching energy dissipation. It can be hard to distinguish the impacts of module parasitic capaciatnce, since these capacitances in turn affects the switching dynamics which changes the switching

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energy dissipation. In addition to this the parasitic capacitance also adds losses on its own as will be discussed in this paper. Thus it is difficult without a detailed analysis to quantify the different mechanisms impact on the switching losses. In [25], authors point out the importance of the module parasitic capacitances on the switching losses and investigate the impact for a discrete 10 kV SiC MOSFET package by adding an arbitrary value of an external capacitor in parallel to the MOSFET which essentially acts like a snubber. Even though it mimics the module parasitic capacitance it does not provide a fair comparison in terms of an actual power module layout. Furthermore, authors do not provide the dissection of the switching energy dissipation which is crucial to understand the impact of module parasitic capacitances in relation to the overall switching losses. In this paper, authors provide a complete dissection of the switching energy dissipation to understand the impact of module parasitic capacitance on the overall switching losses. This is done by analysing the switching transients and quantitative comparison of the module parasitic capacitance related losses for the custom made 10 kV SiC MOSFET half bridge power modules in two different layouts.

This paper is organized as follows. In Section II, the details of the case study, i.e custom made 10 kV half bridge SiC MOSFET power modules as well as its key parasitic parameters are presented, while the experimental test bench and measurement methodology utilized to investigate the impact of module parasitic capacitances on the SiC MOSFET switching transients is introduced in Section III. In Section IV, the high dv/dt and module parasitic capacitance induced displacement current paths during the MOSFET turn-on as well as turn-off switching transient is analyzed based on the theoretical analysis and experimental results. Since these displacement currents can not be measured directly, an indirect methodology to obtain the displacement currents from the accessible half bridge module current measurements is proposed and validated experimentally in Section V. In Section VI and VII, a complete dissection of the switching energy dissipation is presented based on which the impact of module parasitic capacitance on the turn-on and turn-off switching energy dissipation is discussed in detail.

II. Device under test - 10 kV half bridge SiC MOSFET power module

In the present case study, two versions of the custom made 10 kV single die half-bridge SiC MOSFET power modules (referred here as A and B) with different DBC layouts are utilized, the difference being the reduced capacitance DBC layout for module B under restraint of keeping the terminal configurations similar. The picture and top view of the DBC layout for the two power modules is presented in Fig. 2. The half-bridge power modules are populated with third generation 10 kV SiC MOSFETs and anti-parallel SiC junction barrier Shcottky (JBS) diodes [26], [27] which are soldered on a 0.63 mm AlN DBC with a 5 mm AlSiC baseplate. The module parasitic capacitances in a half bridge power module resulting from Cu-AlN-Cu layers of the DBC is presented in Fig. 3,

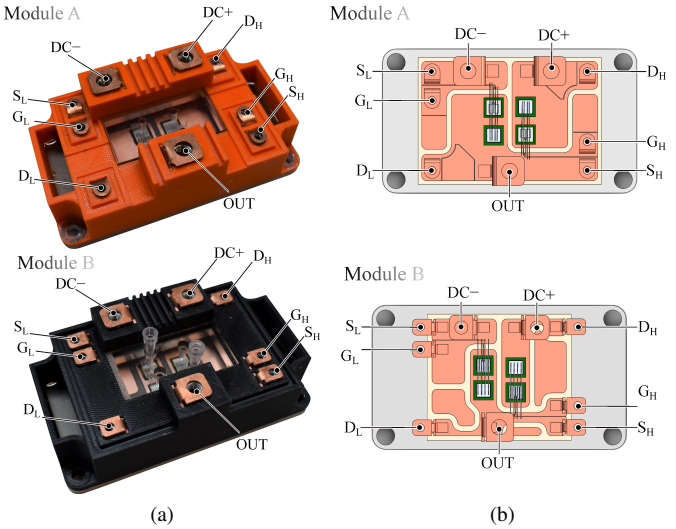


Fig. 2. (a) Picture and (b) Solidworks rendering for the 10 kV half-bridge SiC MOSFET power modules A and B with different DBC layouts.

where $C_{\sigma+}$ is the distributed parasitic capacitance from the DC+ plane to the baseplate, $C_{\sigma\mathrm{GH}}$ is from the high-side (HS) gate plane to the baseplate, $C_{\sigma\mathrm{OUT}}$ is from the output plane to the baseplate, $C_{\sigma\mathrm{GL}}$ is from the low-side (LS) gate plane to the baseplate and $C_{\sigma-}$ is from the DC– plane to the baseplate. (See Fig. 2b for the physical reference.) Although, both modules A and B have unused copper areas on the DBC, which are not etched due to manufacturing reasons. In the design process it was ensured that the EMI performance was still good and the unused copper area on the DBC meets the necessary isolation requirements.

The parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ are crucial since these capacitances experience high dv/dt during the switching transients and have dominant impact on the EMI and switching performance. In [14], [16], [28] various approaches are proposed for reducing the module parasitic capacitances by means of introducing an additional copper layer within a DBC that acts as a shield, by increasing the thickness of the DBC ceramic substrate or using a flip-chip technology for the low side power semiconductor devices. Whereas in [18], portion of a bottom copper layer of the DBC is replaced by introducing a low permittivity material (air), thereby reducing the module parasitic capacitances and consequently attenuating the CM EMI. For the case at hand, the design of power module B was revised with simple measures to obtain reduced coupling capacitances compared to A by reducing the copper area connected to the output as well as high side gate plane without significantly penalizing the stray inductances and serves as a good showcase here [17]. This facilitates in a comparison simple enough to demonstrate the impact of the module parasitic capacitances on switching transients and switching losses. The parasitic capacitances for two power modules were obtained from the ANSYS Q3D [29] are presented in Table I. For the capacitance extraction in the ANSYS simulations, the permittivity for the packaging materials are taken from material datasheet supplied by the manufacturer.

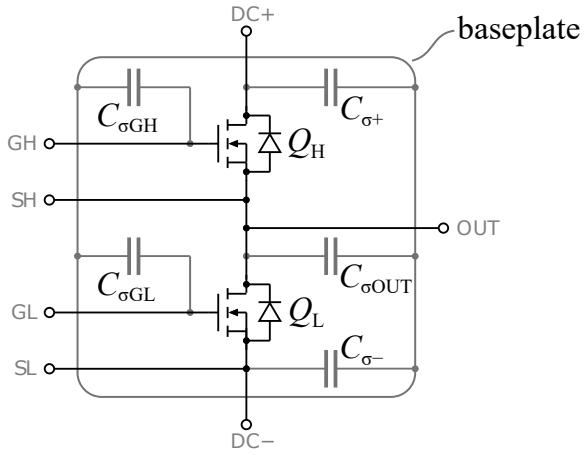


Fig. 3. Schematic representation of the distribution of the parasitic capacitances in a half bridge power module.

TABLE I
VALUES OF PARASITIC CAPACITANCES OBTAINED FROM ANSYS Q3D FOR THE 10 KV HALF-BRIDGE SIC MOSFET POWER MODULES A AND B. (ALL IN [PF])

Module	$C_{\sigma+}$	$C_{\sigma GH}$	$C_{\sigma OUT}$	$C_{\sigma GL}$	$C_{\sigma-}$
A	108	20.5	159.2	23.5	47.5
B	68.1	12.4	81.4	35.6	32.7

A. Equivalent impedance network between power module and the heatsink

Apart from the power module layout and the dv/dt, the displacement currents are also affected by the heatsink grounding impedance [30]. Thus in order to be able to analyze the displacement currents due to module parasitic capacitances, an equivalent impedance network between the power module and the heatsink connection is needed, which in turn enables the prediction of the displacement currents based on the voltage measurements as will be presented later.

Since slowing down the switching speed is adverse to the desired fast switching characteristics and lower switching losses of the SiC MOSFETs, only heatsink grounding is left as an available design choice. In a power electronic converter the power module is mounted on the heatsink which is mostly kept at ground potential owing to the safety reasons but some applications may allow to keep heatsink floating or connected through an impedance network although this is exceptional [11]. Considering the case where heatsink is shorted to ground, during the switching transients the module parasitic capacitances $C_{\sigma \mathrm{OUT}}$ and $C_{\sigma \mathrm{GH}}$ experience the same dv/dt as appearing at the output terminal of the half-bridge, whereas the module capacitances $C_{\sigma+}$, $C_{\sigma \mathrm{GL}}$ and $C_{\sigma-}$ do not experience this dv/dt since these are referenced to a fixed DC+ or DC– potential. Due to the dv/dt appearing at the output terminal of the half-bridge the capacitances $C_{\sigma \mathrm{OUT}}$ and $C_{\sigma \mathrm{GH}}$ get charged or discharged by the displacement currents during the turn-on and turn-off switching transient respectively. The differential voltage between the high side gate and source terminal is comparatively small such that the impedance between the output terminal of the half-bridge and heatsink can be modelled as parallel combination of

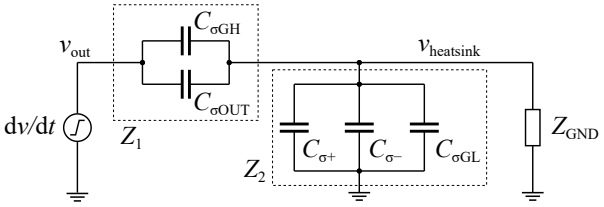


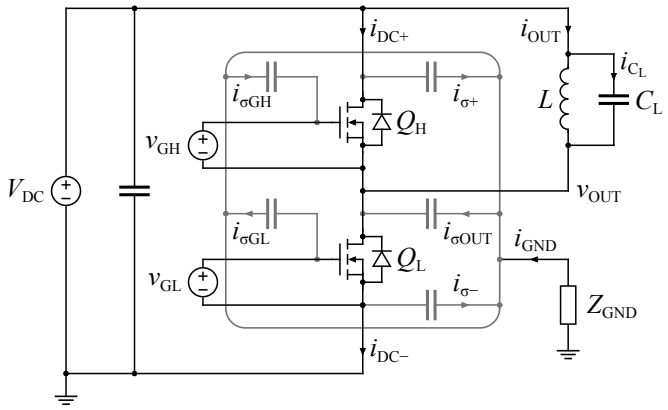
Fig. 4. Schematic of the equivalent impedance network between the half-bridge output terminal and ground.

capacitance $C_{\sigma \mathrm{OUT}}$ and $C_{\sigma \mathrm{GH}}$, which is denoted as Z_1 in Fig. 4. The impedance between the heatsink and the ground node can be modelled as a parallel combination of the module capacitance $C_{\sigma+}$, $C_{\sigma-}$, $C_{\sigma \mathrm{GL}}$ denoted as Z_2 and grounding impedance Z_{gnd}. The resulting equivalent impedance network between the half-bridge output terminal to ground is presented in Fig. 4 [10].

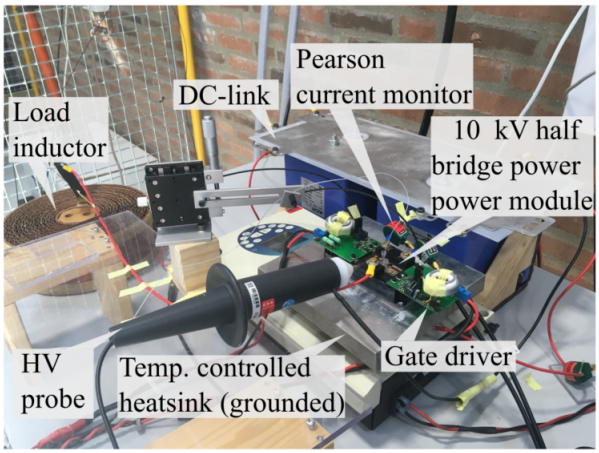
The magnitude of the displacement currents during the turn-on and turn-off switching transient due to the module parasitic capacitance $C_{\sigma \mathrm{OUT}}$ and $C_{\sigma \mathrm{GH}}$ can be determined as $i_{\sigma \mathrm{OUT}} + i_{\sigma \mathrm{GH}} \approx (C_{\sigma \mathrm{OUT}} + C_{\sigma \mathrm{GH}}) \cdot \mathrm{d}(v_{\mathrm{OUT}} - v_{\mathrm{heatsink}})/\mathrm{d}t$. This method thus allows direct prediction of the $i_{\sigma \mathrm{OUT}} + i_{\sigma \mathrm{GH}}$ for the known values of module parasitic capacitances. The displacement currents $i_{\sigma \mathrm{OUT}} + i_{\sigma \mathrm{GH}}$ conduct through the ground loop resulting in an increased amount of conducted EMI and switching energy dissipation.

III. EXPERIMENTAL TEST BENCH

The experiments are performed by mounting the half-bridge power modules A and B in a double pulse test setup. The schematic and image of the experimental setup are presented in Fig. 5a and 5b respectively. The power module is connected to DC power supply (XR 6000-1.0/415/+HS+LXI) through a low stray inductance busbar with two parallel connected 5 kV, 50 μF polypropylene capacitors. A 47 mH air core inductor is used as a load, whose parasitic capacitance (C_{L}) is measured to be approximately 12 pF. The air coil inductor with very low equivalent parasitic capacitance compared to the module parasitic capacitances is utilised to lessen its influence on the switching dynamics and losses. A low isolation capacitance ($\approx$ 4.8 pF) gate driver with active Miller-clamp functionality is utilized to drive the SiC MOSFETs [31]. The heatsink on which the power module is mounted is connected to the DC-potential of the busbar through copper wire providing low inductance connection and shorter ground current loop to avoid propagating the displacement currents through other ground nodes. For consistency all the module current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$, i_{OUT} as well as i_{gnd} are recorded using high bandwidth 200 MHz Pearson 2877 current monitors [32].To measure currents $i_{\mathrm{DC+}}$ and $i_{\mathrm{DC-}}$ with Pearson current monitor a short wire is inserted between the module DC+, DC− terminals and the busbar as can be seen in Fig.5b, where each of these connections introduces approximately 50 nH of stray inductance in the power loop. The voltage at the output terminal of the power module is measured utilizing Lecroy PPE 20 kV 100 MHz high voltage passive probe [33]. Both



(a)



(b)

Fig. 5. (a) Schematic and (b) picture of the double pulse test bench.

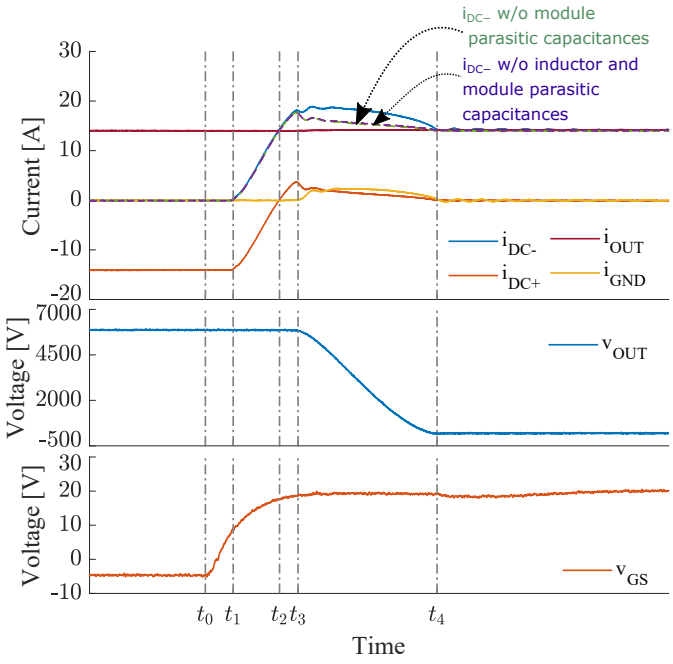


Fig. 6. Experimental switching waveforms for the turn-on switching transient. (V_{DC} = 6 kV and i_L = 14 A)

power modules A and B are tested in the same experimental setup under identical test conditions. To understand the impact of the module parasitic capacitances induced displacement currents on the SiC MOSFET switching performance, the MOSFET turn-on and turn-off switching transients are analyzed separately in Section IV in the double pulse test circuit.

IV. Understanding Impact of Power Module Parasitic Capacitance on MOSFET Turn-On and Turn-Off Switching Transients Based on Experimental Results

A. Analysis for the turn-on switching transient

An impact of power module parasitic capacitance on the MOSFET turn-on switching transient is analyzed utilizing the double pulse test circuit and turn-on switching waveforms presented in Fig. 5a and 6 respectively. As shown in Fig. 6, at time t_0 the turn-on gate command is applied to the low side (LS) MOSFET Q_L. From time t_0 the gate-source voltage v_{GS} start to rise from the turn-off gate bias level and reaches the MOSFET threshold voltage level $v_{GS(th)}$ at time t_1. At this time t_1 the LS MOSFET starts conducting. During the time interval t_1–t_2 the current through LS MOSFET increases and reaches the load current level i_L at time t_2. At this time instant the load current is completely commutated from the high side (HS) diode to the low side (LS) MOSFET. The time instant t_1 and t_2 corresponds to the threshold and Miller level respectively for the LS MOSFET gate-source voltage. The time interval t_2–t_4 also termed as Miller region, is where the diode current goes to its peak reverse recovery and reaches zero current level. A voltage change at the output terminal of the half-bridge power module occurs within the time interval t_3–t_4. In this time interval, the LS MOSFET carries the load current plus an additional current due to charging of the combined HS MOSFET and external JBS diode output capacitance. In addition to this, the negative rate of change of voltage (dv/dt) appearing across the output terminal of the half-bridge in the time interval t_3–t_4 causes the parasitic capacitance $C_{\sigma OUT}$, $C_{\sigma GH}$ to discharge and C_L to charge with the displacement currents $i_{\sigma OUT}, i_{\sigma GH}$ and i_{C_L} respectively which is conducted through the LS MOSFET. These displacement currents $i_{\sigma OUT}, i_{\sigma GH}$, i_{C_L} produce a Joule heating in the LS MOSFET which adds to the turn-on switching losses. The measured ground current (i_{GND}) in Fig. 6, is solely due to the discharging of the module parasitic capacitance $C_{\sigma OUT}$ and $C_{\sigma GH}$. The magnitude of the displacement current i_{C_L}, is significantly small due to the very low parasitic capacitance of the load inductor and therefore its impact on the load current i_{OUT} is not clearly visible. The increased magnitude of the module current i_{DC+} during time interval t_3–t_4 due to the module parasitic capacitance related displacement currents is clearly identified from the module current measurements presented in Fig. 6.

From t_2–t_4 the current through the LS MOSFET consists of the (i) load current, (ii) displacement currents due to charging and discharging of the HS as well as LS MOSFET and diode

combined output capacitance, (iii) HS diode reverse recovery current and (iv) displacement currents due to discharging and charging of the module as well as load inductor parasitic capacitances respectively.

Although the displacement current due to discharging of the LS MOSFET and diode output capacitances is conducted through the LS MOSFET channel it can can not be measured at the DC– terminal of the half-bridge since this discharging current path is confined within the LS MOSFET and JBS diode output capacitance itself. [34].

It should be noted that the gate-source voltage during the Miller region does not remain clamped corresponding to the load current level i_L but increases due to the additional displacement currents that flow through the LS MOSFET channel. The increase in the gate-source voltage will result in a decrease in the gate-drain current charging the Miller capacitance C_{GD} hence resulting in a lower dv/dt at the output terminal of the half-bridge. Thus the turn-on dv_{OUT}/dt decreases with increasing value of module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$.

B. Analysis for the turn-off switching transient

The impact of power module parasitic capacitance on the MOSFET turn-off switching transient is analyzed utilizing the double pulse test circuit and the corresponding switching wave-forms as presented in Fig. 5a and 7 respectively.

At time t_5, the gate-source voltage starts to decrease from the turn-on gate voltage level. And at time t_6, the LS MOSFET enters into the saturation region from the linear region. The time instant t_6 is where the LS MOSFET gate-source voltage reaches the Miller-level. During the Miller plateau which occurs within time interval t_6–t_7, voltage at the output terminal of the half-bridge starts to increase. In time interval t_6–t_7, the current through LS MOSFET starts to decrease and MOSFET turns off when gate-source voltage is below the threshold voltage. This happens before time t_7 and the current measured at the DC- terminal even after the gate-source voltage of the LS MOSFET reaches below threshold voltage is due to the charging of the combined LS MOSFET and JBS diode output capacitance as beyond that point no current conducts through the MOSFET channel.

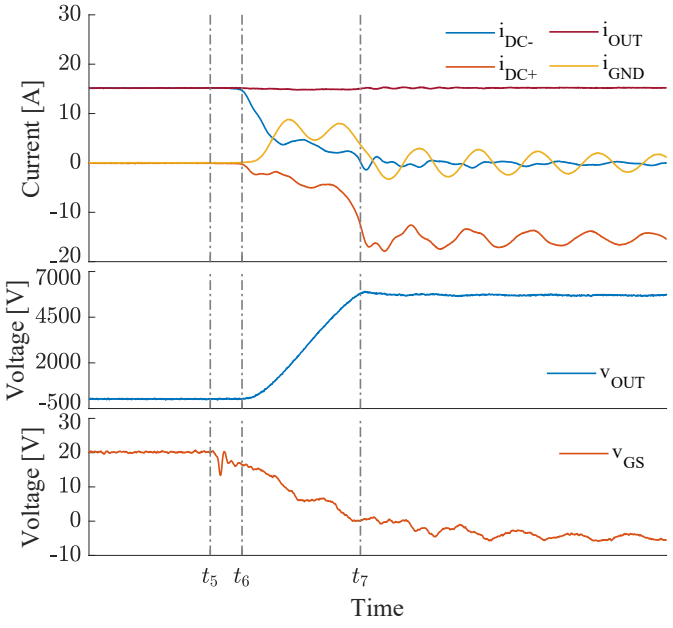


Fig. 7. Experimental switching waveforms for the turn-off switching transient. (V_{DC} = 6 kV and i_{L} = 14 A)

During t_6–t_7, the load inductor current comprises of the displacement currents that are charging and discharging the combined output capacitances of LS and HS MOSFET as well as JBS diode capacitance, displacement currents charging the module parasitic capacitances $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ that conducts through heatsink ground path. In contrast to the turn-on during the turn-off switching transient displacement currents charge the parasitic capacitances through the paths that does not conduct through MOSFET channel hence does not produce a joule heating.

V. Indirect Methodology Utilized to Obtain Module Parasitic Capacitance Related Displacement Currents

The displacement current through the module parasitic capacitances can not be measured directly and therefore an indirect approach for obtaining the displacement current is required. In this section the methodology, which utilizes accessible half bridge current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$ and i_{OUT} to accurately obtain the module parasitic capacitance related displacement currents for both the turn-on and turn-off switching transition is introduced with supporting experimental validation.

At first, the turn-on switching transient is analysed considering the double pulse test circuit presented in Fig. 5a. In this test circuit when heatsink is shorted to ground it is justifiable to consider that no displacement currents flow through capacitances $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ because these capacitances does not experience dv/dt and ground current i_{GND} can be considered to be the total sum of the displacement currents through $C_{\sigma\mathrm{GH}}$ and $C_{\sigma\mathrm{OUT}}$ as presented in (1). In practice the stray inductance in the heatsink grounding path can produce a high frequency displacement currents through $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ due to voltage oscillation at heatsink node. However, for the grounded heatsink the voltage drop across the stray inductance due to the ground current is negligible in comparison to the voltage change across capacitance $C_{\sigma\mathrm{GH}}$ and $C_{\sigma\mathrm{OUT}}$.

$$i_{\mathrm{GND}} \approx i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \tag{1}$$

Considering a fact that for the half-bridge power module accessible points for power loop current measurements are terminals DC+, OUT and DC-, magnitude of the displacement currents through inductor and module parasitic capacitance needs to be obtained indirectly utilizing three current measurements $i_{\mathrm{DC+}}$, $i_{\mathrm{DC-}}$ and i_{OUT} as presented in (2) and (4).

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\mathrm{OUT}} - i_{\mathrm{L}} \\ &\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_2)}}, v_{\mathrm{OUT}} = V_{\mathrm{DS(LS)}}\right] \\ &= C_{\mathrm{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)}(V_{\mathrm{DC+}} - v_{\mathrm{OUT}}) \end{aligned} \tag{2}$$

Since almost no displacement currents flow through the module parasitic capacitance $C_{\sigma+}$, $C_{\sigma\mathrm{GL}}$ and $C_{\sigma-}$ the currents $i_{\mathrm{DC}+}$ and $i_{\mathrm{DC}-}$ can be considered almost equal to the current at the source terminal of the HS MOSFET and current at the drain terminal of the LS MOSFET respectively. For the analyzed test case, circuits external to the power module such as high side gate driver power supply and passive voltage probe utilized to measure the voltage at the power module output terminal also introduce capacitive couplings to ground, which results in displacement currents $i_{\mathrm{C_{AUX}}}$ that is conducted through the LS MOSFET during the turn-on $\mathrm{d}v_{\mathrm{OUT}}/\mathrm{d}t$. Considering this notion and applying Kirchhoff's current law (KCL) at the output terminal of the half-bridge $i_{\mathrm{DC}-}$ can be given as (3).

$$i_{\mathrm{DC}-} = i_{\mathrm{DC}+} + i_{\mathrm{OUT}} + i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} + i_{\mathrm{C_{AUX}}} \tag{3}$$

The displacement currents due to module parasitic capacitances can be approximated as,

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = i_{\mathrm{DC}-} - i_{\mathrm{DC}+} - i_{\mathrm{OUT}} - i_{\mathrm{C_{AUX}}} \tag{4}$$

and

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \frac{\mathrm{d}}{\mathrm{d}(t_4 - t_3)} v_{\mathrm{OUT}} \tag{5}$$

Taking into account that the coupling capacitances due to the probe ($\approx$ 3 pF) and gate driver power supply (4.8 pF) are significantly small compared to the module parasitic capacitances, the magnitudes of the displacement currents $i_{\mathrm{C_{AUX}}}$ are relatively smaller compared to the $i_{\mathrm{C}_{\sigma\mathrm{OUT}}} + i_{\mathrm{C}_{\sigma\mathrm{GH}}}$. Based on this consideration (4) can be further simplified into (6),

$$i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} \approx i_{\mathrm{DC}-} - i_{\mathrm{DC}+} - i_{\mathrm{OUT}} \tag{6}$$

The displacement currents due to inductor and module parasitic capacitances for the turn-off switching transient can be obtained using (7) and (8) similar to the explanation presented for the turn-on switching transient.

$$\begin{aligned} i_{\mathrm{C_L}} &= i_{\mathrm{OUT}} - i_{\mathrm{L}} \\ &\left[i_{\mathrm{L}} = i_{\mathrm{OUT(t_6)}}, v_{\mathrm{OUT}} = V_{\mathrm{DS(LS)}}\right] \\ &= C_{\mathrm{L}} \cdot \frac{\mathrm{d}}{\mathrm{d}(t_7 - t_6)} (V_{\mathrm{DC}+} - v_{\mathrm{OUT}}) \end{aligned} \tag{7}$$

and

$$\begin{aligned} i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}} = &\quad i_{\mathrm{DC}+} - i_{\mathrm{DC}-} + i_{\mathrm{OUT}} - i_{\mathrm{C_{AUX}}} \\ = &\quad (C_{\sigma\mathrm{OUT}} + C_{\sigma\mathrm{GH}}) \cdot \tfrac{\mathrm{d}}{\mathrm{d}(t_7 - t_6)} v_{\mathrm{OUT}} \end{aligned} \tag{8}$$

Fig. 8 and Fig. 9, shows the comparison for the ground current measurements during turn-on and turn-off transients for the power modules A and B respectively for a double pulse test at DC-link voltage of 6 kV and load current of 14 A. In Fig. 8 and Fig. 9, $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$ is the current obtained utilizing the three module current measurements $i_{\mathrm{DC}+}$, $i_{\mathrm{DC}-}$ and i_{OUT} based on (6). The current i_{GND} is the measured current through the wire that is shorting a heatsink to the ground and $i_{\mathrm{GND(sim)}}$ is the simulated ground current obtained by implementing the power module output terminal to heatsink impedance network (as per Fig. 4) in LT Spice simulation. An image of the LT Spice simulation implementation is shown in Fig. 10, where

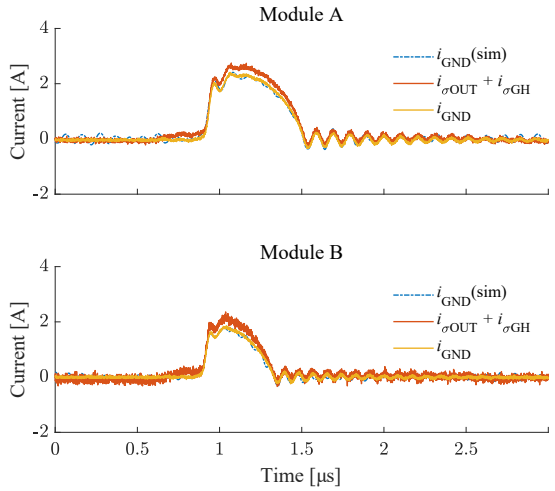


Fig. 8. Experimentally measured/extracted and simulated ground currents during turn-on switching transient for power modules A and B in the case where heatsink is shorted to ground. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A)

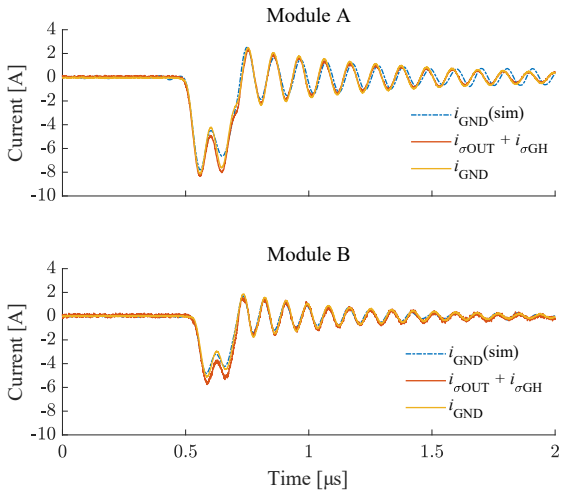


Fig. 9. Experimentally measured/extracted and simulated ground currents during turn-off switching transient for power modules A and B in the case where heatsink is shorted to ground. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A)

input to the simulation is measured half-bridge output voltage. The values of module parasitic capacitances used are extracted from the ANSYS Q3D (see Table I). The parameters R_{GND}, L_{GND} and C_{GND} for the grounding impedance Z_{GND} in this case are obtained form the impedance analyzer as 5 Ω, 700 nH and $\approx$ 0 pF.

For both power modules, measured and simulated ground current show good agreement in terms of their amplitude and frequency response in case of turn-on as well as turn-off switching transients. However, the amplitude of the measured current i_{GND} differ slightly from the $i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$. This difference is attributed to the common mode (CM) currents resulting from the capacitive couplings introduced by the circuits external to the power module such as the high side gate driver power supply ($\approx$ 4.8 pF) and voltage probe ($\approx$ 3 pF). As can be seen in Fig. 8, in case of the turn-on switching transient the peak amplitude of the ground current i_{gnd} for

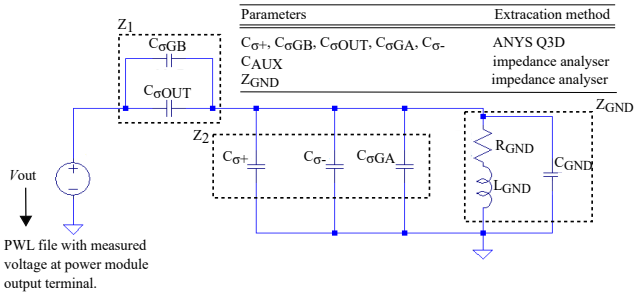


Fig. 10. Image of the LT spice simulation implementation.

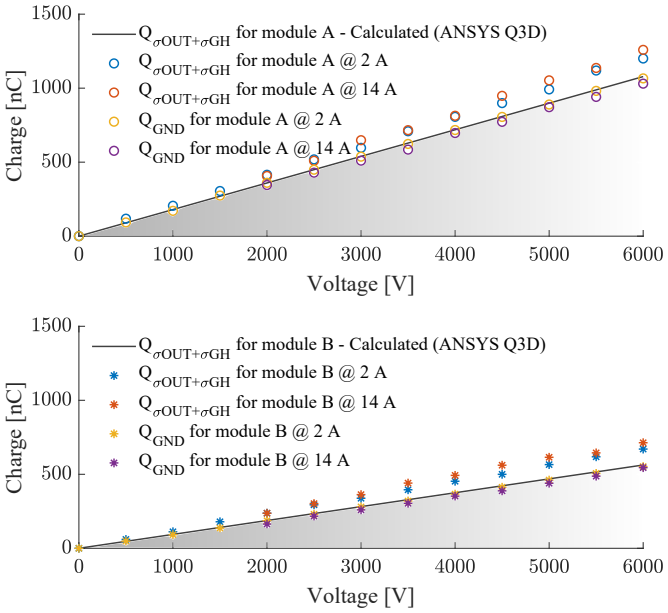


Fig. 11. Comparison of the experimentally obtained and analytically calculated charge for the power module parasitic capacitance $C_{\sigma\mathrm{OUT}}$, $C_{\sigma\mathrm{GH}}$.

module A is 2.4 A at the turn-on dv/dt of 11.2 kV/μs in comparison to the 1.8 A for module B at the turn-on dv/dt of 15.6 kV/μs. Similarly for the turn-off switching transient the absolute peak amplitude of the ground current for module A is 8 A at turn-off dv/dt of 30.7 kV/μs in comparison to 5 A at turn-off dv/dt of 39.3 kV/μs for module B.

The lower peak amplitude of the ground currents in module B in comparison to the module A even with high dv/dt, correlates with the reduced module parasitic capacitance for module B in comparison to module A. For the same DC-link voltage, load current level and gate resistance the turn-on and turn-off dv/dt is higher for the module B in comparison to module A. This is due to the influence of module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ on the voltage rise and fall times as will be discussed in Section VI and VII.

To further corroborate, the charge $Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for the module parasitic capacitances is calculated from double pulse test results using (9) and is then compared with the theoretically computed charge as in (10) utilizing the values of module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ presented in Table. I.

$$Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} = \int_{x}^{y} (i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}) \cdot \mathrm{d}t \tag{9}$$

(for turn on transient x = t_3 and y = t_4 and for turn-off transient x = t_6 and y = t_7.)

For the module parasitic capacitance, the stored charge increases linearly with the increase in DC-link voltage such that.

$$Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}(\mathrm{Calculated} \quad \mathrm{ANSYS}) = (C_{\sigma\mathrm{OUT}}+C_{\sigma\mathrm{GH}})\cdot V_{\mathrm{DC}} \tag{10}$$

In addition to this charge Q_{GND} is also calculated by integrating the measured ground current i_{GND}. Fig. 11 shows, the charge $Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$, Q_{GND} obtained using double pulse test results for DC-link voltage of up to 6 kV with load currents of 2 A and 14 A. The charge Q_{GND} show an excellent agreement with the theoretically computed charge. However, the charge $Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ show a values slightly higher compared to Q_{GND} (160 nC - 230 nC at 6 kV). This is attributed to the capacitive charge contributed by the circuits external to the power module such as the probe and gate driver power supply capacitance as discussed in previous Section. From the known value of the probe and gate driver parasitic capacitance of 3 pF and 4.8 pF respectively, the total charge due to the probe and gate driver capacitance is calculated to be 46.8 nC at DC-link voltage of 6 kV. With this charge added to the analytically obtained module parasitic capacitance charge measurement ($Q_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ - Calculated ANSYS), the maximum difference of 11.9 % and 16.9 % corresponding to the charge of 103 nC and 134 nC is left unaccounted for the modules A and B respectively. It is worth mentioning that this measurement discrepancy only gives approximately 10 pF to 15 pF of observable difference. This can in-fact be due to the undetected circuit stray capacitances, fine details of the current integration time window used to calculate the charge combined with the fine accuracy any measurements will have.

VI. Analysis of Impact of Module Parasitic Capacitance Impact on Turn-On Switching Energy Dissipation

To analyze the impact of the module parasitic capacitance on the overall turn-on switching losses, the turn-on switching energy dissipation E_{on} for the LS MOSFET is split into five segments. Each of these switching energy contribution is denoted as E_{on1}, E_{on2}, $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$, $E_{\sigma\mathrm{L}}$, $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ and is assigned as following.

Segment E_{on1} is the switching energy dissipation during the turn-on switching transient time interval t_1–t_2 and is given by,

$$E_{\mathrm{on1}} = \int_{t1}^{t2} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{11}$$

Whereas, E_{on2} is the switching energy dissipation during time interval t_2–t_4 due to the constant load current magnitude i_{L} ($i_{\mathrm{L}} = i_{\mathrm{OUT}(t_2)}$) and is obtained from,

$$E_{\mathrm{on2}} = \int_{t2}^{t4} i_{\mathrm{L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \quad \left[i_{\mathrm{L}} = i_{\mathrm{OUT}(\mathrm{t_2})}\right] \tag{12}$$

The switching energy dissipation E_{QOSS} and E_{rr} due to the joule heating resulting from a charging of the HS MOSFET and diode output capacitances as well as diode reverse recovery charge is obtained from,

$$E_{\mathrm{QOSS}} + E_{\mathrm{rr}} = \int_{t2}^{t4} i_{\mathrm{DC+}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{13}$$

Switching energy dissipation due to the displacement currents charging the power module and inductor parasitic capacitance can be obtained, using the current magnitudes ($i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}$) and $i_{\mathrm{C_L}}$. (from (2) and (4)

$$E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} = \int_{t3}^{t4} (i_{\sigma\mathrm{OUT}} + i_{\sigma\mathrm{GH}}) \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{14}$$

$$E_{\sigma\mathrm{L}} = \int_{t3}^{t4} i_{\mathrm{C_L}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{15}$$

The total energy dissipation E_{on} that is measured utilizing the module currents and voltage measurements is expressed as,

$$\begin{aligned} E_{\mathrm{on}} &= E_{\mathrm{on1}} + E_{\mathrm{on2}} + E_{\mathrm{QOSS}} + E_{\mathrm{rr}} + E_{\sigma\mathrm{L}} + E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}} \\ &= \int_{t1}^{t4} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \end{aligned} \tag{16}$$

To draw a comparison between the two layouts and understand the impact of the module parasitic capacitance on the turn-on switching performance, the split of turn-on switching energy dissipation as illustrated in Fig. 12 is calculated using (11)-(16) from the double pulse test results obtained using the experimental test bench.

Fig. 13 shows the split of turn-on switching energy dissipation for the DC-link voltage of 6 kV and load currents of 0 A – 14 A along with the turn-on dv/dt comparison for modules A and B. As can be seen in Fig 13, with increase in load current the tun-on dv/dt decreases. This is because, the voltage magnitude at which the gate-source voltage reaches the plateau

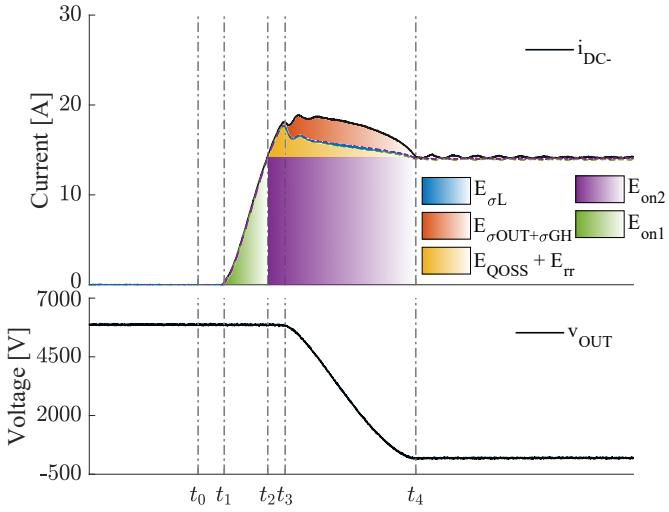


Fig. 12. Illustration of split in turn-on switching energy dissipation. (Test conditions V_{DC} = 6 kV, i_{L} = 14 A))

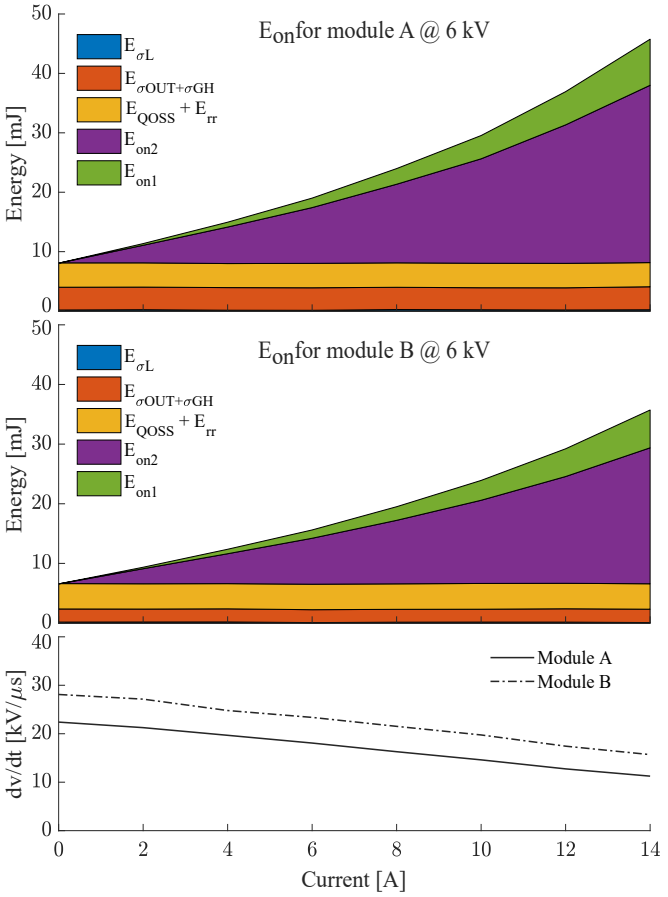


Fig. 13. Comparison of the turn-on switching energy dissipation E_{on} and dv/dt for modules A and B at DC-link voltage of 6 kV and load currents of 0 A – 14 A.

shifts towards the higher value with increasing magnitude of the load current. As the Miller plateau voltage shifts towards higher value, the voltage difference between the gate drive output voltage and gate-source voltage decreases. This results in the increased voltage fall time interval (t_3–t_4) due to lower magnitude of the gate current charging the reverse transfer capacitance C_{GD} and thus reducing the turn-on dv/dt.

Furthermore, for the same magnitude of the load current and similar experimental conditions the turn-on dv/dt, for the module A is lower than that of the module B, because module A in comparison to module B results in a higher plateau voltage during the Miller region as a result of the increased magnitude of the displacement current caused by the higher value of the module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ an $C_{\sigma\mathrm{GH}}$. Meaning the voltage fall time t_3–t_4 corresponding to the turn-on switching transient increases for module A in comparison to module B, resulting in a lower turn-on dv/dt for module A. At the DC-link voltage of 6 kV and load current of up to 14 A, the turn-on dv/dt for the module A is identified to be approximately 28 % lower compared to module B.

From the turn-on switching energy separation presented in Fig.13, the dependency of the E_{on1} and E_{on2} on the load current is noticeable. Both, E_{on1} and E_{on2} increase with the load current. As discussed E_{on1} is the switching energy

dissipation corresponding to the time interval t_1–t_2, where t_1 and t_2 relates to the time at which the gate-source voltage reaches the threshold and plateau voltage respectively. The increase in the $E_{\rm on1}$ for module A is attributed to the increase in time interval t_1–t_2 due to positive shift in the plateau voltage as discussed.

An indirect impact of the module parasitic capacitances on the turn-on switching performance can be clearly observed when comparing switching energy dissipation $E_{\rm on2}$ for both modules A and B. The higher magnitude of $E_{\rm on2}$ for module A in comparison to the module B is because of the lower turn-on dv/dt or increased voltage fall time interval $t_3 - t_4$ for module A as explained in previous text. An increase in the voltage fall time interval will lead to increase in $E_{\rm on2}$, since it is identified as the switching energy dissipation due to the constant load current magnitude over time interval t_2–t_4. For the DC-link voltage of 6 kV and drain current of 14 A, the $E_{\rm on2}$ for module A is 29.8 mJ which is approximately 7 mJ higher compared to module B. For a given DC-link voltage the E_{on2} increases with the load current, both because of the increase in load current magnitude as well as time interval t_3–t_4.

As can be noticed, that the capacitive losses $E_{\sigma \rm OUT+\sigma GH}$, $E_{\sigma \rm L}$ and $E_{\rm QCOSS}$ which occurs during time interval t_2–t_4 are load current independent. This is because the capacitive losses are not dependent on the time duration t_2–t_4, the change in the time interval will only result in the change in current magnitude with which the module and inductor parasitic capacitances are being charged or discharged, however the losses remain constant for a given DC-link voltage since the stored charge on the capacitor only changes with DC-link voltage.

For both modules A and B the measured switching energy $E_{\rm QCOSS} + E_{\rm rr}$ based on (13), is almost constant and is within the range of 4 mJ to 4.2 mJ for the DC-link voltage of 6 kV and load currents of upto 14 A. To further strengthen the analysis and understanding for $E_{\rm QCOSS} + E_{\rm rr}$, a detail comparison is drawn between the double pulse experimental results and static measurements for 10 kV SiC MOSFET and JBS diode obtained using the curve tracer.

Fig. 14a shows the output capacitance measurements as a function of voltage bias for a third generation 10 kV SiC MOSFET with an anti-parallel SiC JBS diode obtained utilizing the B1506 curve tracer. Due to the maximum output voltage limitation of 3 kV for the curve tracer, the capacitance for the voltage range of 3 kV – 5 kV is extrapolated using curve fitting. The charge $Q_{\rm OSS(Static)}$ is calculated from the curve tracer capacitance measurement data (see inset of Fig. 14a) and its comparison with the output capacitance and reverse recovery charge measurements obtained from the double pulse test based on (17) is presented in Fig. 14b for the DC-link voltage of up to 6 kV with the load currents of 2 A and 14 A.

$$Q_{\rm OSS} + Q_{\rm rr} = \int_{t2}^{t4} i_{\rm DC+} \cdot {\rm d}t \tag{17}$$

The combined output capacitance and reverse recovery charge obtained from the double pulse test almost coincide with the static output capacitance charge measurements for both the higher (14 A) and lower (2 A) extreme of load currents,

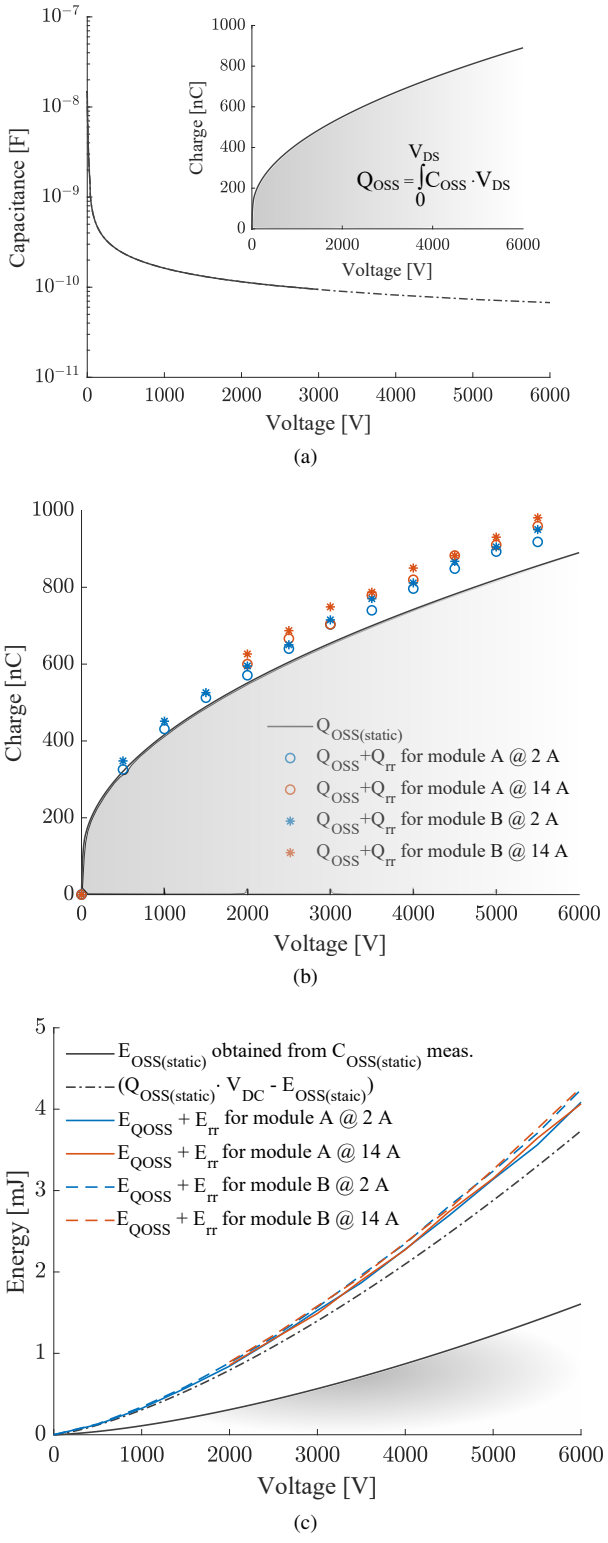


Fig. 14. (a) Output capacitance ($C_{\rm OSS(Static)}$) measurement for the 10 kV SiC MOSFETs and JBS diode obtained form B1506 curve tracer, (b) comparison of the output capacitance charge ($Q_{\rm OSS(Static)}$) with output capacitance as well as reverse recovery related charge obtained form the double pulse test setup (c) comparison of the stored energy on the output capacitance charge ($E_{\rm OSS(Static)}$) with switching energy dissipation $E_{\rm QOSS} + E_{\rm rr}$ for power modules A and B.

indicating almost no charge is present due to the diode reveres recovery. The charge $Q_{\mathrm{OSS(Static)}}$ increases with square root profile because of the non-linear behaviour of the MOSFET and JBS diode output capacitance as a function of bias voltage across it.

The measured $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ results for the DC-link voltage range of upto 6 kV and load currents of 2 A and 14 A are presented in Fig 14c. The switching energy dissipation E_{QOSS}, which is due to the charging current of the complementary or in this case HS device output capacitance passing through the voltage potential of the LS MOSFET (V_{OUT} = $V_{\mathrm{DC+}}$ - $V_{\mathrm{Q_H}}$). As a result the analytical prediction of the losses is $\int i_{\mathrm{OSS_H}} \cdot (V_{\mathrm{DC+}} - V_{\mathrm{Q_H}})$, which when simplified turns out to be $Q_{\mathrm{OSS}} \cdot \mathrm{V_{DC}} - E_{\mathrm{OSS}}$. Some may erroneously believe this energy to be E_{OSS} but note that this is note solely the energy stored in the output capacitance given by E_{OSS}. Therefore the switching energy dissipation $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ needs to be compared with $Q_{\mathrm{OSS(Static)}} \cdot \mathrm{V_{DC}} - E_{\mathrm{OSS(Static)}}$ and not $E_{\mathrm{OSS(Static)}}$. It is interesting to see that the measured $E_{\mathrm{QOSS}} + E_{\mathrm{rr}}$ almost coincide with the $Q_{\mathrm{OSS(Static)}} \cdot \mathrm{V_{DC}} - E_{\mathrm{OSS(Static)}}$ curve calculated from the static measurement leaving almost no room for the reverse recovery losses. This is in agreement with the dynamic charge measurements presented in Fig. 14b justifying negligible contribution of the diode reverse recovery to the total turn-on switching energy dissipation for the full range of the load currents. This is expected due to the excellent reverse recovery performance of the SiC JBS diode [35].

In Fig. 13, the clear difference is identified in the switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ for modules A and B. Switching energy dissipation $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ is approximately 3.8 mJ for module A in comparison to the 2.2 mJ for module B at the DC-link voltage of 6 kV. This accounts for about 8.3 % and 6.1 % of the measured total turn-on switching energy dissipation for modules A and B respectively. It should be noted that for a given DC-link voltage the percentage of $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ to the total turn-on energy dissipation will increase with reduced gate resistance, since with lower gate resistance the overall turn-on switching energy dissipation will reduce due to decrease in E_{on1} and E_{on2} as the voltage fall time shrinks but the capacitive losses $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ do not change. The switching energy dissipation $E_{\sigma\mathrm{L}}$ obtained using (15) is identical for modules A and B as expected and is measured to be in the range of 0.1 – 0.3 mJ for the DC-link voltage of 6 kV and load currents of upto 14 A. Relatively small magnitude of the $E_{\sigma\mathrm{L}}$ is due to the very low parasitic capacitance ($\approx$ 12 pF) of the air core inductor.

From the total turn-on energy dissipation for the power module A and B presented in Fig. 13, it can be seen that the difference in E_{on} for modules A and B is predominantly due to the variation in E_{on2} and $E_{\sigma\mathrm{OUT}+\sigma\mathrm{GH}}$ that result from the indirect and direct effect of module parasitic capacitances respectively. For the DC-link voltage of 6 kV and load current of 14 A the total turn-on switching energy dissipation for module A is 45.7 mJ which is about 22 % higher compared to 35.7 mJ for module B.

It is worth to note that the actual energy dissipation E^*_{on} for the turn-on switching transient is higher than the measured E_{on}. This is because the energy dissipation E_{OSS} as a result of the displacement current due to discharging of LS MOSFET and diode capacitance can not be measured at the DC– terminal of the power module since the current path is confined within the semiconductor itself. The common approach to this remedy is to add E_{OSS} obtained from the device datasheet or static measurement to the measured turn-on switching energy dissipation [34], expressed as (18).

$$E^*_{\mathrm{on}} = E_{\mathrm{on}} + E_{\mathrm{OSS(static)}} \tag{18}$$

VII. Analysis of Module Parasitic Capacitance Impact on Turn-Off Switching Energy Dissipation

The impact of module parasitic capacitance on the turn-off switching energy dissipation is discussed in this Section. Fig. 15, shows the turn-off switching energy dissipation for the DC-link voltage of 6 kV and load currents of 2 A – 14 A along with the turn-off dv/dt comparison for modules A and B. In contrast to the turn-on, for the turn-off switching transient the turn-off dv/dt increases with the increase in load current. During the turn-off switching transient it is the load current magnitude that determines the charging and discharging rate of the combined LS and HS output capacitance of the MOSFET and JBS diode. Therefore it is the load current magnitude that predominantly determines the voltage rise time t_6–t_7 and the gate resistance has very little or no influence. Because of this the turn-off dv/dt in Fig. 15 show almost a linear dependence on the load current magnitude. It is important to notice that during the turn-off switching transient displacement currents due to the module parasitic capacitance does not conduct through the MOSFET channel hence does not result in Joule heating, however it decreases the turn-off dv/dt at the half-bridge output terminal since module parasitic capacitance $C_{\sigma\mathrm{OUT}}$ and $C_{\sigma\mathrm{GH}}$ appear in parallel to the LS MOSFET that acts as a snubber. This is the reason that the turn-off dv/dt for module A is lower than that of the module B. For the case at hand, at the DC-link voltage of 6 kV and load current of 14 A the turn-off dv/dt for module A and module B is identified to be 30.7 kV/μs and 39.3 kV/μs respectively. The turn-off switching energy dissipation for both power modules A and B is obtained using (19). The E_{off} for both power modules is approximately similar ranging within 1.6 mJ – 1.9 mJ for the DC-link voltage of 6 kV and load current range of 2 A – 14 A.

$$E_{\mathrm{off}} = \int_{t6}^{t7} i_{\mathrm{DC-}} \cdot v_{\mathrm{OUT}} \cdot \mathrm{d}t \tag{19}$$

The turn-off switching energy dissipation for the 10 kV SiC MOSFET is significantly small compared to the turn-on switching energy dissipation. Furthermore, the impact of module parasitic capacitance on the turn-on switching transient is more profound since during the turn-off switching transient displacement currents due to module or circuit parasitic does not produce a Joule heating because these currents does not commutate through the MOSFET. An important thing to notice here is that, most of the current measured at DC– terminal during the turn-off transient is due to the charging of the combined output capacitance of the LS MOSFET and JBS diode which does not produce a Joule heating. The portion

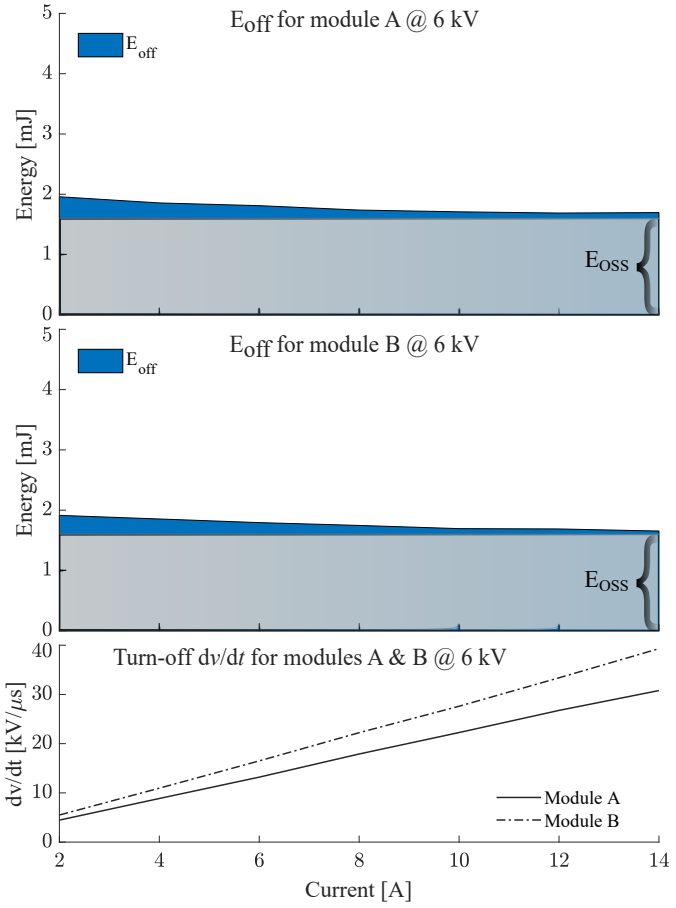


Fig. 15. Comparison of the turn-off switching energy dissipation E_{off} and v/dt for modules A and B at DC-link voltage of 6 kV and load currents of 2 A – 14 A.

of the drain current that flows through the MOSFET channel only contributes to the switching losses. Therefore, the actual switching energy dissipation E^*_{off} during the turn-off transient can be obtained as presented in (20) [34].

$$E^*_{\text{off}} = E_{\text{off}} - E_{\text{OSS(Static)}} \tag{20}$$

The comparison of the $E_{\text{OSS(Static)}}$ which is obtained from the curve-tracer capacitance measurements to the measured E_{off} presented in Fig. 15, reveal that the most of the portion of the measured turn-off switching energy dissipation contribute to the charging of the LS combined MOSFET and JBS diode output capacitance which is capacitive stored energy. This is also the reason that the turn-off losses for both modules almost are not influenced by the turn-off dv/dt and are same for both modules A and B regardless of the turn-off dv/dt.

VIII. Conclusion

This paper provides an in-depth understanding about the impact of power module parasitic capacitances on the SiC MOSFET switching transients in respect to losses and analyzes it quantitatively. An indirect method to obtain the displacement currents due to module parasitic capacitances during the MOSFET turn-on and turn-off switching transients utilizing the accessible power module current measurements is proposed and validated experimentally. Moreover, a simple approach of utilizing the heatsink impedance network to predict the power module parasitic capacitace induced displacement currents was also presented which confirm the high accuracy of the modelled impedance network and extracted parasitic parameters used for the analysis. The experimental results presented in this paper show that the power module parasitic capacitances results in significant magnitudes of the displacement currents, which can lead to increased conducted EMI potentially resulting in difficulties with meeting EMC standards in practical applications. The key contribution of the paper lays in analysing the power module parasitic capacitance induced displacement current paths for the turn-on as well as tun-off switching transients and specifically revealing the impact of the module parasitic capacitances on the switching performance by dissecting the switching energy dissipation with great accuracy. This is showcased based on the experimental results obtained using the custom packaged 10 kV half bridge SiC MOSFET power modules with different DBC layouts. It is shown that the impact of module parasitic capacitance of the turn-on switching energy dissipation is two-fold and is more pronounced in comparison to the turn-off switching energy dissipation. A comparison of the the module parasitic capacitance related switching energy dissipation to the overall switching energy dissipation presented for the DC-link voltage of 6 kV and load current upto 14 A show the significance of the module parasitic capacitance on the switching performance. Failing to account for the module parasitic capacitances in design can lead to incorrect assignments as well as considerable error in estimating switching energy dissipation. Thus the module parasitic capacitance should no longer be neglected for a SiC MOSFET enabled power electronic converter foreseen to be utilized in medium voltage fast switching applications.

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