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BY
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Advanced Modeling of SiC Power MOSFETs aimed to the Reliability Evaluation of Power Modules

By

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"Look up at the stars and not down at your feet. Try to make sense of what you see, and wonder about what makes the universe exist. Be curious."

Stephen W. Hawking

Preface

I would like to acknowledge the Centre of Reliable Power Electronics (CORPE), the Advanced Power Electronic Technology and Tools (APETT) project and the Department of Energy Technology at Aalborg University for making possible and supporting this Ph.D. project. I am also grateful for the funding received by Det Obelske Familiefond and Otto Mønsted Fond, which allowed me to attend several conferences and purchase laboratory equipment for my experimental setups.

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Finally yet importantly, I would like to thank, from the deepest of my heart, my family, for being the rock-solid foundation and sustenance of my curious and open-minded outlook, and my girlfriend Shawna, for sharing the journey on the road through this great life adventure.

Lorenzo Ceccarelli
May 12, 2019
Aalborg, Denmark

Abstract

Power semiconductor devices are the core element in every electronic power conversion system. During the typical 20-year lifespan of a power electronic (PE) application, the devices undergo a significant amount of stress from operating in normal and abnormal conditions. The temperature fluctuations generated by the device power losses are the most significant stressors, eventually leading to thermo-mechanical degradation and failure.

A new range of wide bandgap (WBG) power semiconductor devices, especially those based on Silicon Carbide (SiC) and Gallium Nitride (GaN), are rapidly evolving to replace Silicon-based components. SiC power MOSFETs are already widely manufactured and are becoming the device of choice in the design of many low-to-medium power (<1 megawatt) PE applications. These devices are especially promising for their high power density, high-voltage blocking capability and very fast switching. Nevertheless, the widespread diffusion of such devices is slowed down by their significantly higher cost and the lack of solid reliability data and accurate models to support optimized circuit design. Moreover, high power density comes at the cost of increased thermal stress, especially during short circuit events, which may lead to instabilities and degradation phenomena at a chip and package level.

It is important to bear in mind that advanced models and simulation tools for WBG devices, can support the reliable and optimized design of next-generation power converters. Therefore, this Ph.D. project aimed at developing compact electrothermal models to explore the normal and abnormal behavior of commercial SiC MOSFETs. The research activity started with the implementation and identification of a physical device model, based on earlier work and expanded with additional features, such as self-heating and short circuit behavior. Several SiC discrete devices and power modules have been characterized experimentally in a wide range of operating conditions, providing data to validate the device model. Besides, realistic package models have been created using Finite-Element Analysis (FEA) software, in order to extract lumped circuit elements to couple with the device model, obtaining fast and accurate electrothermal simulations. The combined use of different software environments (e.g. PSpice, MATLAB/Simulink and ANSYS) allowed the optimization of computation time and co-simulation of different timescales. The main outcome of the project has been the implementation of advanced models for commercial SiC MOSFET devices and power modules. Moreover, the simulation results have provided a better understanding of the short circuit behavior and thermal instabilities in SiC power modules, the estimation of the device thermal loading during real mission profiles for DC-AC converter applications, and the impact of aging conditions on the device performance.

Dansk Résumé

Effektelektroniske komponenter er kerneelementet i alle elektroniske strømkonverteringssystemer. I mellem den typiske 20-årige kraftelektronisk applikations levetid, undergår komponenterne en betydeligt beløb af stress fra drift i normale og unormale tilstand. Temperaturfluktuationerne, der genereres af komponents effekttab, er de vigtigste stress-faktorer, som endelig fører til termomekanisk nedbrydning og nederlag.

En ny serie af "wide bandgap" (WBG) komponenter, især dem, der er baseret på siliciumcarbid (SiC) og galliumnitrid (GaN), udvikler sig hurtigt for at erstatte siliciumbaserede komponenter. SiC power MOSFET'er er allerede bredt fremstillet og bliver de præfererede komponenter i designet af mange lav-til-medium strøm (<1 megawatt) kraftelektronisk applikationer. Disse komponenter er især lovende for deres højeffektdensitet, højspændingsblokerende kapacitet og meget hurtig kommutation. Alligevel forsinker den udbredte diffusion af SiC MOSFETs deres højere omkostninger og manglen på solide pålidelighedsdata og præcise modeller til understøttelse af optimeret design af effektomformere. Desuden skaber høj effekttæthed øget termisk stress, især i tilfælde af en kortslutning, som kan føre til ustabilitet og nedbrydning fænomener på en chip og indkapsling niveau.

Det er vigtig at huske, at udviklingen af avancerede modellerings- og simuleringsværktøjer til WBG-komponenter kan understøtte det pålidelige og optimerede design af næste generations kraftomformere.Formålet med dette Ph.D. projekt er at udvikle kompakte elektrotermiske modeller for at undersøge den normale og unormale opførsel af kommercielle SiC MOSFET'er. Forskningsaktiviteten startede med implementering og identifikation af en fysisk enhedsmodel baseret på tidligere arbejde og udvidet med yderligere funktioner, såsom selvopvarmning og kortslutningsadfærd. Flere SiC diskrete komponenter og strømmoduler er blevet karakteriseret i laboratoriet i en bred udvalg af driftsbetingelser, der giver data til validering af modellen. Fokus har været på skabelsen af realistiske indkapsling modeller ved hjælp af Finite-Element Analysis (FEA) software og udvindingen af klumpede elementer, som giver hurtige og præcise elektrotermiske simuleringer. Den kombinerede brug af forskellige softwaremiljøer (fx PSpice, MATLAB / Simulink og ANSYS) tillod optimering af beregningstid og co-simulering af forskellige tidsskalaer. Hovedresultatet af projektet var implementeringen af avancerede modeller til kommercielle SiC MOSFET-enheder og strømmoduler. Resultater af simuleringerne har bl.a. givet en bedre forståelse af kortslutningsadfærd og termiske ustabiliteten i SiC-effektmoduler, estimeringen af termiske stress under ægte mission-profiler til DC-AC kraftomformere og virkningen af aldringsbetingelser på komponent ydeevne.

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Chapter 1
Introduction

1.1 Background

Power electronics (PE) can be defined as the application of solid-state electronics to the conditioning, control and conversion of electric power. As the demand for electricity and the concern for environmental protection grow worldwide, PE is playing an increasingly important role in modern society. Most of the electrical power used nowadays flows through power conversion systems, ranging from household appliances and automotive to high-power, grid-connected applications. It is especially required in the booming market of renewable energy sources, which is estimated to triplicate in size in the next few decades [1]. The PE market was valued at USD 36.93 Billion in 2017 and is expected to reach USD 51.01 Billion by 2023, at a compound annual growth rate (CAGR) of 5.5% [2]. Power conversion includes both voltage conversion (AC-DC, DC-AC, DC-DC, AC-AC) and frequency conversion (AC-AC). The energy conversion efficiency of such systems is typically 85-95%, whit the remaining 5-15% lost as heat. Power semiconductor devices are the core component of all power electronic systems and in most cases the responsible for the largest share of losses in the system [3]. With the wide spread use of electronics in the industrial, consumer and transportation sectors, the study and development of power semiconductor devices has a major impact on the evolution of PE systems, their efficiency and their reliability.

The research for more powerful and efficient electronic devices travels along two parallel paths. On the one hand, the requirement for high power and reduced size/weight has increased in many applications, which has led to the design of compact power modules, embedding multiple devices in a relatively small package [4], [5]. On the other hand, the study and manufacturing of wide bandgap semiconductors, among which Silicon Carbide (SiC) and Gallium Nitride (GaN), moves towards the development of a new generation of devices [6]–[8]. Some of these devices have already reached a quite advanced stage and are now commercialized by many manufacturers. They are capable of withstanding high-temperature and high-voltage operations with great efficiency and enhanced power density.

The development of such new technologies has introduced a number of new

challenges. First, the cost reduction to enable their diffusion in the market. Second, but equally important, the study of the reliability of both single-chip - or discrete - devices and multi-chip modules, specifically by means of advanced simulation tools, is a crucial aspect for the diffusion of these new technologies in the application field, where a guaranteed lifetime and ruggedness to abnormal conditions are always a requirement.

1.1.1 Wide bandgap semiconductors: a new era

The world of PE devices has been dominated by silicon (Si) based technology for over 50 years. The development of power metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs), together with the improvement of computer-aided device simulation, has greatly improved the performance of power switching devices over the last three decades. Despite that, though, Si technology exhibits some relevant limitations, especially concerning voltage blocking capability vs. conduction power loss, switching performance and high temperature operation, which are intrinsically limited by its material properties. At present, the highest blocking voltage rating for commercial devices is 6.5 kV [9], while the current rating for multi-chip power modules goes as far as 3 kA. The use of Si-based devices beyond such power rating is hindered by the aforementioned limitations and affects the overall efficiency of the power converter, requiring, at the same time, expensive, bulky and complex cooling systems and passive components. Figure. 1.1 [10], from Iannuzzo et al. in 2014, shows the use of different types of PE

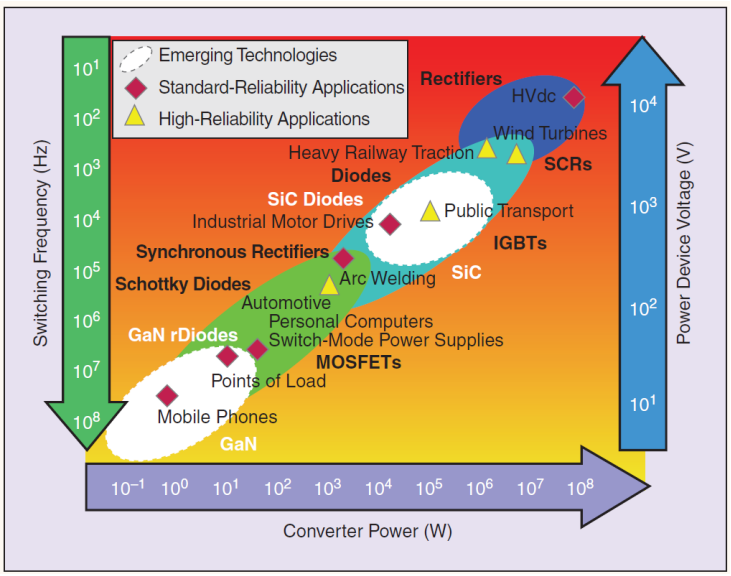


Figure. 1.1. Power semiconductor device application map [10].

switches in applications, related to the power output rating and the switching frequency, as well as their blocking voltage. One can clearly observe how the panorama for Si-based devices is in the range of 10 MW output power at low switching frequencies (<1 kV) and to 100 kHz for low power applications (<10 kW). Nevertheless, increased switching frequency is always desired in power converter applications, since it allows reducing the size of passive components such as transformers and capacitors, as well as the bulk of cases and PCBs. Additionally, a number of industrial, automotive and aerospace applications require power converters to operate at temperatures significantly larger than 200°C, way beyond Si limitations.

Over the past 20 years, a new class of power devices, based on the so-called wide bandgap (WBG) semiconductors, has emerged, demonstrating a number of extremely promising properties. At present, SiC and GaN are by far the ones showing the best tradeoff between material characteristics and maturity of their manufacturing technology [11]. It is worth to note, that the SiC lattice polytipe referred to in this work is 4H-SiC, which, at present, is yielding the best manufacturing outcome for power devices. A comparison of several significant material properties of Si, SiC and GaN is provided in Table 1.1. The larger bandgap of these materials results in a higher critical electric field, enabling the design of power devices with thinner and highly doped drift regions, meaning lower conduction energy loss. Although GaN offers better high frequency and high voltage capability, the manufacturing of good-quality substrates, suitable for HV vertical devices, is still hard to achieve and its thermal conductivity is lower compared to SiC. Looking at Figure. 1.1, currently off-the-shelf WBG devices occupy an area of influence that partly overlaps the ones of Si MOSFETs and IGBTs, but has a perspective margin of improvement towards higher switching frequency and power rating. It is important to notice that the scenario for GaN devices has evolved in recent years, reaching up to 650 V.

At present, SiC is widely acknowledged as a potential replacement to its Si counterparts in the HV, medium-power department. Figure 1.2 shows the development of the SiC power device market in several application fields from 2016,

TABLE 1.1 – SEMICONDUCTOR MATERIAL PROPERTIES

Property	**Silicon**	**4H-SiC**	**GaN**
Bandgap (eV)	1.1	3.26	3.45
Breakdown (x10^6 Vcm^{-1})	0.3	3	>1
Carrier Mobility (cm^2/V s^{-1})			
Electron	1500	1140	1250
Hole	600	50	850
Thermal Conductivity (W/cm K^{-1})	1.5	4.9	1.3
Melting Point (K)	1693	3103	2773
Thermal Expansion (x10^6 K^{-1})	2.6	4.2÷4.68	5.6

projected until 2022, in the analysis carried out in [12]. The market CAGR will soon reach 40%, with a significant expansion in the PV and EV sectors. The research and development activity on this field has already yielded devices with voltage ratings up to 15 kV [13], [14] and power modules with current ratings up to 600 A, and demonstrated their improved efficiency in applications ranging from low-voltage battery chargers to plug-in electric vehicles powertrains and grid-connected PV inverters [15]. SiC material properties make it an excellent choice for the construction of unipolar switching devices, such as MOSFETs or JFETs, and Schottky Barrier Diodes (SBD), based on a metal-semiconductor interface. In particular, the SiC MOSFET has reached an advanced state of maturity and many manufacturers worldwide (among which Wolfspeed, Rohm, Infineon, STMicro, and others) have reached the 3rd generation for their devices. As a unipolar switch, the SiC MOSFET features all the advantages of the traditional Si MOSFET (fast switching, excellent controllability, reverse conduction capability) and of the Si IGBT (high power density with low conduction losses). On the other hand, it does not exhibit some of the IGBT's main disadvantages (bipolar charge recombination, high conduction losses) [16].

These characteristics have a big potential for the optimized design of more power-dense converters where higher switching frequency, reduced volume or higher efficiency are required and can pay off the additional cost for SiC components. In fact, SiC power devices (and in general WBG devices) are sold at roughly 2÷5 times the cost of Si components, which significantly hinders their diffusion in many fields where cost constrains matter. This is mostly due to a still inefficient supply chain, with scarce availability of SiC epi-wafers in large scale and low price, as argued in [17]. The growing volume and demand in the market will allow chip manufacturers to implement an economy-of-scale, obtain wafers at lower prices, or rearrange Si facilities for SiC devices, which might significantly reduce the cost.

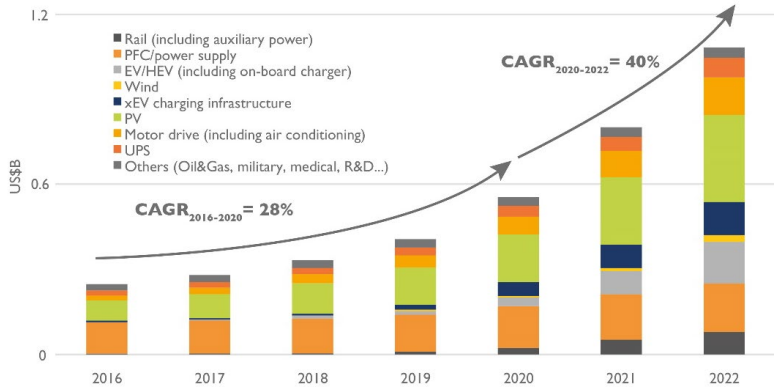


Figure 1.2. SiC device market size split by application (Source: Power SiC: Materials, Devices, Modules, and applications report, Yole Développement, August 2017)

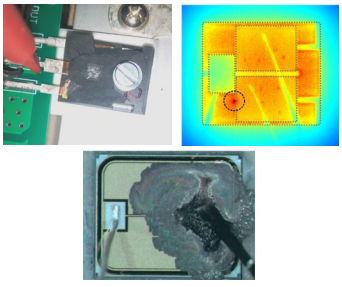
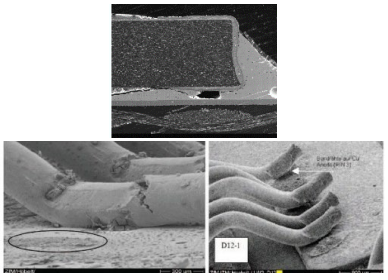
The other great question is whether SiC (and GaN) devices could ever match and exceed Si state-of-the-art reliability and robustness level in relationship to the specific applications.

1.1.2 Reliability of modern power semiconductor devices

As PE systems complexity evolves to reach greater efficiency and power density, the requirement for reliability have become stricter in many application, especially within automotive and aerospace industries. At the same time, the energy sector is following this path and especially focusing on cost-effective and sustainable solutions for improved reliability [18].

Substantial efforts have been invested in the reliability assessment of grid-connected converters, especially for photovoltaic (PV) energy generation [19]. A five-year operation field report conducted in 2008 from a 3.5 MW PV plant, ascribes to the inverter as much as the 34% of the unscheduled maintenance events and 59% of the unscheduled maintenance costs [20]. These shares are much bigger than the

TABLE 1.2. COMMON FAILURE MODES IN POWER DEVICES

Failure Modes			
Device Level		**Package Level**	
Catastrophic	Wear-out	Catastrophic	Wear-out
Thermal Instability	Oxide Degradation	Over-temperature (melting)	Bond-wire Fatigue
Overvoltage	Voltage Threshold Drift	Partial Discharge	Solder Fatigue
Overcurrent	Epitaxial Dislocations		Substrate Creeping
Cosmic Ray Failures	Metallization Degradation		
Activation of Parasitic Devices	Passivation Degradation		
			

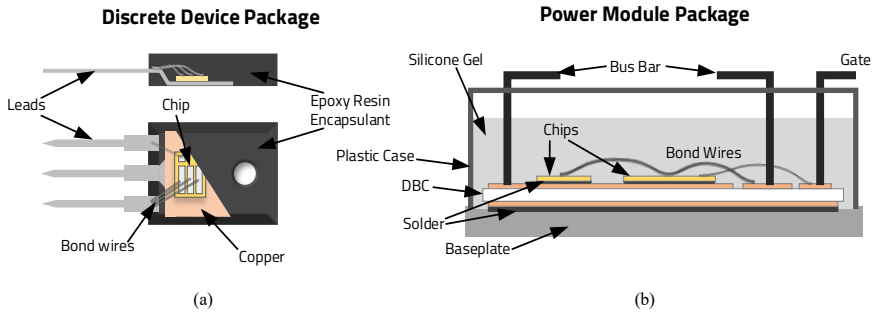


Figure 1.3 Packaging technologies: single-chip discrete device TO-247 package (a); cross section of a multi-chip power module (b).

single contributions from other subsystems like PV panels, data acquisition system, etc. Another survey on reliability in PE converters [21], carried out in 2011, reports that the most frangible components in a converter are, in fact, the power switching devices (34%), followed by capacitors (20%). Therefore, when approaching the system-level reliability prediction, a deeper insight on the component-level reliability and lifetime modeling has to be sought.

Table 1.2 reports the most common failure modes on device (chip) and package level. These can be divided into two subcategories: catastrophic failures and wear-out failures. The former are those failures occurring in the time range of micro- to milliseconds, often unpreceded by any indicator, whereas the latter are related to the device ageing over its operational life, and are always characterized by a slow and detectable degradation process. Many catastrophic failure modes in devices, such as overvoltage, overcurrent and cosmic ray failures, are due to external events – i.e. occurring outside the device packaging- and evolve into self-sustaining internal phenomena [10]. Other chip failures are related to internal instabilities, like thermal unbalances between the device elementary cells or activation of intrinsic parasitic devices (e.g. IGBT's thyristor latch-up or MOSFET's BJT turn-on). Device wear-out failure include oxide-semiconductor or oxide-metal interface degradation; charge migration to/from the oxide resulting in threshold voltage shift; lattice dislocations in the epitaxial layer or the substrate due to poor wafer quality; damage to the top metallization and passivation. So far, WBG devices have most of their device-level failure modes in common with their Si counterparts. In some cases, though, since their manufacturing technology has not reached an advanced stage yet, some of these failure modes tend to occur more frequently and have not been solved or mitigated. For example, the short circuit (SC) ruggedness of SiC power MOSFETs is still a critical issue, with SC withstanding time at nominal voltage much lower than the 10 microseconds required in many applications [22].

The package also heavily influences the reliability of power semiconductor devices [23]. It has to fulfill a series of purposes, all vital for the device operation, such as ensuring electrical connection/insulation between one or more

semiconductor chips and the external circuit; dissipating the heat generated during chip operation to a cooling system; protecting the chip from harmful ambient conditions. Figure 1.3 depicts two of the most common packaging technology used nowadays for power semiconductor chips and the ones studied in this project. The so-called *discrete device* package pictured in Figure 1.3.a, in this case a TO-247 type, is commonly used for components rated below 100 A and 1.2 kV. In this kind of packages, the chips are soldered on a copper lead frame and connected to the other leads via wire bonding. A molded plastic encapsulant, such as epoxy resin, is used to protect and isolate the chip. The *multi-chip power module* technology, whose cross section is depicted in Figure 1.3.b, is adopted for higher power ratings or in order to achieve specific circuit layouts. Here, the chips are soldered on an electrically insulated copper trace. The traces and chips are interconnected via bond wires (commonly made of Al) and the main power and control leads protrude from the module plastic case. The modules are filled with insulating and protecting silicone gel. The *direct-bonded copper* (DBC), consisting in a ceramic substrate sandwiched between two copper layers, allows the insulation, while at the same time providing a good thermal conductive path towards the baseplate. The module is mounted on a heat dissipation system, most likely a heat sink, via the baseplate, with a thermal interface material, in between, e.g. thermal grease. For current ratings above 5 kA, mostly for grid-connected PE applications, the power module is sometimes replaced by press-pack components, where the semiconductor is mounted between two metal discs and thermal and electrical contacts are ensured by pressing them instead of use solder. In addition, many new packaging technologies are emerging, such as flip-chip, press-fit, double-sided cooling or DBC substrate-based molded power modules.

Package-level catastrophic failures are mostly connected to excessive temperature stress, originating from the ambient or produced by the chips within the package, and leading to melting or vaporization of the internal metallic structures or the plastic casing. Moreover, overvoltage or poor design, i.e. not respecting a proper creepage distance between components at different electric potential, can determine a destructive breakdown in the dielectric, e.g. arcing or partial discharge.

The main wear-out failure mechanisms of power semiconductor packaging are induced by thermal stress. The mismatch in coefficient of thermal expansion (CTE) between the different material stacked up in the package determines stress and strain during the intermittent operation of the power switches. Bond wires lift-off, heel cracking, solder joint fatigue and substrate/baseplate cracking are some of the most common failure modes observed in power modules [24]. In particular, bond wires and chip solder are the most critical areas of degradation, being exposed to the full temperature swing caused by the chip self-heating [25]. The degradation process has been extensively studied in the case of Si IGBT modules and several lifetime modeling techniques have been introduced, both physical [26] and empirical [27].

Nowadays, the packaging technology for commercial SiC MOSFET power modules is, in fact, mostly identical to the one widely used for Si IGBT modules. This solution has been adopted by most of the manufacturers to guarantee the

compatibility of their modules with already-existing PE system designs and have better acceptance by the end users. This brings a huge limitation to the exploitation of the full potential of SiC technology due to larger electrical parasitic elements – e.g. stray inductances and capacitive coupling – that worsen the switching performance and, thus, the overall efficiency. However, this also means that the same degradation and failure mechanisms have been observed in SiC modules [28], and bond wire damage and solder degradation are still the predominant causes of thermally-induced failure and ageing. Despite this fact, the operational conditions that make SiC devices a better choice over Si ones, i.e. high temperatures and harsh environments, present a much bigger reliability challenge, since the stress on the package is higher. Thus, it is crucial to carry out a proper lifetime estimation for these new components, in order to assess whether or not they offer acceptable long-term performance. This can be investigated experimentally by performing a series of reliability tests, i.e. power cycling, temperature cycling, SC testing, high-temperature reverse/gate bias (HTRB/HTGB), and others [4]. At the same time, the evolution of advanced modeling and simulation tool can significantly aid the researchers in studying the device performance. A large effort has already been dedicated to the creation and validation of compact WBG device models within circuit-based simulation environment (e.g. PSpice, LTspice, Saber, Plecs, etc.), as well as more detailed finite element method (FEM) models meant for TCAD software. However, a deeper understanding of the device's physics and intrinsic limitations, as well as their mission profile, is most needed in order to obtain meaningful simulation results and

1.2 Aim of the Project

The aim of this Ph.D. project is to investigate the reliability and ruggedness of PE devices and modules through the modeling of SiC power MOSFETs. The project methodologies are specifically oriented towards compact circuit-based modeling, finite-element method (FEM) simulation techniques, an corroborated with extensive experimental characterization and testing of commercially available devices, performed in the laboratory under a wide range of operating conditions. The knowledge acquired from the characterization activity will be employed in the development of new and more complete models, accounting for detailed electro-thermal behavior, abnormal and degradation phenomena, as well as the implementation of a method for the fast and accurate reliability prediction of SiC MOSFET power modules.

1.3 Scientific Questions

The Ph.D. project aims to investigate what the current reliability and robustness challenges are in the emerging market of SiC power MOSFETs and how electro-thermal modeling and simulation can actually boost their optimized and reliable design. Accordingly, the project´s research questions are listed as follows:

- How can the electro-thermal behavior of SiC MOSFETs be described by means of compact physics-based device models under normal and abnormal operation? Are such models equally suitable for multi-chip power modules? How can the model parameters be properly identified?
- What is the state-of-the-art short-circuit robustness of commercial SiC power MOSFETs? Can simulation help estimating the junction temperature and identifying the failure modes? Additionally, how can the short-circuit capability be enhanced?
- How can we enable the fast system-level simulation of SiC-based power converters? How can we perform mission-profile based analysis and lifetime prediction on a very large timescale, preserving the accuracy of the device-level model?

1.4 Objectives

In order to answer the aforementioned scientific questions, the presented Ph.D. project focuses on:

- The study and development of advanced modeling approaches for SiC power MOSFETs, ranging from the single device to high power modules, oriented to the reliability prediction and evaluation. The focus is specifically on the implementation, identification and experimental validation of compact electro-thermal models.
- The study of SiC MOSFETs short-circuit behavior and better understanding of their failure modes. Additionally, the device model should feature short-circuit behavior and be able to describe the abnormal condition (with specific focus on the junction temperature) in both discrete devices and power modules. A parametric study of the device internal structure may offer an insight on how to mitigate or suppress the failure modes.
- Assess the accuracy and performance of the models by means of multi-physics FEM simulations, extensive experimental characterization and testing of commercially available devices, performed in the laboratory under a wide range of normal and abnormal operating conditions.
- The implementation of a fast and accurate converter-level electro-thermal model, suitable for the simulation of long or very-long timescales. More specifically, a mission-profile based lifetime estimation algorithm, oriented to the reliability evaluation of SiC power modules, needs to be developed.

1.5 Limitations

SiC technology is rapidly evolving and penetrating the PE market. Many manufacturers and research facilities worldwide achieve new device structures and module layouts almost on a monthly basis. Devices technology evolution advances in parallel with the availability of better and better quality semiconductor wafers and

doping implantation techniques. Many manufacturers have now reached their 3rd generation SiC devices and started adopting trench [29] and super-junction technologies [30], which are soon to be commercialized. Different device structures may result in different electric behavior and require dedicated models and characterization.

On the other hand, very compact packaging solutions, such as flip-chip, press-pack, molded modules or double-sided cooling, optimized for WBG devices, are emerging - although the packaging for off-the-shelf part numbers is roughly the same as for Si technology. Such an ever-changing scenario poses the biggest challenge for reliability evaluation. An extensive power cycling campaign may last for several months or years, which might rapidly make the devices under test obsolete. Therefore, reliability documentation about SiC devices is still scarce, which hinders the development and validation of accurate lifetime models.

This goes in addition to all the limitations normally connected to reliability analysis and lifetime prediction. Although thermo-mechanical wear-out failure modes have been considered here, these are not the only stressors the component undergoes during its lifetime. An extensive study of multi-stressors failure mechanisms – such as voltage, humidity, vibrations etc. – is out of the scope of this project. Moreover, the lifetime and damage accumulation models are taken from the available literature and applied to the presented electro-thermal simulation strategy.

In conclusion, the purpose of this work is to provide general-purpose modeling and simulation tools for the reliability and robustness study of SiC power MOSFETs rather than focusing on a specific technology, while necessarily relying on a series of assumptions and trying to quantify the resulting inaccuracies.

1.6 Thesis Outline

This Ph.D. thesis sums up the outcome of the Ph.D. project, in the form of "collection of papers". Therefore, the document is structured in two parts: *Report* and *Selected Publications*. The report is organized into six chapters. Chapter 1 has provided the introduction of the Ph.D. thesis, stating the background and the scientific questions connected to the project, as well as the research objectives and the list of publications. The device-level modeling and simulation of SiC power MOSFETs are described in Chapter 2. The device physical normal and abnormal behavior is briefly introduced and thus followed by the model description and implementation. A special attention is given to the characterization short-circuit operation. Additionally, the parameter extraction method and experimental validation process are reported. In Chapter 3, the model implementation and validation for both discrete devices and multi-chip power modules is addressed using two Case Studies (I and II) involving commercial devices. The effect of package parasitics on normal and abnormal switching operation is also considered. Once the full device modeling procedure has been presented, the development of a fast and accurate simulation strategy for SiC-based switching applications is addressed in

Chapter 4. The chapter focuses on Case Study III, where a full-SiC module is chosen for the converter-level simulation of a three-phase inverter. Chapter 5 moves towards the mission-profile based reliability prediction for SiC power MOSFET modules, demonstrating that the fast simulation strategy can be suitable for large timescales and support the reliable design of power converters featuring this technology. Finally, a discussion of the project outcomes and concluding remarks are summarized in Chapter 6 together with the perspective future research on this topic. Additionally, a subsection of this last chapter deals with a side topic, which the candidate has encountered during the study period, yielding interesting findings worth to be mentioned briefly.

1.7 List of Publications

The research outcomes of this Ph.D. project have been disseminated in the form of journal articles, articles in conference proceedings and book chapters. Together with the publication in which the candidate figures as first author, other works containing his relevant contribution are reported in this Ph.D. thesis. The publications are listed below.

Publications in Conference Proceedings

[C1] L. Ceccarelli, F. Iannuzzo, and M. Nawaz, "PSpice Modeling Platform for SiC power MOSFET Modules with Extensive Experimental Validation," in *Proc. of 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[C2] M. M. Hossain, L. Ceccarelli, A. U. Rashid, R. M. Kotecha, and H. A. Mantooth, "An Improved Physics-based LTSpice Compact Electro-Thermal Model for a SiC Power MOSFET with Experimental Validation," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, pp. 1011–1016, 2018.

[C3] L. Ceccarelli, P. D. Reigosa, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "Compact electro-thermal modeling of a SiC MOSFET power module under short-circuit conditions," in *Proc. of IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 4879–4884, 2017.

[C4] L. Ceccarelli, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "A Fast Electro-Thermal Co-Simulation Modeling Approach for SiC Power MOSFETs," in *Proc. of the 32nd IEEE Applied Power Electronics Conference and Exposition*, Tampa, USA, pp. 966–973, 2017.

[C5] L. Ceccarelli, R. Kotecha, F. Iannuzzo, and A. Mantooth, "Fast Electro-thermal Simulation Strategy for SiC MOSFETs Based on Power Loss Mapping," in

Proc. of 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), 2018.

Journal Articles

[J1] L. Ceccarelli, P. D. Reigosa, F. Iannuzzo, and F. Blaabjerg, "A survey of SiC power MOSFETs short-circuit robustness and failure mode analysis," *Microelectronics* Reliability, v. 76–77, pp. 272-276, Sep. 2017.

[J2] L. Ceccarelli, R. Kotecha, F. Iannuzzo, "Impact of Device Aging in the Compact Electrothermal Modeling of SiC Power MOSFETs," *Microelectronics Reliability*, accepted for publication, Apr. 2019.

[J3] L. Ceccarelli, R. Kotecha, F. Iannuzzo, and A. Mantooth, "Mission-profile-based lifetime prediction for a SiC MOSFET power module using a multi-step condition-mapping simulation strategy", in *IEEE Transactions on Power Electronics,* Jan. 2019.

[J4] L. Ceccarelli, H. Luo, and F. Iannuzzo, "Investigating SiC MOSFET body diode's light emission as temperature-sensitive electrical parameter," *Microelectronics Reliability*, v. 88-90, pp. 627-630, Sep. 2018.

Chapter 2
Operation and Modeling of SiC Power MOSFETs

2.1 Power MOSFET Structure and Operation

The earliest Field-Effect Transistor (FET) was patented back in 1925 by J. E. Lilienfeld. Later on, in 1959, the first *Metal-Oxide-Semiconductor Field Effect Transistor* (MOSFET) was theorized and invented at Bell Labs [31]. Nowadays, the power MOSFET is the most commonly used power semiconductor controllable switch for low and medium power applications, up to several kilowatts [32]. It is widely spread in household appliances, power supplies and automotive power electronics. Its operation as power switch does not essentially differ from the low voltage MOSFETs, which are used in digital integrated circuits. Their structure, though, in order to achieve high voltage blocking capability, has evolved into the so-called vertically double-diffused MOSFET (VD-MOSFET) layout. The maximum blocking voltage capability for Si-based MOSFETs available off-the-shelf nowadays is limited to approximately 600 V, because of the significant on-state power loss introduced by thicker epitaxial (EPI) layers.

The vertical cross-section of a state-of-art power MOSFET's cell is depicted in Figure 2.1.a. This structure is defined *enhancement mode*, planar *n-channel* VD-MOSFET. The *gate* and *oxide* structures are placed on top of the semiconductor epi-layers. The power terminals are the top metallization or *source*, and the bottom surface of the heavily n-doped *substrate*, named *drain*. When the gate terminal is protruding into the semiconductor material, like in Figure 2.1.b, the structure is called *trench* or vertical n-channel U-MOSFET (because of the U-shaped gate structure), with a number of advantages in the achievable power density (the cell width is reduced) and reduced losses. Several thousands of these elementary cells (few μm wide) are paralleled into a chip to increase the current capability of the device.

When a negative voltage is applied across drain and source the p+/n-/n+ structure becomes forward biased and the device starts behaving like a diode. It is important to take into account the presence of this intrinsic or *body diode* when designing circuits with power MOSFETs. The diode structure is often optimized by the manufacturer to avoid the use of external diodes – for example as freewheeling

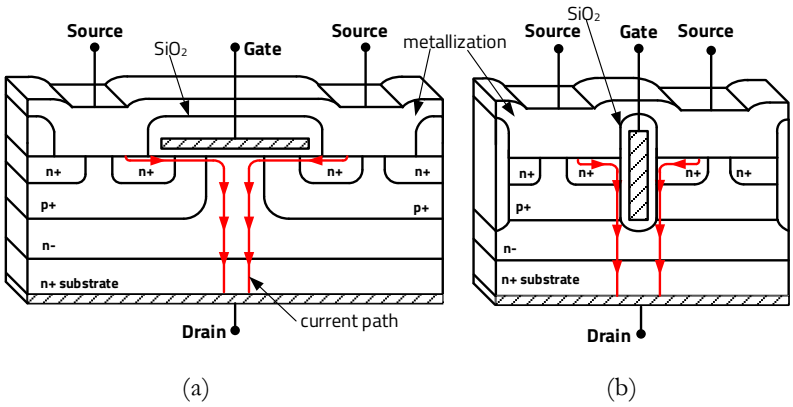


Figure 2.1. Cross-section of a horizontal, n-channel power MOSFET's cell (a), cross-section of a trench power MOSFET structure (b).

current paths in power converters – although its conduction and switching performance is always well below that of a state-of-the-art power diode because of its peculiar geometry.

The structure and operation of SiC power MOSFETs does not differ much from that of their Si counterparts. The wide energy bandgap of SiC, though, as mentioned in Chapter 1, allows for a much thinner and narrower cell structure with both planar and trench technology [33]. Therefore, although the normal on-state, reverse conduction and switching behavior, resembles closely that of a Si power MOSFET, the instabilities and failure modes occurring outside the device Safe Operating Area (SOA), are yet to be fully understood and mitigated.

2.1.1 Short Circuit Operation and Failure Modes

SiC devices come with significantly smaller die size and higher current density in comparison to traditional Si devices. For example, a commercial 2nd-generation 1.2 kV / 36 A SiC MOSFET chip [34] measures 10.4 mm^2 against the 41.4 mm^2 of a Si IGBT with equivalent rating [35], with an almost four times higher current density. The design of power semiconductor chips aims to miniaturization, in order to maximize production, optimize costs and fully exploit the material properties. With SiC, this is possible thanks to the aforementioned physical characteristics, but inevitably leads to a higher thermal stress on the device during both normal and abnormal operations. When abnormal conditions like *short circuit* (SC) or *unclamped inductive switching* (UIS) occur, the smaller die size turns out to be a major downside for the robustness of such devices. The extremely high heat generation density in microsecond-scale time intervals determines a significant temperature increase within the die, which can permanently damage the semiconductor/oxide interface and top metallization and lead to different failure mechanisms. The characterization

and modeling of SC operating conditions is, therefore, of great interest in the robustness evaluation of SiC MOSFETs.

The withstanding time and failure modes observed during the SC testing of discrete SiC MOSFETs in the last few years – about 40 reported failures in total – were surveyed in [J1]. Based on several literature contributions [16], [22], [37]–[41], only part of the tested 1.2 kV-rated discrete devices and none of the multichip modules (from different manufacturers) could withstand more than 10 μs SC time with a drain-to-source voltage of 600 V. These results were further confirmed by the experiments carried out using the non-destructive test (NDT) facility at Aalborg University, several power modules and discrete components were tested to determine their SC withstanding capability.

According to the studies in [42]–[44], it became clear that the root cause of all the SC failure modes is the steep junction temperature increment, reaching rates of about 300-400°C/μs when the nominal drain-to-source voltage is applied. So far, two major instabilities have been observed in the literature:

- *Gate oxide breakdown*: the intrinsic reliability of SiC MOSFETs' gate oxide has been object of several studies, such as [45]–[47], in the latest years. In particular, reducing the SiO_2 thickness in order to keep the gate voltage threshold at reasonable values, together with the intrinsic roughness of the SiO_2/SiC interface, makes the gate structure significantly prone to high-voltage and high-temperature related failure and degradation phenomena. In the test results reported in Figure 2.2, one can clearly see a device (part number C2M0080120D [34]) catastrophic failure due to gate oxide breakdown after a 5.2 μs short-circuit pulse at 600 V drain-to-source voltage and 150°C case temperature. The post-failure analysis of this device was made impossible by the complete destruction of the chip and epoxy resin encapsulant. Before the device catastrophic failure though, a permanent degradation of the oxide structure was observed. The precursor of this mechanism is the on-state gate voltage drop, which can be seen in Figure 2.2, and the increase of the gate leakage current. An in-depth investigation of a degraded device was carried on in [48], where a Focused Ion Beam (FIB) cut of the device was performed to expose a cross-section view of the damaged cell, as shown in Figure 2.3. Cell number 2 exhibits a crack in the SiO_2, spanning from the polysilicon gate finger to the source contact Al metallization. Additionally, a structural modification in the metallization and salicide occurs, suggesting an excessive thermal stress focused in the semiconductor-oxide interface. Similar results, with more severe material alterations, were observed in [49]. The root cause of the oxide crack is yet to be discovered, though it is clear that an extreme temperature increase rate is contributing to this failure mode.

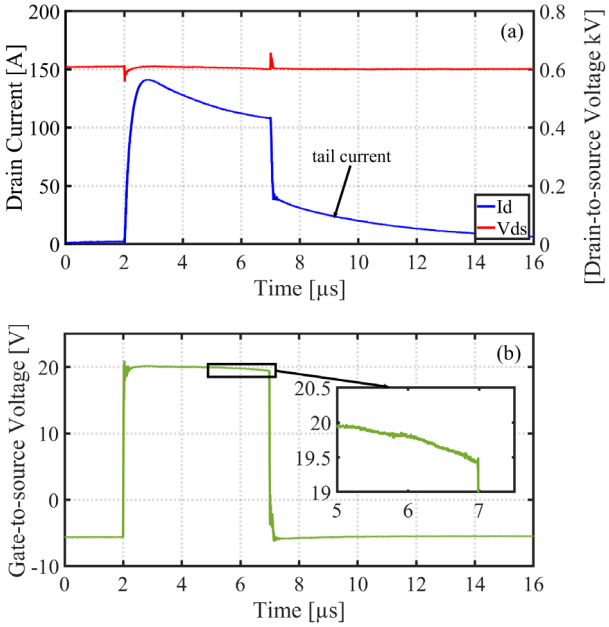


Figure 2.2. Catastrophic gate failure of a 1.2 kV/36 A SiC MOSFET [J1]. Drain current and drain-to-source voltage waveforms (a); gate-to-source voltage (b).

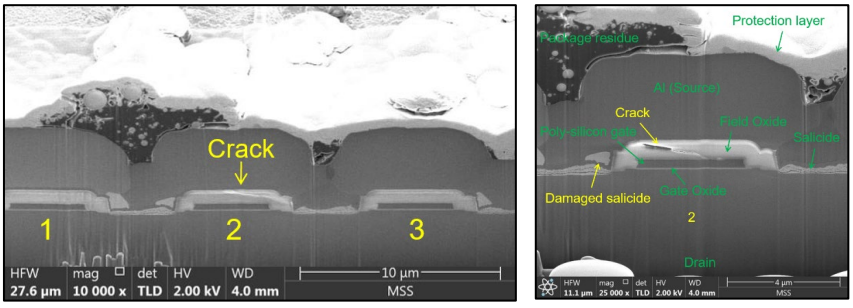


Figure 2.3. Focused Ion Beam (FIB) cut of a damaged device after SC displaying oxide crack on cell number 2 [22].

If the temperature increases enough to reach the Al melting point (660°C) the metal can fill the crack and create a low-resistance conductive path between gate and source contacts, which makes the device no longer controllable and leads to catastrophic failure.

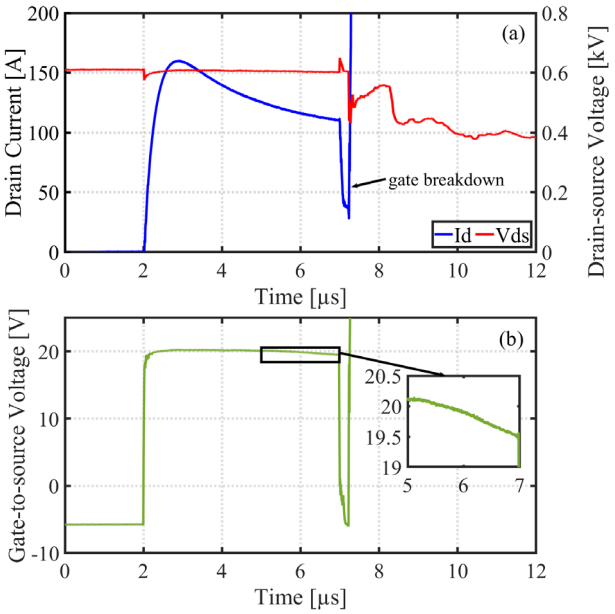


Figure 2.4. SC waveforms of a 1.2 kV/36 A SiC MOSFET exhibiting a large tail current [J1]. Drain current and drain-to-source voltage waveforms (a); gate-to-source voltage (b).

- *Thermal runaway*: the behavior reported in Figure 2.4 has also been observed during experiments. Here, after a 5 µs SC pulse at 600 V, the device [34] displays a current tail of significant amplitude, which is rather atypical in unipolar devices. The studies in [42], [44] have successfully correlated this mechanism to the increasing thermal generation of minority carriers (holes) across the body/drift junction due to the high heat energy released during the SC event. These carriers are pushed towards the source terminal by the high electric field creating a leakage current. The voltage drop caused by the current through the body resistive path may cause the activation of the intrinsic bipolar-junction transistor (BJT) and lead to a self-sustaining feedback mechanism that eventually results to the device destruction via gate breakdown. In fact, the activation may occur in one cell or few adjacent ones, and create an *hot spot* or *current filament*, which focuses most of the SC current in a very limited area of the chip [50], [51]. This kind of failure, as reported in [J1], can occur several µs after the device turns off. Moreover, it is not excluded that the threshold voltage drift due to extreme high temperature may accelerate this failure mode by preventing a complete channel shutdown [52].

2.2 State-of-the-art SiC MOSFET Compact Modeling

The main aim of compact device modeling is to obtain a description of the on-state characteristics and the switching behavior as a function of the applied voltage and currents, the temperature conditions and intrinsic physical characteristics – such as material, geometry and doping level. The model always requires a necessary tradeoff between mathematical complexity and computational speed. The criteria a designer can apply when making such tradeoff are the desired accuracy and the simulation time, together with the intended application for the model. Usually, very simple models provide fast simulations but lack an insight into the device physic and, consequently, accuracy. On the other hand, a complex physics-based model provides accurate estimation of the device behavior but also require longer simulation time.

Power semiconductor device models usually do not have the need for the detailed small-signal behavior required in analog electronic circuit simulation. They are rather used as switches in power electronic applications. This means that the most critical features which should be captured in a device model are: the conduction properties of the various semiconductor layers, influencing the on-state power loss; and the internal capacitances defining the switching speed and charge effects. It is also important to model the variation of these parameters with temperature, accounting for the device self-heating using lumped static or dynamic thermal models. Additionally, if the abnormal conditions are meant to be simulated, the model should include proper elements, such as breakdown and avalanche mechanisms, extreme temperature conditions, activation of parasitic devices, etc.

Compact physics-based or partially physics-based (semi-physics) models are the main focus of this work, since they provide the desired tradeoff between accuracy

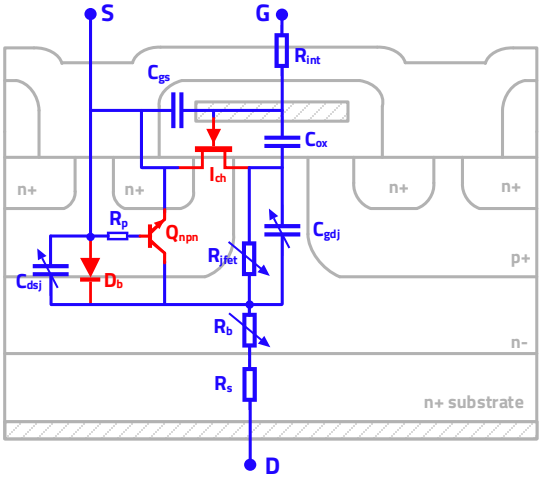


Figure 2.5. Typical equivalent lumped circuit of a power MOSFET.

and simulation time for the circuit-level evaluation of SiC MOSFETs and power modules, both in normal and abnormal operation. Additionally, they are easy to identify using parameter extraction sequences based on static and switching tests or datasheet curves, and do not require a detailed knowledge of the device internal geometry, which is almost never provided by the manufacturer.

A good classification of the available models for SiC power MOSFETs can be found in [53]. Table 2.1 offers an overview of the noteworthy physics- and semi-physics based compact models proposed in the literature during the last decade.

Figure 2.5 shows a general equivalent circuit, which highlights the main Si/SiC power MOSFET features traditionally modeled in the literature. The circuit elements are overlapped to a single MOSFET cell for explanatory purpose, but their parameters are lumped and scaled up to describe the whole chip architecture, made up of several thousand of elementary cells in parallel. It is worth nothing that not all the models reported in Table 2.1 feature the whole circuit and different analytical formulations may appear for each of the elements.

The model originally developed by McNutt and others in 2007 [54] represents one of the first steps in the compact physics-based modeling of SiC MOSFETs and some of its feature have inspired later works, including the presented project. This model is based on the channel current I_{ch} expression provided in the well-established Hefner IGBT model [55].

TABLE 2.1. SIC MOSFET COMPACT MODELS IN LITERATURE

First Author	Year	Main Contributions	Implementation
Mc Nutt [56], [54]	2007	Improved channel current description and simple parameter extraction sequence	IMPACT, MAST
Potbhare [57]	2008	Detailed interface trap modeling	Not indicated
Fu [58]	2012	Non-uniform current distribution in the JFET region	PSpice
Cui [59]	2012	*n-th* power law MOSFET model	PSpice
Mudholkar [60]	2014	Based on McNutt with datasheet-driven parameter extraction	SABER
Sun [61]	2014	Wide temperature range	PSpice
Peng [62]	2016	Body diode model	Not indicated
Riccio [63]	2017	Suitable for simulations outside SOA	SPICE
He [64]	2017	Scalability to different device layouts and non-linear features	SPICE

The expression was refined by introducing temperature-dependency and two separate current components with different gate threshold voltage, which reproduce the gradual transition from linear to saturation region observed in the 1st generation of SiC MOSFETs, now less common. The parasitic MOSFET capacitors C_{gs} and C_{ox} are assumed constant, whereas the C_{dsj} and C_{gdj} are determined by the depletion region thickness. Body diode, intrinsic BJT and JFET region are not described, and the only contributions to the on-state resistance are R_b and R_s. More noticeably, the paper proposed an intuitive parameter extraction sequence that offers the possibility to be implemented and automated in many software environments – the original was coded in IMPACT while the model was developed in MAST. In 2014, another work [60] presented a new simplified parameter extraction sequence for the same model, which only requires data and curves available in the datasheet of commercial devices.

At the early stages of SiC MOSFET manufacturing, the performance and reliability limitation were mostly connected to the large number of defects found at the SiC/SiO2 interface. This is why models like [57] in 2008, filled the gap in the physics-based modeling of charge trapping and Coulomb scattering at the rough semiconductor-oxide interface.

The modeling activity evolved mostly towards the inclusion of additional features, like non-uniform current distribution in the JFET region in [58] and wide temperature range operation [61]. Moreover, a model for the body diode was introduced in [62], featuring a rather detailed description of the charge storage effects and reverse recovery, using a Fourier series solution of the ambipolar diffusion equation (ADE). The parasitic BJT has only been included in recent models, like [63], to describe the device behavior under abnormal (off-SOA) operation.

Additionally, semi-physical models, i.e. partly behavioral, models are sometimes provided by the manufacturers, such as [65]. Their performance has also been explored and compared to that of a physics-based model in this work.

2.3 Model Description and Implementation

The SiC MOSFET device model used for the circuit simulations in this project collects many of the features contained in the aforementioned physics-based model, aiming to provide a compact implementation and an intuitive parameter extraction sequence. The model formulation and complexity has changed throughout the project, depending on the degree of accuracy required in the specific case study. Table 2.2 contains the complete list of equations and parameters enclosed in the model for both normal and abnormal device behavior.

The channel current expressions are divided into two regions, namely *linear* region and *saturation* region. the temperature-dependent gate threshold voltage $V_T(T_j)$ and the pinch-off voltage factor P_{vf} determine the boundary between the two regions. Two lumped transconductance factors, K_f and $K_p(T_j)$, define the current intensity for the chip. The lumped on-state resistance is divided into three contributions: the JFET region resistance R_{jfet}, drift region resistance R_b and substrate resistance R_s.

TABLE 2.2. SIC MOSFET MODEL EQUATIONS

Channel Current

$$I_{MOS} = \frac{K_f K_p \left[(V_{gs}-V_T)V_{ds} - \frac{P_{vf}^{y-1} V_{ds}^{y} (V_{gs}-V_T)^{2-y}}{y} \right]}{1+\theta(V_{gs}-V_T)} \quad for \;\; V_{ds} \le \frac{V_{gs}-V_T}{P_{vf}} \quad (1)$$

$$I_{MOS} = \frac{K_p (V_{gs}-V_T)^2}{1+\theta(V_{gs}-V_T)} \quad for \;\; V_{ds} > \frac{V_{gs}-V_T}{P_{vf}} \quad (2)$$

$$y = \frac{K_f}{K_f - \frac{P_{vf}}{2}} \quad (3)$$

MOSFET On-State Behavior

$$R_b = \frac{W_b - W_{dsj}}{qAN_d\mu_n} \quad (4) \qquad R_{jfet} = \frac{W_{jfet}}{qA_{jfet}N_d\mu_n} \quad (5) \qquad R_s = \frac{W_s}{qAN_s\mu_n} \quad (6)$$

$$\mu_n(T_j) = \frac{947}{1+\left(\frac{N_b}{1.94\cdot 10^{17}}\right)^{0.61}} \cdot \left(\frac{T_j}{300\ \mathrm{K}}\right)^{k_\mu} \quad (7)$$

Intrinsic Capacitances

$$n_i(T_j) = 4 \cdot 10^{16} T_j^{1.5} e^{-\frac{19115.8}{T_j}} \quad (8) \qquad V_{bi}(T_j) = \frac{kT_j}{q} \ln\left(\frac{1\cdot 10^{16} N_d}{n_i^2}\right) \quad (9)$$

$$W_{dsj} = \sqrt{\frac{2\varepsilon_{SiC}(V_{ds}-V_{bi})}{qN_d}} \quad (10) \qquad C_{dsj} = \frac{A_{ds}\varepsilon_{SiC}}{W_{dsj}} \quad (11)$$

$$W_{gdj} = \sqrt{\frac{2\varepsilon_{SiC}(V_{dg}-V_{bi})}{qN_d}} \quad (11) \qquad C_{gdj} = \frac{A_{gd}\varepsilon_{SiC}}{W_{gdj}} \quad (12)$$

$$C_{gd} = \begin{cases} C_{ox} & for \;\; V_{ds} \le V_{gs} - V_{Td} \\ C_{ox} \| \; C_{gdj} & for \;\; V_{ds} > V_{gs} - V_{Td} \end{cases} \quad (13)$$

Body Diode Current

$$I_{bd} = i_s \left(e^{-\frac{V_{ds}}{nV_{bi}}} - 1 \right) \cdot e^{-\frac{V_{gs}}{k_{bd}}} \quad (14)$$

Short Circuit Behavior

$$I_{g,th} = \frac{q\,A\,n_i}{\tau_g} \sqrt{\frac{2\varepsilon_{SiC}}{q}\left(\frac{N_d+N_p}{N_d N_p}\right) V_{ds}} \quad (15) \qquad R_p = \frac{W_p}{qN_p\mu_p(A-A_{jfet})} \quad (16)$$

$$I_{npn} \cong \beta \cdot I_{g,th} \quad (17)$$

Temperature Scaling

$$V_T(T_j) = V_{T0} - V_{T1}(T_j - 300\ \mathrm{K}) \quad (18) \qquad K_p(T_j) = K_{p0} \cdot \left(\frac{T_j}{300\ \mathrm{K}}\right)^{K_{p1}} \quad (19)$$

These values are calculated based only on the chip geometry and SiC material properties. This also applies to the voltage dependent capacitances C_{gd} and C_{ds}, determined by the respective depletion region thickness (W_{dsj} and W_{gdj}). A rather simple expression, contained into the standard SPICE diode model, is used to model the body diode. The thermally generated current $I_{g,th}$ expression derives from the Shockley-Read-Hall semiconductor theory. The parasitic BJT's current amplification is approximated using a gain factor β.

The model has been implemented in SPICE code and can be interpreted by both PSpice and LTspice simulation environments [C1, C2]. The reason for the use of this software lies in the good tradeoff between simulation speed, coding complexity and popularity. Creating a SPICE platform for the compact physical modeling of SiC devices and power modules can provide a useful framework for the prospective designers of WBG-based converters. Moreover, it is relatively easy to interface SPICE models with other software environments, such as MATLAB or ANSYS Simplorer, which ensures great flexibility for multi-physics co-simulation at a system level. The full SPICE code for a discrete component is reported in the Appendix.

2.3.1 Including Self Heating

The heat conduction in an isotropic homogeneous material can be described by (20). The equation models the temperature T evolution, when a one-dimensional heat flow along the x-axis is assumed for simplicity. λ, ϱ and c respectively stand for the material's thermal conductivity, its density and its specific heat.

$$\frac{\partial^2 T}{\partial x^2} = \frac{c \cdot \rho}{\lambda} \cdot \frac{\partial T}{\partial t} \tag{20}$$

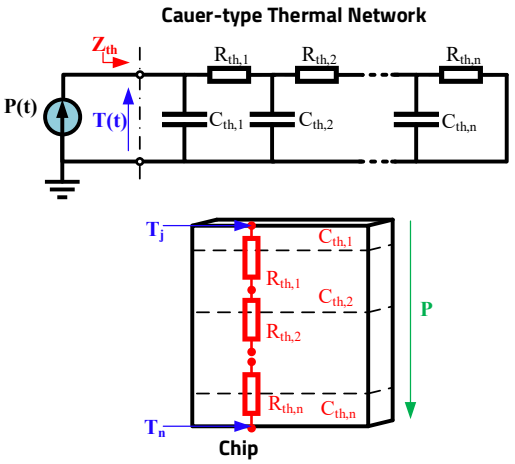


Figure 2.6. *Cauer*-type impedance thermal network

Assuming that the heat conduction can be compared to an electrical transmission line (without inductance) where a RC network defines the system time constant [66], the equation becomes (21). The equivalent thermal resistance R_{th} and capacitance C_{th} account for the thermal properties of the material.

$$\frac{\partial^2 T}{\partial x^2} = R_{th}C_{th} \cdot \frac{\partial T}{\partial t}\frac{\partial T}{\partial t} \tag{21}$$

Lumped impedance thermal networks have been used for a long time to model the thermal response of power electronic systems in compact circuit simulations [67], [68]. Two classic representations for a thermal network have become the standard nowadays: the *Cauer*-type and the *Foster*-type.

The *Cauer*-type thermal network in Figure 2.6 reflects the physical geometry of the material (or stack of layers of different materials) through which the heat spreading occurs. Its elements can be directly calculated by dividing the considered geometry in an arbitrary number of layers with finite volume along the heat propagation path. The *i-th* element's thermal time constant ($R_{th,i} \cdot C_{th,i}$) depends exclusively on its thermal and geometrical properties and can be calculated as in (22) and (23),

$$R_{th,i} = \frac{d}{\lambda \cdot A} \quad (22) \qquad C_{th,i} = c \cdot \rho \cdot d \cdot A \quad (23)$$

Where d is the thickness of the *i-th* element and A is the heat conducting cross section. This thermal impedance model offers better results when studying simple geometries and heat flow condition, such as a single homogeneous chip with the junction located in proximity to the top surface. Moreover, being a physical equivalent of the system structure, this network provides correct information about the temperature in each of the internal nodes. Compact one-dimensional Cauer networks can only roughly estimated the temperature when several layers with different material properties, geometries and multiple heat sources coexist, such as

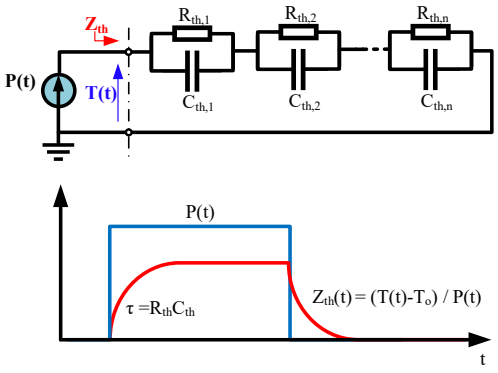


Figure 2.7. *Foster*-type impedance thermal network

in a multichip power module package.

Another way to obtain a thermal equivalent circuit is to fit the transient temperature step response of a system to a defined power source with an analytical function. This approach is very useful when the system is already available as a prototype and its detailed geometry and materials are not fully known. The usual procedure consists in measuring the temperature evolution *T(t)* when a constant power dissipation *P* is generated in the chip until the thermal equilibrium is reached ("heating curve") or when the power is turned off and the system cools down to the ambient temperature T_o ("cooling curve"). Both these transients can be described by means of the analytical step response function in (24), whose electrical equivalent is a chain of parallel RC elements, as the one depicted in Figure 2.7.

$$Z_{th}(t) = \frac{T(t)-T_o}{P} = \sum_{i=1}^{n} R_{th,i}\left(1 - e^{-\frac{t}{R_{th,i}C_{th,i}}}\right) \tag{24}$$

This "transfer-function" representation of the system's thermal behavior does not provide any information about the temperature evolution within the structure, which is modeled as a black box with a defined transfer function. Segmenting the network to access the voltage (temperature) in one of the internal nodes would require measuring the thermal response of the system in that point and reiterate the fitting. Besides, the number of RC elements for each segment and their order is arbitrary and dependent on the fitting accuracy. The Foster-type thermal network is suitable for complex systems and, most importantly, can be extracted by running transient FEM simulations, as proven in [69], including thermal cross coupling effects between different heat sources [70].

Since the material thermal properties change with temperature, the accuracy of these representations is limited to a defined range of injected power. Device operation outside this range requires new RC element values, as demonstrated in [71]. Nevertheless, thermal networks represent a very versatile and useful tool when implementing fast and compact electrothermal models.

2.3.2 A MATLAB-based GUI for parameter extraction

A graphic-user interface (GUI) was developed in MATLAB for the parameter identification of the presented model based exclusively on static I-V and C-V measurements and information available from the device datasheet [C1]. The steps used for the extraction sequence are similar to those reported in [54], [60] and are depicted in the flowchart in Figure 2.8. The device breakdown voltage, on-state voltage and current ratings are first used to extract the device active area and drift-region properties. Thus, it is possible to identify the MOSFET forward conduction characteristics in the saturation and linear region, by uploading I-V curves at different temperature and gate bias levels. Finally, the C-V characteristics are used to extract the capacitance parameters defining the device's switching transient. All the parameters are found by rearranging the model equations. The GUI shows the

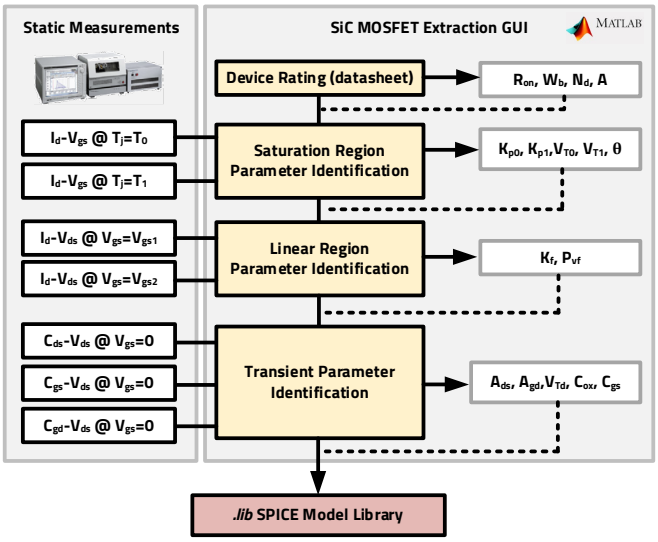


Figure 2.8. Parameter extraction sequence flowchart.

measured characteristics against the simulated ones, allowing the user to manually tune the parameters for a better fitting. Eventually, when the sequence is complete, the GUI allows the user to save the full parametrized SPICE model library (*.lib* file) of the device. The main concept in this work was to provide a complete and user-friendly MATLAB tool to create a turn-key PSpice/LTspice compatible model without necessarily needing SPICE coding skills.

2.3.3 Experimental Setup for Model Validation

Static I–V and C–V measurements are carried out in order to extract the model parameters and verify the accuracy of the model over the defined range of operation. The static measurements are pulsed, to avoid self-heating, and are generally performed by using a curve tracer / device analyzer. A Keysight B1506A fixture has been used for most of the static testing during the project, allowing full static characterization of the device up to 10 kV/1.5 kA and 150°C, by using a controlled airflow heater.

A double-pulse test (DPT) setup, like the one shown in Figure 2.9 [C5] is usually built to validate the simulated switching behavior of the device against experimental waveforms. The design and measurements methods used in a DPT are crucial for obtaining clear waveforms and calculating the device switching energy loss correctly. Especially when dealing with WBG devices, the presence of significant parasitic inductance and capacitance in the power and gate current loops and the very high switching dV/dt and dI/dt, will provoke undesired oscillations and couplings [72].

A series of measurements can be adopted for suppressing the ringing phenomena, such as reducing the current loop areas, using EMI filters and snubber circuitry and slowing down the switching by increasing gate resistance and capacitance [73]. Similar solutions were applied in the DPT setups designed to validate the SiC MOSFET model presented in this project. A dedicated evaluation PCB for discrete SiC MOSFETs in TO-247 package was used in [C2, C4, C5], featuring RC snubber branches on both top and bottom side of the half-bridge leg and small buffer capacitors on the DC-link side used to reduce the power loop area. A new setup (Figure 2.10) was developed to test new-generation discrete devices in TO-247-4 packages [J2]. The custom-designed PCB allows connecting two device in half-bridge configuration that can be used for DPT or other converter topologies. In both the fixtures, the DUTs were mounted on specifically designed hotplates to map the device switching performance over a wide range of junction temperature value. A fiber optic temperature measurement system was also used to monitor the device case temperature. The choice among different kinds of current probes has also to be made carefully, since the bandwidth requirements for WBG devices are

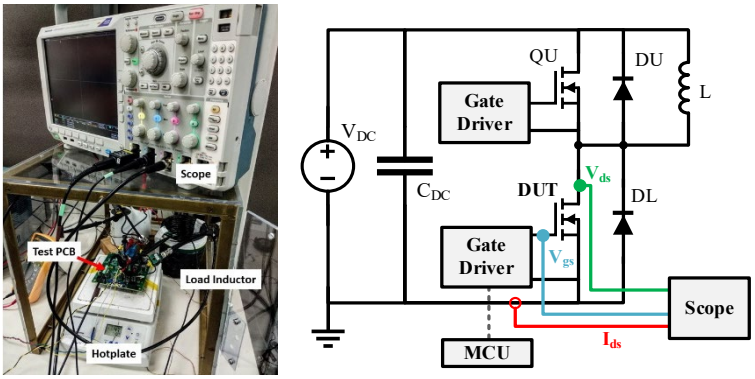


Figure 2.9. DPT experimental setup (a) and schematic (b) [C5].

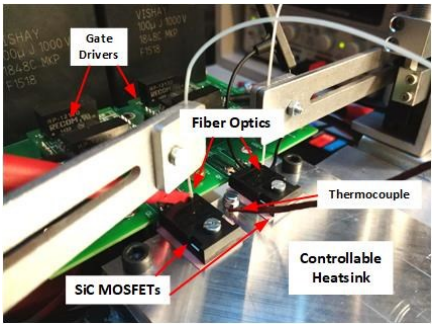


Figure 2.10. Test bench for TO-247-4 discrete SiC MOSFETs.

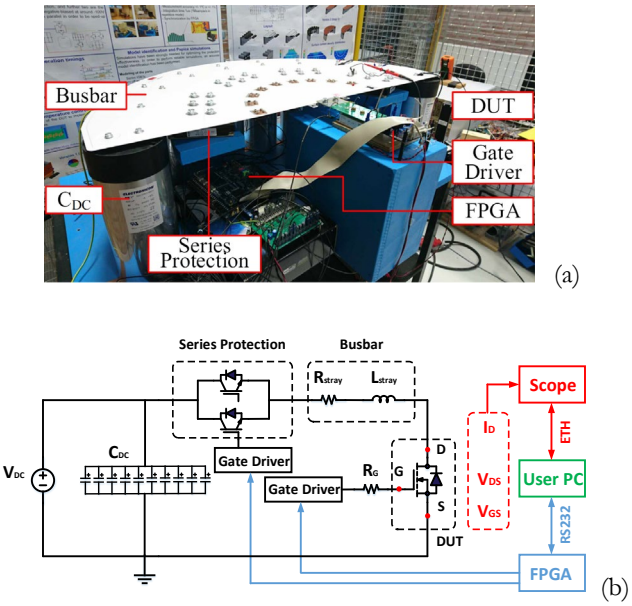


Figure 2.11. Experimental NDT setup (a) and schematic (b) [J1].

much higher in comparison to Silicon, ranging from tens to hundreds of MHz [74], [75]. Both Pearson current transformers and Rogowski coils specifically designed for power devices were used in the presented test setups and can guarantee reliable current measurement results for the considered devices. Where necessary, the measurement results have been compensated for nanosecond-scale delays.

It is important that the additional elements used to mitigate the oscillation in the experiment, as well as the test circuit parasitics, are included in the simulated circuit, in order to achieve matching oscillation frequency and magnitude.

A non-destructive test (NDT) bench [76] has been used for the SC characterization of both discrete devices and modules. The setup and its schematic is shown in Figure 2.11. A DC power supply with 2.4 kV maximum voltage rating is used to charge up a bank of large capacitors C_{DC}, which can provide the required SC pulsed energy. A custom-designed busbar ensures homogeneous distribution and low inductance path (10 nH) for the SC current. A series protection made up of paralleled IGBT modules – 10 kA total maximum current rating – is used as a circuit breaker to prevent catastrophic damage to the test sample and allow post-failure analysis. A FPGA controller with a computer interface is programmed with the necessary pulse timings and controls the activation of the series protection.

2.4 Summary

In this chapter, the structure, normal operation and SC behavior of SiC power MOSFETs were briefly described. In particular, a literature survey of the most common SC-related failure modes and instabilities has been provided, identifying the vulnerability of this devices in the high current density and heat generation at the chip junction. Subsequently, the state-of-the art modeling of SiC MOSFETs has been presented, together with an overview of the physics based equations selected to implement a compact model. This improved device model features a complete and temperature-dependent description of both normal and abnormal behaviors, suitable for fast and accurate circuit simulation and estimation of the conduction and switching power loss. Self-heating can be included in the model by using lumped-impedance thermal networks. The model has been implemented in SPICE, providing a simulation platform in a widespread software environment. A novel MATLAB-based GUI was created in order to provide a general-purpose, user-friendly tool for identifying the model parameter using datasheet information and static curves. The tool has been used to parametrize several models for discrete devices and power modules during the project. Finally, the experimental setups used for the model validation in static, switching and short circuit conditions has been presented. This chapter was meant to provide a thorough overview of the device model and operation. In the following chapters, the comparison between the simulated device behavior and the experimental data will be discussed, as well as more advanced uses of the presented model in multi-physic simulation approaches.

Chapter 3
From Discrete Device to Power Module

3.1 Case Study I: SPICE Simulation of a discrete SiC MOSFET

The TO-247 discrete device package is currently the state-of-the-art choice for encapsulating single SiC MOSFET chips. The common three-lead version has proven high ruggedness and reliability for low-power Si devices [77]. With the introduction of high-power density chips and fast-switching semiconductors, the impact of the package parasitic has become significant [78]. More recently, the use of Kelvin connection to decouple the load current loop from the gate control loop, has shown a benefit in terms of switching power losses and reliability [79]. For this reason, some of the SiC MOSFET manufacturers have introduced a four-lead TO-247 package (TO-247-4) with an auxiliary Kelvin-source connection in their latest generation devices. In this case, the correct modeling the package parasitic is crucial in the simulation of WBG discrete devices.

Discrete SiC MOSFETs were characterized and modeled in [C1,C2,C4,C5]. A new-generation discrete component was chosen as case study in [J2] to validate the compact electrical model. The MOSFET (part number C3M0065100K) [80] is manufactured by Wolfspeed and enclosed in the TO-247-4 package. The bare die used in the device is a 3rd generation SiC MOSFET (part number CPM3-0900-0065B).

3.1.1 Static Validation

The model parameters were extracted using both datasheet values and experimental static characterization, as described in Subsection 2.3.2. Table 3.1 lists some of the main extracted parameters.

The static characterization of the device has been carried out using a B1506A Keysight curve tracer/device analyzer and TP04390A ThermoStream airflow heater.

TABLE 3.1– DEVICE MODEL PARAMETERS

	Parameter	Value	Unit	Temp. Dep.
C3M0065100K SiC MOSFET – forward and 3rd quadrant conduction				
C_{GS}	Gate-source capacitance	0.66	nF	No
C_{ox}	Gate oxide capacitance	2.13	nF	No
N_d	Drift region dopant density	1.6×10^{15}	cm^{-3}	Yes
μ_n	Drift region carrier mobility	890	$cm^2V^{-1}s^{-1}$	Yes
A	Device active area	0.066	cm^2	No
R_b	On-state Drift resistance	65	mΩ	Yes
V_T	Gate threshold voltage	3.5	V	Yes
C3M0065100K SiC MOSFET – Body diode				
V_d	Diode forward voltage	4.8	V	Yes
R_s	On-state diode resistance	43	mΩ	Yes
n	Diode ideality factor	10.4	-	No
tt	Charge transit time	2.5	ns	Yes
is	Reverse saturation current	146	nA	No

The *I-V* curves have been measured up to 150°C, which is the maximum rated temperature for the device recommended by the manufacturer.

In addition, the parasitic capacitors were measured up to blocking-voltage (1 kV). The measured and simulated static *I-V* curves in the 1st quadrant are reported together in Figure 3.1.a-b at 25°C and 150°C. There, it can be observed that, at higher temperature, the characteristics shift in different directions depending on the gate voltage. In particular, the curves at higher gate voltage shift downwards, because of the dominant effect of the reduced mobility in the drift region. On the contrary, at lower gate voltage, the current capability increases due to the dominant effect of the lower channel resistance. Figure 3.1.c-d show instead the measured and simulated 3rd quadrant I-V curves at different gate voltages and respectively at 25°C and 150°C. The typical diode characteristic curve can be observed when the gate voltage is -4 V and the current is flowing through the body diode. The curve shifts at high temperature because of the reduced built-in potential in the p+/n- junction. When the gate voltage increases, the current gradually starts flowing through the MOS channel, which offers a lower-resistance path, and the reverse conduction curve degrades towards that of a resistor. The validation of the internal MOSFET capacitance curves vs. drain-to-source V_{ds} is reported in Figure 3.2.

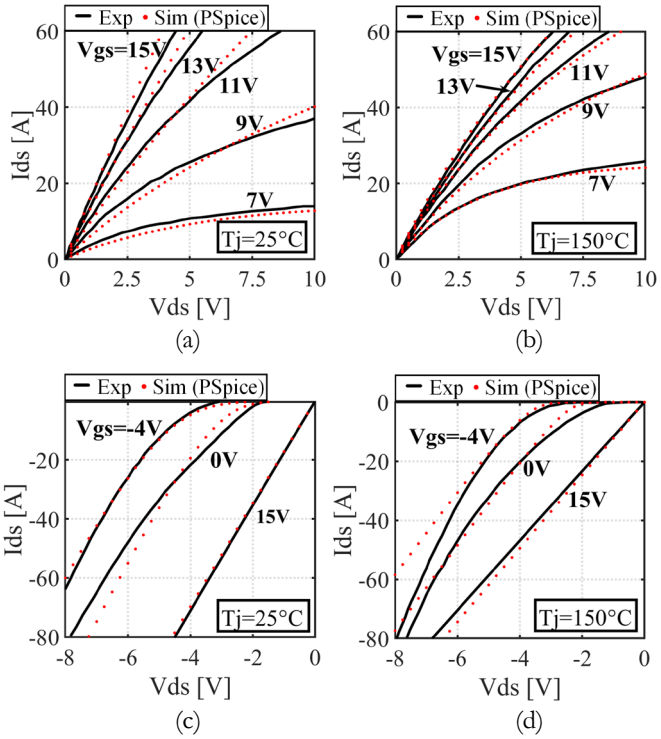


Figure 3.1. Validation of static I-V curves: 1st quadrant curves at Tj=25°C (a) and Tj=150°C (b) under different gate bias; 3rd quadrant curves at Tj=25°C (c) and Tj=150°C (d) under different gate bias [J2].

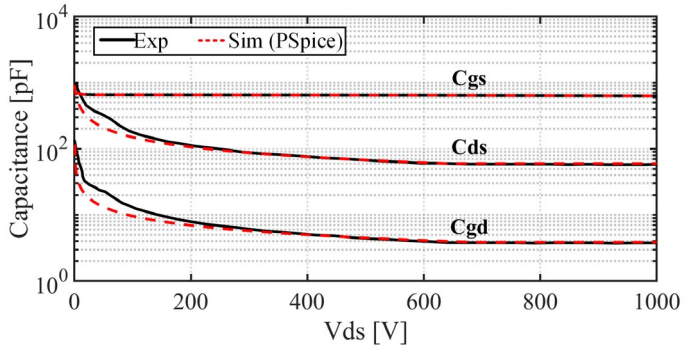


Figure 3.2. Validation of C-V curves at Tj=25°C and Vgs=0 V [J2].

The model can successfully simulate the device behavior in the full operating range. In particular, the simulated and experimental curves show good matching in the nominal operating area, with less than 5% maximum relative error.

3.1.2 Switching Validation

The validation of the simulated switching behavior is usually made using switching waveforms from a DPT setup. Since the parasitic circuit elements in the package and the setup play an important role in the switching performance, an identification of such parameters is needed for an effective validation.

The extraction of a detailed electrical model for the package parasitics has been explored extensively for Si IGBTs [81], [82]. The extraction method usually consists in designing the complete or partial 3D geometry of the device and importing it in an electromagnetic FEM analysis software, such as ANSYS Q3D or Maxwell. Once the user defines materials and EM sources, the software creates a matrix of RLC elements for each of the possible current paths. Other procedures, based on direct measurements, were proposed in [83], [84] for SiC MOSFETs. In this case study, an accurate CAD geometry of the discrete device without the epoxy encapsulation and complete with bond wires (Figure 3.3.a), was built for this task. The extracted parasitic values are reported in Table 3.2, while a contour map of the simulated current density is shown in Figure 3.3.b.

The equivalent circuit of the DPT used for the switching characterization, whose schematic is depicted in Figure 3.4, was simulated in PSpice. The circuit includes two sub-circuits for the upper and lower MOSFETs, the PCB stray elements and the snubber branches used in the real setup.

The validation of the simulation results with experimental waveforms is reported

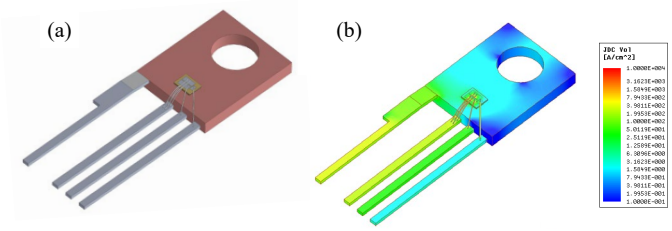


Figure 3.3. CAD drawing of the discrete device without epoxy resin (a) and contour map of the current density resulting from FEM simulation in Q3D for parasitic extraction (b).

TABLE 3.2 – LUMPED PARASITIC ELEMENTS FOR A TO-247-4 PACKAGE

Path	Resistance [mΩ]	Inductance [nH]
Drain lead and baseplate	0.56	9.5
Source terminal	4.8	10.4
Auxiliary source terminal	17.6	11.4
Gate terminal	24.5	12

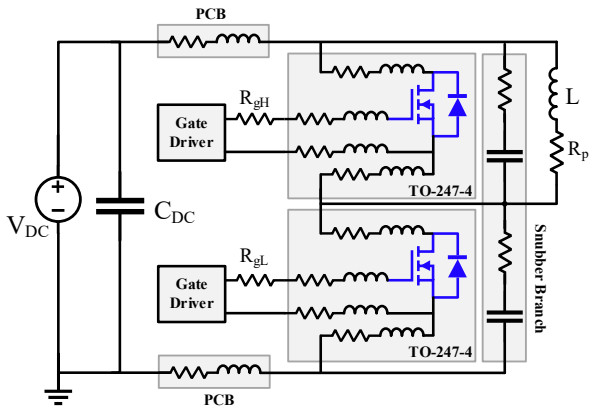


Figure 3.4. Schematic of the DPT circuit used for switching simulations complete with parasitic elements.

in Figure 3.5 for turn-on (Figure 3.5.a) and turn-off (Figure 3.5.b) with 30 A load current, DC-bus voltage is set at 500 V and at the maximum rated temperature (150°C). The oscillation frequency and amplitude and the rise/fall time in the

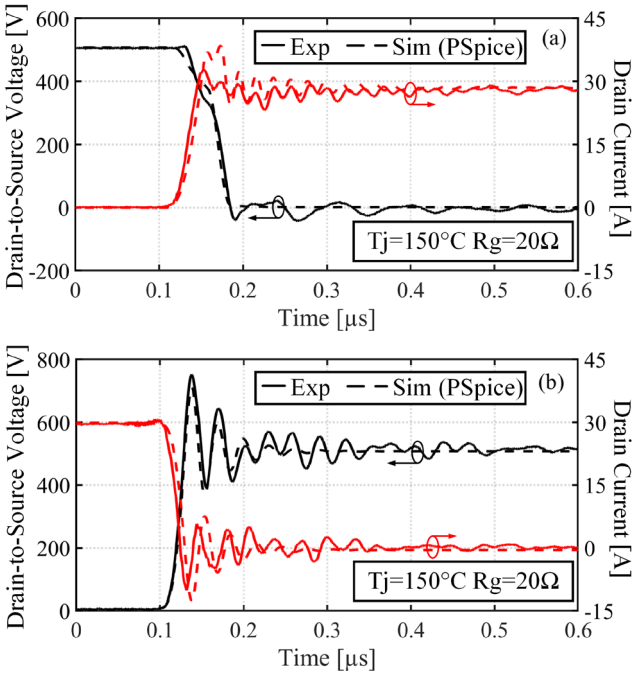


Figure 3.5. Comparison of measured and simulated turn-on (a) and turn-off (b) of MOSL at T_j=150°C and R_g=20 Ω.

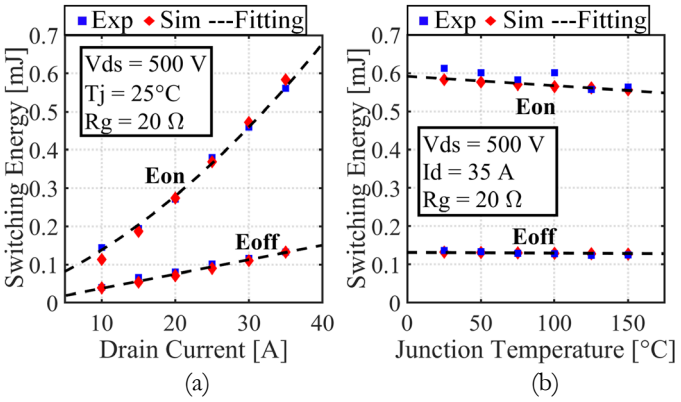


Figure 3.6. Comparison of simulated and measured switching energy loss at V_{ds}=500V, with increasing I_d (a) and T_j (b).

measured waveforms are accurately captured in the simulations.

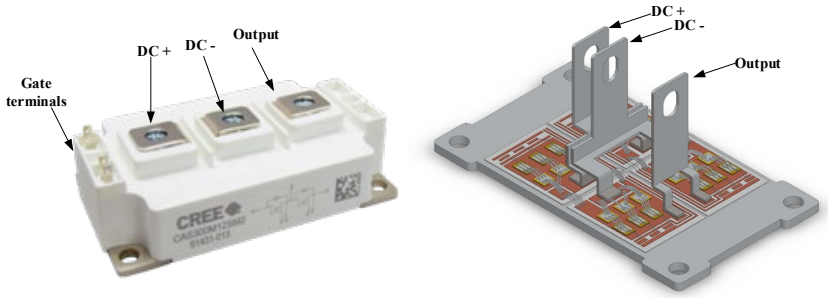
The turn-on (E_{on}) and turn-off (E_{off}) switching energy loss from the measurements and simulations were calculated by integrating the instantaneous power ($p(t)=v_{ds}(t)\cdot i_d(t)$) during the commutation events and compared.

The losses were calculated over the full operating range of the device (up to 35 A current and 150°C junction temperature) at the nominal voltage V_{ds}=500 V. The comparison is reported in Fig. 3.6, showing a good matching, with maximum relative error below 3.5%.

3.2 Case Study II: SPICE Simulation of a SiC MOSFET power module

The circuit simulation of SiC multi-chip power modules was addressed in [C1]. In this study, three full-SiC commercial half-bridge modules from different manufacturers have been fully characterized. The first modeling assumption was to consider several devices connected in power as a single switch, without an in-depth investigation on the internal layout and parasitic elements. Although this represents a significant approximation, the scope was rather to provide a user-friendly SPICE modeling methodology for high-power SiC modules. The model identification and validation for one of the studied modules is presented in the following Section. The component is a 1.2-kV/300-A rates full-SiC power module from CREE (part number CAS300M12BM2 [85]), whose picture is shown in Figure 3.7.a.

In [C3], the model for the same component was refined and extended to include the internal module layout, parasitic elements and thermal behavior. The creation of a more detailed model was driven by the necessity of studying the short-circuit behavior in a multi-chip layout and finding possible thermal instabilities. The CAD geometry of the module's internal structure is depicted in Figure 3.7.b.



(a) (b)

Figure 3.7. Picture of the 1.2-kV/300-A full-SiC MOSFET module characterized in [C1] (a) and its internal CAD geometry (b).

3.2.1 Model Validation

Once the model parameters were extracted using the method presented in Section 2.3.2, the validation has been carried out in a similar way as the one employed for the discrete device in subsections 3.1.1 and 3.1.2. The main model parameters are listed in Table 3.5. The static curve validation can be found in [C1].

The DPT for this module has been carried out by connecting the upper half of the inverter leg in parallel with the load inductor. In this way, the antiparallel Schottky barrier diodes (SBDs) act as freewheling path for the inductive current. The tests

TABLE 3.5. EXTRACTED PARAMETERS

Parameter		Unit	Value
V_{bd}	Module Rated Breakdown Voltage	kV	1.7
I_d	Module Rated Drain Current	A	325
V_T	Gate Threshold Voltage	V	5.287
K_p	Saturation Transconductance	A/V^2	28.04
K_f	Linear Transconductance Factor	-	1.043
Rs	Drain Series Resistance	Ω	1.2
A	Active Area	cm^2	0.174
N_b	Bulk Doping Concentration	cm^{-3}	0.906×10^{16}
W_b	Bulk Thickness	μm	14
P_{vf}	Pinch-off Voltage Factor	-	0.65
C_{gs}	Gate-Source Capacitance	nF	20.05
C_{ox}	Oxide Capacitance	nF	12.14
A_{gd}	Gate-Drain Depletion Area	cm^2	0.054
V_{T0}	Gate Threshold Temperature Coeff.	-	5.609
V_{T1}	Gate Threshold Temperature Coeff.	-	-0.0166
K_{p0}	Saturation Transconductance Temp. Coeff.	-	28.04
K_{p1}	Saturation Transconductance Temp. Coeff.	-	2

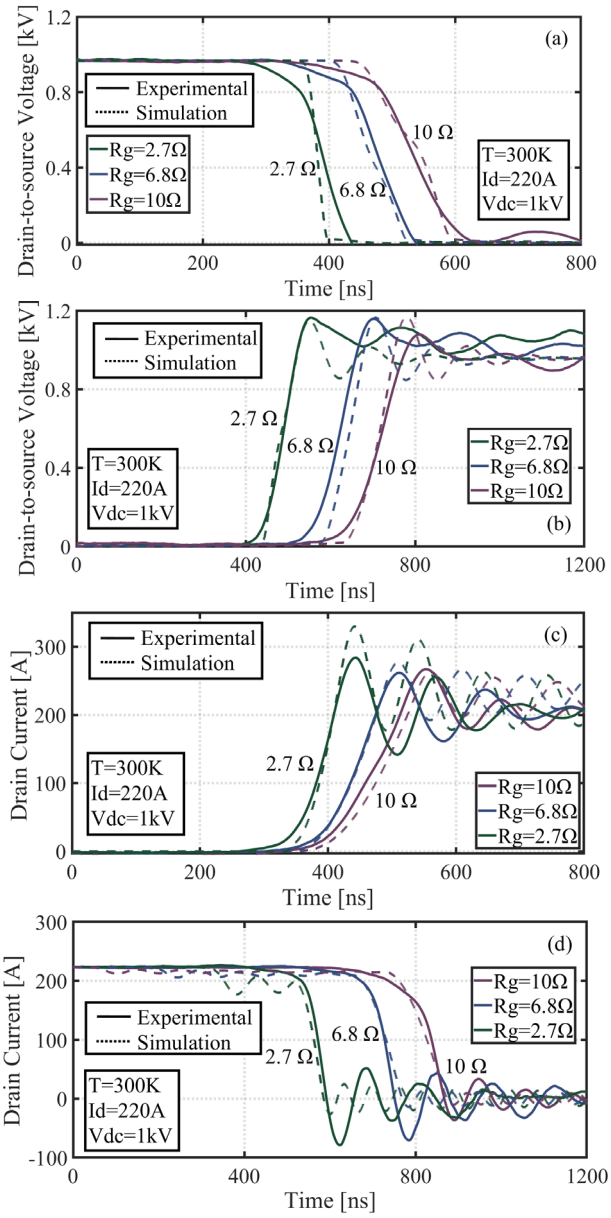


Figure 3.8. Comparison of simulated and measured switching waveforms with different Rg values: drain-to-source voltage at turn on (a) and turn off (b) ; drain current at turn on (c) and turn off (d) [C1].

have been conducted with V_{DC} = 1 kV and changing the gate driver resistance Rg from 2.7 to 10 **Ω**. The measured and simulated voltage waveforms are reported in

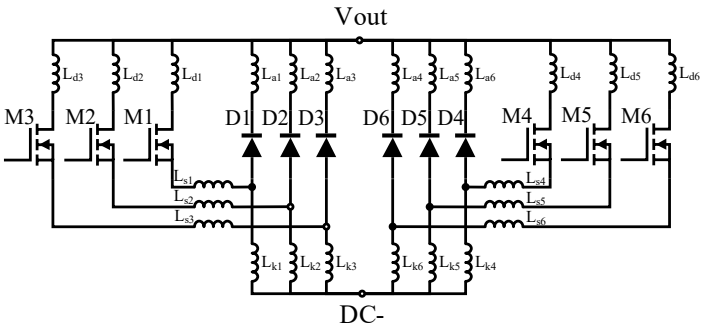


Figure 3.9. Equivalent circuit schematic of the low-side switch in the SiC power module [C3].

Figure 3.8.a (turn on) and Figure 3.8.b (turn off), while the drain current is plotted in Figure 3.8.c (turn on) and Figure 3.8.d (turn off). The switching behavior is properly captured by the simulation, including the turn-off voltage overshoot and the increased commutation time in presence of higher R_g.

3.2.2 Extraction of Parasitic Elements

The presence of several chips connected in parallel to boost the power rating of a switching cell comes with a series of challenges [4]. The manufacturing process, especially for new generation devices like SiC MOSFETs, introduces a statistical variability in the device parameters. Additionally, the physical layout of the chips on the DBC substrate and the bond wire connections can produce current and voltage sharing unbalances among the paralleled chips. The combined action of these phenomena can represent a critical reliability issue, affecting thermo-mechanical stress distribution and creating abnormal behavior such as parasitic turn on [86], [87]. The study of such unbalances for SiC MOSFET modules and how to mitigate them was conducted in [74], [88].

As mentioned in Section 3.1.2, methods based on FEM simulation are usually employed for the extraction of parasitics in power modules. The stray parameters can also be calculated by means of analytical formulas derived from EM theory. A similar approach was applied, among others, in [89], where the principle of partial inductances was used to calculate the self-inductance for the commutation open loops. This is especially useful when a fast calculation of the stray elements is necessary for the layout optimization of power modules [90], [91]. A simple stray inductance model was adopted in [C3] to define the lumped circuit elements in the module. The equivalent circuit for the lower-side switch (power loop only), with a total of 6 MOSFET and 6 SBD dies, is depicted in Figure 3.9Figure 3.9. The inductors $L_{d1\text{-}6}$ and $L_{a1\text{-}6}$ describe the inductance of the DBC top copper trace, while $L_{s1\text{-}6}$ and $L_{k1\text{-}6}$ model the bond-wire connections.

3.2.3 Extraction of the Thermal Model

A Cauer-type thermal network model was chosen to describe the thermal behavior of the chip during SC. Similarly to what proposed in [92], the chip volume has been divided in a number of equally-thick elements, as depicted in Figure 3.10.a. Assuming that the heat flows downward from the chip junction, the thermal resistance and capacitance of each layer can be found by knowing the material thermal properties, as described in Section 2.3.1. The thermal network was built for the only purpose of estimating the junction temperature evolution in the chips during SC. Therefore, the chip boundaries are also the boundaries of the thermal model, and all the chip surfaces are considered adiabatic. This is justified by the fact that the SC duration (in the order of few microseconds) is much shorter than the chip thermal time constant, estimated in the order of few milliseconds [42], [93].

In other words, the heat generated during SC does not spread beyond more than a few micrometers in the device substrate. This is proven in Figure 3.10.b, where the temperature evolution during SC at different depth within the chip is simulated using the thermal network. It is understandable that this model is only suitable as long as SC operation is considered and not for the simulation of longer events (>1 ms), where a more complex model for the thermal stack materials would be required.

3.2.4 Short-circuit Simulation Results and Validation

The complete electrical and thermal model was implemented in PSpice (available in the Appendix) and used to simulate SC condition in the low-side switch (the same that had been tested in the experiments), i.e. between the phase output terminal V_{out} and the DC-bus. In [22], the SC-SOA of the same module had been defined by means

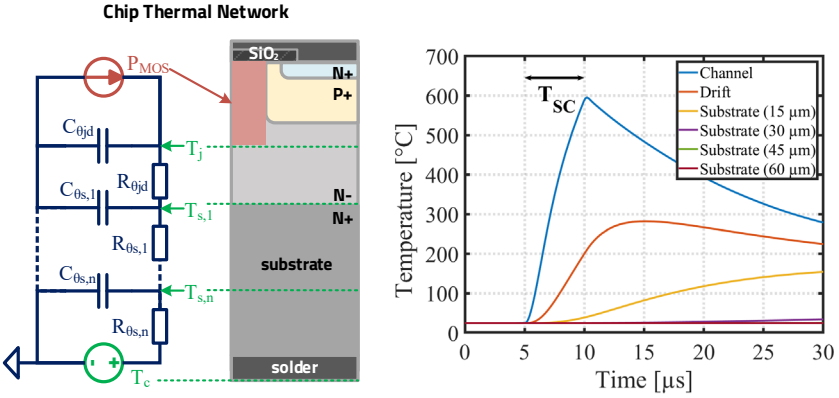


Figure 3.10. Proposed thermal model for the SiC MOSFET chip (a) and simulated temperature during a 5-µs SC at different depth within the chip vertical structure [C3].

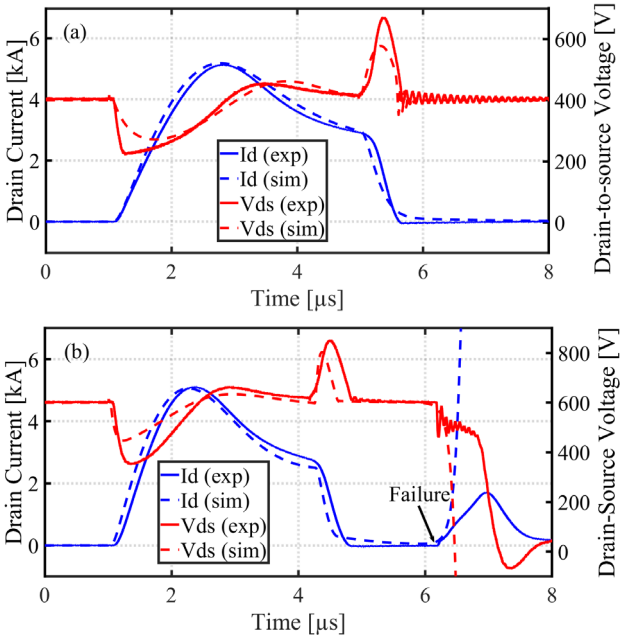


Figure 3.11. Comparison of simulated and measured current and voltage waveforms during SC: a 4-µs pulse at V_{DC}=400 V (a) and a 3.2-µs pulse at V_{DC}=600 V and thermal runaway failure (b) [C3].

of the NDT setup described in Section 2.3.3. One of the failure modes reported for this module is a thermal runaway after 3.2-µs SC time, also described in [42], [44].

The simulation results are reported in Figure 3.11 along with the NDT waveforms [C3]. One can observe how the model can correctly estimate the drain current turn on transient and the subsequent carrier mobility degradation due to the very high self-heating. In particular, in Figure 3.11.a, when the DC-bus voltage is set to 400 V, the SC energy is not high enough to trigger the thermal runaway mechanism. On the other hand, in Figure 3.11.b (V_{DC}=600 V), the model can roughly predict the activation of the parasitic BJT due to the increasing drain leakage current after turn off. In this simulation, the MOSFET model parameters are identical for each of the chips.

In fact, it has been proven in [51] that device parameter mismatches can affect the SC behavior within parallel cells of the single chip. That study attributed the formation of current-crowding regions, or *hotspots*, within the die due to non-uniformity in size and doping among adjacent cells. Such manufacturing-related mismatches are also usually observed at a die level as deviation in the on-state resistance or gate threshold voltage [88], which might be significant and affect the circuit performance when the dies work in parallel [C1]. Therefore, the question whether such deviation might have an impact on the SC behavior as well. The post-

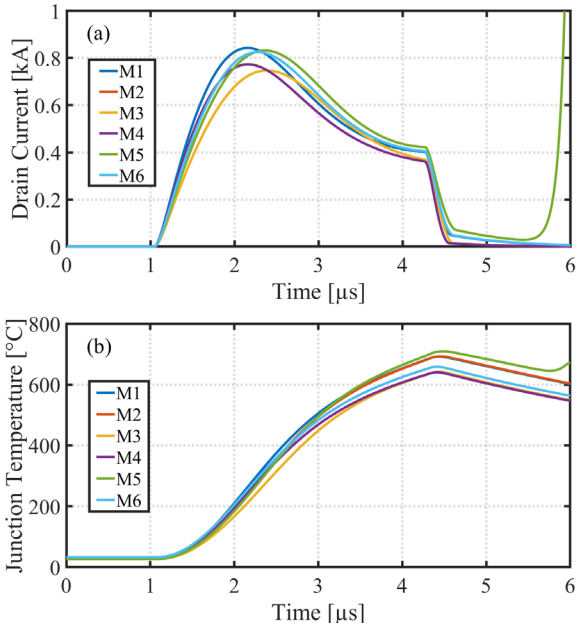


Figure 3.12. Simulated SC drain current (a) and junction temperature (b) distribution in the paralleled MOSFET chips for a 3.3-µs SC at V_{DC}=600 V and threshold voltage mismatch of 20 %.

failure analysis of this module in [22] hints towards this hypothesis, showing that only one of the paralleled dies exhibits signs of burn-out. Since measurements of SC current sharing in a power module are impractical to achieve, the simulation approach might offer a valuable aid. Therefore, after the model has been validated with homogeneous die parameters, a mismatch in the gate threshold voltage V_T up to ±20% the initial value has been introduced among the devices.

The distribution of SC drain current and junction temperature for each of the paralleled dies in the module has been reported respectively in Figure 3.12.a and Figure 3.12.b. One may observe that the drain current distribution is quite uneven, as the saturation current value changes with V_T in each die. Additionally, the mismatch in the commutation loop stray inductance also affects the current rise time. Eventually the MOSFET with the lowest V_T (M5 in this case) reaches the highest T_j, i.e. the highest SC energy dissipation, and is driven into thermal runaway before the others, thus confirming the behavior observed in the experiments. This also supports the findings in [J1], where the power module SC capability was found inferior to the discrete devices' one. In other words, according to the physical interpretation of the simulation results, the SiC MOSFET modules are more prone to SC failure, not because of an intrinsic weakness of the chips, but rather due to a mismatch in their parallel connection and package parasitics.

3.3 Summary

In this chapter, the SiC MOSFET model implementation, parameter identification and validation for both discrete devices and power modules was demonstrated. In particular, the accurate electrical modeling of the package was included, to extend the chip model and account for the parasitic elements affecting the device behavior. The comparison of the simulated static characteristics and switching waveform from PSpice showed good agreement with the experimental data in a wide range of operating conditions, including high-temperature, within and beyond the device's normal operation. Moreover, the extension of the model to a multi-chip module layout has proven the capability of estimating SC conditions. A thermal network for the chip has allowed the study of thermal instabilities generated within the module during SC. The simulation results suggest that a feedback mechanism between the leakage current increase and the extremely high junction temperature can trigger thermal runaway faster in the parallel of several MOSFETs.

Moreover, the simulation time for the presented models, with maximum time step of 1 ns, is comprised within the range of few seconds. The model compactness and accuracy can therefore be considerably beneficial in the fast electro-thermal simulation at a converter level, which will be faced in the next chapter.

Chapter 4
Fast and Accurate Electrothermal Simulation Strategy

4.1 Multi-domain and Multi-timescale Simulation at a Glance

Although SiC MOSFET are gaining popularity in the design of power converters, their higher cost and limited reliability assessment still hinder their widespread diffusion. As already mentioned, nowadays' packaging solutions do not allow to fully exploit the high-temperature and high-speed potential of SiC devices. Therefore, the choice of SiC over Si with the current state-of-the-art depends greatly on the desired application performance/reliability/cost trade-off. In these respect, modeling and simulation are crucial in order to assess the capabilities of new-generation SiC devices during both normal and abnormal operation; saving high prototyping and testing time and costs. Looking at Figure 4.1 [94], depicting the typical design workflow for a SiC power electronic system, one can notice how digital prototyping spans different physical domains (mainly electromagnetic and thermal). Additionally the analysis of the system behavior encompasses very different

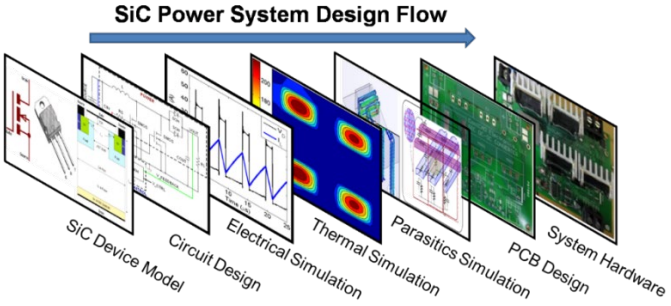


Figure 4.1. Typical design flowchart for a SiC power electronic system (Source: CoolCAD Electronics, 2015).

timescales, as described, among others, in [95] and [96]. These different timescales can be classified into:

- *Short or very-short timescale* (<10 μs): this timescale is the one that encompasses one or few device switching events. It is crucial to take into account this timescale when calculating the device switching and conduction power losses. For most of the applications and during normal operation, the device junction temperature does not increase significantly and the variation of power loss is negligible. Circuit simulators can easily handle this timescale, estimating the device behavior with very high accuracy.
- *Medium timescale* (<1 second): after hundreds or thousands of switching events, the device temperature changes significantly and eventually reaches steady state. The time constant of this transient depends on the cooling system design, but it is usually in the order of hundreds milliseconds. Simulating such a timescale with a compact circuit model is feasible, but the required simulation time is in the order of minutes or hours, or higher when using multi-physics FEM software.
- *Long or very-long timescale* (>1 minute): in this timescale, the operative conditions of the converter can change significantly due to slow ambient temperature variation or the electric load. During this timescale, a power electronic system can experience aging, which will affect its performance and eventually lead to its end of life. Reliability analysis aims to investigate long-term mission profiles that are comparable with this timescale.

It is challenging to overcome the gap between these timescales without introducing approximations to reduce the model complexity and obtain acceptable simulation time. Many kinds of electrothermal models and simulation approaches have been proposed in this perspective [97]. These strategies usually rely on circuit-based simulators and FEM software to obtain a lumped model that can be used for system-level simulations. This process usually goes under the name of Model Order Reduction (MOR).

4.1.1 Integrating a Compact Device Model in an Electrothermal Model

Fast electrothermal simulation approaches have already been implemented for Si technology in [96], [98], [99] and for SiC in [100] with rather simple device models. In these works, analytical or behavioral device models were used to calculate the power losses or create lookup tables (LUTs). An average value of power losses can be found by using the LUT values as an input for the lumped thermal network model. In some cases, the losses model includes temperature dependency and therefore the electrical and thermal model are interdependent. Although, this strategy can offer very fast simulation, behavioral device models are not usually valid over a wide range of operating conditions and do not take into account detailed package stray elements and/or temperature dependency.

On the other hand, physics-based models offer a good trade-off between

accuracy and simulation speed, performing much better than simple behavioral fittings, and can be used for the fast calculation of the device losses in a very short time, as presented in Chapter 3. Therefore, two integrated simulation strategies were proposed and used in [C4, C5, J2, J3], where the advantages of a physics-based device model are combined with a thermal network extracted from the FEM modeling of the device and heatsink 3D structure.

The proposed simulation flowcharts are depicted in Figure 4.2. In the first case (Figure 4.2.a [C4]), the PSpice electrical model is used in co-simulation with the thermal network. This means that the device losses are re-calculated after a certain number of switching cycles, when the temperature/load condition of the converter change. In the second approach (Figure 4.2.b [C5, J3]) the PSpice model is only used at the beginning to map the power losses (*offline mapping*) in all the possible operating conditions expected in the converter and create dedicated LUTs. In both cases, a MATLAB platform is used to interface the electrical model and the thermal network, implemented in Simulink. The MATLAB code is available in the Appendix. A converter model defines the operating voltage, load current, duty-cycle and switching frequency for the single device. The losses are then injected in the thermal network, which allows for the calculation of the device junction temperature. The estimated

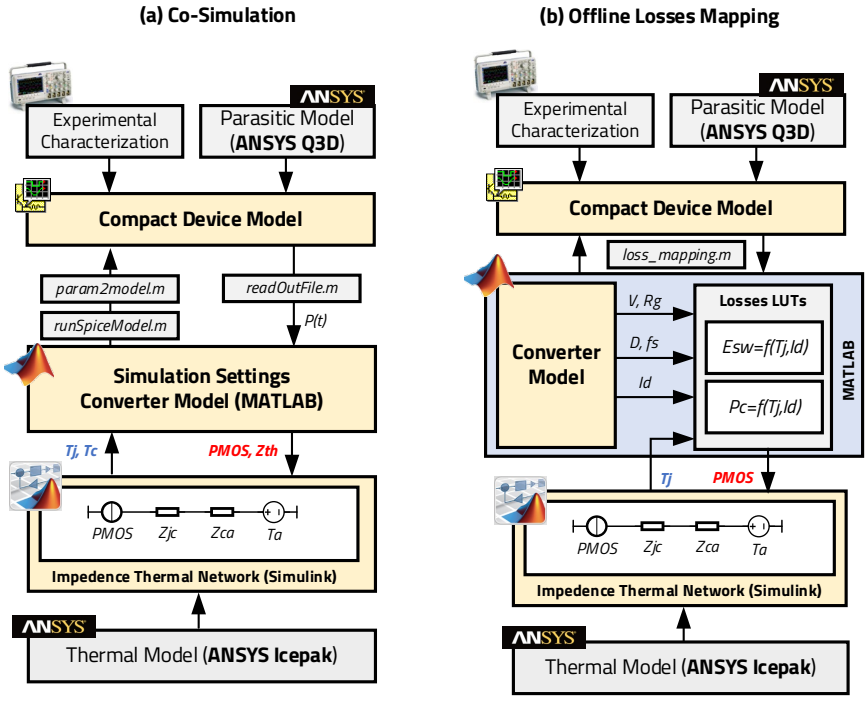


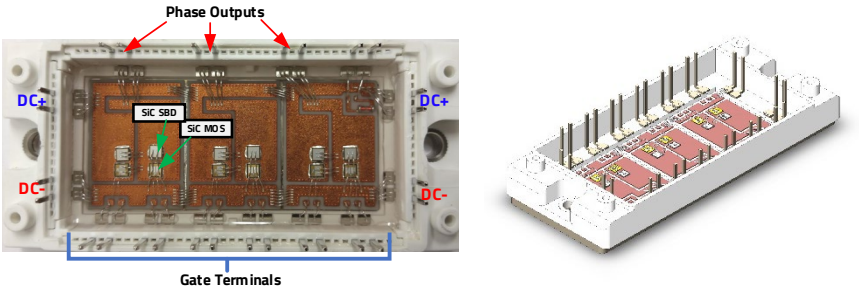
Figure 4.2. Fast electrothermal simulation strategy flowchart: based on co-simulation (a); based on offline power losses mapping (b).

junction temperature is fed back to the losses model for the next iteration.

These two approaches have proven different performance. The main challenge with the co-simulation strategy has been the interface between the PSpice simulation environment and MATLAB. Dedicated MATLAB scripts (available in the Appendix) have been coded in order to transfer data and run the PSpice *.cir* files. The transfer between the two environments is time consuming and may cause loss of data and/or convergence failure unless proper solutions are adopted in the code. Additionally, the time interval before updating the power losses in the thermal model have to be chosen carefully to have a trade-off between simulation speed and accuracy. On the other hand, the offline loss mapping allows the complete decoupling between electrical and thermal domains, with improved simulation speed and convergence [J2, J3]. However, proper boundaries for the mapping process have to be defined at the beginning of the simulation. Inaccurate results can be generated when the operating conditions of the device/converter exceed the map boundaries.

4.2 Case study III: ET Modeling of a 3-phase 1.2-kV SiC Power Module

The proposed ET simulation strategies were demonstrated in [C4, C5, J2] for discrete components, while in [J3] it was implemented for a 1.2-kV/20-A three-phase (3P) SiC module. The component (part number CCS020M12CM2 from CREE [101]) features a 3P-inverter configuration (six-pack) with 6 SiC MOSFET dies (part number CPM2-1200-0080B) and 6 antiparallel SiC SBDs (part number CPW4-1200-S020B) within a standard EconoPIM2 package frame. The module is depicted in Figure 4.3.a (the lid has been removed). A detailed CAD geometry of this module, shown in Figure 4.3.b, was designed in SolidWorks. The objective was to create a digital twin of the module to use in the electrical and thermal FEM simulation (with



(a) (b)

Figure 4.3. Top view of the SiC module internal layout (a) and 3D CAD geometry (b).

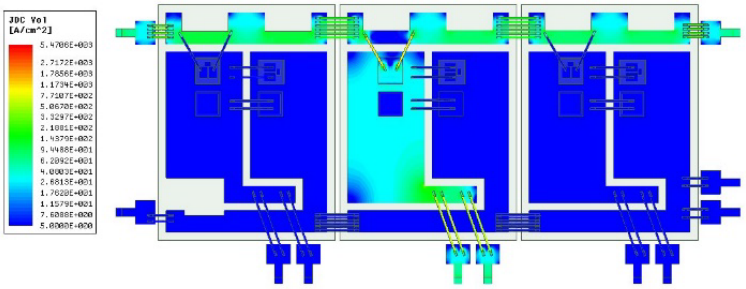


Figure 4.4. Current density plot from the FEM simulation of one of the module's conductive path in ANSYS Q3D.

necessary simplifications) and extract the full compact ET model based on the real geometry.

4.2.1 Electrical Model

The identification of the MOSFET and Schottky-barrier Diode (SBD) models has been conducted in a similar way to what described in Chapter 3. The main difference here is that the parameter extraction was performed in a SABER-based platform [102]. Some of the bare die information were obtained from the datasheet while the rest of the parameters were identified using the Synopsis Power MOSFET tool. Both the conduction and switching losses have been experimentally validated [J3] under a wide range of operating conditions. Additionally, the package parasitics have been calculated using FEM simulation in Q3D. Since the module layout is a 3P inverter configuration, each of the conductive paths had to be analyzed. An example is provided in Figure 4.4, showing the simulated current density distribution for the conductive path going from a phase output to the low-side DC bus. The split design of the DC-bus terminals reduces the unbalance in the stray inductance for this layout.

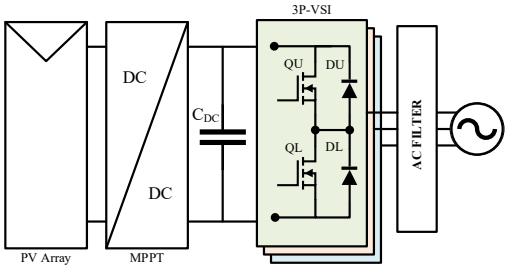


Figure 4.5. Schematic of a typical PV grid-connected system topology.

TABLE 4.1– CONVERTER SPECIFICATIONS

3P-VSI rating	
Rated maximum power	P = 20 kW
Input DC-bus voltage	V_{DC} = 800 V
Switching frequency	f_s = 50 kHz
Output frequency	f_{AC} = 60 Hz
SiC MOSFET module – CCS020M12CM2	
Blocking drain voltage	$V_{ds,max}$ = 1200 V
Maximum drain current	$I_{d,max}$ = 25 A

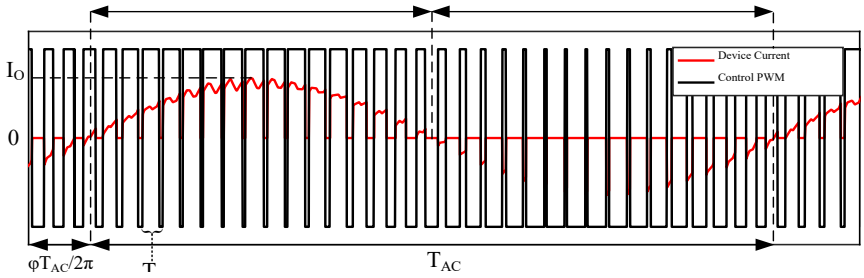


Figure 4.6. SPWM waveforms for a power switch in an inverter topology (Simulink) [J3].

4.2.2 Converter Model

The chosen application for this case study was a photovoltaic (PV) grid-connected three-phase micro-inverter (3P-VSI) [103]. Figure 4.5 depicts a typical circuit topology for this PE system. The voltage generated by the PV array is boosted and regulated by a DC/DC conversion stage before being supplied to the 3P-VSI. The proposed ET simulation only focuses on the inverter stage, i.e. the power module. Therefore, the DC-bus voltage is assumed constant and the grid modeled as a RL load. The converter and power module specifications are listed in Table 4.1.

The converter is controlled by a 2-level sinusoidal PWM (SPWM). An analytical model was implemented to calculate the power loss generated by each device. Considering the SPWM switching waveforms in Figure 4.6, the duty-cycle (DC) for MOSFET and SBD at the n-th switching period T_s can be derived as in (25), where M is the modulation index and T_{AC} is the AC output fundamental period. The average device power loss for the n-th T_s is calculated as in (26), where the V_{on} and the E_{sw} are obtained from the compact device model.

$$DC^n = \begin{cases} DC^n_{MOS} = \frac{1}{2}[1 + M \cdot \sin(2\pi f_{AC} \cdot nT_s)] & if \ \ 0 \le nT_s < \frac{T_{AC}}{2} \\ DC^n_{SBD} = \frac{1}{2}[1 + M \cdot \sin(2\pi f_{AC} \cdot nT_s)] & if \ \ \frac{T_{AC}}{2} \le nT_s < T_{AC} \end{cases} \quad (25)$$

$$P_{tot}^{n} = \begin{cases} V_{on,MOS}^{n}\left(I_o^n, T_j^n\right) \cdot I_o^n \cdot DC_{MOS}^{n} + E_{sw,MOS}\left(I_o^n, T_j^n\right) \cdot f_s & if\ \ 0 \le nT_s < \frac{T_{AC}}{2} \\ V_{on,SBD}^{n}\left(I_o^n, T_j^n\right) \cdot I_o^n \cdot DC_{SBD}^{n} + E_{sw,SBD}\left(I_o^n, T_j^n\right) \cdot f_s & if\ \ \frac{T_{AC}}{2} \le nT_s < T_{AC} \end{cases} \quad (26)$$

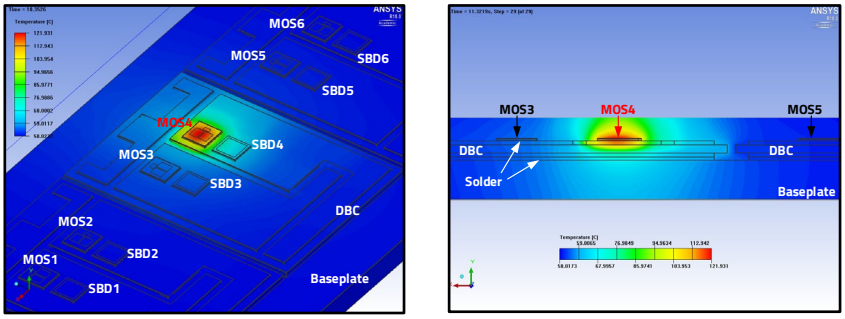
4.2.3 Thermal Model

Foster-type thermal impedance networks (Section 2.3.1) have shown great versatility and performance in the ET modeling of power modules [69]. The extraction of a Foster-type thermal model for a power module comes with a series of consideration about its operating conditions and boundaries. FEM software to observe the transient temperature evolution for a given power loss injection needs to be properly gauged to obtain meaningful results. Primarily, the geometry and material properties have to be properly defined. Table 4.2 lists the layers making up the thermal stack from the chip to the baseplate and reports their thickness and material properties. The temperature dependency of 4H-SiC and Al_2O_3 thermal properties was taken into account, since it shows a non-negligible variation in the considered temperature range [10], [11]. On the other hand, the other materials' properties do not present a strong dependency with temperature and can be assumed constant in the same range.

Additionally, the geometry has been simplified by removing bond wires, terminals and plastic case, in order to reduce the number of mesh elements. These parts, in fact, are not significantly influenced by the heat flow from junction to baseplate. The use of a constant case temperature or a heat-transfer coefficient

TABLE 4.2 – THERMAL STACK GEOMETRY AND MATERIAL PROPERTIES

Layer	Thickness [μm]	Density [kg/m³]	Thermal Conductivity [W/m·K]		Specific Heat Capacity [J/kg·K]	
			Temp. [°C]	Value	Temp. [°C]	Value
Chip (4H-SiC)	180	3240	25	353.3	25	551.8
			125	257.7	125	585.1
			225	202.8	225	634
Solder (SnAgCu)	100	7370	all	57	all	220
DBC Copper	300	8960	all	401	all	385
DBC Al_2O_3	380	3965	25	37	25	785.5
			125	27.2	125	942
			225	20.9	225	1076
DBC Copper	300	8960	all	401	all	385
Solder (SnAgCu)	250	7370	all	57	all	220
Baseplate (Cu)	3000	8960	all	401	all	385



(a) (b)

Figure 4.7. Simulated temperature distribution map on the top surface (a) and vertical cross section (b) of the studied module (ANSYS Icepak).

(HTC) is extensively discussed in [71] and heavily influences the simulation results. While a constant baseplate temperature can emulate the effect of a controlled hotplate in a lab setup, an HTC is a significantly more realistic approximation of the behavior of a cooling system in a PE application. In fact, the amount of heat that a heatsink can dissipate defines much of the temperature distribution within the module, including the amount of thermal cross-coupling among different chips [70]. An HTC between 3 and 10 kW/m^2·K (typically obtained with forced water-cooling) represents a reasonable value for the studied module. Figure 4.7 shows the temperature distribution plot in a steady-state simulation where 50 W are constantly dissipated by one MOSFET chip and the baseplate bottom surface is set to HTC=10 kW/m^2·K with a reference temperature of 50°C for the heat exchange. The power source has been modeled as a rectangular surface placed 1 µm below the chip's top surface, i.e. at the junction. Looking at the top surface (Figure 4.7.a) and cross-section (Figure 4.7.b) temperature distribution, it is clear that the heat spread reaches the antiparallel SBD in the proximity of the MOSFET, while the other chips are negligibly affected.

If only the cross coupling between MOSFET and SBD on the same copper trace are considered, the equivalent thermal network for each couple can be constructed as in Figure 4.8.a [J3]. The thermal cross coupling is included as a dependent source ΔT_{cc}, whose value is defined by the power injected by the coupled chip. The transient thermal impedance curves for MOSFET and SBD are plotted respectively in Fig. Figure 4.8.b and Figure 4.8.c, including the cross-coupling impedance. The junction temperature was measure in the chip's top surface center pint. A MATLAB-based curve fitting tool has been used to extract the chain of equivalent RC elements. The fitting curves, also reported in Figure 4.8, approximate the simulated curve with >99.7% accuracy in every case. A three-element chain models the $Z_{jc}(t)$, whereas two element are sufficient for the $Z_{cc}(t)$. Simulations for the other chips in the module did not reveal a significant difference in the thermal impedance curves, confirming the assumption of heat flowing downwards through the thermal stack. Therefore,

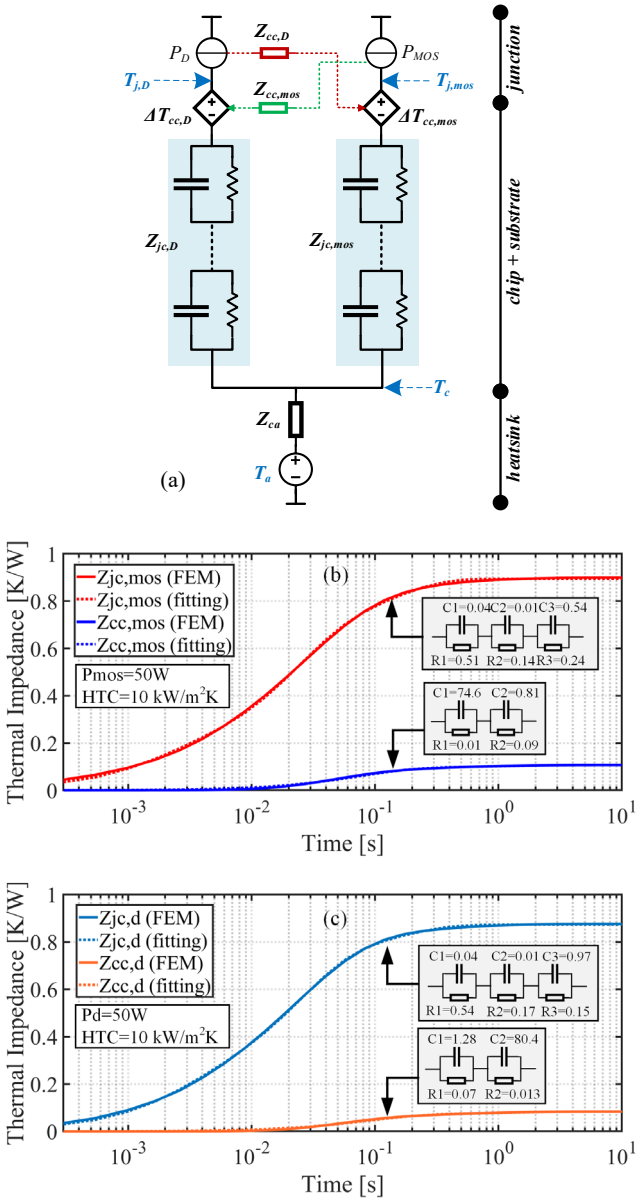


Figure 4.8. Thermal impedance network structure [J3] (a) and transient thermal impedance (junction-to-case and cross coupling) plot for the SiC MOSFET (b) and the SiC SBD (c).

the network structure for the whole model was obtained by using six networks like the one in Figure 4.8 and connecting them to a common T_c node. The dependency

of the $Z_{jc}(t)$ curve on the injected power was found to be not particularly significant for this case study, with about 6% maximum variation within the device SOA, as also observed in [C4]. Additionally, the variation in HTC only shows a limited influence on the Z_{jc}, while affecting mostly the heatsink temperature [71].

4.2.4 Electrothermal Simulation Results

The complete electrothermal model was implemented and simulated in different operating conditions for the 3P-VSI. At first, the power conduction loss and switching energy mapping has been performed in the nominal operating range of the devices, i.e. up to 25 A load current and 150°C. The maps are charted in Figure 4.9.a-b for the SiC MOSFET and Figure 4.9.c-d for the SiC SBD.

In order to compare the estimated junction temperature to circuit-based simulation, an equivalent inverter topology was created in SABER and connected to the extracted thermal network. The devices' instantaneous power losses, calculated by multiplying on-state voltage and current, are injected in the thermal network. Additionally, the FEM model has been modified by adding power sources to each of

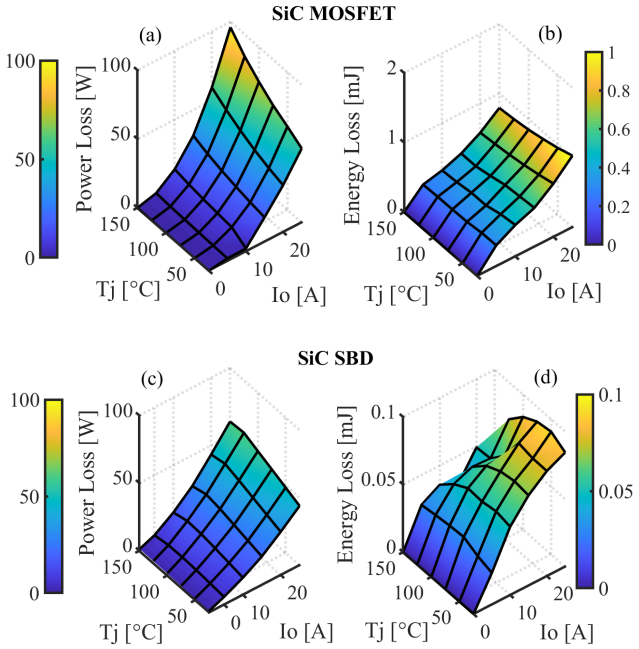


Figure 4.9. Conduction power losses and switching energy charts for (a-b) SiC MOSFET and (c-d) SiC SBD obtained from the compact model [J3].

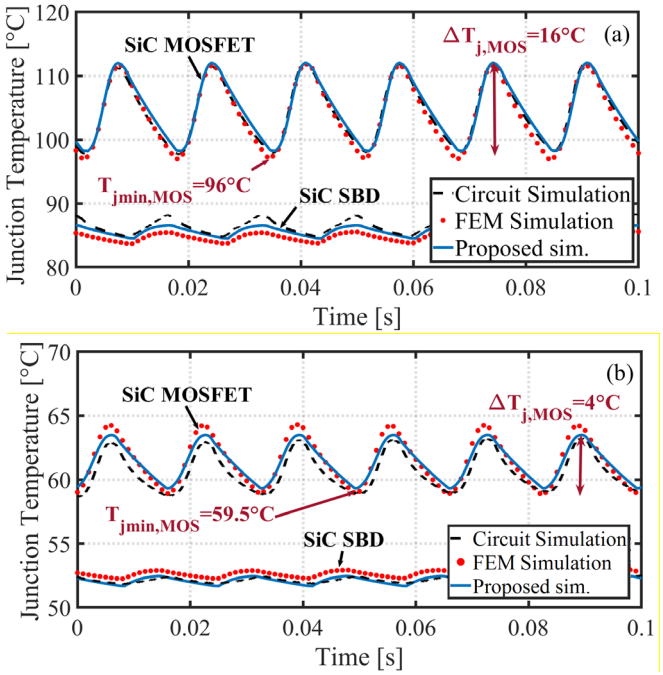


Figure 4.10. Comparison of simulated MOSFET and SBD junction temperature during inverter operation: Tc=80°C (a) and Tc=50°C (b) [J3].

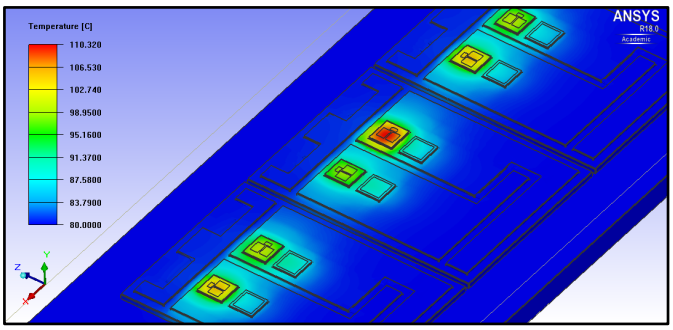


Figure 4.11. Simulated temperature map during inverter operation (ANSYS Icepak).

the chips and injecting an alternating power loss profile, generated using the LUTs, with 1 ms resolution. The case temperature was set to a fixed value in order to accelerate the convergence to steady state.

A comparison of the steady-state junction temperature fluctuation for MOSFET and SBD is plotted in Figure 4.10.a (Tc=80°C and Io=25 A) and Figure 4.10.b (Tc=50°C and Io=15 A). The results obtained in the three simulation methods show

TABLE 4.3 – SIMULATION SPEED COMPARISON

Simulated Time Span [s]	Elapsed Simulation Time / Maximum Time Step		
	Circuit-based Model (SABER)	FEM Thermal Model (ANSYS Icepak)	Fast ET Simulation
0.1	402 s / 1 ns	632 s / 1 ms	4 s / 100 μs

good matching in both the conditions. Figure 4.11 is a snapshot of the thermal simulation in ANSYS Icepack, showing the temperature distribution during the inverter operation.

Table 4.3 reports the comparison in elapsed computation time and maximum time step for the three different methods when simulating 100 ms of converter operation. While both the circuit-based and the FEM simulations take few minutes to complete, the ET strategy terminates in just few seconds. Nevertheless, the temperature estimation accuracy is preserved and the method offers an in-depth insight in the ET behavior of the module.

4.3 Summary

A procedure for the fast ET modeling of SiC power MOSFET modules has been presented in this chapter. The main scope of the simulation was the estimation of the junction temperature evolution in the chips, during a converter switching operation. A case study with a 3P-VSI was exemplified in this context. A combination of circuit-based and FEM simulation has enabled the extraction of an accurate lumped multi-physics model which fully takes into account temperature dependency and module geometry. The proposed simulation approach yields results comparable to other approaches in a significantly smaller amount of time. Therefore, the method was proven suitable for system-level optimized design and the analysis of long term-mission profiles in SiC MOSFETs. This latter feature will be explored in the next chapter, where the proposed approach is used for reliability prediction.

Chapter 5
Lifetime Prediction and Aging Effects in SiC Power MOSFETs

5.1 Mission-profile-based Lifetime Estimation

In the reliable design of PE systems, the analysis and consideration of the target mission profile (MP), i.e. the real ambient and load conditions in the field, can be crucial in the development of cost-effective and robust solutions [106]. In particular, the long term-reliability of each component depends significantly on the amount of stress received in the studied application [18]. For instance, the lifetime consumption of a switching device is largely influenced by the level of usage and the related thermal stress, which can be obtained by translating the application MP into the respective device loading [107]. In many MPs, especially those related to renewable energy conversion, the fluctuations in ambient and loading conditions might be

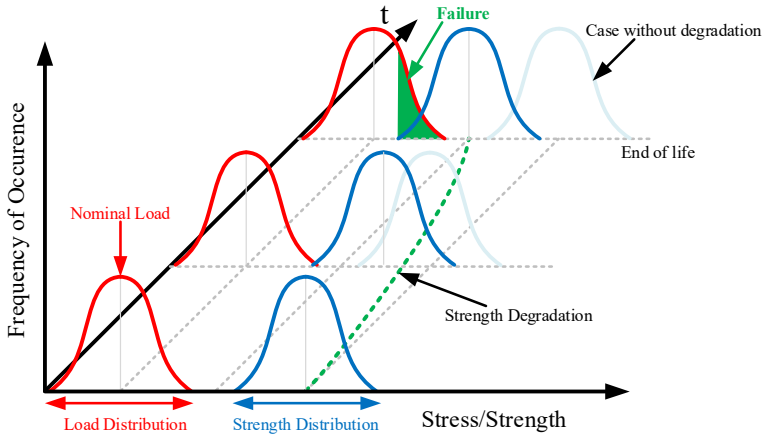


Figure 5.1. Evolution of load and strength distributions over the lifetime of a PE component [106].

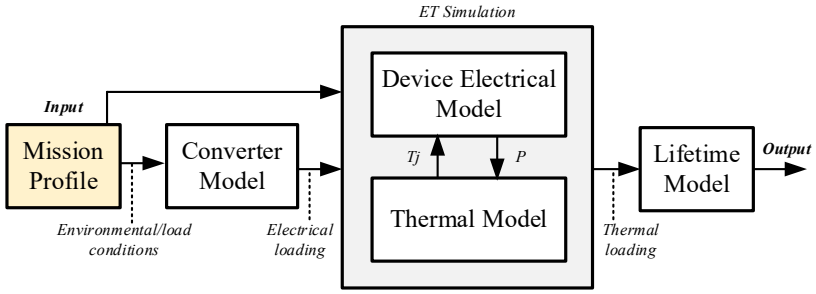


Figure 5.2. Typical workflow of a MP-based lifetime estimation.

significant throughout the lifetime of a device. The load (MP) and the strength, i.e. the robustness boundaries for the chosen design, can be represented by two probability density functions [108], like in Figure 5.1 [106], determined respectively by the variation in operating condition and manufacturing. When the component undergoes degradation over time, its strength distribution shifts. If the load and strength distribution overlap, the common area is a probability of failure. This explains how the reliability and robustness of the system are ultimately defined by the load/stress distribution associated with a certain MP. Therefore, the choice of proper design margins for a reliable and cost-effective system needs to be driven by the analysis of a real MP. This is especially true for WBG devices, where cost-effective and tailored solutions could drastically improve the diffusion of this technology in the field.

Previous studies have addressed the MP-based reliability estimation of power converters and devices in [95], [96], [109]–[114]. The handling of a long timescale often requires a very high degree of approximation, which affects the result's accuracy. Many of these approaches rely on simple analytical device models or look-up tables to extract the power losses, with limited or no temperature dependency. The assumption of constant heatsink temperature further reduces the accuracy in some of these studies. Additionally, the choice of the MP sampling time should be specifically related to the selected degradation mechanism and lifetime model [115].

Although using different assumptions and complexity, all MP-based approaches roughly follow the simulation workflow depicted in Figure 5.2. The MP, containing information about environmental conditions (i.e. ambient temperature, wind speed, solar irradiance, etc.) is translated into an electrical loading profile for the power semiconductor using a converter model, which accounts for the switching pattern and power output. Therefore, similarly to what presented in Chapter 4, an ET simulation allows the estimation of the device thermal loading during the MP. At last, a lifetime model, often accompanied by a cycle counting algorithm, provides the prediction of accumulated damage and remaining useful lifetime (RUL) for the component.

5.1.1 Characterization of a Mission Profile

An MP-based lifetime prediction strategy for a SiC PV inverter has been presented in [J3]. This approach links the ET simulation procedure presented in Section 4.2 with a novel MP mapping strategy aimed to increase the simulation speed, while at the same time preserving enough resolution to observe the junction temperature evolution on a millisecond timescale. This degree of precision is required if the aim is studying the lifetime consumption due to bond wire aging, since

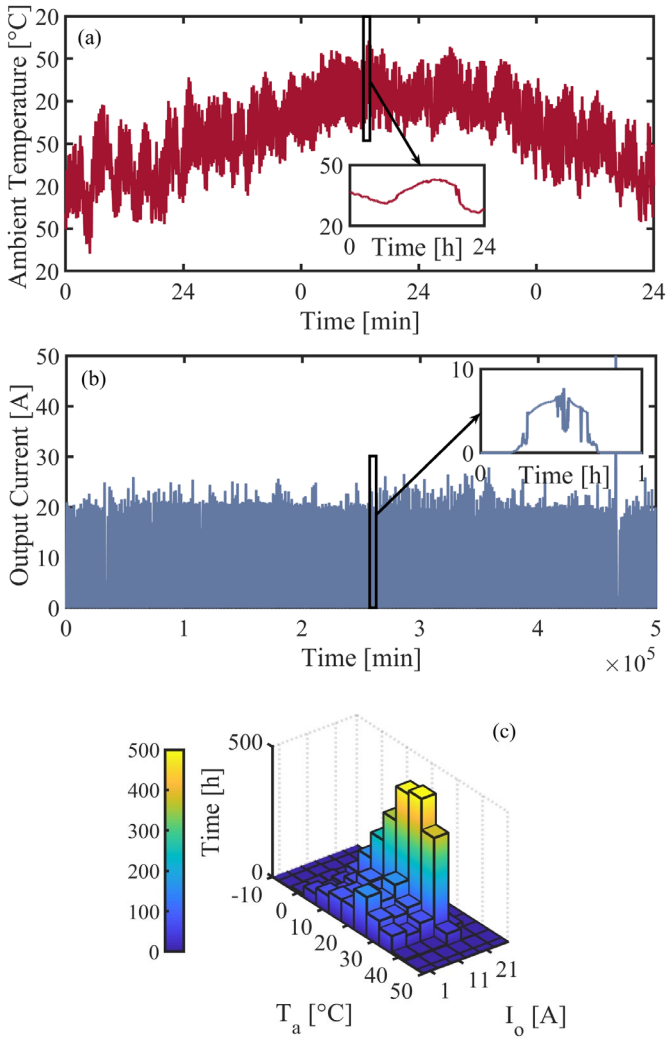


Figure 5.3. Ambient temperature (a) and output current (b) for 1-year PV mission profile; operating condition occurrence mapping (c) [J3].

the fast temperature cycles due to AC-frequency load fluctuation may cause this kind of degradation.

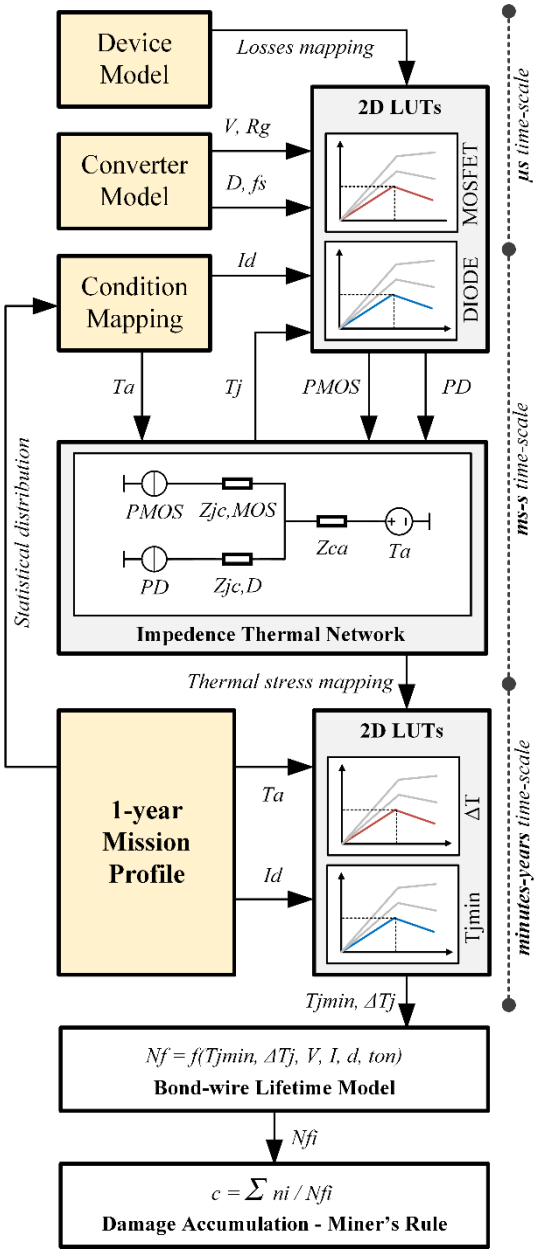


Figure 5.4. Flowchart of the proposed MP-based lifetime prediction algorithm [J3].

An MP for a PV application usually consists in ambient temperature T_a and solar irradiance field data. If a 1-minute sampling time is used, a 1-year MP will comprise 525600 points. The continuous simulation of such a time span using the fast ET simulation in Section 4.2, with a resolution of 1 ms, would be extremely lengthy and unpractical. However, the MP, rather than a time-sequence can be interpreted as a statistical distribution of operating conditions for the converter. For example, the MPs in Figure 5.3 (solar irradiance has been translated into converter output current I_o), has been mapped into 2D histograms based of the occurrence of matching T_a and I_o conditions, with a grid resolution of 5°C and 5 A, respectively [J3]. The histogram offers a visual indicator of the environmental and loading conditions for the same converter in the field – in this case a site in Arizona. Assuming that the converter sustains a steady-state operation within the MP sampling time, every couple of T_a and I_o will lead to a specific steady-state temperature evolution on the device. By discretizing the number of operating conditions in the histogram, only a reduced number of ET simulations are required to estimate the device temperature. In fact, the number of ET simulations only depends on the mapping grid resolution. The temperature information, for instance minimum junction temperature $T_{j,min}$ and cycle amplitude ΔT_j, for each operating condition, resulting from the ET simulation, can be collected into lookup tables (LUTs) and interpolated to reconstruct the thermal loading of the device during the whole MP and calculate the lifetime consumption, saving a significant amount of computation time.

The full flowchart of this procedure is reported in Figure 5.4. The algorithm consists in a two-step condition mapping: the first used to extract the power loss LUTs from a compact device model and the second to obtain the thermal loading LUTs in the operating range defined by the MP using the ET simulation. The LUT values depend greatly on the cooling system considered used in the design, which is included in the model in the form of a case-to-ambient thermal impedance Z_{ca}. An example of the thermal load mapping is reported in Figure 5.5 [J3], where the $T_{j,min}$

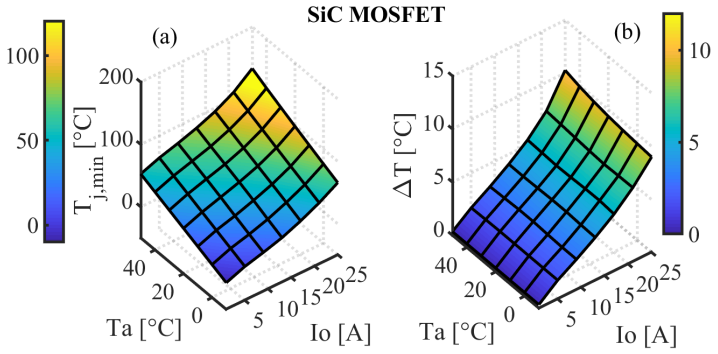


Figure 5.5. SiC MOSFET thermal loading maps over the full operating range defined by the MP: minimum junction temperature (a) and cycle amplitude (b) during AC steady-state operation [J3].

(Figure 5.5.a) and ΔT_j (Figure 5.5.b) of one of the SiC MOSFET dies are charted in function of T_a and I_o, for Z_{ca}= 0.3 K/W. The mapping time with the chosen grid is around 2 minutes, requiring 49 iterations in total. Of course, the use of a finer or coarser grid affects the simulation time and the lifetime prediction (see Section 5.1.2).

The reason for the use of $T_{j,min}$ and de ΔT_j as indicators for the thermal loading is driven by the choice of the lifetime model and the damage accumulation method, which is discussed in the next subsection.

5.1.2 Lifetime Modeling and Damage Accumulation

The long-term reliability analysis for SiC power devices and modules in real operation is still at his early stage. In fact, the scarce diffusion in the applications does not allow having comprehensive field data about their aging process and failure modes yet. The information available in the literature is mostly resulting from accelerated power cycling tests of commercial components, for instance those conducted in [28], [116]–[119]. An active (or DC) power cycling consists in pulsing constant DC current through the devices under test (DUTs), generating a cyclical temperature swing and monitoring the evolution of the devices' on-state voltage drop. In these contributions, the main cause of failure is attributed to the package, whose technology is actually identical to the one used for Si power semiconductors. In other studies, like [120] and [121], the die degradation, especially drift in the threshold voltage and increased leakage currents, were observed to have a significant impact on the device lifetime. In some of the reported tests, the number of cycles to failure N_f is lower than those obtained for Si devices with similar rating, and the samples reach end-of-life (EOL) within 30-40% of the Si device lifetime. Based on the simulation study carried out in [122], the reduced size and greater stiffness of the 4H-SiC die, worsens the thermo-mechanical stress at the die-attach interface, reducing the power-cycle lifetime. However, the available reliability data is still too limited for the development of an effective lifetime model for SiC technology. Nevertheless, it is possible to carry out a reliability analysis for SiC devices, by using available lifetime models resulting from the testing of established packaging technology [110]. Bond wire damage and solder fatigue are the most common aging factors observed in nowadays power modules [24], [123]. Various factors influence the power-cycling lifetime of wire-bonded and soldered power modules, as observed in [25], among which wire bond diameter and aspect-ratio, cycle duration, average temperature and temperature swing. Other contributions have identified bond-wire cracking and liftoff as the modes with major impact on the EOL [124], [125], since solder fatigue rarely leads to a complete open-circuit failure. The reduction in chip size is the general trend for SiC devices – about 40% footprint reduction since 1st generation (Wolfspeed) [126] – resulting in higher thermal impedance, thus in larger thermal stress due to electrical load variation. This might be especially true for the stress resulting from output frequency temperature swing and its influence on bond-wire damage [124], [127], which is usually neglected in other reliability studies such

as [113]. In [J3], a mission-profile-based simulation has been implemented to investigate this effect in a SiC power module. The model used for the lifetime prediction was the one proposed by Bayerer et al. [27] from Infineon in 2008, resulting from the interpolation of extensive power cycling test data. The commercial 1.2 kV IGBT4 modules used in this study [128] feature a standard Al wire-bonded packaging technology with baseplate, DBC substrates and soldered dies. The similarity in structure and power rating to 1.2 kV multi-chip modules by CREE, as the one studied in [J3], justifies the application of this model. The N_f are calculated as in (27), accounting for the effect of heating pulse time t_{on}, the blocking voltage V, the current per bond wire I and its diameter d. The equation brings together the dependency on the temperature cycle amplitude ΔT_j as a Coffin-Manson equation and an Arrhenius-law dependency on the minimum cycle temperature $T_{j,min}$ in the exponential term [129]. The parameters A and β are derived from the regression of experimental curves in [27]. A modification of the A parameter has been made to take into account the

$$N_f = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j,min}+273}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot d^{\beta_6} \tag{27}$$

Once the Nf has been calculated for each operating condition, a damage accumulation method can be applied to quantify the consumed lifetime. The Miner's rule [130] is the most used damage accumulation method for power semiconductors. In (28), the damage c consists in the linear sum of the damage that the power device undergoes during each stress condition, where the number of cycles n_i elapsed in the *i-th* conditions are divided by the $(N_f)_i$ estimated for the same condition. According to this method, the EOL is reached when c=1.

$$c = \sum_i \frac{n_i}{(N_f)_i} \leq 1 \tag{28}$$

Experimental evidence of the effectiveness of this rule, has been found in [32] and [33] for IGBT multi-chip modules where bond-wire fatigue was identified as the main failure mechanism.

Applying the described mapping procedure and based on (27) and (28), the accumulated bond-wire damage prediction resulting from the MP shown in Figure 5.3 is reported in Table 5.1for both SiC MOSFET and SBD. The low usage and power losses (see Section 4.2.3) of the SBDs in the module (i.e. only freewheeling) determines a very low damage. The prediction for the MOSFET bond wires would result in about 38.5 years of operation with the same mission profile before EOL. However, the results of this prediction are only considering the impact of the fast

TABLE 5.1 – 1-YEAR ACCUMULATED BOND-WIRE DAMAGE

SiC MOSFET bond-wire damage	SiC SBD bond-wire damage
0.026 (2.6 %)	$<10^{-2}$ %

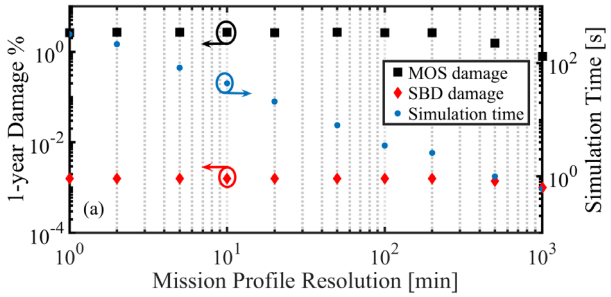


Figure 5.6. Impact of MP resolution on estimated damage and simulation time [J3].

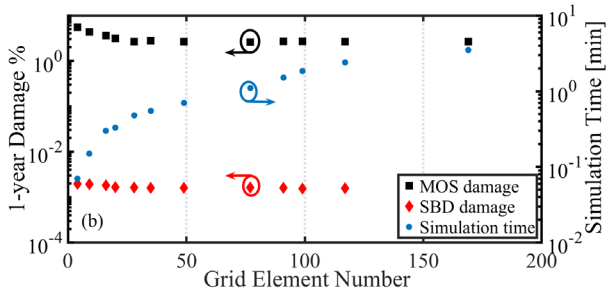


Figure 5.7. Impact of mapping grid resolution on estimated damage and simulation time [J3].

output-frequency thermal cycling, while there are other factors influencing the EOL of a power module. It is hard to assess a range of tolerance of the values resulting from the prediction, due to the complex propagation of uncertainties between the different parts of the algorithm. Nonetheless, [J3] provides additional insight on how this fast lifetime prediction strategy can be useful to run comparative analysis and optimizing the system design for reliability; for instance by comparing the effect of two or more different MPs, variation in switching frequency or case-to-ambient thermal impedance.

Additionally, it is interesting to evaluate how the damage prediction is affected by a change in the MP sampling time (Figure 5.6) and the number of elements in the mapping grid (Figure 5.7). One can see that MP resolution up to 1 h does not significantly influence the accumulated damage, whereas the simulation time is drastically reduced. On the other hand, a coarse mapping grid yields inaccurate lifetime results, even though the simulation time is sped up considerably. It is worth to note that this considerations hold for the specific MP. In fact, the load changes in one hour of PV operation may not be considerable, especially with favorable weather conditions, and the inaccuracy on the damage prediction tends to be higher when considering slow temperature cycles, as observed in [115].

5.2 Including Aging Impact

While the previous section provided an estimation of the accumulated damage for a given degradation mechanism during a MP, it did not consider what the impact of such degradation could be on the device performance throughout its lifetime. The study in [J2] aimed to evaluate the deviation in thermal stress during a MP by introducing different stages of degradation in the model. Rather than using reliability prediction to assess the remaining lifetime, this work was meant to calculate the impact of device and package wear on the device electrothermal performance, based on the recurring aging phenomena observed in the literature. In particular, the power cycling conducted in [28], [116], [118], identify and separate package- and die-related degradation mechanisms for both 1.2 kV discrete SiC MOSFETs and power modules. The two main aging effects included in [J2] were:

- The gate threshold voltage V_T shift, which has been repeatedly observed in the literature as an aging precursor both in DC power cycling [28] and high-temperature gate bias (HTGB) tests [133], with deviation up to 10% from the initial value;
- The thermal impedance degradation due to solder fatigue, which appears to be worsened by the reduced chip size and higher stiffness of SiC material [122], [134]. The studies in [135] and [136] clearly point out the formation of cracks and void areas in the solder, which can propagate during the lifetime.

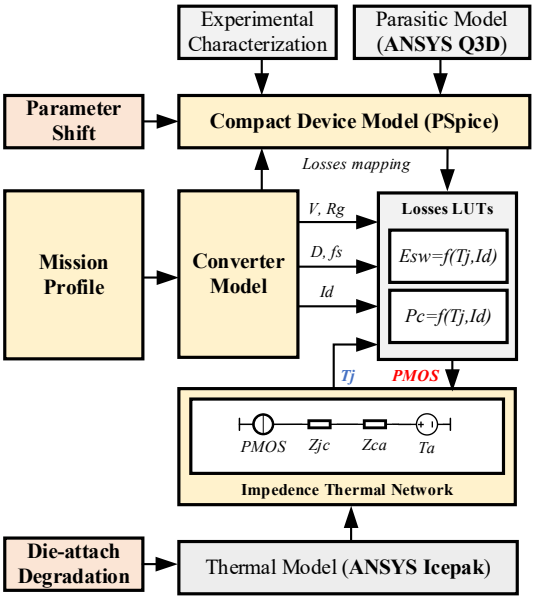


Figure 5.8. Modified MP-based ET simulation flowchart including aging impact [J2].

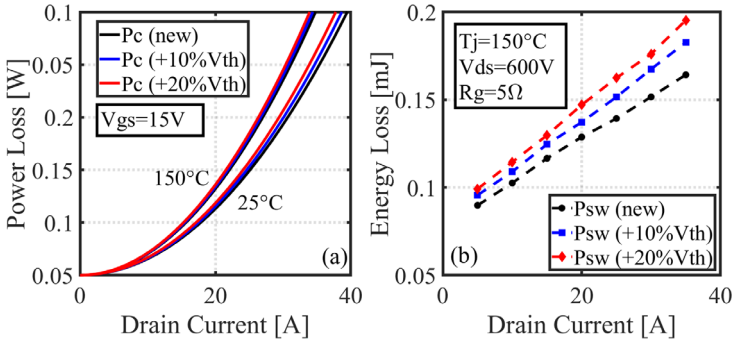


Figure 5.9. V_T drift impact on the conduction power losses (a) and switching energy (b) vs. drain current [J2].

The fast ET simulation algorithm presented in Section 4.1, has been modified in [J2] to include the parameter shift in the compact device model (PSpice) and the thermal impedance extraction from FEM simulation (ANSYS Icepak), as shown in Figure 5.8.

The same 1-kV/35-A discrete device characterized in Case Study I (Chapter 3) has been used for this simulation. The conduction power losses P_c and switching energy losses Esw have been extracted in case of a 10% and a 20% shift in the V_T and reported in Figure 5.9.a-b against drain current. This has shown a maximum increase in P_c ranging from 3 to 6%, depending on the T_j, and a significant increase (12% on average) in the E_{sw}.

The change in junction-to-case thermal impedance Z_{jc} due to different levels of die-attach degradation is shown in Fig. 5.10. The results have been extracted from the FEM transient thermal simulation of the TO-247-4 package structure, where a 1-µm thick void volume was introduces in the die attach with respectively 20% and 40% of the solder area, starting from the die edges, as depicted in Figure 5.10. Up to 35% deviation in $Z_{jc}(t)$ was found in these conditions.

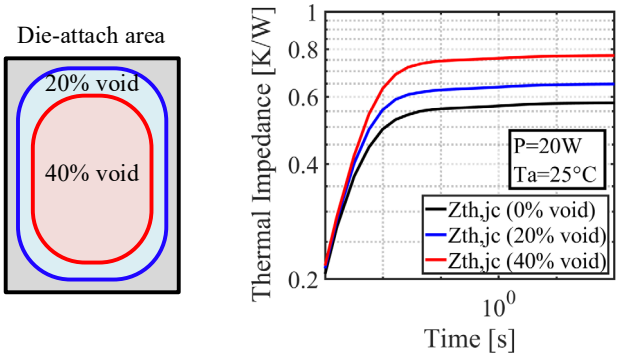


Figure 5.10. Degradation of $Z_{jc}(t)$ due to different degrees of solder voids.

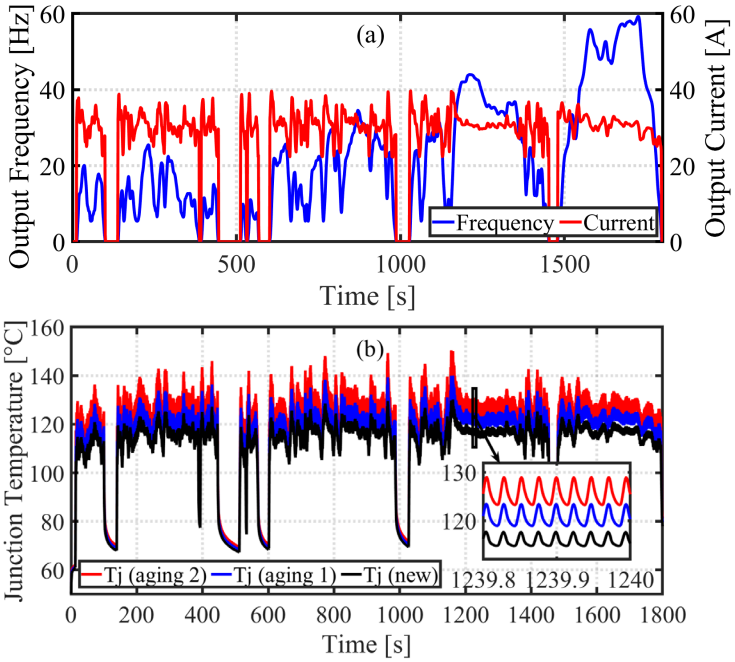


Figure 5.11. Electrical loading MP for a traction 3P-VSI (a) and simulated T_j evolution at different levels of device degradation (b) [J2].

A 30-min drive-cycle for automotive [137] was translated into electrical loading for a 30 kW 3P-VSI, generating the output current and frequency MPs shown in Figure 5.11.a. The electrical loading was therefore translated into thermal loading, assuming a simple six-switch topology with the devices connected to the same heatsink. Additional details about the simulation are provided in [J2]. Two aging levels were defined: *aging 1* with +10% V_T and 20% solder void area; and *aging 2* with +20% V_{TH} and 40% solder void. The T_j evolution during the mission profile for the pristine device and the two aging levels is reported in Figure 5.11.b. The thermal loading is consistently higher for the degraded device, with an increase in average cycle temperature and cycle amplitude.

The occurrence of higher temperature and larger temperature swings during the lifetime of the device due to aging is an important factor and has to be taken into account when designing the safe-operating area (SOA) margins for the system. Operating condition out of the SOA boundaries might be harmful for the device and trigger additional failure mechanisms.

5.3 Summary

The mission-profile-based lifetime prediction of a SiC power module has been addressed in this chapter. A fast condition-mapping technique for the 1-year MP and

the thermal loading has allowed shrinking the overall simulation time down to a few minutes, preserving an insight on the sub-second junction temperature dynamics, which contribute to the degradation of bond wire interconnections. In comparison to previous art, where the MP was simulated sequentially and very simple device models were used, this approach represents a significant step forward in speed and accuracy. Additionally, the influence of device and die-attach aging on the thermal stress resulting from a 30-min MP has been evaluated for the first time in a discrete SiC MOSFET, implying that the converter design margins have to be chosen according to the loading and degradation undergone in the selected application.

Chapter 6
Conclusion and Future Work

6.1 Summary

In the fast development of power electronic (PE) technologies, the revolutionizing potential of WBG semiconductor devices is yet to be fully exploited. This project aimed to explore the behavior of SiC MOSFETs by means of different modeling and simulation approaches, aiming to provide a functional toolbox for the reliable design of PE systems based on these devices. A brief summary of the Ph.D. thesis is reported in the following section.

An introduction to the project background and main research questions was provided in Chapter 1. The main challenges related to the diffusion of WBG and especially SiC power semiconductors were thoroughly addressed, as well as the current reliability stage of modern power devices. Chapter 2 sets a deeper focus on the normal and abnormal operation of SiC power MOSFETs and describes the structure and identification of the compact device model. Moreover, the low SC withstanding capability and failure mechanisms of these devices was identified as one of the main weaknesses. Thereafter, a Spice-based implementation of an existing physics-based device model has been extended and modified with SC simulation capability and improved temperature dependency. A user-friendly MATLAB tool was developed to identify the model parameters using experimental static curves, resulting in an accurate matching of the characteristics. The device-level characterization and simulation process is described in Chapter 3, where two Case Studies with commercial devices are reported. The model transition from a discrete single-chip package to a high-power multi-chip module is addressed and supported with experimental data. The first simulation of SC behavior in a SiC module with paralleled chips allowed identifying the impact of parameter and layout mismatch on the robustness against thermal instability mechanisms that lead the module to catastrophic failure. Once the full validation of the device model was completed, the project focus shifted towards the fast ET simulation of SiC-based circuit topologies, presented in Chapter 4, aimed to the estimation of the semiconductor thermal loading. Different algorithms were tested for this purpose, based on a multi-physics approach, which spans various software environments to combine the device model with lumped-element models for the package parasitics and the thermal behavior.

The offline mapping of the device power losses in the full operating range resulted in very fast simulation time for a 3P-VSI inverter module. While the circuit-based simulation focused on events in very short timescales, the fast ET approach can be used to simulate long MP in a relatively short time, as described in Chapter 6. It has been demonstrated that the simplification of a MP into a number of recurring operating conditions heavily affects the computation time when quantifying the consumed lifetime of the bond wires. As emerged from the simulations, with small-area SiC MOSFET chips, the fast junction temperature fluctuations during inverter operation may determine non-negligible damage over large timespan. Further sensitivity analysis assessed the influence of MP resolution and other factors on the lifetime prediction. Additionally, the influence of the degradation in device and package properties on the thermal stress has been evaluated and reported.

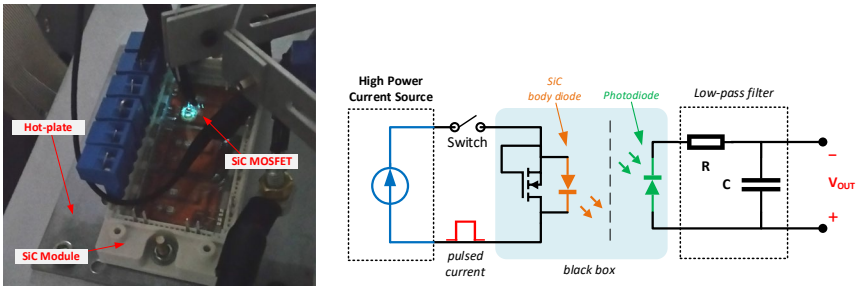
6.2 A Side Topic: Using SiC Photoemission as a temperature-sensitive optical parameter (TSOP)

Accurate temperature sensing and monitoring is a key element in the reliability analysis of power semiconductors. Many direct and indirect measurement methods have been experimented in the latest years, including infrared (IR) imaging, fiber optics and temperature-sensitive electrical parameters. Nevertheless, the search for cheap, non-invasive and accurate sensing approaches is still ongoing.

The phenomenon of visible light emission (photoemission or electroluminescence) in SiC MOSFET chips has been observed in laboratory tests during the project. While the photoemission from semiconductor material has been used for decades in the manufacture of light-emitting diodes (LEDs), this phenomenon is parasitic in power semiconductor switches. The observations in [138] and [139] demonstrate that a 4H-SiC p-n junction emits photons in two different wavelengths: one related to the bandgap energy (about 3.2 eV peak emission) and the other to the deep-level defect bands (around 2.45 eV). Therefore, the light emission occurs in the visible spectrum, although in an indirect bandgap semiconductor such as SiC the radiative recombination process is rather inefficient. Nevertheless, the luminescence intensity is dependent on both junction temperature T_j and current I_f, which represents a valuable indicator for device-monitoring purposes. In a MOSFET, the light emission is only triggered during third quadrant operation, i.e. conduction through the body diode.

The experimental characterization conducted in [J4] represents the first proof of concept for the use of electroluminescence as a temperature- (and current-) sensitive optical parameter (TSOP). A similar study was conducted and published by Winkler et al. [140] shortly afterwards, with rather interesting current-sensing results.

The experimental setup, visible in Figure 6.1, included a multi-chip power module [141] (the picture also shows the MOSFET luminescence), a hotplate and a simple sensing circuit based on a Si PiN photodiode with good sensitivity over a wide visible wavelength range (400-1000 nm) [142]. A RC filter was added to



(a) (b)

Figure 6.1. Picture (a) and electrical schematic (b) of the light emission measurement setup [J4].

transduce the photodiode current signal in a voltage and reduce the measurement noise. The measurement method consisted in biasing the MOSFET body diode with different current levels and at different junction temperature, while the photodiode was placed 2 mm away from the chip, in contact with the gel.

The measurement procedure and the compensation for self-heating are described in detail in [J4]. The tests were conducted for two samples. Figure 6.1 shows he sensed photodiode voltage output at different I_f (Figure 6.1.a) and T_j values (Figure 6.1.b) for one of the samples. A behavioral calibration function relating the light emission sensed by the photodiode with T_j and I_f could be worked out after the measurements. The results of the characterization are charted in Figure 6.3.

The measurements have proven a good sensitivity and linearity for this method, especially for the current dependency of V_{out}, found at 1-5 mV/A, while the temperature dependency is around 0.5-1.2 mV/°C. It has been observed that he photoemission level changes for different samples, which is due to the manufacturing

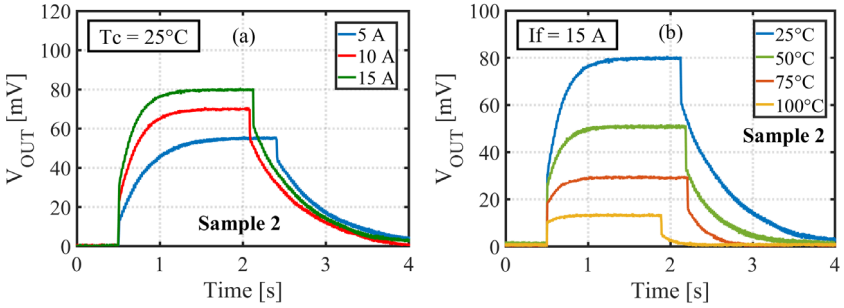


Figure 6.2. Measured photodiode output voltage for different current (a) and temperature (b) conditions [J4].

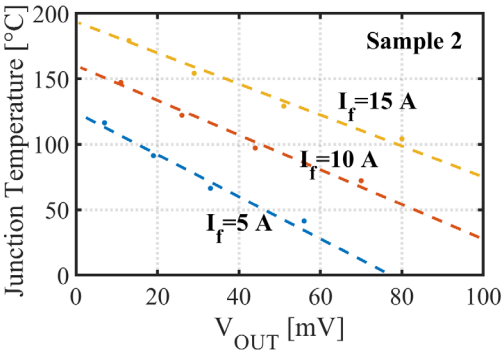


Figure 6.3. Photoemission characterization results: T_j vs. photodiode V_{out} at different I_f [J4].

deviation and defect concentration. This means that individual calibrations have to be performed for different chips. Nonetheless, this TSOP has a remarkable potential for implementation in PE applications, being cheap, non-invasive and electrically isolated. More recent studies, like [143] in 2019, although using more sophisticated optical measurement systems, have already demonstrated promising results.

6.3 Research Highlights

The main contributions of this Ph.D. project are summarized as follows:

Comprehensive survey of the state-of-the-art reliability of SiC MOSFETs

The literature contributions concerning the present stage of research about SiC MOSFET power semiconductor devices and modules have thoroughly been explored and collected. The literature research covered several aspects of the reliability and robustness, including SC behavior and degradation phenomena. The resulting survey, collected in different publications and in the final report, may represent a valuable basis for further research in the field.

Implementation of a compact Spice-based SiC MOSFET model

The initial phase of the Ph.D. project has been dedicated to the refinement and extension of an existing physics-based SiC power MOSFET model. The main innovative features of this model include improved temperature dependency and SC behavior. Additionally, a Spice-based implementation of this model and a Matlab-based parameter extraction tool have been an essential element in the following simulation work. The model has been validated with experimental data from static and switching measurements in a wide range of normal and abnormal operating conditions.

Simulation of short circuit in a SiC multi-chip power module

The implemented compact device model enabled the SC simulation of a commercial multi-chip power module. The simulation results evidenced the inherent low SC robustness of paralleled chips, due to the occurrence of thermal instabilities caused by parameter and layout mismatch, thus confirming the experimental results. An insight on the junction temperature evolution during SC has also been provided.

Development of fast ET simulation strategies for discrete SiC devices and power modules

Several commercial SiC power components have been characterized in this project, as seen in the Case Studies reported in this work. Multi-physics FEM simulation has been used to extract lumped models for package parasitics and thermal impedance. This allowed the implementation of ET simulation and co-simulation algorithms that exploit the benefit of compact models to offer low computation time and at the same time, preserve the accuracy and resolution to observe small timescales. The proposed algorithms can be used for the reliability- and/or performance-driven optimization of SiC PE converters or to define the SOA for a chosen design.

Study of SiC MOSFET reliability based on mission-profile simulation

The device model and fast ET simulation implemented in the first stages of the project have been employed to evaluate the reliability of SiC power modules using a MP-based approach. This was especially effective at estimating the different levels of thermal stress resulting from variable load and ambient conditions. Different aging mechanisms have been selected and included in the model through parametric variations. The degradation impact on the thermal loading of the MOSFETs was discovered to be non-negligible and occasionally leading to operation outside the system SOA.

6.4 Proposals for Future Research Topics

The following section lists the possible future developments of this research project:

Use of simulation to enhance short-circuit withstanding capability

In order to improve the SC robustness in SiC MOSFETs, a more detailed device modeling required. FEM simulation could be a necessary step to observe in depth the SC behavior and operate modifications in the cell layout to mitigate the thermal stress at the chip top surface. Thereafter, a lumped ET model may be extracted to reduce the simulation complexity and estimate the temperature evolution. However it is essential that high-temperature dependency of thermal properties is accurately

considered to obtain accurate results, including melting of the top metallization.

Estimation of uncertainty in electrothermal simulation and mission-profile-based lifetime prediction

The MP-based simulation strategies presented in Chapter 4 and 5 contain a number of assumptions and approximations, combining multiple error sources, which could significantly influence the thermal stress and final consumed lifetime estimate. For many of the simulation steps the real entity of the error is quite difficult to evaluate. Nevertheless, it is possible to carry out an estimate of the result tolerance by propagating the known uncertainties in the process. For instance, the comparison of simulated and experimental device characteristics can be used to quantify the error in the calculated power losses and junction temperature. This would require the design of a laboratory test bench capable of simulating real MPs and measuring the device temperature.

Development of a reliability model for SiC power MOSFETs

A better understanding of the long-term degradation and failure mechanisms of SiC MOSFET discrete devices and modules is needed for developing a dedicated lifetime model. This would require a comprehensive amount of power cycling test data on a significant number of samples. Nevertheless, the testing activity can be combined with the thermomechanical stress simulation in multi-physics FEM software platforms.

Design of a temperature monitoring system based on photoemission

A cheap and non-invasive junction temperature measurement system based on the light emission of SiC MOSFETs can be designed and integrated in real applications. Photodiodes or photomultipliers appear to be the best candidate for light sensing. However, several challenges have to be overcome in this task. High sensitivity and noise immunity are necessary, as well as large measurement bandwidth. In fact, in real switching applications, the body diode conduction only occurs during dead time, requiring measurement speed in the range of nanoseconds.

Appendix

Half bridge topology for switching loss extraction (PSpice/LTspice)

```
XDUT D G S1 S Tj Tc C3M0065100K
X2 D3 Gh S1H D Tj Tc C3M0065100K

*GATE DRIVE CHARACTERISTICS
Rg    G1    G     Rg_var
Lg    G1    G2    5n
VgsL  G2    S1    PULSE(-4 15 0.1us 10ns 10ns {2us*0.4}
2us)
VgsH  Gh    S1H   -4

RDSENSE D S 10E12
RGSENSE G S 10E12

*DC BUS
Vd    D4    0     Vd_var
Cd    D4    0     200u

* LOAD CURRENT
Id    D3    Di    Id_var
Cload D3    D     50p
R_load Di   D     0.05

* SNUBBER CAPACITANCE
Csn   D3    Dsn   220p
Rsn   D     Dsn   10
Csn1  D     Dsn1  220p
Rsn1  S     Dsn1  10

* POWER LOOP STRAY INDUCTANCE/RESISTANCE
Lstray D4 D6 1n
Rstray D6 D3 0.5
LstrayS S S3 1n
RstrayS S3 0 0.5

.OPTIONS ABSTOL=1e-3 CHGTOL=0.01e-12 GMIN=1e-12
ITL1=1500 ITL2=2000 ITL4=10 RELTOL= 0.005 VNTOL=1e-3
.TRAN 0ns 2us 0ns 0.5n
.PROBE
.PRINT TRAN I(XDUT.VSENSE) V(RDSENSE) V(RGSENSE)
.ENDS
```

1 kV/35 A SiC MOSFET model in TO-247-4 (PSpice/LTspice) [J3]

```
.subckt C3M0065100K Dx Gx SKx Sx Tj Tc

*** PACKAGE PARASISTICS ***

Ld          D     Dp    9.5n
R_Ld        D     Dp    1e10
R_rld       D     Dx    0.56m

Lg          Gp    Gx    12n
Rg_int      G     Gp    4.64
R_Lg        Gp    Gx    1e10

Ls          S     Sp    10.4n
R_rls       S     Sx    4.8m
R_Ls        S     Sp    1e10

Lsk         sb    S     11.4n
RSK         SKx   sb    17.4m
R_Ls1       sb    S     1e10

*** THERMAL MODEL ***

GPloss 0 Tj value = {SDT(V(D,S)*I(VSENSE))}
R0    N1    Tj    407m
R1    N2    N1    243m
R2    N3    N2    210m
R3    Tc    N3    240m
C0    Tj    0     2.95m
C1    N1    0     8.42m
C2    N2    0     61.5m
C3    N3    0     500m

 ***** ON-STATE RESISTANCE MODEL *****

* device active area [cm^2]
.param A = {0.066}
* JFET area [cm^2]
.param Ajfet = {0.3*A}
* drift region dopant density [cm^-3]
.param Nb = {1.6e+15}
* foundamental electronic charge [C]
.param q = 1.6e-19
* drain series resistance [ohm]
.param Rs = {0.001}
* SiC dielectric constant [F/cm]
```

```
.param eps_semi = {9.66*8.854e-14}
* Boltzmann´s constant
.param k = 1.38e-23
* metallurgical drift region width [cm]
.param Wb = {6e-4}
* jfet region width [cm]
.param Wb = {0.6e-4}
* intrinsic carrier concentration
Eni   3     0     value =
{LIMIT(4.81E15*PWR(v(Tj),1.5)*exp(-18567/v(Tj)),0,1E11)}
REni  3     0     1E10
* built-in junction potential
EVbi  2     0     value =
+{LIMIT(k*v(Tj)/q*LOG(1E19*Nb/PWR(v(3),2)),0,100)}
RVbi  2     0     1E12
* quasineutral drift region width (W=Wb-Wdsj) [cm]
EW    1     0     value = {LIMIT(Wb-
+SQRT(2*eps_semi*(v(D)+v(2))/q/Nb),0,Wb)}
RW    1     0     1E12
* drift electron mobility
Eun   4     0     value =
+{LIMIT(947/(1+PWR(Nb/1.94e17,0.61))*PWR(v(Tj)/300,-
+1.1),0,1E3)}
Run   4     0     1E12
* drift+substrate resistance
ERb   5     0     value = {LIMIT(Rs + (Wb-
+v(1))/(q*A*Nb*v(4)),0,1)}
*JFET resistance
ERjfet 6    0     value = {LIMIT((Wjfet-
+v(1))/(q*Ajfet*Nb*v(4)),0,1)}
*total on-state resistance
ERon D D2 value = {I(VSENSE)*(v(5)+v(6))}

VSENSE D2   D1    0V

 ***** INTRINSIC CAPACITANCE MODEL *****

* gate-drain overlap area [cm^-2]
.param Agd = {0.01}
* source-drain overlap area [cm^-2]
.param Ads = {0.145}
* gate-drain overlap depletion threshold
.param Vtd = 0
* gate-drain overlap oxide capacitance
.param Coxd = 0.112n
* gate-source capacitance
.param Cgs = 0.66n
```

```
* GATE-SOURCE CAPACITANCE
Cgs   G     S      {Cgs}
* gate-drain depletion capacitance
ECgdj       7     0     value = {
+LIMIT(Agd*eps_semi/SQRT(2*eps_semi*(v(D1,G)+Vtd)/q/Nb),
+4p,200p) }
RCgdj       7     0     1E12
* GATE-DRAIN CAPACITANCE
ECgd  10    0     value={ IF(v(G,S)-Vtd>=V(D1,S), Coxd,
+Coxd*v(7)/(Coxd+v(7))) }
GCgd  D1    G     value={ IF(Time>1n,
DDT(v(D1,G))*v(10),0) }
* drain-source junction capacitance
ECdsj       9     0     value = {
+LIMIT(Ads*eps_semi/SQRT(2*eps_semi*(v(D1)+v(2))/q/Nb),6
+0p,1.2n) }
RCdsj       9     0     1E12
* DRAIN-SOURCE CAPACITANCE
GCds D1 S value={IF(Time>1n,limit(v(9)*DDT(v(D1,S)),-
+100,100),0)}
*Cds D1 S 100p

  **** MOSFET CHANNEL MODEL ****

* low current transconductance factor
.param Kfl = {0}
* pinch-off voltage factor
.param Pvf = {0.18}
* gate threshold voltage
EVT   1a    0     value={4.8-0.01*(V(Tj)-300)}
RVT   1a    0     10e12
* high gate bias factor
Etheta      4a    0 value={0.01*PWR(V(Tj)/300,-6.44)}
Rtheta      4a    0     10e12
*saturation transconductance factor
EKp   5a    0     value={5*(1+0.02*(v(G,S)-
v(1a))^2)*PWR(V(Tj)/300,-0.4)}
RKp   5a    0     10e12
*linear transconductance factor
EKf 6a 0 value={0.42}
RKf 6a 0 10e12
Ey 7a 0 value={V(6a)/(V(6a)-Pvf/2)}
Ry 7a 0 10e12

GIMOS       D1    S     value = { (IF(v(D1,S)<=(v(G,S)-
+V(2a))/Pvf,(1.0-Kfl)*V(6a)*V(5a)*((v(G,S)-
+V(2a))*v(D1,S)-1/V(7a)*PWR(Pvf,(V(7a)-
```

```
+1))*PWR(v(D1,S),V(7a))*PWR(v(G,S)-V(2a),(2-+V(7a))))
+ /(1+V(4a)*(v(G,S)-V(2a))),(1.0-Kfl)*V(5a)*PWR(v(G,S)-
+V(2a),2)/2/(1+V(4a)*(v(G,S)-V(2a))))) }

*** BODY DIODE ***

* reverse saturation current
.param is = 146n
* diode ideality factor
.param n = 10.4
* gate-bias factor
.param Kbd = -5
Gbd   S     D1    value = { is*(EXP(v(D1,s)/n/v(2))-
+1)*EXP(v(G,S)/Kbd) }

* LEAKAGE CURRENT MODEL

* thermal generation carrier lifetime
.param tauG = {1p}
* acceptor doping concentration
.param Na = {2e17}
* parasitic BJT current gain
.param beta = {5}
Gleak D1    S     value= {q*A*v(3)
/tauG*SQRT(2*eps_semi/q*(Na+Nb)/(Na*Nb)*v(D,S))}
Gbjt  D1    S     value = {LIMIT(beta*I(Gleak),0,10E9)}

.ends C3M0065100K
```

Co-simulation function: assign model parameters (MATLAB)

```
function [ o ] = param2model( fileName, paramName,
paramVal )
fid = fopen(fileName);
txt = '';
tline = fgetl(fid);
while ischar(tline)
    txt = [txt tline '\n'];
    tline = fgetl(fid);
end
fclose(fid);
txt = strrep(txt,[paramName,'_var'],num2str(paramVal));
fid = fopen(fileName, 'w');
fprintf(fid,txt);
fclose(fid);
o = txt;
end
```

Co-simulation function: executes PSpice *.cir* file (MATLAB)

```
function runPspiceModel( pspiceCmd, fileName )
    cmd = [pspiceCmd,' "',(fileName),'"'];
    system(cmd);

end
```

Co-simulation function: reads PSpice *.out* file (MATLAB)

```
function [ simout ] = readOutFile( fileName )
fid = fopen(fileName);
simout = [];
tline = fgetl(fid);
while ischar(tline)
    tline = fgetl(fid);
    try
        testNumber = ['[',tline,']'];
        x = eval(testNumber);
        if(~isempty(x))
        simout = [simout; x];
        end
    catch e
        ;
    end
end
fclose(fid);
end
```

Co-simulation function: calculates power losses from PSpice model (MATLAB)

```
function [ Esw,Pcond ] = MOSFET_loss( Tj,Vd,Id,Rg )

copyfile('C3M0065100K.cir','C3M0065100K_temp.cir');

param2model('C3M0065100K.cir','Tj',Tj);
param2model('C3M0065100K.cir','Vd',Vd);
param2model('C3M0065100K.cir','Id',Id);
param2model('C3M0065100K.cir','Rg',Rg);

runPspiceModel('C:\Cadence\SPB_16.6\tools\pspice\psp_cmd
.exe','C3M0065100K.cir');
pause(0.01);

A=readOutFile('C3M0065100K.out');

pause(0.01);
```

```
time=A(:,1);
Id=A(:,2);
Vds=A(:,3);
Pcond=Id(length(Id)/2)*Vds(length(Vds)/2);
Px=Id.*Vds;
Px(Px<=100)=0;
Esw=trapz(time,Px); % [J]

pause(0.01);

delete('C3M0065100K.cir');
movefile('C3M0065100K_temp.cir','C3M0065100K.cir');

end
```

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