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MODULAR UNINTERRUPTIBLE POWER SUPPLY SYSTEM

BY
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MODULAR UNINTERRUPTIBLE POWER SUPPLY SYSTEM

PH. D THESIS

by

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AALBORG UNIVERSITY
DENMARK

Dissertation submitted

.

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CV

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ENGLISH SUMMARY

Online uninterruptible power supply systems (UPS) have been actively growing during the past decades due to the fast development of modern technologies. A great number of advanced electrical loads, e.g. communication facilities, academic laboratory equipment, etc, are constantly emerging in our everyday lives. That is why, power electronics interfaces, which can regulate the power quality and cooperate actively with the main grid, are becoming more and more significant in an online UPS system. However, the exiting product is lack of flexibility. Thus the objective of the project is to study power electronics converters control in a flexible modular online UPS system. Numbers of emerging potentials and challenges will be discussed.

First, different UPS architectures are reviewed and two modularized strategies are proposed by considering the drawbacks and main advantages. Based on the different architectures, variable control methods are discussed, especially the importance of how to parallel different modules in the system. The controls methodologies should follow the UPS product standard IEC 62040-3 in order to consider it into a real application, such as data center, hospital and IT loads integration scenarios. The basic behavior for the parallel modules is presented and it should be taken into account when designing the system.

Based on the basic knowledge of modular system, advanced control architectures and their concepts are discussed and compared in detail. The control mechanism of the modules in the online UPS system is shown and simulation models were conducted in PLECS. On the other hand, other functionalities for a modular online UPS system such as active power filter, and UPQC are also investigated in Chapter 2 with experimental results. In Chapter 3, a mathematical model is proposed for a modular online UPS system, which emulates a real modular system and study its behavior in both steady and dynamic state. Experimental data was acquired to analysis the proposed system behavior together with the mathematic model. Thermal analysis for the modular system was presented in Chapter 4 while Chapter 5 presents the practical issues for an industrial prototype.

It is concluded that power electronics converters are playing a critical role in modular online UPS systems as well as the module parallel technology. Output voltage stability, dynamic performance, power sharing among modules and reliability issues of modules are the most important aspects that should be taken into account while designing the modular system. The proposed control strategies have been simplified, easy to implement and provided a better performance.

DANSK RESUME

Online nødstrømsanlæg (UPS) er aktivt voksende i de seneste årtier på grund af den hurtige udvikling af moderne teknologi. Et stort antal avancerede elektriske belastninger, feks kommunikationsfaciliteter, akademisk laboratorieudstyr, etc, der konstant dukker op i vores hverdag. Det er grunden til, magt elektronik grænseflader, der kan regulere strømmen kvalitet og samarbejder aktivt med de vigtigste nettet, bliver mere og mere markant i en online UPS -system. Men den spændende produkt er mangel på fleksibilitet. Således er formålet med projektet er at studere magt elektronik omformere kontrol på en fleksibel modulopbygget online UPS system. Antallet af nye potentialer og udfordringer vil blive drøftet.

Først forskellige UPS arkitekturer revideret og to modulariserede strategier er foreslået af overvejer ulemperne og vigtigste fordele. Baseret på de forskellige arkitekturer, fremgangsmåder variabel styring diskuteres, især betydningen af , hvordan man parallelle forskellige moduler i systemet. Kontrollerne metoder bør følge UPS produkt standard IEC 62040-3 for at overveje det til en rigtig program, f.eks datacenter, hospital og IT indlæser integration scenarier. Den grundlæggende adfærd for de parallelle moduler præsenteres og det skal tages i betragtning ved udformningen af systemet.

Baseret på den grundlæggende viden om modulsystem, er avancerede kontrol arkitekturer og deres koncepter diskuteret og sammenlignet i detaljer. Mekanismen kontrol af modulerne i online UPS system er vist og simuleringsmodeller blev udført i PLECS. På den anden side er andre funktionaliteter for et modulært online UPS-system såsom aktiv effekt filter, og UPQC også undersøgt i kapitel 2 med eksperimentelle resultater. I kapitel 3, er en matematisk model, der foreslås for et modulopbygget online UPS system, der emulerer en reel modulsystem og studere dens adfærd i både stabil og dynamisk tilstand. Eksperimentel data blev erhvervet til analyse det foreslåede system adfærd sammen med den matematiske model. Termisk analyse for det modulære system blev præsenteret i kapitel 4, mens kapitel 5 præsenterer de praktiske spørgsmål til en industriel prototype.

Det konkluderes, at power elektronik omformere spiller en afgørende rolle i modulære online UPS-systemer samt modulet parallel teknologi. Udgangsspænding stabilitet, dynamisk ydeevne, magtdeling blandt moduler og pålidelighed spørgsmål af moduler er de vigtigste aspekter, der bør tages i betragtning, samtidig med at designe det modulære system. De foreslåede kontrolstrategier er blevet forenklet, let at implementere og givet en bedre ydeevne.

ACKNOWLEDGEMENTS

The Ph. D study was carried out during the period of between December 2013 and September 2016 and was under the supervision of Prof. Josep M. Cuerrero from the Department of Energy Technology in Aalborg University. The famous academic atmosphere is one of the main reasons that I choose to come here. After three years' research experiences and unforgettable life here, I am realizing that modular uninterruptible power supply system (UPS) is received more attention due to the burst development of different kinds of electronic loads. And numbers of technical problems for the modular system is still required to be investigated.

The purpose of this project is to investigate advanced control architectures for a modular UPS system, which can be implemented in real products. It will be a great honor for the author if this thesis can present some helpful hints for both researchers and engineers in this field.

I would like to show grateful thanks to Prof. Josep M. Guerrero for the effective and impressive supervision during my Ph. D study for giving me so many directive instructions, constructive proposals and help during my stay in Barcelona. And I would like to give my sincere acknowledgement to Dr. Juan C. Vasquez. I also want to show my regards to Prof. Min Chen from Zhejiang University for his support and help.

I appreciate the funding support for my research provided by the China Scholarship Council and the Department of Energy Technology. Special thanks to the head of department John K. Pedersen from Aalborg University and Mr. Chenggang Liu, Mr. Yun Zhang from Chinese Embassy of Denmark for their kind support.

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Finally, the sincerest gratitude to my parents for their love, encouragement and support and to Jiangyuan Li for her kind help and support especially during my stay in Barcelona, Spain.

Richard Nixon, American 37th President, ever said,

"Our destiny offers no the cup of despair, but the chalice of opportunity."

After three years Ph. D study here, I have a better understanding what Richard Nixon has said. Never feel despair while being faced with difficulty because it may be the chance to reverse the situation. Great appreciation to all of my friends and wish you all have a happy life in the future.

Chi Zhang

May. 2016, Aalborg

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PART I THESIS REPORT MAIN CONTENT

Part I is the main content for the Ph. D thesis. It is a collection of the published paper. It gives a detailed presentation, explanation of the Ph. D project.

The main content of the thesis report is based on the papers that the author had published in the international journals, conferences and the work in the company.

The relationship between thesis report and published papers, collaborative work in a Spanish UPS company, Salicru S/A is shown in the following table. And the in the main content, the relationship is marked detailed in each chapter.

Chapters	Relevant publications
1	
2	A1, A3, A4, A5, A6, A8
3	A2, A3
4	A7
5	collaborative work in a Spanish UPS company, Salicru S/A
6	

CHAPTER 1. INTRODUCTION

This chapter gives the background, motivation and organization of my Ph. D work. The state-of-art of uninterruptible power supply (UPS) system is illustrated as well as the existing products of modern modular UPS system. Finally, the structure of the thesis is presented given in details.

1.1. STATE OF ART OF UNINTERRUPTIBLE POWER SUPPLY SYSTEMS

The booming development of the modern electronic devices, such as data center, mobile base station, among others, is emerging in human being's everyday life [1]. Normally such kind of loads either is distributed widely across a big area or requires continuous reliable energy supply. As a consequence, UPS system is receiving more and more attention from both vendors and consumers. On the other hand, continuing demand from the downstream refining and petrochemicals, upstream oil & gas, mining industries and investments in automation to raise productivity, flexibility, and address regulatory and safety needs will also drive the demand for the industrial UPS equipment [2]. For the evaluation of UPS products, vendor and product side evaluation share the same importance as shown in Figure 1-1 [3].

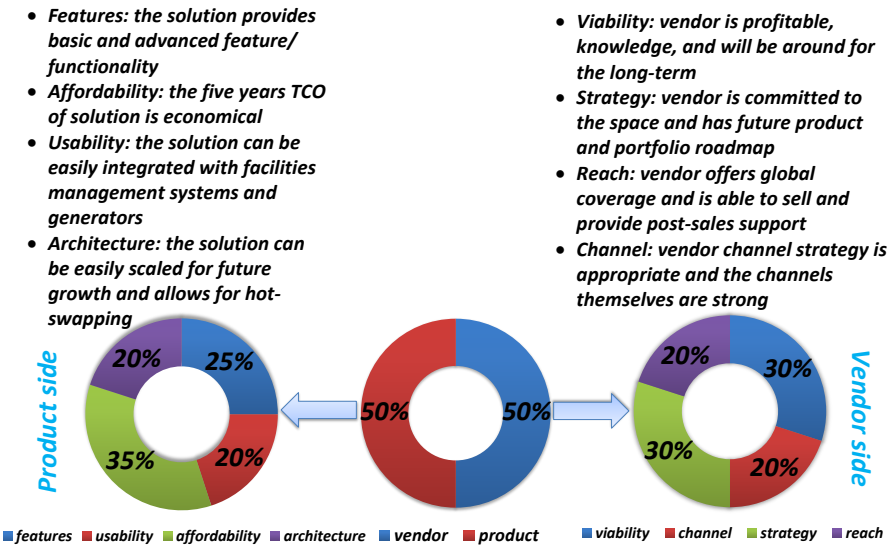


Figure 1-1 UPS products evaluation criteria.

It can be seen that from the point view of product side, affordability is the most important factor that users consider. Then it is the features of the UPS product. Outstanding performance, user friendly interface and excellent reliability are all quite attractive for users. So it means that performance and cost is the most important two elements for a competitive UPS product. On the other hand, from the point view of vendor side, viability and strategy share the same percentage regarding the evaluation of UPS products.

In the market, there are various kinds of manufactures, such as Emerson Network Power, Eaton Powerware, Gamatronic, Schneider, Active Power among others, which provide different kinds of UPS equipment in different power rate. In Figure 1-2, market performance of different UPS vendors is shown [3]. It can be seen that different vendors are against Liebert/Emerson Network Power's product performance to provide a complete relative view of their product offerings.

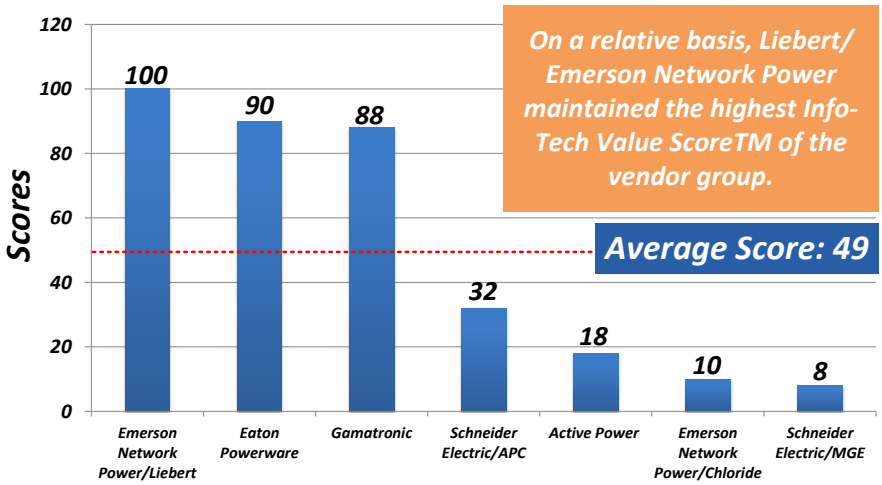


Figure 1-2 UPS product performance score of different vendors.

In addition to the rapid growth and improved performance of different UPS products, the power rate of the UPS products is also increasing actively. Different power rate, namely 0.5-1kVA, 1-5kVA, 5-10kVA, 10-20kVA, 20-100kVA and >100kVA, can be found in the market [4] as shown in Figure 1-3. Recently, power rate tends to increase to several mega-watts since the modern loads are become more and more integrated. For instance, data centers for IT purpose or financial purpose requires a reliable, continuous and a higher power rate supplier. On the other hand, modularization is another trend since it is more flexible and easy to be integrated. Furthermore, modularized system structure also provides a lower difficulty for system repair or maintenance. Modules can be removed or inserted into the power supply system in a safer, more reliable and less difficult way.

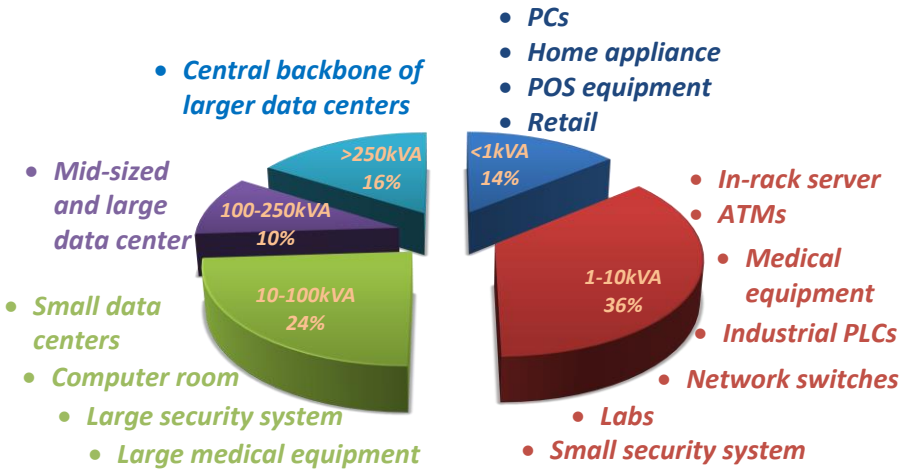


Figure 1-3 Global UPS market and typical applications.

1.2. UPS SYSTEM ARCHITECTURES

1.2.1. THREE TYPES OF CONVENTIONAL UPS SYSTEM ARCHITECTURES

On the basis of the International Electrotechnical Commission Standard 62040-3, three basic categories can be found, namely offline UPS [5], [6], line interactive UPS [7]-[10] and online UPS [11], [12] based on the energy flow direction in different operating conditions. In the following sub-sections, each kind of UPS system architectures will be analyzed.

1.2.1.1 Offline UPS system

Figure 1-4 shows a conventional offline type UPS. Normally, offline UPS module is rated below 2kVA [5]. It is composed of AC/DC, DC/AC, battery pack and static bypass switch (SCR). If the utility is in good condition, energy will flow through the SCR and support the load directly. Nevertheless, SCR will be open and battery pack will be started and transfer energy to load. When battery pack uses up its energy, AC/DC will start to charge the battery and support the load at the same time. It can be seen that offline UPS doesn't provide any isolation between the utility and the loads. As a result, any utility distortion will affect the load directly. This puts a higher requirement on the protection of loads. In some specific application scenarios, passive filter is used to reduce this kind of impact, such as voltage spikes, sags or oscillations [11].

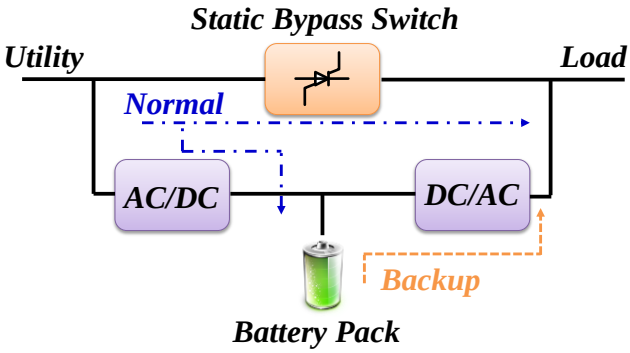


Figure 1-4 Offline UPS system.

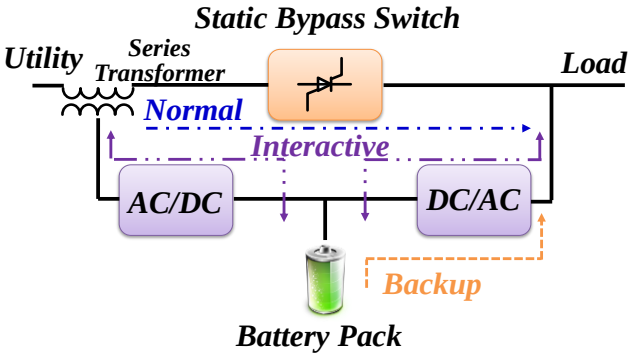


Figure 1-5 Line interactive UPS system.

1.2.1.2 Line interactive UPS system

Figure 1-5 presents a typical line-interactive UPS system. Normally, it operates in medium power rate application. The operating rule is a little bit different than the offline UPS system. The AC/DC, DC/AC and battery pack works together not only as a power supporter but also as a compensation loop. For instance, the AC/DC can suppress the utility voltage distortion through the series transformer [7], [8]. On the other hand, the PFC function can be also achieved [9]. Since the loads are supported by the two energy paths at the same time, thus DC/AC only provide around 10%-20% of the total load power, which means a higher efficiency [10]. However, the control structures for AC/DC and DC/AC are different and complex. Operating modes transient process will happen during the UPS operation. On the other hand, the line series transformer will increase the cost and volume of the UPS system. Nowadays, it is difficult for vendors to accept a higher cost and lower reliability. At the same time, the DC/AC can inject active power into the load to regulate the power factor. Such kind of the equipment is called unified power quality compensator (UPQC).

1.2.1.3 Online UPS system

Online UPS system, also known as inverter preferred UPS or double conversion UPS, is more popular due to its outstanding regulation ability on power quality [11]. It is designed for higher power rate application scenarios. Its good decoupling ability of the utility and the load under power outage is another reason that makes it attractive for consumers [12].

As shown in Figure 1-6, a typical online UPS module is composed of a double conversion stage structure and a static bypass switch. However, the static bypass switch is not the main role of transferring power. The AC/DC, battery and DC/AC will take the role of regulating power. Only in some emergency conditions, the static bypass switch will be activated.

In Figure 1-6, a conventional online UPS system is shown. Under utility normal condition, the utility power is regulated through the two stage converter and injected into the load while AC/DC also acts the charger for the battery pack. Once the utility errors occur, system enters backup mode and battery pack starts to regulate system output power. Furthermore, static bypass will be turned on in event of power conditioner failure [11]. By removing the series transformer, online UPS system is cost-effective and weight-effective.

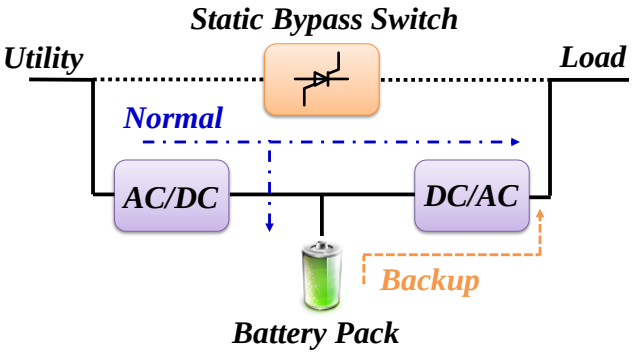


Figure 1-6 Line interactive UPS system.

It can be seen that this structure is more direct on power regulating without any galvanic isolation or transformers. AC/DC is responsible for the harmonic controlling of the utility side while DC/AC modules are regulating the output voltage quality of the system. Normally, the required load power will regulate a two stage system and then transferred to the load. Although it may have a larger amount of losses, its outstanding power regulating capability makes it more attractive. Similarly, it has a lower controllability on the battery power management.

1.2.2. EVOLUTION OF ONLINE UPS SYSTEM ARCHITECTURE

Since the online UPS system is aimed at high power and voltage application scenarios, a series of improved online UPS structure have been proposed in [13]-[22], which are better at regulating active power consumption to achieve unity power factor. Additional DC/DC [13]-[17] and high frequency transformer [18]-[21] are the two main issues that are chosen to achieve a cost-effective, volume-effective and more reliable online UPS system.

1.2.2.1 Half transformer-less online UPS system

In half transformer-less online UPS as shown in Figure 1-7, one additional DC/DC is inserted into the system to improve power quality [13], [14] and the controllability on battery pack in the system. On the other hand, a lower DC bus voltage is achieved, which indicates fewer battery packs in series and higher safety. However, input or output line frequency transformer still decrease system's efficiency and lead to more current stress on converters [15]. On the other hand, the system becomes three stages at least, which means a lower overall efficiency of the whole system. The cascaded converter structure also requires more efforts on the converter design. Converter type load impedance feature is a constant power type, which is a negative resistive type. From the point of control side, such kind of load is easy to trig the instability of the system.

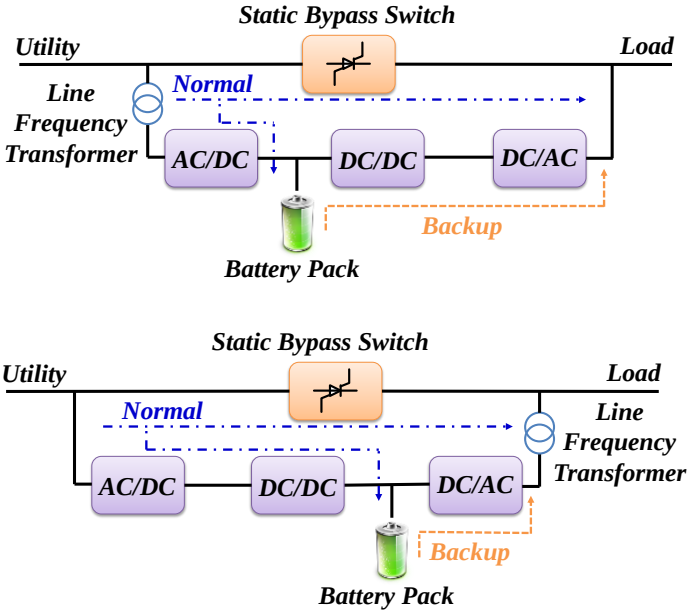


Figure 1-7 Half transformer-less online UPS system.

1.2.2.2 Total transformer-less online UPS system

By adding one more DC/DC, a total transformer-less online UPS system is proposed as shown in Figure 1-8 Nevertheless, there is no galvanic isolation issue in the system. The controllability of the system on the battery pack is enhanced furthermore, which will contribute to a longer life for the battery. At the same time, the control burden on the AC/DC is reduced since the DC/DC will take charge part of the task to regulate power. Moreover, DC bus voltage can be reduced in a large scale meaning that fewer battery units and a higher system safety issue can be achieved. Similarly, the cascaded converter structure requires more efforts on designing and maintaining the overall system stability.

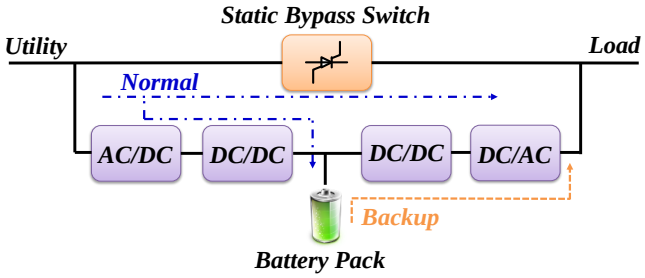


Figure 1-8 Total transformer-less online UPS system.

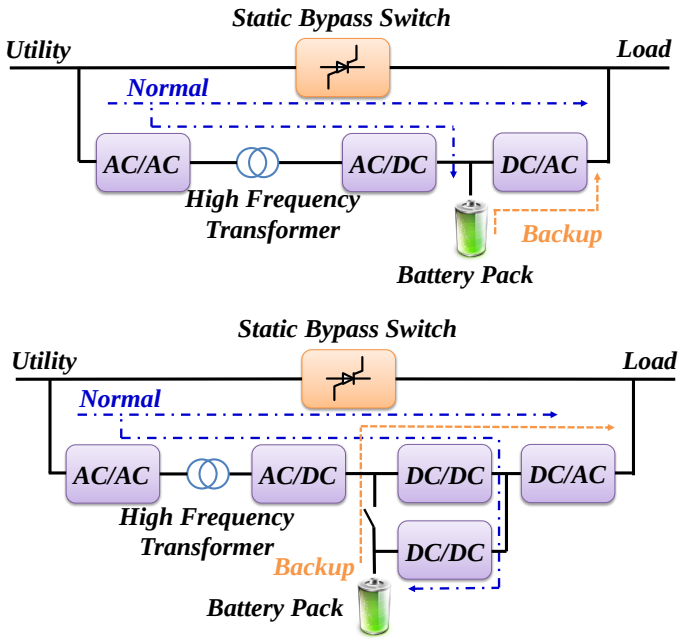


Figure 1-9 High frequency transformer online UPS system.

1.2.2.3 High frequency transformer online UPS system

In [18]-[22], improved online UPS systems with high frequency transformer were presented as shown in Figure 1-9. High frequency transformer guarantees the galvanic isolation between battery, input and output as well as the reduction of volume and weight. Since it is a similar topology as solid state transformer, it can act as a multi-functional interface equipment for AC system and DC system. However, more problems will occur due to the high frequency transformer, such as noise and reliability issues. Specific attention should be paid more attention to the design of such kind of transformers.

1.2.3. POWER ELECTRONIC TOPOLOGIES IN A UPS SYSTEM

1.2.3.1 Topology for DC/AC stage

Figure 1-10 presents three types of the most frequently used DC/AC topologies in UPS system. Three phase half-bridge (3P-HB), as one of the most conventional DC/AC topologies, is shown in Figure 1-10(a). It is easy to design. But the DC voltage utilization efficiency is low, which increase the cost of the DC link capacitor. Due to the manufacture process of DC link electrolytic capacitor, the price will be increased exponential to its volume [23].

Thus three-level neutral-point diode-clamped topology (3L-NPC) is proposed as shown in Figure 1-10(b). Smaller size DC link capacitors are required. However, the midpoint voltage level fluctuation becomes a major concern regarding the converter performance, which must be paid specific attention [24]. On the other hand, the loss distribution in one arm is unbalanced, *ie* T_1 has smaller conduction loss than T_2 while it has higher switch loss than T_2. This may lead to an ineffective utilization of the power semiconductor devices as well as the heat sink for the converter [26]. Also the freewheeling diode D_{npc} is also an important element. SiC devices or outstanding snubner circuit is the possible issues that will be used to solve this problem.

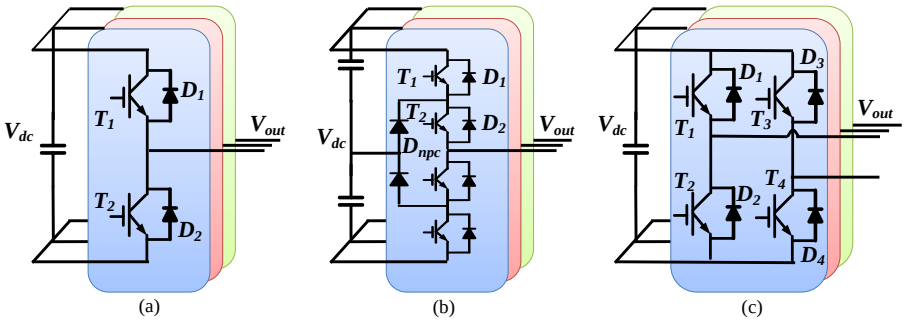


Figure 1-10 Power electronic topologies for DC/AC. (a) 3P-HB (b) 3L-NPC (c) 3P-FB.

The three phase full bridge (3P-FB) shown in Figure 1-10(c) could be another choice for the DC/AC on the online UPS system. Without clamped diodes, it can also achieve three level output [27]. Moreover, 3 phases can work in a flexible and independent way. However, more devices are used and large filter size, losses are major drawbacks. On the other hand, it also provides possible paths for potential zero sequence circulating current to flow [28], [29], which will affect the performance in a negative way.

1.2.3.2 Topology for AC/DC stage

Apart from the topology shown in Figure 1-10(a) and (b), two topologies in Figure 1-11 shown that it could be the suitable selection for AC/DC stage. Vienna rectifier is widely used due to its control simplicity [30]. Nevertheless, it is single direction power flow. In some low power application scenarios, the battery charger is also integrated with the AD/DC stage as shown in Figure 1-12 based on interleaved buck/boost [31]. An auxiliary circuit, which is made up of conventional Buck, is inserted. Thus the AC/DC stage is responsible for not only rectifier but also the battery charge and discharge. This simplifies the control the whole UPS system.

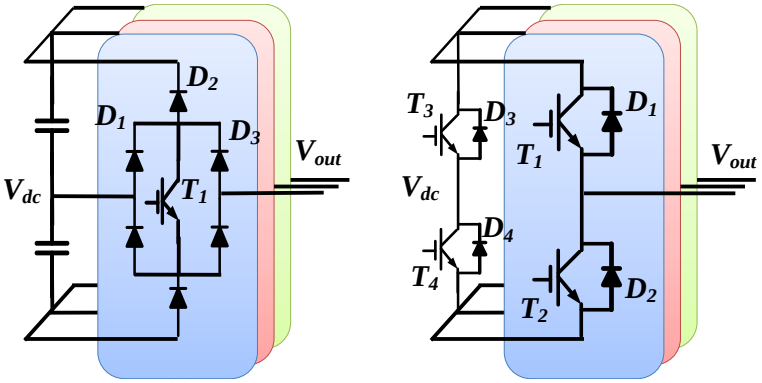


Figure 1-11 Power electronic topologies for AC/DC. (a) Vienna rectifier. (b) 3L-4P-HB.

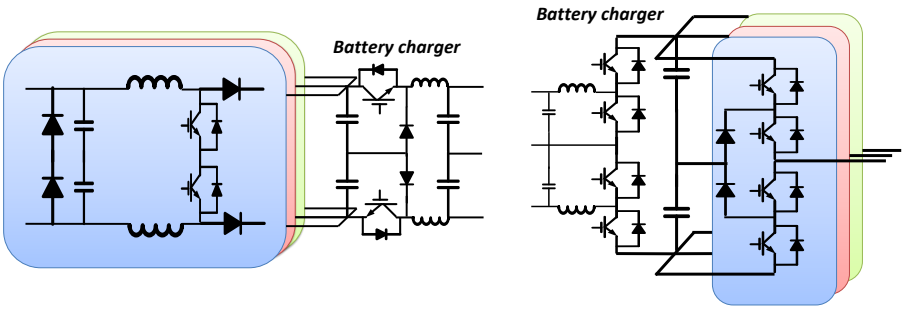


Figure 1-12 AC/DC stage integrated with battery charger.

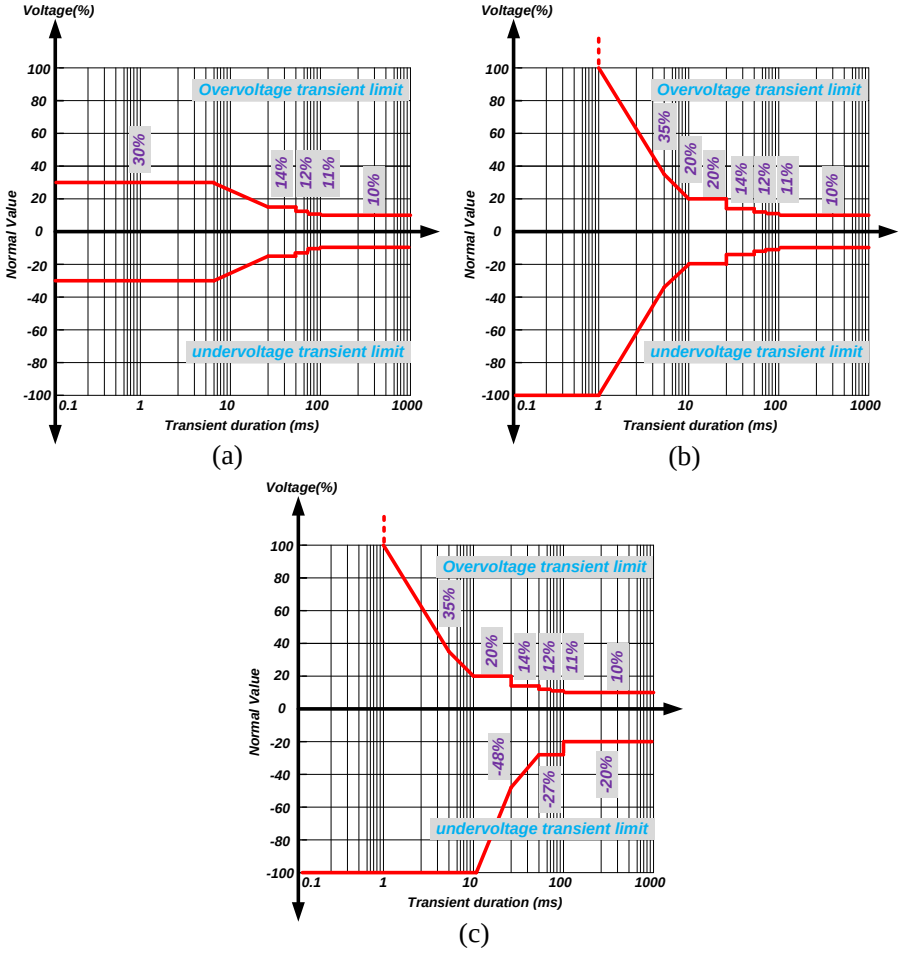


Figure 1-13 Transient duration requirements for online UPS system. (a) Limit for mode change. (b) Limit for linear load change. (c) Limit for nonlinear load change.

1.3. MODULAR ONLINE UPS SYSTEM AND CHALLENGES

The main challenge in the system is the parallel technology for the modules and the modules plug in and out performance of the UPS system. The most popular is the one which is being used as the Master-slave type based on control area network (CAN) bus network. Each module is tightly controlled and synchronized with the support of CAN bus. However, such kind of system depends too much on the communication issues. Once communication fails, the synchronization between modules will be lost and the power is uncontrollable. On the other hand, there is also another important thing that should be considered. It is the Master decision rules in the system. Since there is always only one Master in the system, the system

is required to choose another Master automatically once the Master fails in a fast, smooth way. This will put more challenge on the system supervisor. Apart from UPS output voltage shape quality, the dynamic time while the system is choosing Master is tightly limited and the output voltage overshoot or sags must follow the IEC 62040-3 [32], which is shown in Figure 1-13.

For different operation scenarios, different requirements are presented. Normally Figure 1-13(a) is accepted by sensitive critical load while Figure 1-13(b) is applicable to most types of critical load. And Figure 1-13(c) is accepted by general purpose IT loads. It can be seen that the voltage shoot or sags and the duration time limit are in inverse proportion. No matter what kind of operation the system is doing, if the voltage overshoot or sags can be limit to a small value, for instance 10%, the duration time can be between 10***ms*** and 1000***ms***, which means that a longer dynamic performance can be accepted by different appliances.

For a modular UPS system, another one of the most challengeable operations is the module "*hot-swap*" operation. When the module just starts and plug into the system, it will present as a nonlinear load behavior that will make the output current for the other modules become distorted. And UPS output voltage will be affected and distorted. In case of any module plugging out of the system, the rest modules may suffer from the possibility of overload power or under-voltage sags. Thus the control for the system should have the capability supporting such kind of conditions.

On the other hand, active and reactive power sharing is another critical issue that should be taken into account. Any kind of circulating current of will decrease the system efficiency and harm converter. This is the reason why, both zero-sequence circulating current and power circulating should be considered. A higher accurate power sharing performance should be achieved with the help of simplified control algorithms. Due to the cost limitation, complex control will increase the hardware resource requirement for the digital controller used in the system.

Additionally, the modular UPS system should also have the capability of being immune to failure condition. It means that when some specific control issues in the system fail, the system control could also support the load continuously without losing all the required performance and wait for the orders from supervisor or users. Once everything is back to normal condition, it can be moved back to the right control path.

1.4. SCOPE OF THE THESIS

The objective of this Ph. D project is to investigate advanced control architectures in high power modular online UPS systems, which aims at higher power level. Simplified control methods achieving active and reactive power sharing at any load

condition, mathematical models and also thermal analysis will be investigated in order to evaluate the performance of the whole system. In conjunction with this Ph. D project, a modular online UPS system will be developed.

1.5. OUTLINE OF THE THESIS

The Ph. D thesis is a collection of papers that had been published and is mainly consisting of two parts – the thesis report in Part I and attached paper in Part II. Eight papers are given to support the theoretical analysis in the thesis. The report is made up of six chapters, which is illustrated as follows:

Chapter 1 gives the introduction, motivation and background of the Ph. D project.

Chapter 2 depicts the existing control methods for the modular online UPS system and discusses improved control methods, which are validated through simulation and experimental results.

In Chapter 3, the mathematical model of the system is presented from the perspective of single module and parallel system. On the other hand, by using the experimental data obtained from the experimental setup, the parallel system stability is analyzed together with the proposed small signal mathematical model.

Chapter 4 gives the thermal stress analysis considering the circulating current flowing among the modules. The two conditions – large circulating current and suppressed circulating current, are investigated respectively. The loss and temperature performance of different switches in each leg is also presented.

In Chapter 5, experimental validation in a real product development is presented regarding digital control implementation, hardware design issues, and final prototype tests. The results from the final prototypes are presented.

In Chapter 6, conclusion and future works are presented.

The attached 8 papers are listed as follows:

[A1] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez, C. Seniger, "Modular Plug'n'Play Control Architectures for Three-phase Inverters in UPS Applications," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2405-2414, May-June 2016.

[A2] **Chi Zhang**, E. Coelho, J. Guerrero; J. C. Vasquez, "Modular Online Uninterruptible Power System Plug'n'Play Control and Stability Analysis," *IEEE Trans. Ind. Electron*, vol. 63, no. 6, pp. 3765-3776, June 2016.

[A3] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez and E. A. A. Coelho, "Control Architecture for Parallel-Connected Inverters in Uninterruptible Power Systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5176-5188, July 2016.

[A4] **Chi Zhang**, J. M. Guerrero and J. C. Vasquez, "A simplified control architecture for three-phase inverters in modular UPS application with shunt active power filter embedded," *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on*, Seoul, 2015, pp. 413-420.

[A5] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez, E. A. Coelho and C. Seniger, "High-performance control of paralleled three-phase inverters for residential microgrid architectures based on online uninterruptable power systems," *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, Charlotte, NC, 2015, pp. 3232-3239.

[A6] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez and C. Seniger, "Modular Plug'n'Play control architectures for three-phase inverters in UPS applications," *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on*, Seoul, 2015, pp. 659-666.

[A7] **Chi Zhang**, J. M. Guerrero and J. C. Vasquez, "Thermal impact analysis of circulating current in high power modular online uninterruptible power supplies application," *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Geneva, 2015, pp. 1-10.

[A8] **Chi Zhang**, T. Dragicevic, J. C. Vasquez and J. M. Guerrero, "Resonance damping techniques for grid-connected voltage source converters with LCL filters — A review," *Energy Conference (ENERGYCON), 2014 IEEE International*, Cavtat, 2014, pp. 169-176.

CHAPTER 2. CONTROL STRATEGIES FOR MODULAR ONLINE UPS SYSTEM

In this chapter, several existing control strategies are discussed. Regarding the drawbacks of these conventional control methods, some improved control methods are derived in order to obtain an enhanced system performance.

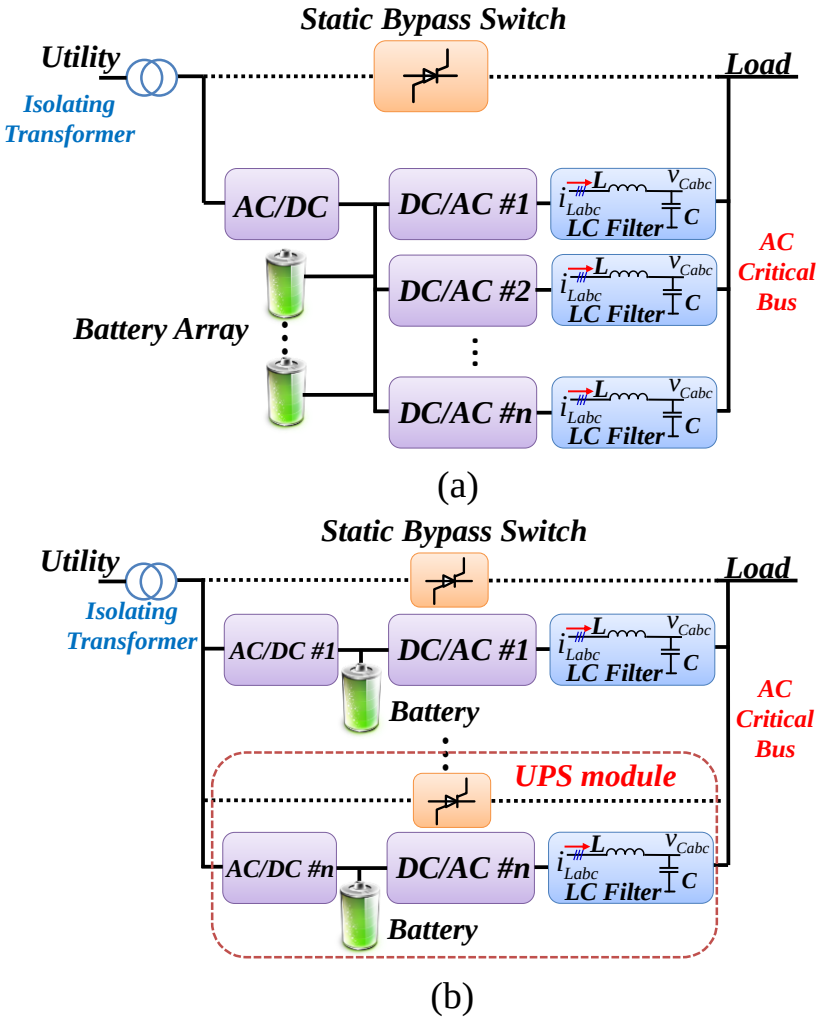


Figure 2-1 Two promising modular UPS structures. (a) Partial modularized. (b) Total modularized.

2.1. TWO PROMISING STRUCTURES FOR ONLINE UPS SYSTEMS

In order to achieve a more flexible and easy-use system, a novel structure is used, which is shown in Figure 2-1. It can be seen that there are two basic modular structures. In Figure 2-1 (a), only the DC/AC side is modularized with one common grid-connected AC/DC. It is more convenient to control such kind of structure because only parallel issue for the DC/AC modules is required to be taken into consideration. However, the power rate for AC/DC modules will be increased and a larger battery pack will be needed to support the whole system. On the other hand, with DC/AC modules plugging in or out of the system, the capacitance on the DC bus bar will be changing all the time, which will give a heavy working burden to the AC/DC. Additionally, since all the DC/AC modules share the same DC and AC bus, it is possible to have zero-sequence circulating current in the system. In Figure 2-1(b), another kind of modular structure is proposed. Hereby, UPS modularized is used to increase the system flexibility. Each module is a small fully functional UPS structure. Thus each module can work totally independent. Nevertheless, this system will have a quite complex and challenge in bypass process. In other words, it can be concluded that no matter what kind of modular structure is used, parallel control technology is essential in the whole system operation. Here the structure in Figure 2-1(a) is further discussed since the other one is being used in a real industrial product.

2.2. CONTROL FOR MODULAR ONLINE UPS SYSTEM

Different from conventional UPS system, modular UPS system adopts several modules to work in parallel instead of using only one DC/AC module. Consequently, how to parallel numbers of DC/AC modules becomes a challenge. Until now, numbers of parallel technologies have been proposed, which can be categorized into three types, namely communication based (CB) [33]-[47], droop based (DB) [48]-[62] and hybrid based (HB) [63]-[74].

CB methods are based on using the communication line between different DC/AC modules. Since CB depends on the communication network performance, reliability issues are receiving more and more challenge. As a result, DB methods are proposed. Parallel DC/AC modules can be simplified represented by a simple model as shown in Figure 2-2. Thus active power and reactive power that each module injects to the load can be determined by the output voltage amplitude and phase. In [60], it mentioned that if the Z_L is inductive, the active power can be regulated by the voltage phase angle or frequency and the reactive power is able to be regulated by the voltage amplitude. Nevertheless, the active power is regulated by the voltage amplitude and reactive power is regulated by the voltage phase angle or frequency if the line impedance is resistive.

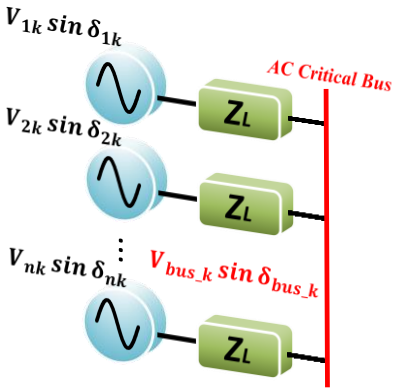


Figure 2-2 Simplified model for DC/AC parallel modules.

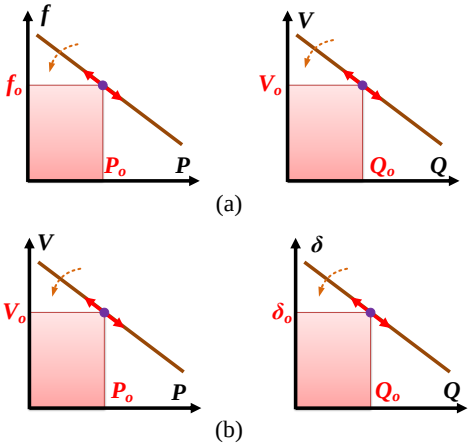


Figure 2-3 (a) Inductive condition. (b) resistive condition.

Thus output voltage amplitude, phase angle or frequency are always regulated and have deviations with the given reference as shown in Figure 2-3. Consequently, AC critical bus voltage becomes load dependent. With higher load power, the AC critical bus voltage amplitude, phase angle or frequency will be changed to a non-reference value. Since there are standards that propose specific requirements for UPS system output voltage amplitude, phase angle or frequency performance, it should be paid especial attention while designing the system parameters. Thus a higher level controller is required to recover the voltage amplitude, phase angle or frequency [63].

By combing CB with DB, hybrid methods are proposed as a multi-level controller structure. DB methods are employed to guarantee the DC/AC modules working in parallel and sharing the load power in an equal way. Since the DB methods will bring voltage amplitude, frequency or phase deviation to the DC/AC modules, CB are used to recover the output voltage by modifying the voltage references for DC/AC modules and broadcasting these values to each of the modules through the communication network. Normally CAN bus communication network is used since mature DSP technology has provided a time-saving and reliable communication technology for the CAN bus. On the other hand, the communication function can be integrated with the module control in a single DSP chip.

2.3. PROPOSED CONTROLS FOR MODULAR ONLINE SYSTEM

2.3.1. BASIC PARALLEL CONTROL [PUBLICATION A3, A5]

Conventional hybrid based methods are designed based on the fact that the line impedance is designed to be mainly inductive. Thus active power can be regulated by the system frequency and reactive power is controlled by the output voltage amplitude as shown in Figure 2-3(a). However, with such kind of method, the UPS system frequency is fluctuated, which is an undesired condition for an online UPS system because the changeable frequency will have negative impact the online UPS system bypass process. On the other hand, both active power and reactive power are required to be calculated in order to achieve the control. This means that a complex control architecture is mandatory for the system. In order to simply the control, virtual impedance [75]-[80] concept is introduced to replace the real inductive line impedance. Thus DC/AC module output impedance can be designed manually to be mainly inductive.

As a consequence, similar idea is used. Through changing the virtual impedance to be resistive, thus output impedance of DC/AC module can be forced to be designed as resistive. In this condition, the DC/AC module output power can be controlled in a different way, as shown in Figure 2-3(b), *ie* active power is related to the amplitude while the reactive power is concerned by the phase angle for frequency. Considering the fact that a variation in the system frequency is not desired for the bypass process for the online UPS system, phase signal is chosen to regulate the DC/AC module output reactive power. Since the phase angle is obtained from the phase lock loop (PLL), the phase angel is tightly related with the frequency. Thus during the time that control starts to modify the phase angle, the system frequency will be jumped suddenly and move back to nominal value afterwards, which is called *"Q–ϕ"* control.

Based on Figure 2-2, DC/AC module output power can be derived as

$$P_{nk} = \frac{V_{nk}V_{bus\_k}}{R_{vir}}\cos(\delta_{nk} - \delta_{bus\_k}) - \frac{V_{bus\_k}^{\ 2}}{R_{vir}} \tag{2-1}$$

$$Q_{nk} = -\frac{V_{nk}V_{bus\_k}}{R_{vir}}\sin(\delta_{nk} - \delta_{bus\_k}) \tag{2-2}$$

being P_{nk} and Q_{nk} the active and reactive power injected by the module n in phase k, V_{nk} voltage value of the module n in phase k, δ_{nk} module n phase k angle information, V_{bus_k} the critical bus phase k voltage, and δ_{bus_k} the critical bus phase k

phase information. In real application scenarios, the phase angle difference (δ_{nk}-δ_{bus_k}) between DC/AC module and AC critical bus is quite small. So it can be treated as zero. Thus the two equations are rewritten as following,

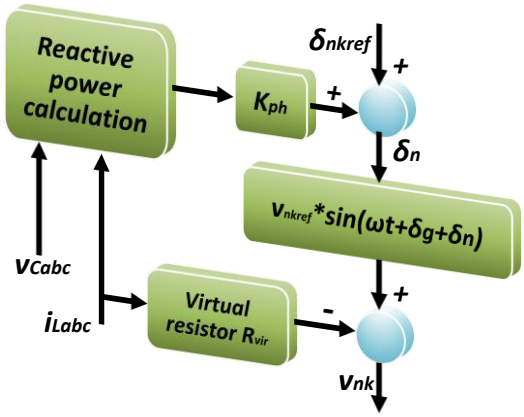


Figure 2-4 Virtual impedance and "Q–ϕ" control diagram.

$$P_{nk} \approx \frac{V_{bus\_k}}{R_{vir}}\left(V_{nk} - V_{bus\_k}\right) \tag{2-3}$$

$$Q_{nk} \approx -\frac{V_{nk}V_{bus\_k}}{R_{vir}}\left(\delta_{nk} - \delta_{bus\_k}\right) \tag{2-4}$$

From the equations above, it can be concluded that the output active power of the DC/AC module can be estimated by the output voltage amplitude while phase angle can be used to regulate the output reactive power of DC/AC modules. By using the virtual impedance (resistive), inductor current will be used to regulate the voltage amplitude. Consequently, the output active power can be controlled. The proposed control architecture is shown in Figure 2-4,

$$V_{nk} = V_{nkref}\sin\left(\omega t + \delta_g + \delta_n\right) - R_{vir}i_{nLabc} \tag{2-5}$$

$$\delta_n = \delta_{nkref} + k_{ph}Q_{nk} \tag{2-6}$$

Here n is DC/AC module sequence number, k is the phase order, V_{nkref} is phase k reference voltage, R_{vir} is virtual resistor value, δ_g is the grid phase information, δ_{nkref} is module n phase k phase reference, k_{ph} is Q–ϕ coefficients, and Q_{nk} is module n phase k reactive power. The inner loop for each DC/AC module use the

conventional double loop structure (voltage and current loop), which uses two typical *PR* controllers due to its capability of suppressing harmonics [81]-[85],

$$G_v(s) = k_{pv} + \frac{k_{rv}s}{s^2 + \omega_o^{\,2}} + \sum_{h=5,7} \frac{k_{hrv}s}{s^2 + (\omega_o h)^2} \tag{2-7}$$

$$G_c(s) = k_{pc} + \frac{k_{rc}s}{s^2 + \omega_o^{\,2}} + \sum_{h=5,7} \frac{k_{hrc}s}{s^2 + (\omega_o h)^2} \tag{2-8}$$

being k_{pv}, k_{rv} the basic voltage loop *PR* controller parameter, ω_o the 2*π*50 rad/s, k_{hrv} the compensation term for h^{th} harmonic, h the harmonic number, k_{pc}, k_{rc} the basic current loop *PR* controller parameter, and k_{hrc} the h^{th} harmonic current compensation value.

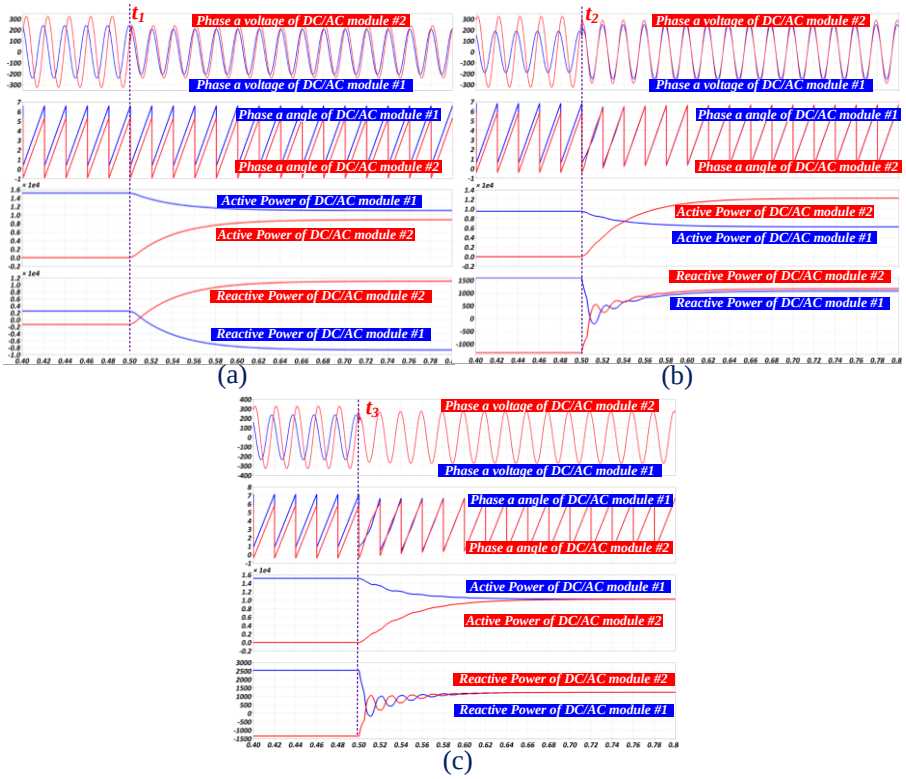


Figure 2-5 Active and reactive power sharing transient process. (a) only virtual impedance (kph=0). (b) only Q–ϕ loops (Rvir=0). (c) using both virtual impedance and Q–ϕ loops.

With the help of the simulation software PLECS, a basic parallel system composed of two DC/AC modules was established to verify the proposed control mechanism. The results are presented in Figure 2-5. In Figure 2-5, the result was obtained by disabling reactive power regulation, *ie* k_{ph} is set to 0. Although the virtual impedance part intends to make two DC/AC modules output active power be convergent to the same value, there are still some static errors due to the initial given phase angle difference. DC/AC module #1 gives higher output active power that DC/AC module #2 and this means that DC/AC module #2 output voltage amplitude is larger than #1 based on (2-5). Then (2-6) is enabled, two modules output voltage amplitude is controlled further until they reach the same value by modifying phase angle, *ie* DC/AC module reactive power. On the other hand, the phase angle difference between two DC/AC modules is moved to the same value, which contributes to reactive power equally sharing as shown in Figure 2-5(c).

Moreover, virtual impedance part is disabled and the Q–ϕ takes the roles of parallel two DC/AC modules. The test result is shown in Figure 2-5(b). The phase angle difference is eliminated to zero, which force two modules output reactive power move to the same value. Nevertheless, due to the output voltage amplitude deviations, the reactive power is not well shared. By applying (2-5), the voltage amplitude is regulated to the same value. And both active power and reactive power are well shared between two DC/AC modules as shown in Figure 2-5(c).

2.3.2. VOLTAGE AMPLITUDE RECOVERING AND PHASE ANGLE SYNCHRONIZATION [PUBLICATION A1-6]

Due to the existence of virtual resistor, AC critical bus voltage amplitude, which is made up of several DC/AC modules output voltage, will have voltage drop compared with reference value. Moreover, reactive power regulation will generate a phase shift on the AC critical bus voltage. Thus voltage amplitude recovery and phase angle reduction and synchronization should be taken into account. There are two kinds of control strategies considered here – Average Type and Simple Type.

2.3.2.1 Average Type [Publication A3, A5]

Average type utilizes the average information of voltage, phase of different DC/AC modules as the feedback information for recovery. Through the CAN bus network, each DC/AC module will broadcast its own voltage amplitude information and phase angle value to the recovery control part.

For the voltage amplitude recovery, when all DC/AC modules output voltage amplitude is received, the averaged value will be calculated,

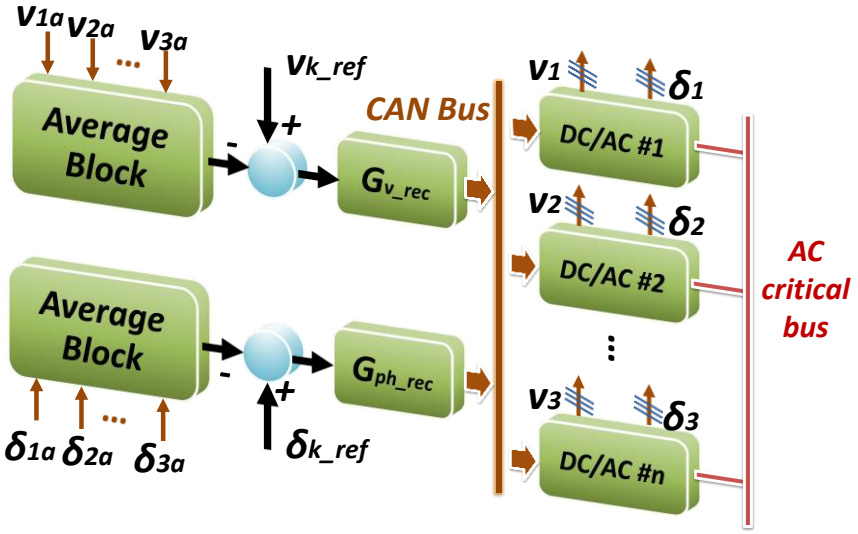


Figure 2-6 Proposed overall control diagram for the paralleled UPS system.

$$V_{a\_avr} = \frac{1}{n}\sum_{i=1}^{n}\left(V_{ia}\right) \tag{2-9}$$

Here V_{ia} is phase *a* RMS voltage amplitude of module #i. Compared with the reference, a compensated value for the voltage amplitude reference is generated by using a *PI* controller each phase respectively as shown in Figure 2-6,

$$\begin{aligned} v_{k\_rec} &= \left(V_{kref\_r} - V_{k\_avr}\right)\cdot G_{v\_rec}(s) \\ &= \left(V_{kref\_r} - V_{k\_avr}\right)\cdot\left(k_{pv\_\sec} + \frac{k_{iv\_\sec}}{s}\right) \end{aligned} \tag{2-10}$$

being v_{k_rec}, V_{kref_r}, V_{k_avr}, k_{pv_sec} and k_{iv_sec} as restoration value of voltage amplitude, RMS voltage reference of phase *k* in central controller, average value of phase *k* RMS voltage value, voltage proportional control parameter and voltage integral control parameter respectively. And this value will be broadcast through CAN bus network to each module.

On the other hand, the phase angle regulation and synchronization will be carried out in a similar way. Hereby the phase angle is required to be tightly synchronized with the utility voltage in case of bypass operation under emergency condition. Thus the phase synchronization reference is the utility voltage angle. This control is

also executed in three phase respectively. Take phase *a* for instance, the averaged phase angle is derived,

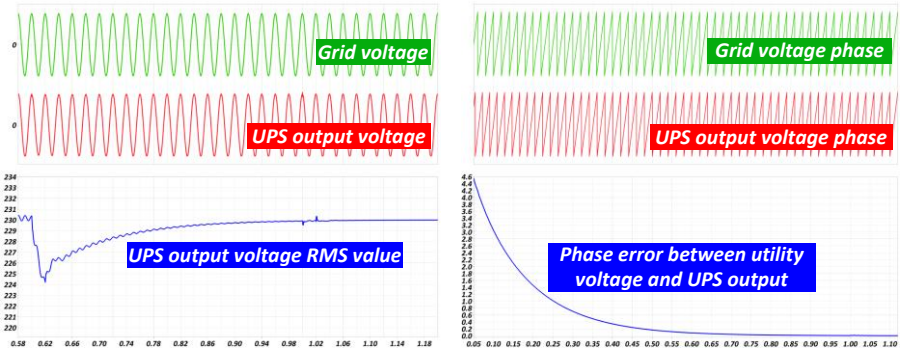
$$\delta_{a\_avr} = \frac{1}{n}\sum_{i=1}^{n}(\delta_{ia}) \tag{2-11}$$

where δ_{ia} is the phase *a* angle of module #i. By comparing it with the utility phase angle, the compensated value for each phase angle reference is calculated through a typical PI controller and sent through the CAN bus network as shown in Figure 2-6,

$$\begin{aligned}\delta_{k\_rec} &= \left(\delta_{kref\_r} - \delta_{k\_avr}\right)\cdot G_{ph\_rec}(s) \\ &= \left(\delta_{kref\_r} - \delta_{k\_avr}\right)\cdot\left(k_{p\theta\_rec} + k_{i\theta\_rec}/s\right)\end{aligned} \tag{2-12}$$

being δ_{k_rec}, δ_{kref_r}, δ_{k_avr} $k_{p\theta\_rec}$ and $k_{i\theta\_sec}$ as phase restoration value of phase *k*, phase reference in central controller (utility phase angle), average value of phase *k* angle, phase synchronization proportional control parameter and phase synchronization integral control parameter respectively.

Simulation results are presented in Figure 2-7, which is obtained from PLECS. Figure 2-7(a) shows the performance of voltage amplitude recovery. A load step is given at 0.6*s*, there will be a voltage sag based on (2-5) as shown in Figure 2-7(a). Due to the voltage recovery control, the RMS value of the UPS output voltage amplitude and RMS value is increased gradually to the nominal value – 230V. Moreover, the phase regulation and synchronization performance is shown in Figure 2-7(b). Through enabling the phase control part, the phase error between grid voltage and UPS AC critical bus voltage will be decreased until it will reach zero.



(a) (b)

Figure 2-7 Phase synchronization performance. (a) Voltage amplitude recovery. (b) Phase synchronization.

2.3.2.2 Simple Type – plug'n'play capability[Publication A1, A2, A6]

According to the aforementioned analysis, Average Type highly depends on the communication network. If one of the modules voltage or phase information is lost, this will be a disaster for the whole system operation. For example, if one of the DC/AC modules suddenly stops working, the averaged value of the voltage amplitude will be changed if the DC/AC module working number *n* is not updated on time. As a consequence, the voltage amplitude reference compensation value will be changed. And the AC critical bus voltage amplitude can't be maintained to the nominal value as shown in Figure 2-8.

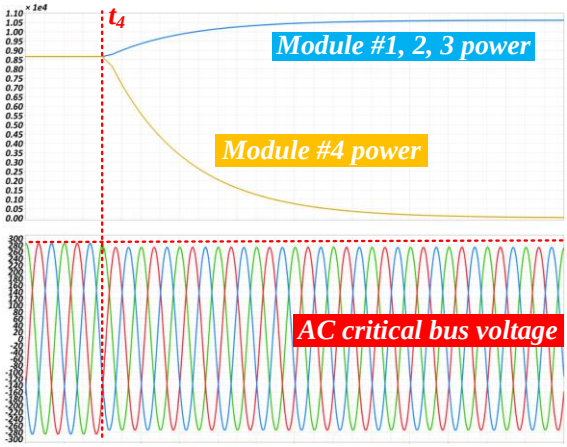


Figure 2-8 AC critical bus voltage when one module plugs out of the system.

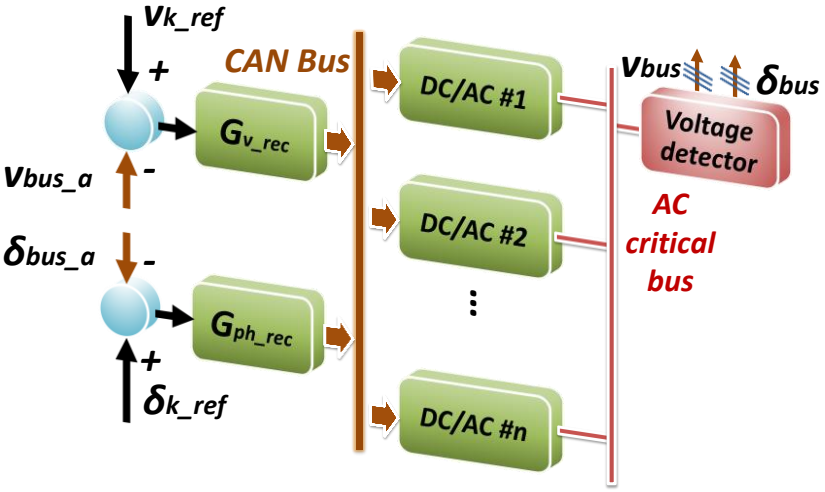


Figure 2-9 Control diagram for online UPS system for plug'n'play capability –Simple Type.

On the other hand, Average Type method also requires that each DC/AC module sends its own phase angle to the recovery control block through CAN bus network. In addition, if the DC/AC modules working numbers *n* can be refreshed on time, the communication network speed will suffer from the heavy work burden. It does not only increase the complexity of single module control code in DSP but also makes the system to highly rely on the CAN bus network. Although modern DSP technology provides small transportation time delay, there is still some possibility that the communication fails. As a result, reliability issues should be taken into consideration. Hence, Average Type cannot allow the system to operate in a "*hot-swap*" way. As a consequence, Simple Type is proposed.

AC critical bus voltage amplitude and phase angle is monitored directly and the information is sent to recovery part. Consequently, the communication task is reduced by a large scale by eliminating the communication channel between DC/AC modules and recovery control part. The control diagram is presented in Figure 2-9. The voltage reference compensation value is derived as follows,

$$\begin{aligned} v_{k\_rec} &= \left(V_{utility\_k} - V_{bus\_k}\right) \cdot G_{v\_rec}(s) \\ &= \left(V_{utility\_k} - V_{bus\_k}\right) \cdot \left(k_{pv\_rec} + \frac{k_{iv\_rec}}{s}\right) \end{aligned} \tag{2-13}$$

$$\begin{aligned} \delta_{k\_rec} &= \left(\delta_{utility\_k} - \delta_{bus\_k}\right) \cdot G_{ph\_rec}(s) \\ &= \left(\delta_{utility\_k} - \delta_{bus\_k}\right) \cdot \left(k_{p\delta\_rec} + \frac{k_{i\delta\_rec}}{s}\right) \end{aligned} \tag{2-14}$$

being v_{k_rec}, k, $V_{utility\_k}$, V_{bus_k}, G_{v_rec}, δ_{k_rec}, $\delta_{utility\_k}$, δ_{abus_k} and G_{ph_rec} as restoration value of voltage amplitude, phase order (*a, b, c*), RMS voltage reference of phase *k* in central controller (utility voltage amplitude), AC bus voltage RMS value of phase *k*, voltage compensation block transfer function, phase restoration value of voltage phase, phase reference in central controller of phase *k* (utility phase angle), AC bus voltage phase angle of phase *k* and phase compensation blocks transfer function respectively. Simulations are done in PLECS and the results are shown in Figure 2-10. At t_5, module #4 is ordered to plug out of the system. The AC critical bus voltage has small dip and then moves back to nominal value.

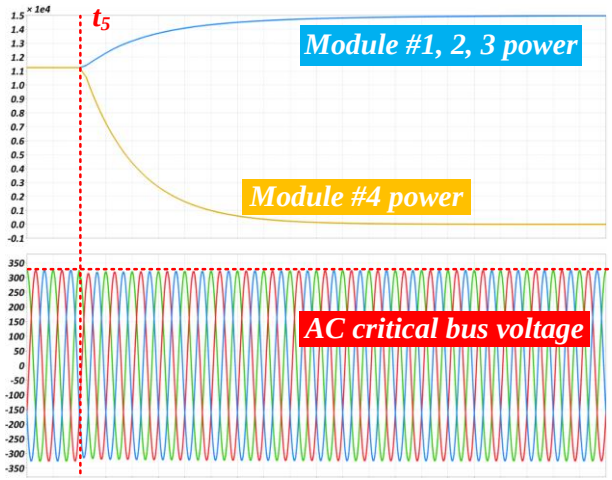


Figure 2-10 AC critical bus voltage when one module plugs out of the system.

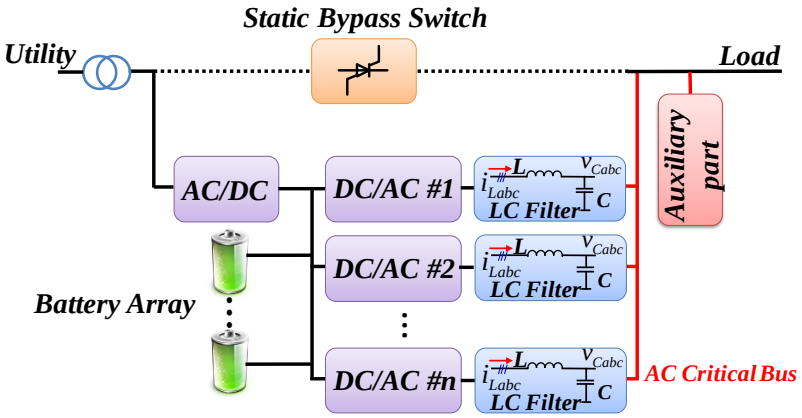


Figure 2-11 Proposed Modular Online UPS Structure with active power filter.

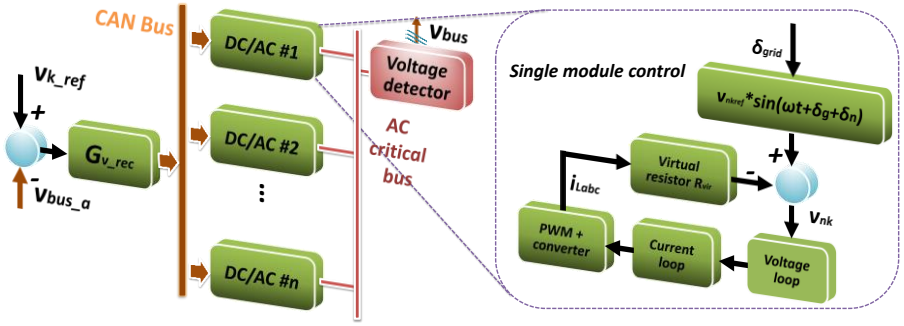


Figure 2-12 Overall control diagram for the UPS part.

2.3.3. SHUNT ACTIVE POWER FILTER [PUBLICATION A4]

Shunt active power filter (SAPF), known as the parallel type active power filter, aims to eliminate the harmonics produced by the nonlinear loads in motor drive application scenarios. It can also inject or absorb reactive power in order to achieve a certain power factor, which is known as UPQC function. Consequently, by inserting it into the UPS system, the reactive power and harmonics can be mainly eliminated by the APF module. Thus the control for single DC/AC modules in the system will be simplified. For parallel operation, only active power sharing is required to be taken into consideration. And for the recovery control part, only voltage amplitude recovery is considered since there is no reactive power that can be seen by the DC/AC modules. The modified control diagram for the parallel modules part is shown in Figure 2-12, in which an auxiliary part is inserted into the system.

For the APF function control, numbers of control methods have been proposed during the past years in [86]-[94]. Basically, it can be divided into two main parts, namely harmonic detection and harmonic current controller. As for the harmonic detection methods, FFT and DQ transformation are two main types that are being used now. Normally, DQ transformation relies on the phase angle and frequency. Since the UPS system phase angle is modified, DQ transformation lacks accuracy in this condition. So FFT is a better choice here. On the other hand, for three-phase independent control, FFT is less complicated than the DQ transformation method. The control diagram for APF is shown in Figure 2-13. Therefore, each phase current harmonics is detected independently and then transferred to *dq* frame.

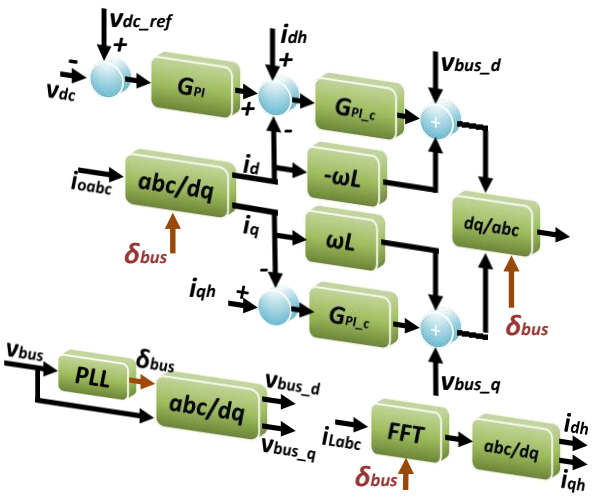


Figure 2-13 Control scheme for the active power filter.

Simulations were carried out in PLECS and the results are shown from Figure 2-14 to Figure 2.15. It can be seen that power is well shared among the modules in each mode. And no matter in bypass mode or normal model, the current THD is kept low, which is smaller than 5% based on the Fourier analysis at t_6, t_8 and t_{10}. Since the load current is controlled as sinusoidal, it means that the load impedance that modules support is mainly resistive. Thus the THD of the AC critical bus voltage is also quite low, as shown in Table 2-1. In the simulation test, the phase angle of the AC critical bus voltage is also synchronized with the utility since there is no reactive power regulation for each module. As a consequence, a smooth transient results can be seen when the system transfers between normal mode and bypass mode as shown in Figure 2-14.

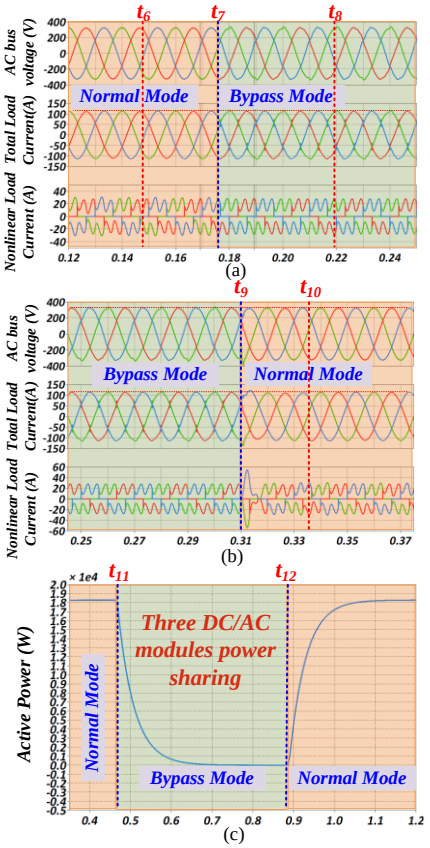


Figure 2-14 Performance under non-ideal utility. (a) Normal to Bypass. (b) Bypass to Normal. (c) active power sharing.

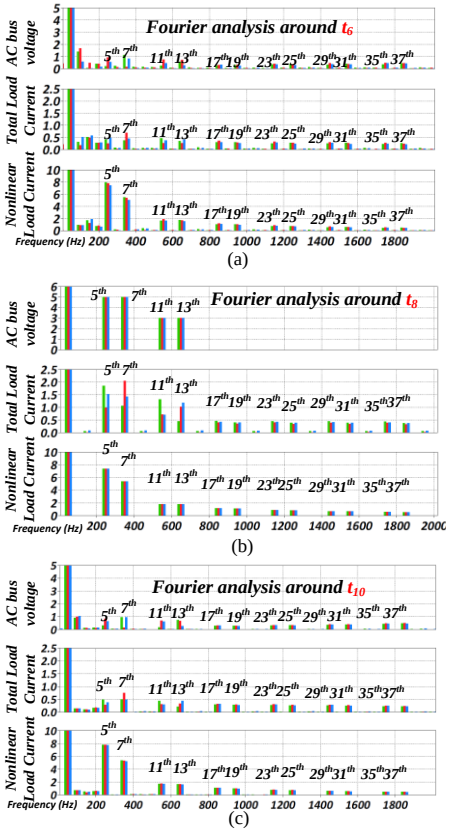


Figure 2-15 FFT Analysis in different modes. (a) details at t_6. (b)details at t_8. (c) details at t_{10}.

Table 2-1. THD Analysis results

	AC bus voltage %			Total load current %			Nonlinear load current %		
phase	a	b	c	a	b	c	a	b	c
Normal	0.7425	0.8793	0.7117	1.4790	1.5451	1.511	49.1109	55.358	46.8117
Bypass	2.5337	2.5337	2.5337	3.0647	2.9601	2.9843	48.8329	48.8258	48.8135
Normal	0.7874	0.7862	0.8151	1.4674	1.4788	1.4179	49.7656	51.8558	48.1405

2.4. EXPERIMENTAL RESULTS AND VALIDATION [PUBLICATION A1-6]

In the standard IEC 62040-3, there are requirements that relates to online UPS system both steady and dynamic performance. In this section, experiments were carried out in the Microgrid Research Laboratories to validate the proposed control methods feasibility.

2.4.1. POWER SHARING AND VOLTAGE TRANSIENT PERFORMANCE [PUBLICATION A3, A5]

At time t_a (around 4s), DC/AC module #3 is ordered to be plug into the system, which is connected to a hybrid load (uncontrolled rectifier and resistive load). It can be seen that the active power is gradually shared among the three modules in Figure 2-16(a). A similar process is taking place for the reactive power in Figure 2-16(b).

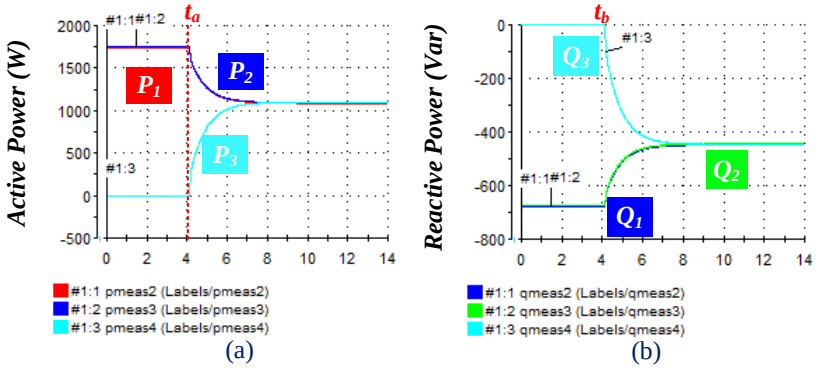


Figure 2-16 DC/AC modules parallel performance. (a) Active power sharing between three modules. (b) Reactive power sharing between three modules.

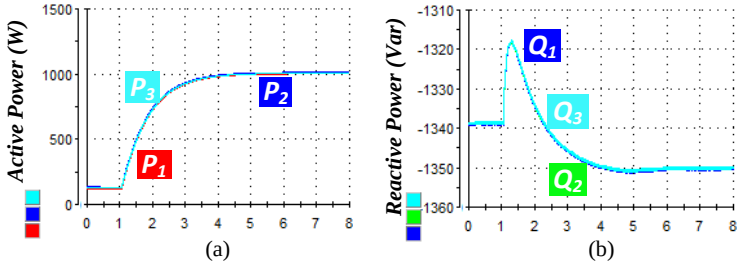


Figure 2-17 Active and reactive power of 3 DC/AC modules. (a) Three DC/AC active power. (b) Three DC/AC reactive power.

In case of a load step of the system (Figure 2-17), it can be observed that both active power and reactive power are well shared among the modules. The low pass filter (LPF), which aims at eliminating power calculation ripple, slows the power dynamic performance.

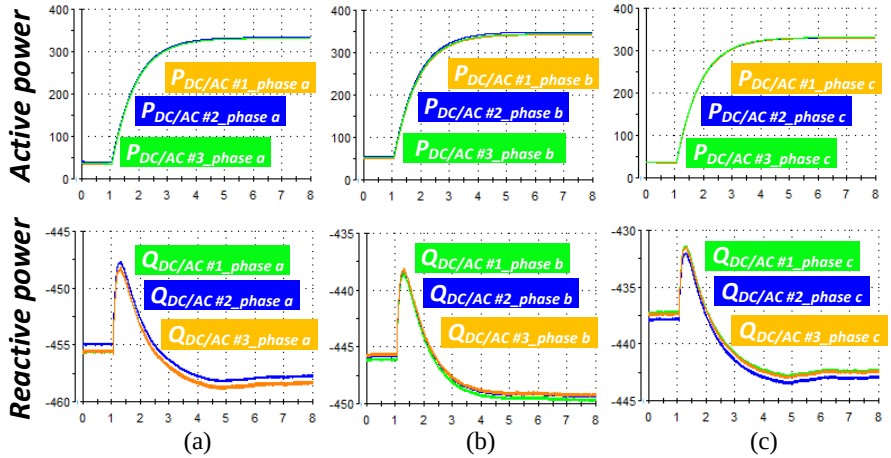


Figure 2-18 Active and reactive power sharing performance per phase. (a) Phase a active and reactive power of three DC/AC. (b) Phase b active and reactive power of three DC/AC. (c) Phase c active and reactive power of three DC/AC.

Since the active power and reactive power is regulated respectively by each phase, it should be also tested the power sharing performance phase by phase respectively and the results are shown in Figure 2-18. Both reactive and active power are well shared in each phase.

On the other hand, the load step brings voltage sags in both module output voltage and AC critical bus voltage. Similar voltage sags occurred due to the load step as shown in Figure 2-19(a)-(c). It can be calculated that the sag is around 8.695%, which is 20V/230V. In Figure 2-19(d), a similar sag for AC critical bus voltage sags can be also observed, which is calculated as 20/230=8.695%.

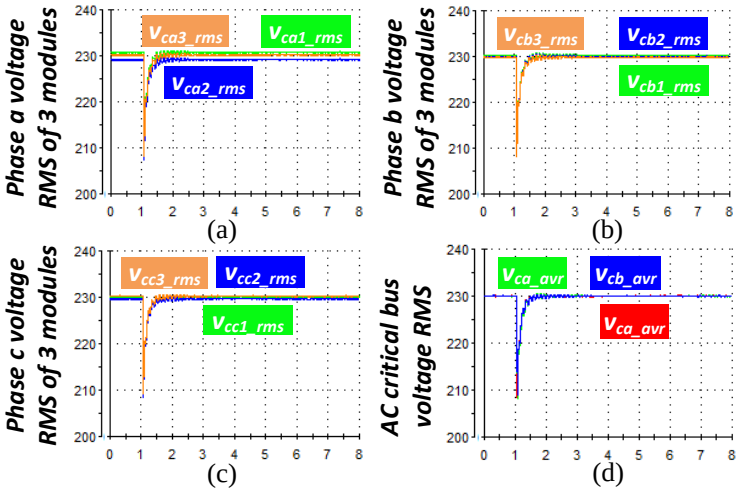


Figure 2-19 RMS voltage (Three DC/ACs and AC critical bus). (a) Phase a voltage RMS. (b) Phase b voltage RMS. (c) Phase c voltage RMS. (d) AC critical bus voltage RMS.

2.4.2. PHASE SYNCHRONIZATION PERFORMANCE [PUBLICATION A3, A5]

Another capability of the system is the phase synchronization with the phase reference, which may be the utility phase angle of each phase or an external source phase angle information, such as diesel generator or other kinds of generator. At around 0.5***s***, the phase synchronization function is enabled and phase errors between module output voltage and main grid is reduced gradually, as shown in Figure 2-20(a). And the errors are controlled around zero finally. However, when the phase synchronization function is enabled, this will bring a voltage spike on the modules output voltage, which is shown in Figure 2-20(b). Since the amplitude recovery function is also active, the output voltage amplitude is tightly regulated. After a few cycles, the output voltage moves back to 230V (RMS). In Figure 2-20(b), the spike is 7.5V/230V (3.26%), which is under 10% of the nominal output voltage amplitude.

For a typical online UPS system, it should have the capability of keeping itself tightly synchronized with utility voltage all the time. This will allow the system to transfer to bypass operation smoothly without bringing any voltage oscillation. Figure 2-21 shows the synchronization performance for the proposed modular online UPS system. Hereby, the line to line voltage (phase *a* to phase *b*) is presented. With the phase error reducing gradually, UPS output voltage and the utility voltage is moving towards together. And during the whole process, it can be seen that the voltage is stable during the whole synchronization process. Once the phase error reaches zero, the error is tightly controlled around zero and two voltages are matched.

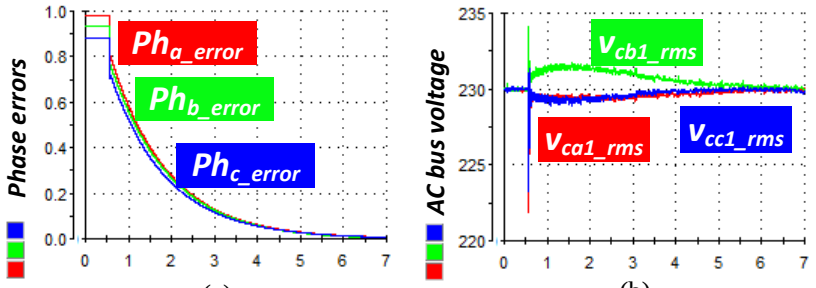


Figure 2-20 Phase synchronization tests. (a) Phase errors of 3 phases. (b) RMS voltage of AC critical bus.

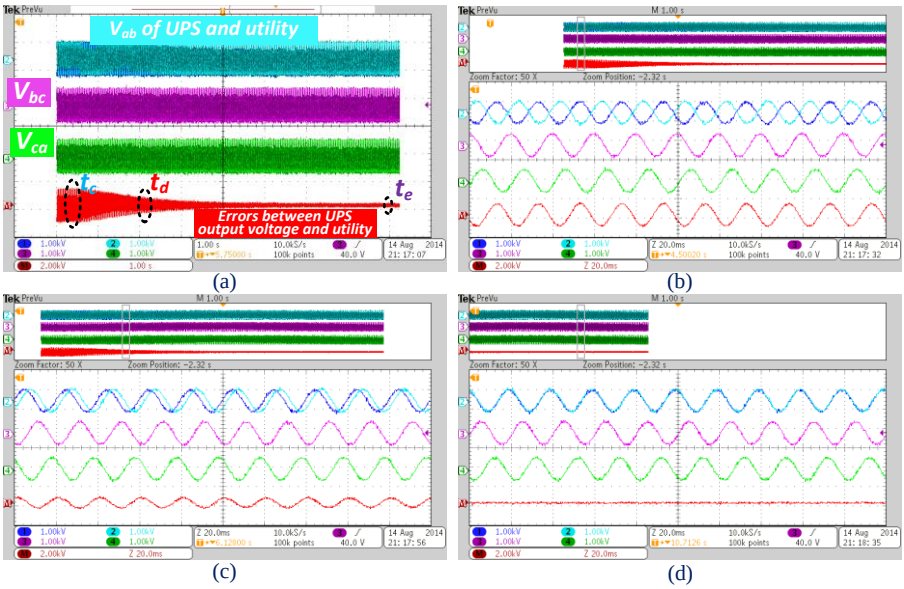


Figure 2-21 Synchronization process between $v_{ab\_utility}$ *and* v_{ab_UPS}*. (a) Overall process. (b) Details at* t_c*. (c) Details at* t_d*. (d) Details at* t_e*.*

2.4.3. LINEAR LOAD PERFORMANCE [PUBLICATION A3, A5]

Linear load condition is the basic load type for an online UPS system. Hereby resistors are used to emulate linear load condition-balanced type and unbalanced type.

First, unbalanced type is tested. Figure 2-22 shows the system performance when one resistor is connected between phase ***a*** and phase ***b*** while phase ***c*** is left unconnected. In this condition, the load is highly unbalanced and the system requires more time to recover the amplitude to the nominal value. It can be seen that

it needs around 5 cycles, *ie* 100***ms***. In the overall process, the voltage shape is kept sinusoidal.

Moreover, more types of unbalanced load are tested in order to verify the control feasibility. An ***L+R*** type load is put between phase ***a*** and phase ***b*** and phase ***c*** is vacant. In the scenario, each phase had to deal with different amount of reactive power, which means that its phase angle is regulated respectively. In Figure 2-23, it can be observed that when the load step was performed at t_f and t_g, each phase reactive power is well shared during the whole process as well as the active power of each module.

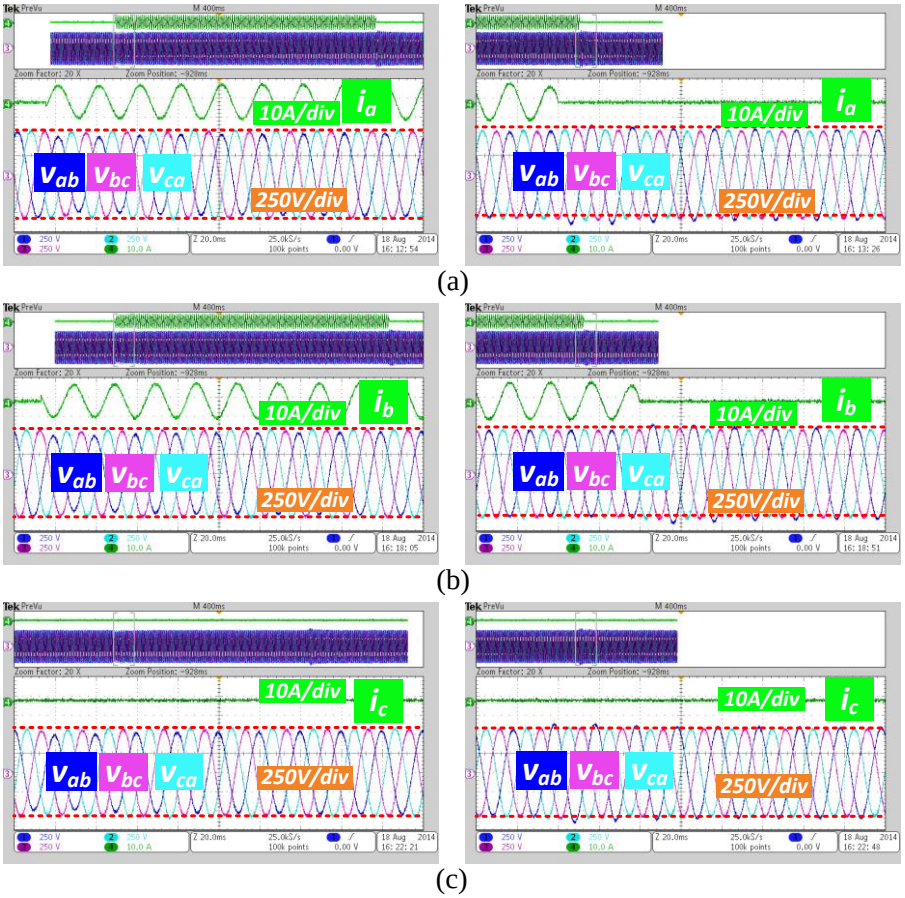


*Figure 2-22 Voltage and current under unbalanced linear load condition. (a) Output voltage and phase **a** current. (b) Output voltage and phase **b** current. (c) Output voltage and phase **c** current.*

The AC critical bus voltage real-time performance at t_f and t_g is presented in Figure 2-24(a) and (b). A quite small voltage overshoot is observed. In case of the load connection, the AC critical bus voltage amplitude needs around 30***ms*** to recover to its nominal value. When the load is disconnected, the transient time is smaller, which is around 20***ms***. In order to test the performance further, a pure ***L*** type load is replaced. In Figure 2-24(c) and (d), the results are presented and it can be concluded that the voltage transient is smooth and faster.

Finally, the simplest type of linear load is balanced type. Three phases are all connected with the same resistor. The performance is shown in Figure 2-25. It can be seen that when the balanced resistive load is connected and disconnected, the voltage transient time is around 40***ms***.

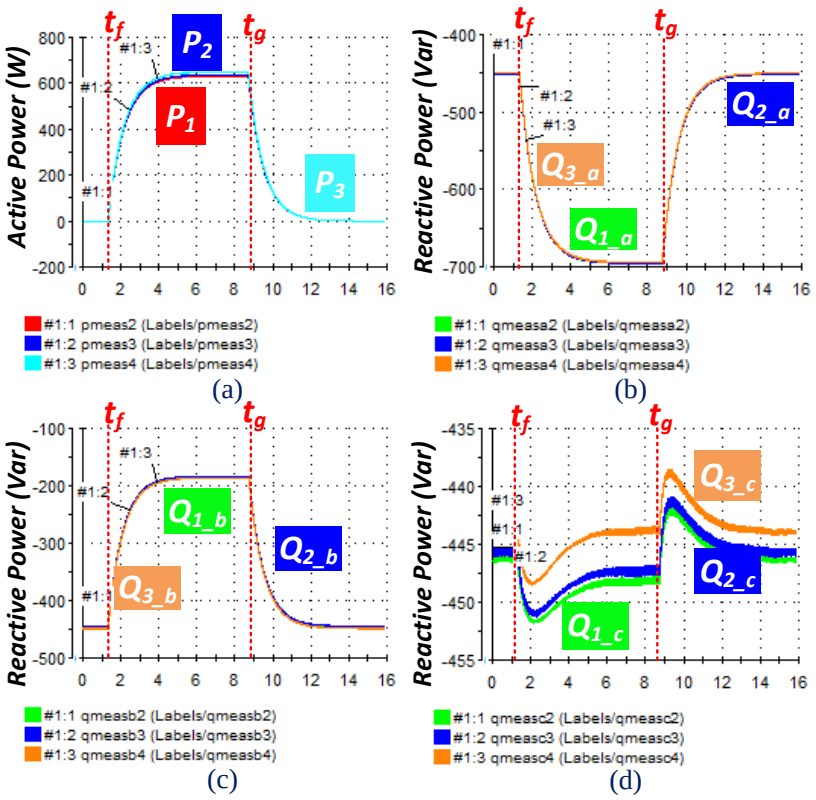


Figure 2-23 Active and reactive power sharing performance under unbalanced nonlinear load condition. (a) Active power. (b)-(d) Reactive power of phase a, b and c.

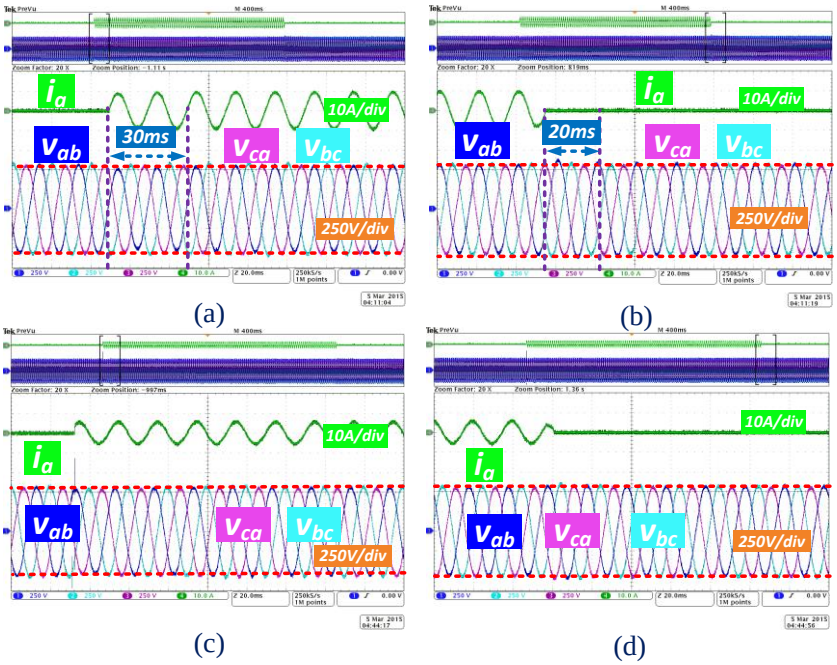


Figure 2-24 Voltage and current under unbalanced load condition. Output voltage and phase a current when load is turned on and off (a)-(b) ***L+R*** *type load. (c)-(d)* ***L*** *type load.*

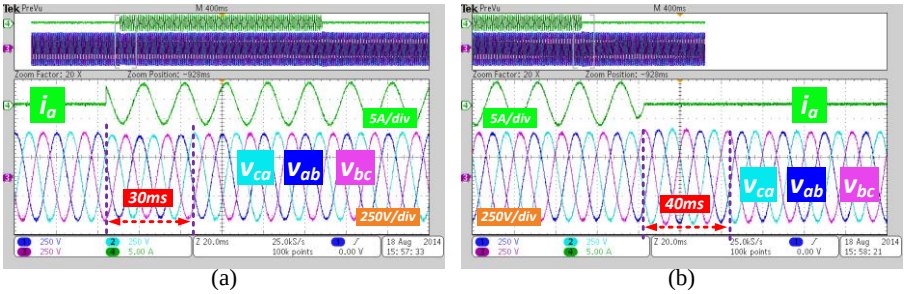
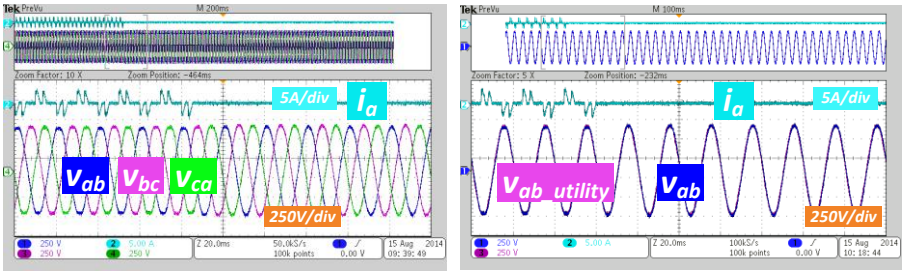


Figure 2-25 UPS line to line voltage (phase a to b) and phase a current. (a) Balanced load connected. (b) Balanced load disconnected.

2.4.4. NONLINEAR LOAD PERFORMANCE [PUBLICATION A1, A3, A5]

The nonlinear load test results are shown in Figure 2-26. With the nonlinear load voltage connecting and disconnecting, the AC critical bus voltage is not highly distorted and it is able to be maintained in sinusoidal waveform. On the other hand, the synchronization performance in such kind of transient test is also presented in Figure 2-26(b). It can be observed that the AC critical bus voltage is tightly synchronized with the grid. And the module output current is shown in Figure 2- 27 and it can be seen that it is well shared.



(a) (b)

Figure 2-26 UPS line to line voltage (phase a to b) and phase a current. (a) Balanced load connected. (b) Balanced load disconnected.

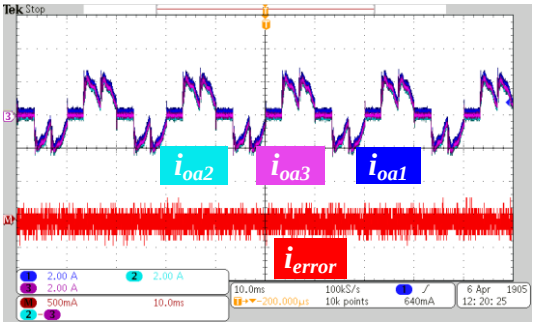


Figure 2-27 Nonlinear load sharing performance.

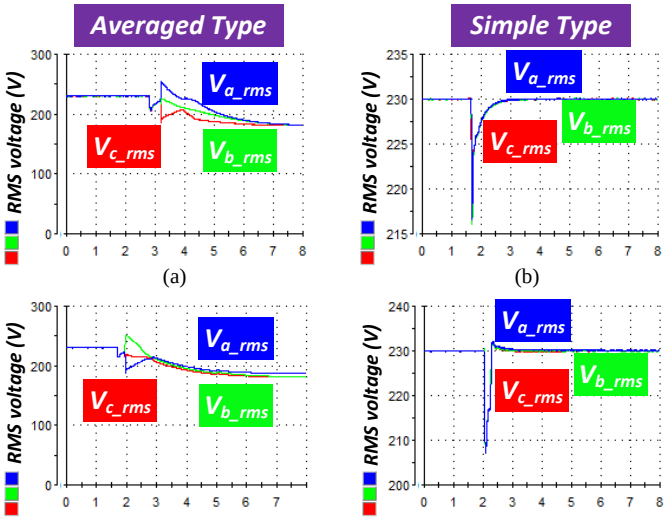


Figure 2-28 AC critical bus voltage performance when one DC/AC stops. (a) Average type under linear load. (b) Simple type under linear load. (c) Average type under nonlinear load. (d) Simple type under nonlinear load.

2.4.5. PLUG'N'PLAY CAPABILITY [PUBLICATION A1, A2, A6]

According to the aforementioned analysis, it is concluded that the Average Type control depends too much on the exact working numbers of the DC/AC modules. When one of the modules starts or stops, the AC critical bus voltage is not able to be maintained to the nominal value (230V) anymore. With the proposed Simple Type control, as shown in Figure 2-9, AC critical bus voltage is directly used to achieve the voltage amplitude recovery and phase synchronization control. The test results comparison is shown in Figure 2-28. It can be observed that AC critical bus voltage is maintained at the nominal value for both linear load and nonlinear load condition with Simple Type control.

The power performance of the system is shown in Figure 2-29. At t_h, one module is ordered to stop working. It can be seen that both reactive power and active power are equally distributed among remaining modules during the whole performance. Similarly, when one module is ordered to plug into the system at t_i, the power is well shared.

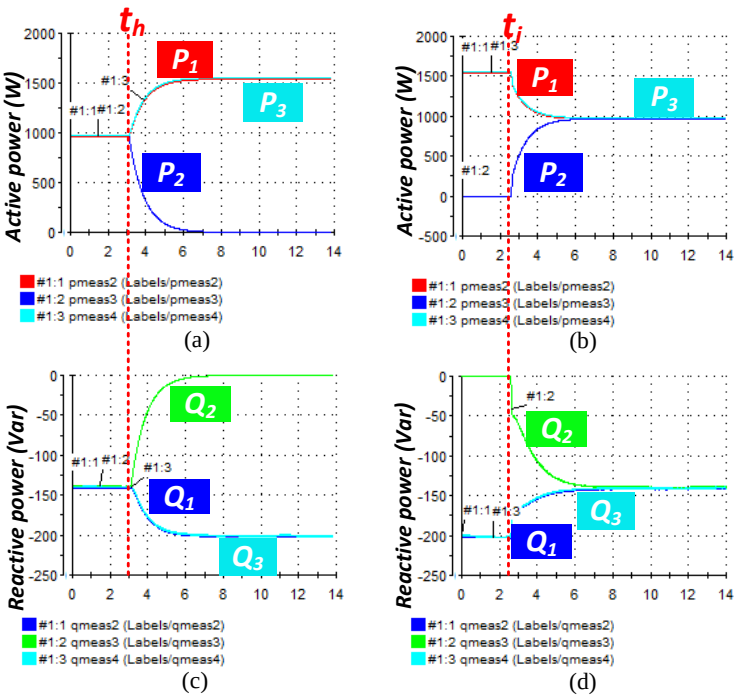
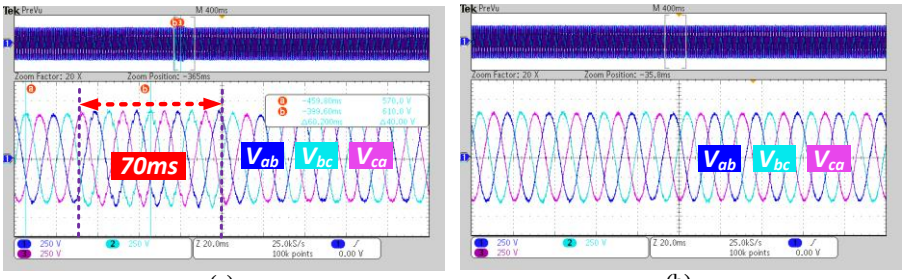


Figure 2-29 Power performance when modules are plugging in and out. (a) active power when module plugs out. (b) active power when module plugs in. (c) reactive power when module plugs out. (d) reactive power when module plugs in.

At the same time, the real time voltage performance of the AC critical bus is shown in Figure 2-30. In Figure 2-30(a), it can be observed that when the module plugs into the system, there is voltage overshoot in the AC critical bus. The overshoot amplitude is calculated as 7.01% (40V/570V), which is below 10% of the nominal value. According to the IEC62040-3, the transient duration time requirement is between 100***ms*** and 1000***ms*** shown in Figure 1-13. In Figure 2-30(a), it can be seen that the transient time duration is around 70***ms***. It means that the dynamic performance meets the standard requirement. Figure 2-30(b) shows the voltage performance when one module plugs out the system. There is no obvious voltage fluctuation in the transient performance.

The synchronization capability with the utility is presented in Figure 2-31. Figure 2-31(a) shows the whole process. No obvious voltage fluctuation can be seen. And the details of different time are shown in Figure 2-31(b) to (d). The voltage error between the utility and output voltage of the UPS system is reduced gradually until it reaches zero. Than the error is kept controlling around 0 and synchronized with the utility.



(a) (b)

Figure 2-30 Real-time voltage performance of AC critical bus. (a) module plugs in. (b) module plugs out.

2.4.6. ACTIVE POWER FILTER AND UPQC FUNCTION [PUBLICATION A4]

The active power filter harmonic mitigation capability is shown in Figure 2-32. With the typical nonlinear load (uncontrolled rectifier) as shown in Figure 2-32(a), both DC/AC module #1 and #2 output voltage will become distorted. Than the APF is ordered to start to compensate the load harmonic current, it can be seen that the output voltage of both DC/AC modules become more sinusoidal, which means that the APF has eliminated nearly all the harmonics. The APF module performance is presented in Figure 2-33. It can be seen that the output current controller of APF can track the reference in a precise way but has some static errors due to the *PI* controller used in the control loop. And the power sharing performance for the DC/AC modules is shown in Figure 2-34. It can be observed that the active power is well shared with the virtual impedance loop. In Figure 2-34(a) both modules reactive power is around 1360Var.

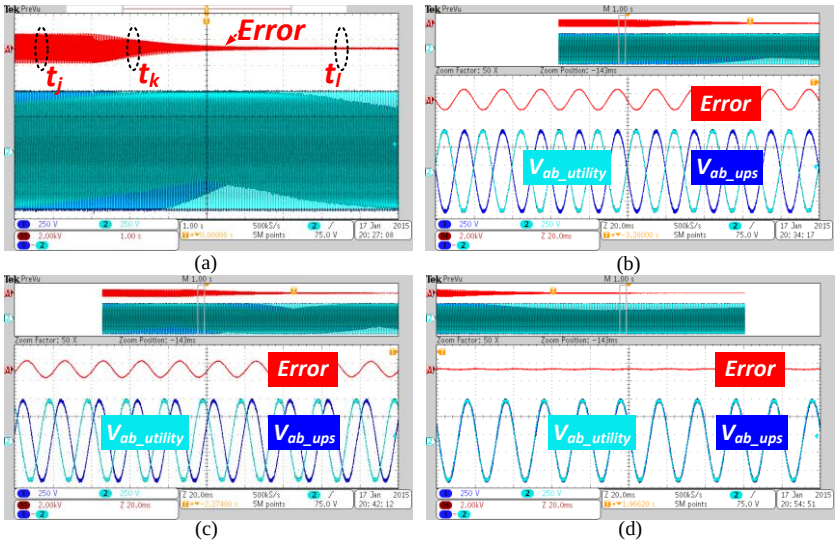


Figure 2-31 Synchronization performance. (a) overall process. (b) details at t_j. (c) details at t_k. (c) details at t_l.

Reactive power generated by filter capacitance should be considered here because inductor current is used to calculate reactive power. It can be derived as $3*230^2*2*\pi*50*27e^{-6}$ and it is equal to 1346Var. Thus It can be said that a small amount of reactive power, about 15Var, is still circulating in the system due to APF function control static errors.

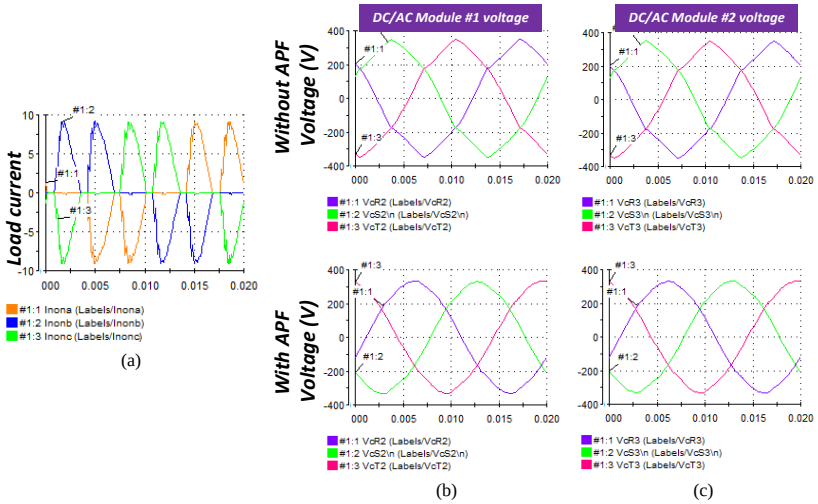


Figure 2-32 Active power filter performance. (a) load current. (b) DC/AC module #1 output voltage with and without APF. (c) DC/AC module #2 output voltage with and without APF.

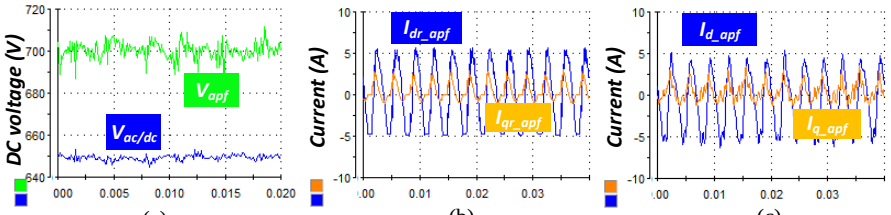


Figure 2-33 APF module performance. (a) DC capacitor voltage. (b) current reference in dq frame. (c) output current in dq frame.

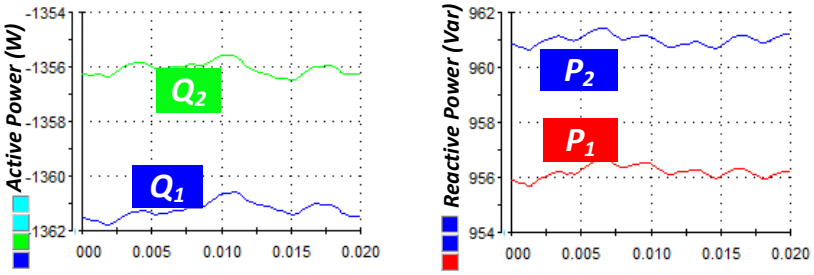
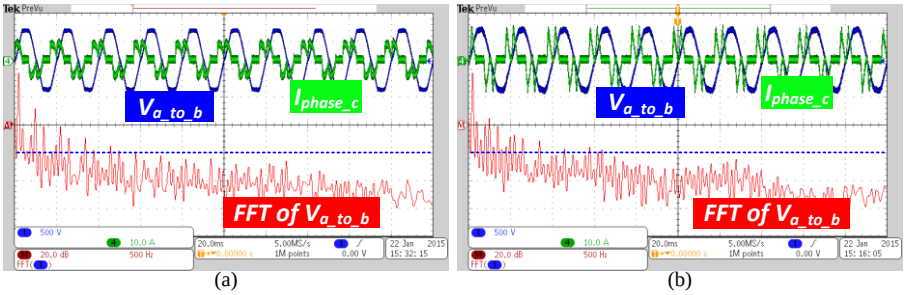


Figure 2-34 Power sharing performance among the DC/AC modules. (a) reactive power. (b) active power.

Since the real time performance for the APF is also critical for real application, the real time voltage performance is also presented. In Figure 2-35(a), it can be seen that the voltage is distorted while the APF is disabled. Once the APF is enabled, the voltage shape of the AC critical bus is becoming more sinusoidal as shown in Figure 2-35(b). With the FFT of the AC critical bus voltage, it is also able to be concluded that the voltage is more sinusoidal with higher distorted load current.

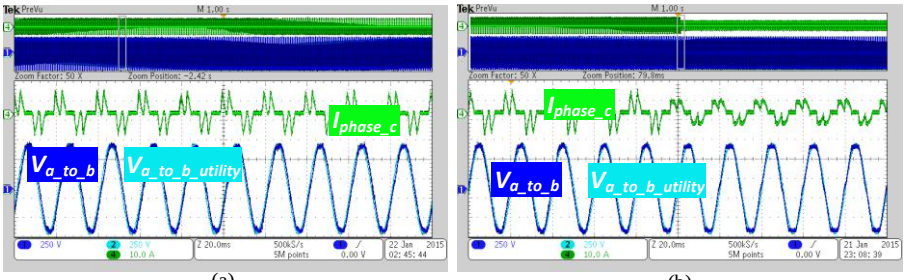
Moreover, the synchronization capability is required to be tested again since one more module is introduced to the system. Figure 2-36(a) shows the performance while the APF module is always enabling. It can be concluded that the voltage is tightly synchronized with the utility since the phase reference for UPS modules is given the same as the utility phase angle. Moreover, there is no phase angle regulation. In Figure 2-36(b), the APF module is disabled. During the whole process, the output voltage of the UPS system is synchronized with the utility voltage.

In order to achieve the UPQC function, the APF control is modified by adding an extra reactive power control block. Thus the q axis current reference is changed, which is shown in Figure 2-37. And the experimental results are presented in Figure 2-38. Since the ControlDesk had displayed too many variables and it made the PC start to be slow. Experimental data was recorded and analysis in Matlab.



(a) (b)

Figure 2-35 AC critical bus voltage performance. (a) without APF. (b) with APF.



(a) (b)

Figure 2-36 Synchronization performance with the utility. (a) with APF enabled. (b) transient performance while enabling and disabling the APF.

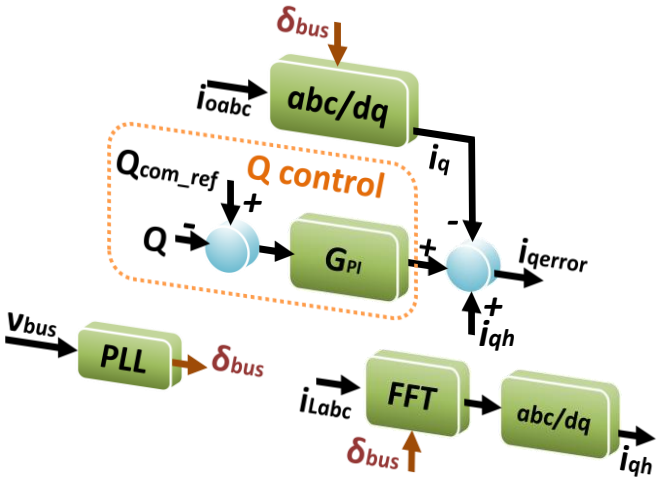


Figure 2-37 UPQC control modification in q axis.

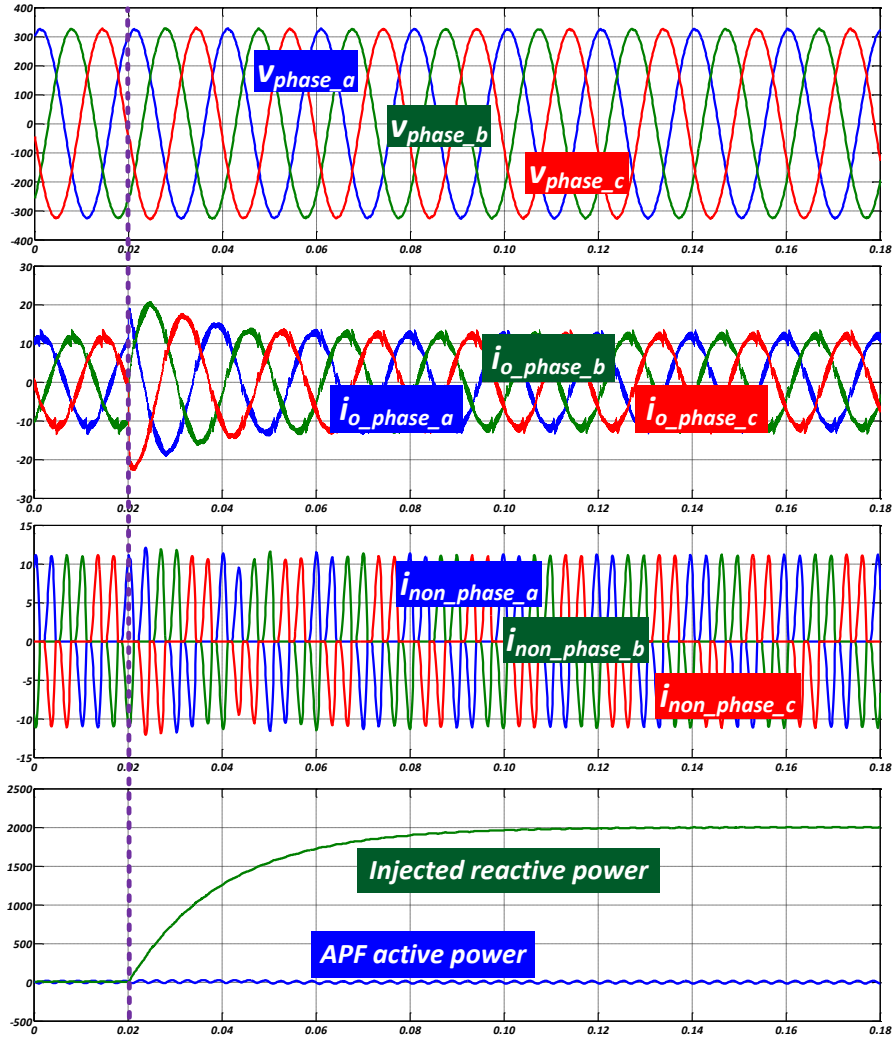
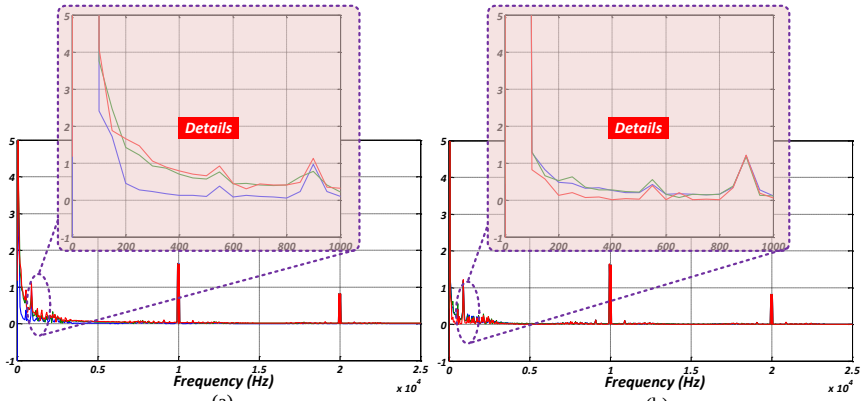


Figure 2-38 UPQC voltage and current performance.

At 0.02***s***, the APF module is ordered to inject 2000Var reactive power into the load as shown in Figure 2-38. It can be seen that the UPS output current $i_{o\_phase\_a,\ b\ or\ c}$ has some overshoot and start to have phase shift due to the reactive power injection. Through the FFT results analysis before 0.02***s*** and after 0.02***s*** (Figure 2-39), it can be seen that such reactive power injection didn't affect the AC critical bus voltage quality. A similar FFT results was obtained as shown in Figure 2-39. In Table 2-2, the detailed THD value of the AC critical bus voltage and output current is presented. It can be concluded that the voltage THD was decreased a little bit due to

the reactive power injection while the current THD almost kept around the same value.



(a) (b)

*Figure 2-39 FFT performance of AC critical bus voltage. (a) before 0.02**s**. (b)after 0.02**s**.*

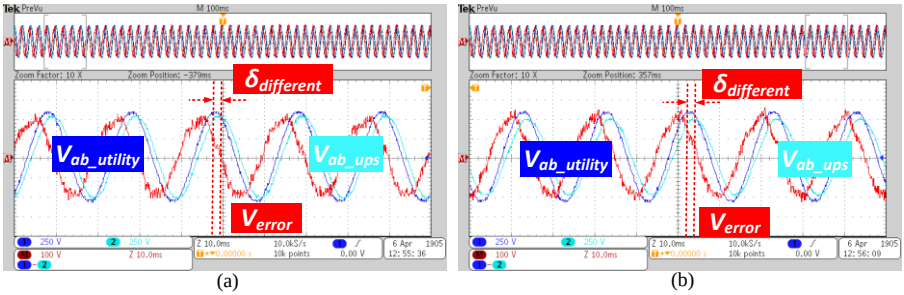
Table 2-2. AC critical bus voltage and UPS output current THD.

	AC critical bus voltage			**UPS output current**		
phase	a	b	c	a	b	c
<0.02s	0.0182152	0.0184915	0.0128386	0.0784401	0.0785025	0.0801257
>0.02s	0.0117029	0.0117312	0.0107105	0.0746191	0.0750722	0.0753867

2.4.7. COMMUNICATION FAILURE TEST [PUBLICATION A1]

Since the voltage recover and phase synchronization are implemented based the communication network (CAN bus), there is possibility that the communication bus fails to transfer require information in a proper way. Thus communication failure condition should be taken into account and carefully tested. By removing the communication lines directly, the CAN bus network for DC/AC modules is broken. In order to present a clear comparison results, the parameter R_{vir} and k_{ph} have been set to a big value in order to obtain an obvious comparison. And the results are shown in Figure 2-40. Since there is no voltage amplitude recovery and phase regulation control, the voltage amplitude deviations and phase shift is able to be seen clearly. In Figure 2-40(a), two DC/AC modules are tested, and UPS output voltage has a phase difference $\delta_{different}$ and amplitude drop compared with the utility

voltage. Furthermore, another one was started. Thus it can be seen that the difference becomes more obvious. This means that in case of failure, the system can can't perform a normal bypass behavior. It should keep working until the failure disappears. Considering real application scenarios, R_{vir} and k_{ph} can be optimized to minimize the observed difference in order to reduce the negative impact on the electronic load as much as possible.



(a) (b)

Figure 2-40 Performance in case of communication failure. (a) Two modules in parallel. (b) Three modules in parallel.

2.5. CONCLUSION

In this chapter, the proposed control for a modular online UPS system is presented. Detailed control diagram and equations are given. Combining with the simulation results, the control mechanics for different purposed are illustrated. Experimental results validation is also shown in this chapter. Based on the IEC 62040-3, the proposed control presents a fast and stable dynamic performance. At the same time, with a simplified parallel control for the modules, the power is well shared among all the DC/AC modules.

CHAPTER 3. MATHEMATICAL MODEL AND SYSTEM ANALYSIS

Since the system is composed of several modules and two-layer control architecures, there are a numbers of parameters that are required to be analyzed-single module parameters and system level control parameters. In this chaper, mathematical model for the single module and overall system was developed in order to analyze the parameters impact on system performance. Additionally, a small single model was also derived in detail in order to analysis the modular system in therory. Experimental results are obtained in order to validate the model feasiblity.

3.1. MATHEMATICAL MODEL IN SINGLE MODULE PERSPECTIVE [PUBLICATION A3, A5]

Inner loop that each DC/AC module uses is quite critical since it is the basis of a modular UPS system. Hereby, it is modelled in a conventional mathematical way. Since the control is considered in $\alpha\beta$ frame, the transfer function in s domain is derived as follows,

$$G(s) = \frac{Z_{Load} G_v(s) G_c(s) G_{PWM}}{L Z_{Load} C s^2 + as + b} \tag{3-1}$$

where the control delay is given as,

$$G_{PWM}(s) = \left(1/1.5T_s s + 1\right) \tag{3-2}$$

and

$$a = L + G_c(s) G_{PWM} Z_{Load} C$$
$$b = Z_{Load} + G_c(s) G_{PWM} + G_v(s) G_c(s) G_{PWM} Z_{Load}$$

The bode diagram of the inner loop control is given in Figure 3-1. It can be seen that a bandwidth, about 1.52kHz, is achieved since the switch frequency for the converter in the lab is 10kHz. For a typical *PR* controller, a band-pass filter behavior is mandatory as shown in Figure 3-1. In this condition, the 0dB gain is achieved at certain frequencies (50Hz, 250Hz, 350Hz). By giving a changing k_{pv} from 0.25 to 2, the features mentioned above is maintained similar. And a similar

performance is obtained while k_{pc} is changed in a given range manually as shown in Figure 3-1(b).

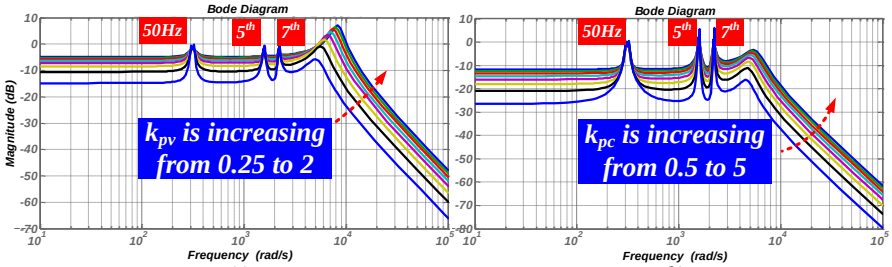


Figure 3-1 Bode diagram of inner loop. (a) Bode diagram with variable k_{pv}. (b) Bode diagram with variable k_{pc}.

From the point of voltage amplitude recover and phase synchronization, the voltage reference for each DC/AC module is composed of two parts, namely amplitude and phase angle. Thus the control can be divided into two aspects respectively as shown in Figure 3-2. However, several points should be kept in mind:

- DC/AC module control is treated as ideal and properly designed, meaning that reference voltage is equal to output voltage.
- CAN bus has a fixed transfer delay.

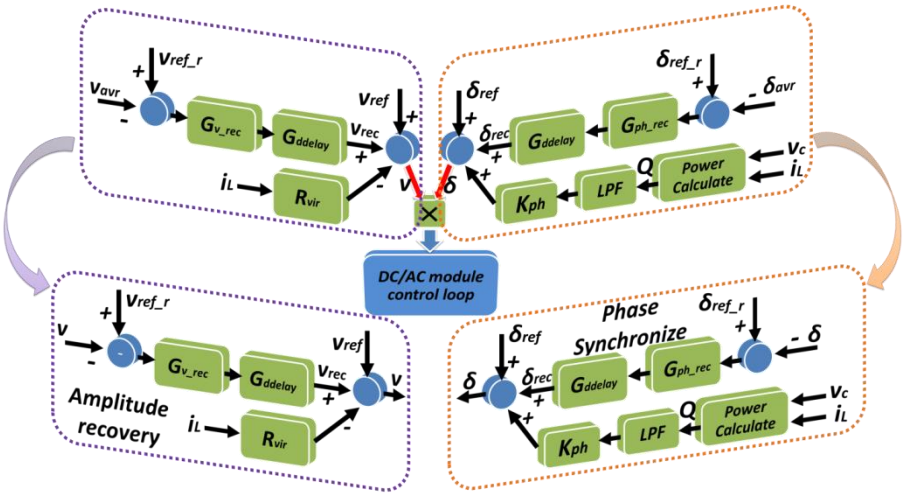


Figure 3-2 Control loops simplification for voltage restoration and phase synchronization.

Thus for voltage amplitude recovery, a small closed loop system can be obtained by considering that reference voltage is equal to output voltage as shown in Figure 3-2. And the transfer function is derived,

$$v = \frac{G_{v\_rec} G_{delay} v_{ref\_r} + v_{ref} - R_{vir} i_L}{1 + G_{v\_rec} G_{delay}} \tag{3-3}$$

And the dynamic of the system can be represented,

$$G(s) = -\frac{R_{vir} T_c s^2 + s}{T_c s^2 + (1 + k_{pv\_sec}) s + k_{iv\_sec}} \tag{3-4}$$

The *pole-zero* map of the voltage amplitude recovery is presented in Figure 3-3. Through changing the parameter k_{pv_sec} (from 0 to 2), the poles and zeros movement can be obtained. It can be observed that one of the dominating poles moves obviously into the stable region and towards the origin point while the other one moved slightly near the stable region boundary but inside the unit circle. R_{vir} exists in numerator and it only affects the zeros position.

On the other hand, an increasing k_{iv_sec} is given, both poles and zeros of the system didn't move obviously. So it can be concluded that the proportional value of voltage amplitude recovery determines the system performance.

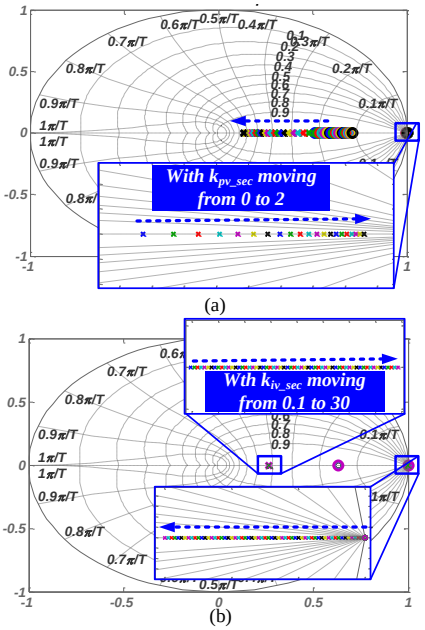


Figure 3-3 pole-zero map for amplitude restoration. (a) PZ map with variable kpv_sec. (b) PZ map with variable kiv_sec.

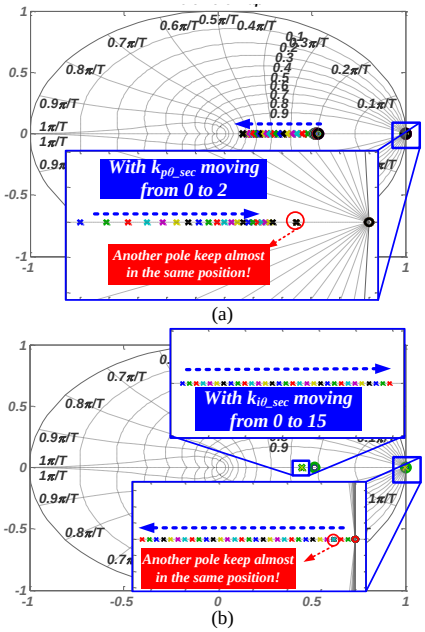


Figure 3-4 pole-zero map for phase restoration. (a) PZ map with variable kpθ_sec. (b) PZ map with variable kiθ_sec.

In a similar way, the phase regulation is able to be analyzed by getting the similar small closed loop as shown in Figure 3-2,

$$\delta = \frac{G_{ph\_rec}G_{delay}\delta_{ref\_r} + \delta_{ref} + G_{LPF}k_{ph}Q}{1 + G_{ph\_rec}G_{delay}} \tag{3-5}$$

As a result, model is able to be derived,

$$\delta = \frac{G_{LPF}k_{ph}}{1 + G_{ph\_rec}G_{delay}}Q \tag{3-6}$$

$$G_{LPF} = \frac{\omega_c}{s + \omega_c} \tag{3-7}$$

$$\frac{\delta}{Q} = \frac{T_c\omega_c k_{ph}s^2 + \omega_c k_{ph}s}{T_c s^3 + \left(T_c\omega_c + k_{p\theta\_\sec} + 1\right)s^2 + \left(\omega_c + k_{i\theta\_\sec} + k_{p\theta\_\sec}\omega_c\right)s + k_{i\theta\_\sec}\omega_c} \tag{3-8}$$

$$G_{delay}(s) = 1/\left(T_c s + 1\right) \tag{3-9}$$

Here T_c is CAN bus transfer delay time. The *pole-zero* map is shown in Figure 3-4. It can be seen that a similar movement phenomenon was obtained. So it can be concluded that it is still the proportional term for phase angle regulation has more impact on system performance. k_{ph} is in the numerator, indicating that it has no impact on poles movement, *ie* system performance.

Another important factor that will affect the system performance is the communication time delay T_c. By using (3-4) and (3-5), the poles and zeros movement can be plotted by giving an increasing communication time delay as shown in Figure 3-5.

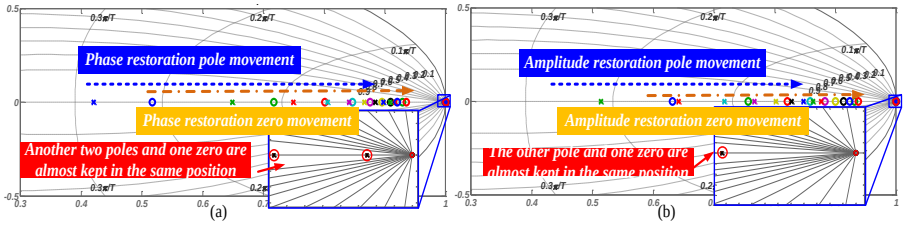


Figure 3-5 Pole-zero map for phase restoration. (a) Poles and zeros movement for phase synchronize. (b) poles and zeros movement for amplitude recovery.

T_c is kept increasing until it reaches 0.5***s***. For phase control, one pole is moving obviously towards the unstable region which is outside of the unit circle. And one zero is also going in the same direction, which means that the system dynamic process will become slower as shown in Figure 3-5(a). Moreover, the same results can be seen for the voltage amplitude recovery in Figure 3-5(b). DSP, using nowadays, provide a smaller time delay that is quite smaller than 0.5***s*** while sending data. Thus based on Figure 3-5 results, it can be said that the dominant poles are always able to be kept inside unit circle and therefore, system is stable.

3.2. MATHEMATICAL MODEL IN OVERALL SYSTEM PERSPECTIVE [PUBLICATION A2]

3.2.1. SMALL SIGNAL MODELLING

A detailed small signal mathematical model is presented, which is able to be a tool to analyze the overall system behavior. Since the inner loop parameters are studied previously, the proposed detailed mathematical model will be mainly studied the remained 6 parameters impact - k_{pv_sec}, k_{iv_sec}, $k_{p\theta\_sec}$, $k_{i\theta\_sec}$, k_{ph} and R_{vir}. Before starting the modelling process, several points should be pointed out:

- Inner controller is designed to work in high frequency (10kHz) to track a low frequency signal (50Hz). Thus its dynamic behaviour can be neglected. Thus DC/AC module can be treated as a unit gain loop.
- The model is considered in $\alpha\beta$ frame since the inner loop controller is carried out in the same framework.

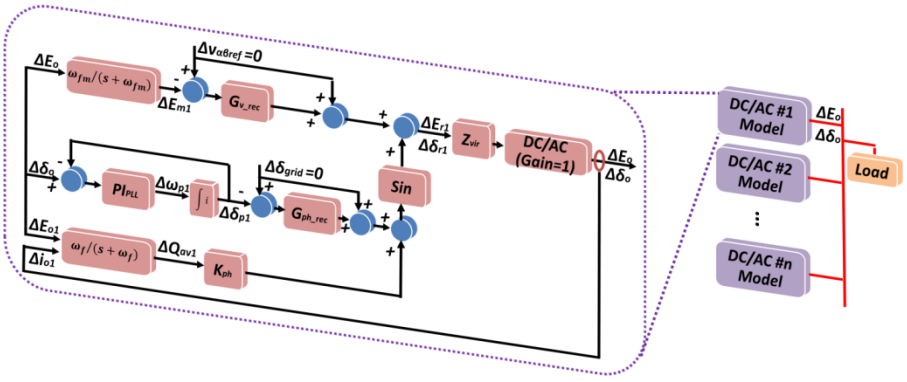


Figure 3-6 Block diagram of the small-signal model for the proposed control.

The modelling diagram is shown in Figure 3-6. It can be seen that the ***LC*** filter dynamics is not taken into account here. The model starts with three DC/AC modules,

$$\Delta E_o = \Delta E_{o1} = \Delta E_{o2} = \Delta E_{o3} = \frac{1}{3}\left(\Delta E_{o1} + \Delta E_{o2} + \Delta E_{o3}\right) \tag{3-10}$$

$$\Delta \delta_o = \Delta \delta_{o1} = \Delta \delta_{o2} = \Delta \delta_{o3} = \frac{1}{3}\left(\Delta \delta_{o1} + \Delta \delta_{o2} + \Delta \delta_{o3}\right) \tag{3-11}$$

Here ΔE_{ox} is the bus and module voltage and $\Delta \delta_{ox}$ is the bus and module phase angle.

ΔE_{m1} is able to be calculated through a low pass filter,

$$\begin{aligned} \Delta E_{m1} &= \frac{\omega_{fm}}{s+\omega_{fm}} \Delta E_o = \frac{1}{3}\frac{\omega_{fm}}{s+\omega_{fm}}\left(\Delta E_{o1} + \Delta E_{o2} + \Delta E_{o3}\right) \\ &= \frac{1}{3}\left(\Delta E_{m1} + \Delta E_{m2} + \Delta E_{m3}\right) \end{aligned} \tag{3-12}$$

being ΔE_{m1} the module *#1* output voltage RMS. The same equation is considered for #2 and #3.

By splitting the system into amplitude and phase respectively, the model will be composed two main parts – amplitude recovery and phase synchronization. Thus the voltage reference amplitude and phase signal can be derived,

$$\begin{aligned} \begin{bmatrix} \dot{\Delta E}_{r1} \\ \dot{\Delta E}_{r2} \\ \dot{\Delta E}_{r3} \end{bmatrix} &= -\frac{1}{3}\begin{bmatrix} k_{pv\_\sec} & k_{pv\_\sec} & k_{pv\_\sec} \\ k_{pv\_\sec} & k_{pv\_\sec} & k_{pv\_\sec} \\ k_{pv\_\sec} & k_{pv\_\sec} & k_{pv\_\sec} \end{bmatrix}\begin{bmatrix} \dot{\Delta E}_{m1} \\ \dot{\Delta E}_{m2} \\ \dot{\Delta E}_{m3} \end{bmatrix} \\ &\quad -\frac{1}{3}\begin{bmatrix} k_{iv\_\sec} & k_{iv\_\sec} & k_{iv\_\sec} \\ k_{iv\_\sec} & k_{iv\_\sec} & k_{iv\_\sec} \\ k_{iv\_\sec} & k_{iv\_\sec} & k_{iv\_\sec} \end{bmatrix}\begin{bmatrix} \Delta E_{m1} \\ \Delta E_{m2} \\ \Delta E_{m3} \end{bmatrix} \end{aligned} \tag{3-13}$$

$$\begin{bmatrix} \dot{\Delta\delta}_{r1} \\ \dot{\Delta\delta}_{r2} \\ \dot{\Delta\delta}_{r3} \end{bmatrix} = -\frac{1}{3}\begin{bmatrix} k_{p\theta\_\sec} & k_{p\theta\_\sec} & k_{p\theta\_\sec} \\ k_{p\theta\_\sec} & k_{p\theta\_\sec} & k_{p\theta\_\sec} \\ k_{p\theta\_\sec} & k_{p\theta\_\sec} & k_{p\theta\_\sec} \end{bmatrix}\begin{bmatrix} \dot{\Delta\delta}_{p1} \\ \dot{\Delta\delta}_{p2} \\ \dot{\Delta\delta}_{p3} \end{bmatrix}$$
$$-\frac{1}{3}\begin{bmatrix} k_{i\theta\_\sec} & k_{i\theta\_\sec} & k_{i\theta\_\sec} \\ k_{i\theta\_\sec} & k_{i\theta\_\sec} & k_{i\theta\_\sec} \\ k_{i\theta\_\sec} & k_{i\theta\_\sec} & k_{i\theta\_\sec} \end{bmatrix}\begin{bmatrix} \Delta\delta_{p1} \\ \Delta\delta_{p2} \\ \Delta\delta_{p3} \end{bmatrix} \quad (3\text{-}14)$$
$$+\begin{bmatrix} k_{ph} & 0 & 0 \\ 0 & k_{ph} & 0 \\ 0 & 0 & k_{ph} \end{bmatrix}\begin{bmatrix} \dot{\Delta Q}_{av1} \\ \dot{\Delta Q}_{av2} \\ \dot{\Delta Q}_{av3} \end{bmatrix}$$

being ΔE_{ri} the amplitude reference of module #*i*, ΔE_{mi} the RMS voltage value of module #*i*, $\Delta\delta_{pi}$ the phase angle of module #*i*, $\Delta\delta_{ri}$ phase reference of module #*i*, and ΔQ_{avi} output reactive power of module #*i* respectively.

Considering the 1st order low pass filter that is used to represent the RMS voltage calculation,

$$\begin{bmatrix} \dot{\Delta E}_{m1} \\ \dot{\Delta E}_{m2} \\ \dot{\Delta E}_{m3} \end{bmatrix} = -\begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix}\begin{bmatrix} \Delta E_{m1} \\ \Delta E_{m2} \\ \Delta E_{m3} \end{bmatrix} \quad (3\text{-}15)$$
$$+\begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix}\begin{bmatrix} \Delta E_{o1} \\ \Delta E_{o2} \\ \Delta E_{o3} \end{bmatrix}$$

being ΔE_{oi} the output voltage of module #*i* and ω_{fm} the cut-off frequency of low pass filter.

Then (3-13) is modified,

$$\begin{bmatrix} \dot{\Delta E}_{r1} \\ \dot{\Delta E}_{r2} \\ \dot{\Delta E}_{r3} \end{bmatrix} = \left(\frac{1}{3}\begin{bmatrix} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\ k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\ k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{bmatrix}\begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix} - \frac{1}{3}\begin{bmatrix} k_{iv\_sec} & k_{iv\_sec} & k_{iv\_sec} \\ k_{iv\_sec} & k_{iv\_sec} & k_{iv\_sec} \\ k_{iv\_sec} & k_{iv\_sec} & k_{iv\_sec} \end{bmatrix} \right)\begin{bmatrix} \Delta E_{m1} \\ \Delta E_{m2} \\ \Delta E_{m3} \end{bmatrix} - \frac{1}{3}\begin{bmatrix} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\ k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\ k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{bmatrix}\begin{bmatrix} \omega_{fm} & 0 & 0 \\ 0 & \omega_{fm} & 0 \\ 0 & 0 & \omega_{fm} \end{bmatrix}\begin{bmatrix} \Delta E_{o1} \\ \Delta E_{o2} \\ \Delta E_{o3} \end{bmatrix} \quad (3\text{-}16)$$

In the system, phase angle information is calculated through a conventional type of PLL. So phase error is,

$$error = error_{\alpha} - error_{\beta} = \sin(\delta_o - \delta_p) \approx \delta_o - \delta_p \quad (3\text{-}17)$$

The final output of the phase detector is considered as ($\Delta\delta_o$–$\Delta\delta_p$). Consequently, according to (3-11), phase-signal equations are obtained,

$$\begin{bmatrix} \dot{\Delta\omega}_{p1} \\ \dot{\Delta\omega}_{p2} \\ \dot{\Delta\omega}_{p3} \end{bmatrix} = \begin{bmatrix} k_{pp} & 0 & 0 \\ 0 & k_{pp} & 0 \\ 0 & 0 & k_{pp} \end{bmatrix}\begin{bmatrix} \dot{\Delta\delta}_{o1} \\ \dot{\Delta\delta}_{o2} \\ \dot{\Delta\delta}_{o3} \end{bmatrix} + \begin{bmatrix} k_{ip} & 0 & 0 \\ 0 & k_{ip} & 0 \\ 0 & 0 & k_{ip} \end{bmatrix}\begin{bmatrix} \Delta\delta_{o1} \\ \Delta\delta_{o2} \\ \Delta\delta_{o3} \end{bmatrix} - \begin{bmatrix} k_{pp} & 0 & 0 \\ 0 & k_{pp} & 0 \\ 0 & 0 & k_{pp} \end{bmatrix}\begin{bmatrix} \Delta\omega_{p1} \\ \Delta\omega_{p2} \\ \Delta\omega_{p3} \end{bmatrix} - \begin{bmatrix} k_{ip} & 0 & 0 \\ 0 & k_{ip} & 0 \\ 0 & 0 & k_{ip} \end{bmatrix}\begin{bmatrix} \Delta\delta_{p1} \\ \Delta\delta_{p2} \\ \Delta\delta_{p3} \end{bmatrix} \quad (3\text{-}18)$$

being k_{pp} and k_{ip} as the proportional term and the integral term in PLL scheme. Consequently, an equation system consisting up of four differential equations can be obtained as shown from (3-19) to (3-22) according to (3-14), (3-16) and (3-18),

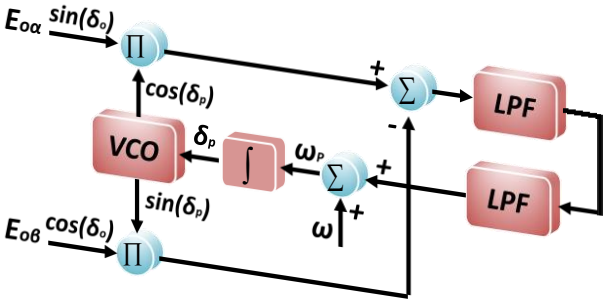


Figure 3-7 Conventional PLL diagram.

$$\Delta\dot{E}_r = (K_{pv}\omega_{fm} - K_{iv})\Delta E_m - K_{pv}\omega_{fm}\Delta E_o \tag{3-19}$$

$$\Delta\dot{\delta}_r = -K_{p\theta}\,\Delta\dot{\delta}_p - K_{i\theta}\Delta\delta_p + K_{ph}\,\Delta\dot{Q}_{av} \tag{3-20}$$

$$\Delta\dot{\omega}_p = K_{PP}\,\Delta\dot{\delta}_o + K_{ip}\Delta\delta_o - K_{pp}\Delta\omega_p - K_{ip}\Delta\delta_p \tag{3-21}$$

$$\Delta\dot{\delta}_p = \Delta\omega_p \tag{3-22}$$

In order to modify the equation system clearly, two vectors ΔX_r and ΔX_o is used,

$$\Delta X_r = \begin{bmatrix} \Delta E_{ri} & \Delta\delta_{ri} & \Delta\omega_{pi} & \Delta\delta_{pi} \end{bmatrix}^T$$
$$\Delta X_o = \begin{bmatrix} \Delta E_{oi} & \Delta\delta_{oi} & \Delta\omega_{pi} & \Delta\delta_{pi} \end{bmatrix}^T$$

Thus the equation system can be modified as,

$$\begin{aligned}\Delta\dot{X}_r = &\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & K_{pp} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}\Delta\dot{X}_0 + \begin{bmatrix} -K_{pv}\omega_{fm} & 0 & 0 & 0 \\ 0 & 0 & -K_{p\theta} & -K_{i\theta} \\ 0 & K_{ip} & -K_{pp} & -K_{ip} \\ 0 & 0 & I_3 & 0 \end{bmatrix}\Delta X_o \\ &+ \left(\begin{bmatrix} K_{pv}\omega_{fm} \\ 0 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} K_{iv} \\ 0 \\ 0 \\ 0 \end{bmatrix} \right)\Delta E_m + \begin{bmatrix} 0 \\ K_{ph} \\ 0 \\ 0 \end{bmatrix}\Delta\dot{Q}_{av}\end{aligned} \tag{3-23}$$

In this situation, ΔXr and ΔX_o are two vectors that is made up of 12 variables because ΔE_{ri}, $\Delta\delta_{ri}$, $\Delta\omega_{pi}$, $\Delta\delta_{pi}$, ΔE_{oi} and $\Delta\delta_{oi}$ each is a 1x3 matrix. Thus,

$$\Delta\dot{X}_r = M_1\Delta\dot{X}_o + M_2\Delta X_o + M_3\Delta E_m + M_4\Delta\dot{Q}_{av} \tag{3-24}$$

Since the reactive power is considered in a Cartesian coordinate system, module output voltage can be derived as,

$$\vec{E}_{oi} = e_{odi} + je_{oqi} = E_{oi}\cos\delta_{oi} + jE_{oi}\sin\delta_{oi} \tag{3-25}$$

$$\delta_{oi} = \arctan(e_{oqi}/e_{odi}) \tag{3-26}$$

Thus,

$$\begin{aligned}\Delta\delta_{oi} &= \frac{\partial\delta_{oi}}{\partial e_{odi}}\Delta e_{odi} + \frac{\partial\delta_{oi}}{\partial e_{oqi}}\Delta e_{oqi} = m_{odi}\Delta e_{odi} + m_{oqi}\Delta e_{oqi} \\ &= -\frac{e_{oqi}}{e_{odi}^2 + e_{oqi}^2}\Delta e_{odi} + \frac{e_{odi}}{e_{odi}^2 + e_{oqi}^2}\Delta e_{oqi}\end{aligned} \tag{3-27}$$

On the other hand, the amplitude of the voltage is derived as $E_{oi} = \left|\vec{E}_{oi}\right| = \sqrt{e_{odi}^2 + e_{oqi}^2}$. By using a similar linearizing way,

$$\Delta E_{oi} = n_{odi}\Delta e_{odi} + n_{oqi}\Delta e_{oqi} = \frac{e_{odi}}{\sqrt{e_{odi}^2 + e_{oqi}^2}}\Delta e_{odi} + \frac{e_{oqi}}{\sqrt{e_{odi}^2 + e_{oqi}^2}}\Delta e_{oqi} \tag{3-28}$$

So modules output voltage E_{oi} is,

$$\begin{bmatrix}\Delta E_{o1}\\ \Delta E_{o2}\\ \Delta E_{o3}\\ \Delta\delta_{o1}\\ \Delta\delta_{o2}\\ \Delta\delta_{o3}\end{bmatrix} = \begin{bmatrix} n_{od1} & n_{oq1} & 0 & 0 & 0 & 0\\ 0 & 0 & n_{od2} & n_{oq2} & 0 & 0\\ 0 & 0 & 0 & 0 & n_{od3} & n_{oq3}\\ m_{od1} & m_{oq1} & 0 & 0 & 0 & 0\\ 0 & 0 & m_{od2} & m_{oq2} & 0 & 0\\ 0 & 0 & 0 & 0 & m_{od3} & m_{oq3}\end{bmatrix}\begin{bmatrix}e_{od1}\\ e_{oq1}\\ e_{od2}\\ e_{oq2}\\ e_{od3}\\ e_{oq3}\end{bmatrix} \tag{3-29}$$

And it symbolic form is derived,

$$\Delta E\delta_o = T_o E_{odq} \tag{3-30}$$

So,

$$\Delta X_o = \begin{bmatrix} T_o & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{odq} = T_{odq} \Delta X_{odq} \tag{3-31}$$

Hereby, I_6 is a 6x6 unit matrix and ΔX_{odq} is obtained,

$$\Delta X_{odq} = \begin{bmatrix} \Delta e_{odq1} & \Delta e_{odq2} & \Delta e_{odq3} & \Delta \omega_{pi} & \Delta \delta_{pi} \end{bmatrix}^T \tag{3-32}$$

Similarly, the vector E_{ri} is calculated by using the same process as the vector E_{oi},

$$\begin{bmatrix} \Delta E_{r1} \\ \Delta E_{r2} \\ \Delta E_{r3} \\ \Delta \delta_{r1} \\ \Delta \delta_{r2} \\ \Delta \delta_{r3} \end{bmatrix} = \begin{bmatrix} n_{rd1} & n_{rq1} & 0 & 0 & 0 & 0 \\ 0 & 0 & n_{rd2} & n_{rq2} & 0 & 0 \\ 0 & 0 & 0 & 0 & n_{rd3} & n_{rq3} \\ m_{rd1} & m_{rq1} & 0 & 0 & 0 & 0 \\ 0 & 0 & m_{rd2} & m_{rq2} & 0 & 0 \\ 0 & 0 & 0 & 0 & m_{rd3} & m_{rq3} \end{bmatrix} \begin{bmatrix} e_{rd1} \\ e_{rq1} \\ e_{rd2} \\ e_{rq2} \\ e_{rd3} \\ e_{rq3} \end{bmatrix} \tag{3-33}$$

Thus,

$$\Delta X_r = \begin{bmatrix} T_r & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{rdq} = T_{rdq} \Delta X_{rdq} \tag{3-34}$$

And

$$\Delta X_{rdq} = \begin{bmatrix} \Delta e_{rdq1} & \Delta e_{rdq2} & \Delta e_{rdq3} & \Delta \omega_{pi} & \Delta \delta_{pi} \end{bmatrix}^T \tag{3-35}$$

Combining 3-32 and 3-35 with 3-24,

$$T_{rdq} \Delta \dot{X}_{rdq} = M_1 T_{odq} \Delta \dot{X}_{odq} + M_2 T_{odq} \Delta X_{odq} + M_3 \Delta E_m + M_4 \Delta \dot{Q}_{av} \tag{3-36}$$

(3-36) represents the small signal mathematical part of the controller shown in Figure 3-6. The next step is to combine this model with the load part including line impedance and load impedance - $Z_{pi} = R_{pi} + jX_{pi}$ and $Z_L = R_L + jX_L$. And the admittances are calculated, $Y_{pi} = 1/Z_{pi}$ and $Y_L = 1/Z_L$.

Thus modules output current is obtained,

$$\begin{bmatrix} i_{od1} \\ i_{oq1} \\ i_{od2} \\ i_{oq2} \\ i_{od3} \\ i_{oq3} \end{bmatrix} = \begin{bmatrix} G_{11} & -B_{11} & G_{12} & -B_{12} & G_{13} & -B_{13} \\ B_{11} & G_{11} & B_{12} & G_{12} & B_{13} & G_{13} \\ G_{21} & -B_{21} & G_{22} & -B_{22} & G_{23} & -B_{23} \\ B_{21} & G_{21} & B_{22} & G_{22} & B_{23} & G_{23} \\ G_{31} & -B_{31} & G_{32} & -B_{32} & G_{33} & -B_{33} \\ B_{31} & G_{31} & B_{32} & G_{32} & B_{33} & G_{33} \end{bmatrix} \begin{bmatrix} e_{od1} \\ e_{oq1} \\ e_{od2} \\ e_{oq2} \\ e_{od3} \\ e_{oq3} \end{bmatrix} \quad (3\text{-}37)$$

Here $Y_{cij} = G_{ij} + jB_{ij}$ and (3-37) symbolic form is,

$$i_{odq} = Y_o e_{odq} \quad (3\text{-}38)$$

After linearizing,

$$\Delta i_{odq} = Y_o e_{odq} \quad (3\text{-}39)$$

Then it is the reactive power calculation. Since it is derived under an orthogonal system,

$$q_i = e_{odi} i_{oqi} - e_{oqi} i_{odi} \quad (3\text{-}40)$$

Thus each module reactive power is,

$$\begin{bmatrix} \Delta q_1 \\ \Delta q_2 \\ \Delta q_3 \end{bmatrix} = I_o \begin{bmatrix} \Delta e_{od1} \\ \Delta e_{oq1} \\ \Delta e_{od2} \\ \Delta e_{oq2} \\ \Delta e_{od3} \\ \Delta e_{oq3} \end{bmatrix} + E_o \begin{bmatrix} \Delta i_{od1} \\ \Delta i_{oq1} \\ \Delta i_{od2} \\ \Delta i_{oq2} \\ \Delta i_{od3} \\ \Delta i_{oq3} \end{bmatrix} \quad (3\text{-}41)$$

where,

$$I_o = \begin{bmatrix} i_{oq1} & -i_{od1} & 0 & 0 & 0 & 0 \\ 0 & 0 & i_{oq2} & -i_{od2} & 0 & 0 \\ 0 & 0 & 0 & 0 & i_{oq3} & -i_{od3} \end{bmatrix},$$

$$E_o = \begin{bmatrix} -e_{oq1} & e_{od1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -e_{oq2} & e_{od2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -e_{oq3} & e_{od3} \end{bmatrix}.$$

(3-40) is rewritten,

$$\Delta q = I_o \Delta e_{odq} + E_o \Delta i_{odq} \tag{3-42}$$

Considering (3-39) and (3-42) together,

$$\Delta q = \left(I_o + E_o Y_o \right) \Delta e_{odq} \tag{3-43}$$

By taking the low pass filter for power calculation into account,

$$Q_{avi} = q_i \, \omega_f \Big/ \left(s + \omega_f \right) \tag{3-44}$$

After linearizing,

$$\begin{bmatrix} \Delta \dot{Q}_{av1} \\ \Delta \dot{Q}_{av2} \\ \Delta \dot{Q}_{av3} \end{bmatrix} = -\begin{bmatrix} \omega_f & 0 & 0 \\ 0 & \omega_f & 0 \\ 0 & 0 & \omega_f \end{bmatrix} \begin{bmatrix} \Delta Q_{av1} \\ \Delta Q_{av2} \\ \Delta Q_{av3} \end{bmatrix} + \begin{bmatrix} \omega_f & 0 & 0 \\ 0 & \omega_f & 0 \\ 0 & 0 & \omega_f \end{bmatrix} \begin{bmatrix} \Delta q_1 \\ \Delta q_2 \\ \Delta q_3 \end{bmatrix} \tag{3-45}$$

Then considering (3-43), (3-45) can be represented as,

$$\Delta \dot{Q}_{av} = -\omega_f \Delta Q_{av} + \omega_f \left(I_o + E_o Y_o \right) \Delta e_{odq} \tag{3-46}$$

Then considering the vector e_{odq} with X_{odq},

$$\Delta\dot{Q}_{av} = -\omega_f \Delta Q_{av} + \omega_f \left(I_o + E_o Y_o \right) K_{xdq} \Delta X_{odq} \tag{3-47}$$

where

$$K_{xdq} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$$

Using (3-15) and two vectors ΔE_o with ΔX_o,

$$\Delta E_o = K_x \Delta X_o = K_x T_{odq} \Delta X_{odq} \tag{3-48}$$

where

$$K_x = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$$

So (3-15) is,

$$\Delta\dot{E}_m = -\omega_{fm} \Delta E_m + \omega_{fm} K_x T_{odq} \Delta X_{odq} \tag{3-49}$$

As a consequence, (3-36), (3-47) and (3-49) form an equation system. At the same time, virtual impedance should be also included,

$$\vec{E}_{ri} = \vec{E}_{oi} + Z_v \vec{I}_{oi} \tag{3-50}$$

Here

$$Z_v = \begin{bmatrix} Z_{v1} & 0 & 0 \\ 0 & Z_{v2} & 0 \\ 0 & 0 & Z_{v3} \end{bmatrix} = \begin{bmatrix} R_{v1} + jX_{v1} & 0 & 0 \\ 0 & R_{v2} + jX_{v2} & 0 \\ 0 & 0 & R_{v3} + jX_{v3} \end{bmatrix}$$

So,

$$e_{rdqi} = e_{odqi} + Z_{vr} i_{odqi} \tag{3-51}$$

And

$$Z_{vr} = \begin{bmatrix} R_{v1} & -X_{v1} & 0 & 0 & 0 & 0 \\ X_{v1} & R_{v1} & 0 & 0 & 0 & 0 \\ 0 & 0 & R_{v2} & -X_{v2} & 0 & 0 \\ 0 & 0 & X_{v2} & R_{v2} & 0 & 0 \\ 0 & 0 & 0 & 0 & R_{v3} & -X_{v3} \\ 0 & 0 & 0 & 0 & X_{v3} & R_{v3} \end{bmatrix}.$$

Combing (3-38) with (3-51),

$$e_{rdqi} = e_{odqi} + Z_{vr} Y_o e_{odqi} = \left(I_6 + Z_{vr} Y_o \right) e_{odqi} = K_{ZY} e_{odqi} \tag{3-52}$$

Its linearized form can be written as,

$$\Delta e_{rdqi} = K_{ZY} \Delta e_{odqi} \tag{3-53}$$

ΔX_{rdq} and ΔX_{odq} are put into (3-53),

$$\Delta X_{rdq} = \begin{bmatrix} K_{ZY} & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{odq} = K_{rdq} \Delta X_{odq} \tag{3-54}$$

$$\Delta \dot{X}_{rdq} = \begin{bmatrix} K_{ZY} & 0 \\ 0 & I_6 \end{bmatrix} \Delta \dot{X}_{odq} = K_{rdq} \Delta \dot{X}_{odq} \tag{3-55}$$

By combining (3-36) with (3-54),

$$T_{rdq}K_{rdq}\,\Delta\dot{X}_{rdq} = M_1T_{odq}\,\Delta\dot{X}_{odq} + M_2T_{odq}\Delta X_{odq} + M_3\Delta E_m + M_4\,\Delta\dot{Q}_{av} \quad (3\text{-}56)$$

By using (3-47) and (3-56),

$$\begin{aligned}\Delta\dot{X}_{rdq} &= T_{km}^{-1}\left(M_2T_{odq} + M_4\omega_f\left(I_o + Y_oE_o\right)K_{xdq}\right)\Delta X_{odq} \\ &+ T_{km}^{-1}M_3\Delta E_m - T_{km}^{-1}M_4\omega_f\,\Delta\dot{Q}_{av}\end{aligned} \quad (3\text{-}57)$$

where $T_{km} = T_{rdq}K_{rdq} - M_1T_{odq}$. Through (3-47), (3-49) and (3-57), a new equation can be obtained,

$$\begin{bmatrix}\Delta\dot{X}_{rdq}\\ \Delta\dot{E}_m\\ \Delta\dot{Q}_{av}\end{bmatrix} = M\begin{bmatrix}\Delta X_{rdq}\\ \Delta E_m\\ \Delta Q_{av}\end{bmatrix} \quad (3\text{-}58)$$

where

$$M = \begin{bmatrix}T_{km}^{-1}\left(M_2T_{odq} + M_4\omega_f\left(I_o + Y_oE_o\right)K_{xdq}\right) & T_{km}^{-1}M_3 & -T_{km}^{-1}M_4\omega_f\\ \omega_{fm}K_xT_{odq} & -\omega_{fm} & 0\\ \omega_f\left(I_o + E_oY_o\right)K_{xdq} & 0 & -\omega_{fm}\end{bmatrix} \quad (3\text{-}59)$$

This equation represents the dynamic performance of the modular system in a mathematical way.

3.2.2. MODEL ANALYSIS WITH EXPERIMENTAL RESULTS

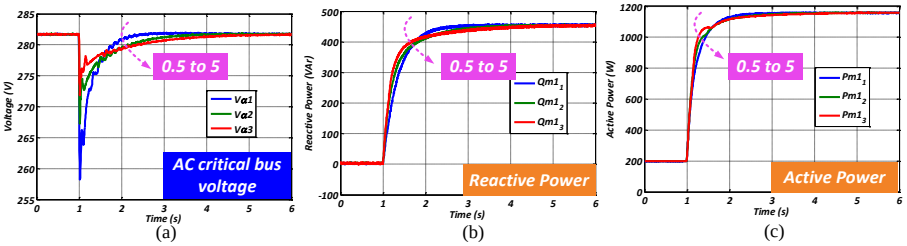
In order to have a better understanding of the modular system, experimental data was recorded through ControlDesk with the help of a real-time control and monitoring platform dSPACE 1006. Thus, system behavior will be compared with the mathematical behavior to analyze the system in a clearer way.

3.2.2.1 Voltage amplitude recovery (k_{pv_sec} and k_{iv_sec})

These two parameters are mainly responsible for the voltage amplitude recovery. Their impact on system performance is evaluated in three aspects respectively – AC

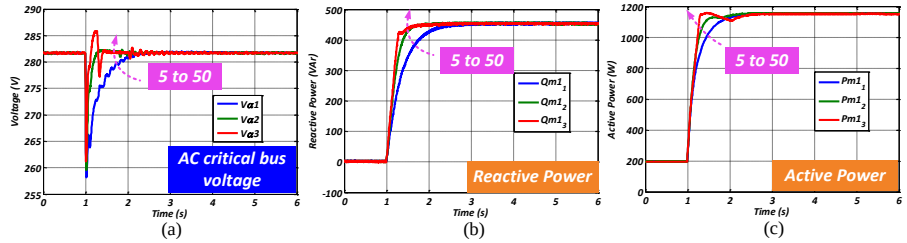
critical bus voltage, reactive power and active power. Through changing k_{pv_sec} and k_{iv_sec}, a series of dynamic performance is obtained and the data was recorded and plotted in Matlab to analysis the system performance. On the other hand, the same changing range will be adopted in the proposed mathematical model to check the mathematical behaviour.

Hence, k_{pv_sec} and k_{iv_sec} was given three values respectively – 0.5, 2.5, 5 for k_{pv_sec} and 5, 20.5, 50 for k_{iv_sec}. Figure 3-8 shows the AC critical bus voltage, reactive power and active power performance under a load step condition using the aforementioned three k_{pv_sec} value while Figure 3-10(a) presents the mathematical behavior of the model. It can be said that while k_{pv_sec} is increasing the dynamic process of AC critical bus and power step are becoming more damped. Hereby, the mathematical model is in in $\alpha\beta$ frame, *ie* 230V rms value means 281.69V in $\alpha\beta$



(a) (b) (c)

Figure 3-8 System performance while k_{pv_sec} is 0.5, 2.5 and 5 (a) AC bus voltage. (b) Reactive power. (c) Active power.



(a) (b) (c)

Figure 3-9 System performance while k_{iv_sec} is 5, 20.5 and 50. (a) AC bus voltage. (b) Reactive power. (c) Active power.

frame. The experimental data of AC critical bus voltage is transformed to $\alpha\beta$ frame. Similarly, in the mathematical model, the dominating poles of the system is moving towards the real axis as presented in Figure 3-10(a). This indicates a more damped system.

As for k_{iv_sec}, a similar process was carried out. It can be seen that the system damp level is decreasing and has the symbol of oscillation while the k_{iv_sec} is increasing from 5 to 50. There is because one of the dominant poles is trying to leave the real axis as much as possible as shown in Figure 3-10(b).

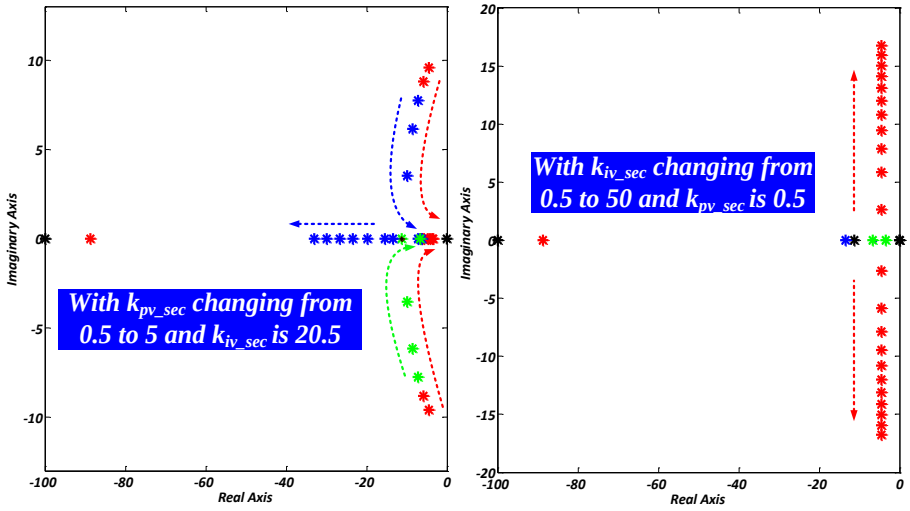


Figure 3-10 Poles movements of the system. (a) k_{pv_sec} from 0.5 to 5. (b)) k_{iv_sec} from 5 to 50.

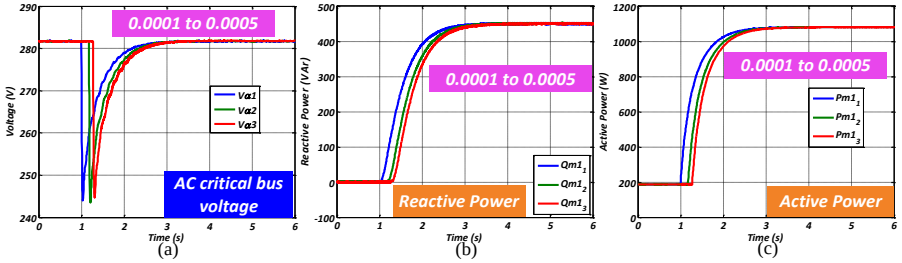
3.2.2.2 Active power and reactive power share (k_{ph} and R_{vir})

Hereby, the impact of k_{ph} and R_{vir} is studied in a similar way as before. When k_{ph} is set to 0.0001, 0.0003 and 0.0005, a series of same dynamic performance is shown in experiments. For the sake of a clear present, the dynamic process start time is made a little bit different through plot code as shown in Figure 3-11. This means that k_{ph} has no impact on stability performance. At the same time, a similar dominating poles movement was obtained as shown in Figure 3-13(a). All of them stayed in the same position with the same parameter changing range.

As for the virtual impedance R_{vir}, it is given three different values – 20, 30 and 40 respectively. With bigger R_{vir} value, the voltage abrupt drop at the starting time edge of dynamic process was becoming bigger. Thus while designing the system, this drop should be controlled as,

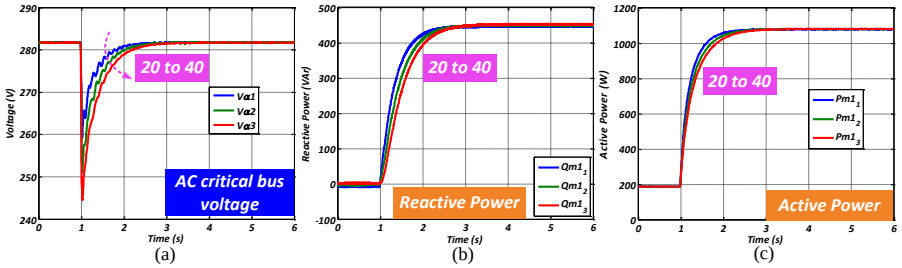
$$\left| i_o R_{vir} / V_o \right| \le 10\% \tag{3-60}$$

being i_o and V_o the maximum output current and nominal output voltage. This is because IEC62040-3 mentioned that with a smaller overshoot, the requirement for the controller dynamic performance can be degraded, which can be good for the control based on communication network. As for the dynamic process, it has slight impact on the AC critical bus voltage as well as reactive and active power as shown in Figure 3-12. Figure 3-13(b) shows the poles movement, it can be seen that the dominant poles are moving slowly.



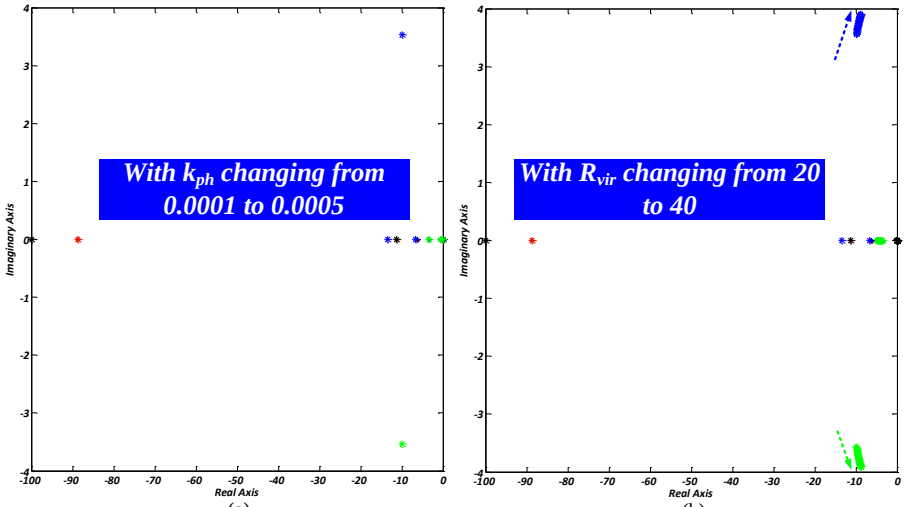
(a) (b) (c)

Figure 3-11 System performance while kph is 0.0001, 0.0003 and 0.0005. (a) AC bus voltage. (b) Reactive power. (c) Active power.



(a) (b) (c)

Figure 3-12 System performance while Rvir is 20, 30 and 40. (a) AC bus voltage. (b) Reactive power. (c) Active power.



(a) (b)

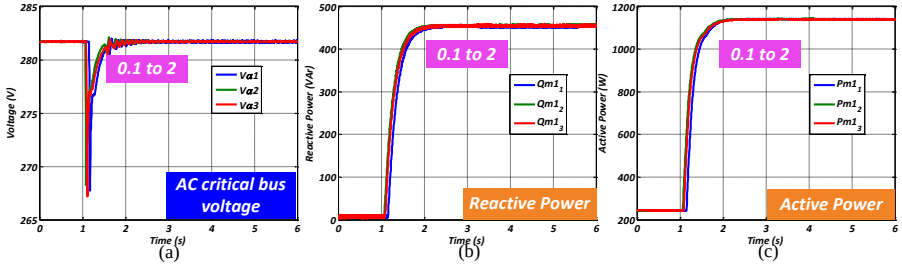
Figure 3-13 Poles movements of the system. (a) k_{ph} from 0.0001to 0.0005. (b) R_{vir} from 20 to 30.

3.2.2.3 Phase regulation ($k_{p\theta\_sec}$ and $k_{i\theta\_sec}$)

A similar process as before was performed. First, $k_{p\theta\_sec}$ was given a series of values while $k_{i\theta\_sec}$ was kept the same value. While $k_{p\theta\_sec}$ was changing from 0.1 to 2, it

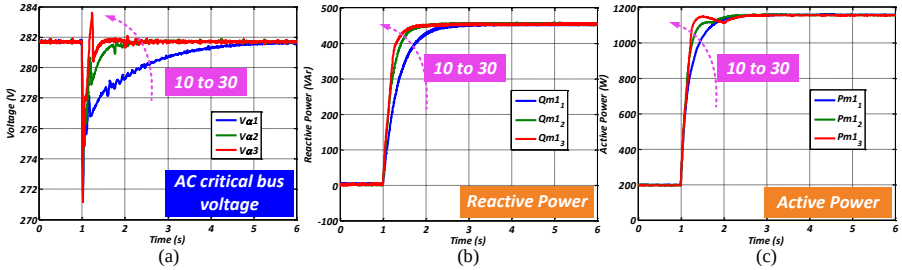
can be seen that a similar dynamic performance was obtained as shown in Figure 3-14 for AC critical bus voltage, reactive power and reactive power. No big different occurs with different parameters. Thus by plotting the dominating poles movements, one of the dominating poles tended to leave far from imaginary axis, which means that its impact on system performance is decreasing. And the other remaining poles almost stayed in the same position as shown in Figure 3-16(a).

As for $k_{i\theta\_sec}$, a different result was shown in Figure 3-15. With a bigger value, the dynamic performance is less damped and started to have oscillations. This means that there should be some poles trying to moving away from the real axis, which is shown in Figure 3-16(b) using the same parameter changing range. On the other hand, it can be seen that another pole started to move towards the imaginary axis. This indicated that its impact on the system performance was becoming stronger and stronger.



(a) (b) (c)

Figure 3-14 System performance while $k_{p\theta\_sec}$ is 0.2, 1 and 2. (a) AC bus voltage. (b) Reactive power. (c) Active power.



(a) (b) (c)

Figure 3-15 System performance while $k_{i\theta\_sec}$ is 10, 20 and 30. (a) AC bus voltage. (b) Reactive power. (c) Active power.

For $k_{p\theta\_sec}$ and $k_{i\theta\_sec}$, they have another important impact on system performance – the convergence speed for phase errors reduction for synchronization purpose. The results are shown in Figure 3-17. It can be concluded that, bigger $k_{i\theta\_sec}$ will decrease the system damp level for dynamic process while bigger $k_{p\theta\_sec}$ will damp the system in a higher level.

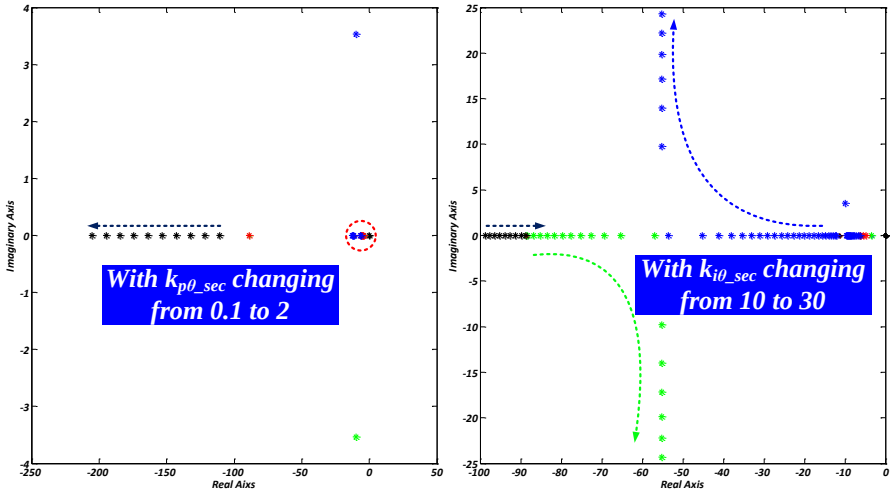


Figure 3-16 Poles movements of the system. (a) $k_{p\theta\_sec}$ from 0.2 to 2. (b)) $k_{i\theta\_sec}$ from 10 to 30.

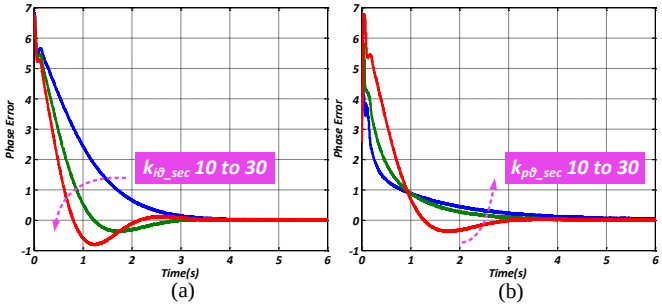


Figure 3-17 Synchronization process regarding different $k_{p\theta\_sec}$ and $k_{i\theta\_sec}$. (a) $k_{i\theta\_sec}$ is 10, 20 and 30. (b)) $k_{p\theta\_sec}$ is 0.2, 1.2 and 2.2.

3.3. CONCLUSION

This chapter presented the mathematical model from the perspective of both single module and the overall modular system.

From the single module perspective, it can be said:

- Inner loop is a conventional double loop system. $k_{p\theta\_sec}$ and k_{pv_sec} dominates the voltage amplitude recovery and phase regulation performance while $k_{i\theta\_sec}$ and k_{iv_sec} have slight impact on system dynamic performance.
- k_{ph} and R_{vir} have no impact on system poles movements.

From the whole modular system perspective, it can be said:

- k_{pv_sec} will damp the system in a higher level if it is increased too much while $k_{p\theta\_sec}$ has slight impact on the system regarding AC critical bus voltage, active power and reactive power.
- $k_{i\theta\_sec}$ and k_{iv_sec} will decrease the damp level of the system and trigger system oscillation if it is given a bigger value.
- k_{ph} has no impact on system dynamic performance regarding AC critical bus voltage, active power and reactive power.
- R_{vir}, with bigger values, will generate a bigger voltage drop on AC critical bus voltage level if a load step is performed. Since it directly works on the voltage performance, it slightly affects the power dynamic process in an indirect way.
- $k_{i\theta\_sec}$ and $k_{p\theta\_sec}$ also shows dominating impact on the phase synchronization process.

It can be seen that different conclusion is obtained from different perspectives. This is because in single module perspective modeling process, all the loops are totally decoupled and independently considered. For instance, for phase regulation, it is only considered in a small closed loop. However, in the overall system model process, all of them are combined and operated in a unified model. Its impact on other loops or other function block impact on it will not be neglected.

CHAPTER 4. THERMAL ANALYSIS OF MODULAR ONLINE UPS SYSTEM

In a real modular system, power semiconductors will be faced with different kind of working conditions, especially the circulating current, which will result in different temperature condition in different devices. Temperature condition on power semiconductors is one of the most important variables that are tightly related with the reliability issues. Different application scenarios, control states and operation modes will result in different temperature performance. Thus it is necessary to analyze the temperature performance in different conditions, which can be a guidance to design both the power stage and cooling system.

4.1. THERMAL MODEL BASICS AND ANALYSIS METHODOLOGY [PUBLICATION A7]

In order to analyze the temperature performance, mathematical thermal model for devices is required. In [95]-[98], the thermal model is presented for power semiconductor such as IGBT, which is shown in Figure 4-1. A *RC* network equalized circuit, as shown in Figure 4-1(b), is used to represent the thermal behaviour of IGBT. The detailed information for *RC* network can be found in the datasheet from vendors [99] and edited in the simulation software PLECS. Thus in simulation, the thermal results of different devices in various kinds of working conditions can be monitored. However, there are some hints that should be kept in mind for the simulation. The equalized thermal capacitance in $Z_{T/D(c\text{-}h)}$ and $Z_{(h\text{-}a)}$ should be given a small value or not considered to reduce the simulation time between start and final steady state. Since the main concern here is the final temperature of the devices in each module, the trade-off can be made on the dynamic details since there two parameters are mainly related with the dynamic process before steady state [100].

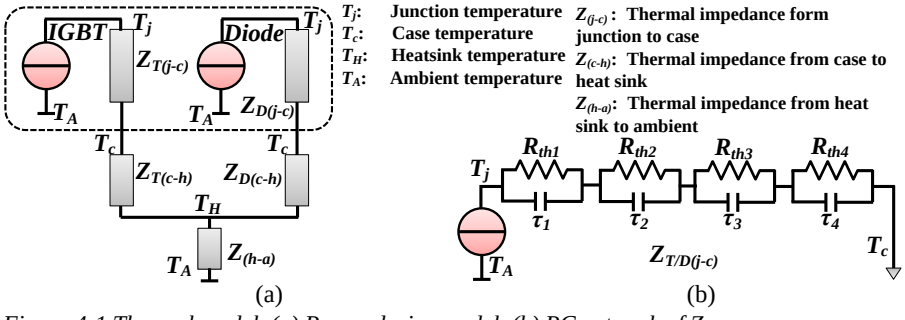


Figure 4-1 Thermal model. (a) Power device model. (b) RC network of $Z_{T/D(j\text{-}c)}$.

In analysis, each DC/AC module is rated with 200kW and its detailed information is shown in Table 4-1. Consequently, IGBT pack 5SND-0800M170100 from ABB is chosen as the power semiconductor devices, whose thermal information is shown in Table 4-2 [101].

Table 4-1. DC/AC electrical information

Power	*Switch frequency*	*DC side*	*Nominal voltage*	*Norminal current*	*Inductor*	*Capacitor*
200kw	5kHz	800V	325V	410A	0.6mH	200μF

Table 4-2. IGBT pack thermal information

Parameters	$Z_{T/D(j\text{-}c)}$			
	1	***2***	***3***	***4***
R_{i_igbt}(K/kW)	15.2	3.6	1.49	0.74
τ_{i_igbt}(ms)	202	20.3	2.01	0.52
R_{i_diode}(K/kW)	25.3	5.78	2.6	2.52
τ_{i_diode}(ms)	210	29.6	7.01	1.49

As mentioned in the UPS product guide [102], UPS product is normally required to work normally for load condition from 50% to 70%. However hereby, the load is considered up to 100%. This is because due to the *plug'n'play* operation, modules may be faced with full load, or even over load. H-bridge is considered (Figure 1-10(a)). And thermal information of T_1, T_2, D_1 and D_2 is obtained and discussed.

Circulating current, including zero sequence circulating current and unbalanced power sharing, will result in different loss and temperature condition for devices. It has been known that the module shares more power will suffer from worse loss and temperature. However, how zero sequence circulating current, as shown in Figure 4-2, affects temperature and loss is still required to be investigated.

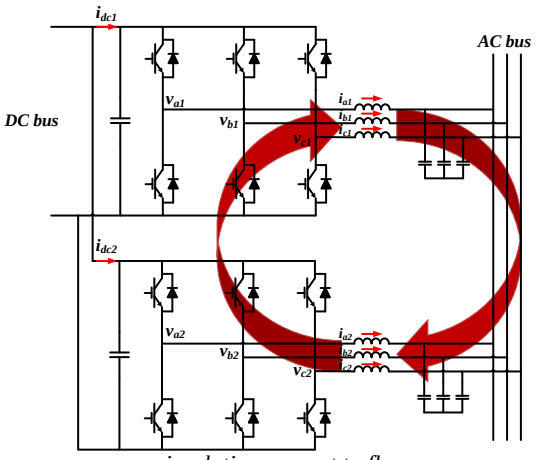


Figure 4-2 Path for zero sequence circulating current to flow.

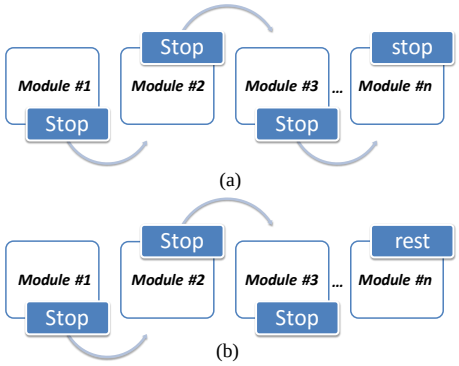


Figure 4-3 Cycle and backup rules. (a) N module cycling and n rests. (b) N-1 module cycling.

4.2. DC/AC MODULES CYCLING OPERATION

Modules cycling operation should be taken into account in case of module failure, overload or any other emergency condition om order to enhance system reliability. Supervisory controllers will take action of stopping or starting any modules. As a result, such kind or issues will trigger the possible path for zero sequence circulating current.

4.2.1. CYCLING AND BACKUP RULES

Normally, there are two kinds of cycling rules as shown in Figure 4-3. *N* module cycling rule is shown in Figure 4-3(a). It means that all the DC/AC modules will participate in the cycling operating. One DC/AC module will start if one of the

working modules stops. Thus each module shares similar percentage of power, heat, loss and so on. Another rule, shown in Figure 4-3(b), is called *N-1* style. In this rule, one DC/AC module always stands by and the remaining *N-1* modules take part in cycling like *N* module style. Once something happens, it will immediately start to work. *N-1* has a higher reliability. But there is always one module standing by, which is a kind of increasing system cost.

4.2.2. POTENTIAL ZERO SEQUENCE CIRCULATING CURRENT IN CYCLING

From the research during the past decades, it has been discussed that several reasons, namely control and physical parameters mismatch, unsynchronized PWM problems, common DC and AC side for converters [103], may bring the zero sequence circulating current into the system. It can be concluded that all this conditions may happen in the proposed modular UPS system shown in Figure 2-1(a). Due to the manufacture process, modules difference is difficult to be avoided. On the other hand, the cycling rule will also result in unsynchronized PWM signals.

In order to eliminate such kind of circulating current, numbers of methods have been proposed, which can be categorized into four types, namely insulation [104]-[106], impedance modification [107], [108], synchronized issues [109]-[112] and vector adjustment [113]-[121]. From cost point, insulation and impedance modification are difficult for vendors to accept since it will require extra equipment such as extra dc sources. As a consequence, synchronize PWM and vector adjustment are considered here.

4.3. THERMAL ANALYSIS [PUBLICATION A7]

First, the thermal analysis result for a single module is presented in order to provide a clear comparison. To create the flowing paths for zero sequence circulating current, different control parameter and physical parameters difference is manually given, in each module such as at least 30% inductor value and 10% capacitor value. Furthermore, the PWM signals for each module are also forced to be unsynchronized.

4.3.1. SINGLE MODULE THERMAL ANALYSIS

The result for single module is shown in Figure 4-4. It can be seen that both switches (T_1 and T_2) and diodes (D_1 and D_2) share the same loss and temperature distribution condition in each kind of load condition. Moreover, a similar distribution condition of temperature variation amplitude and its different as shown in Figure 4-4 (c) and (d). Figure 4-5 shows temperature details at 100% load.

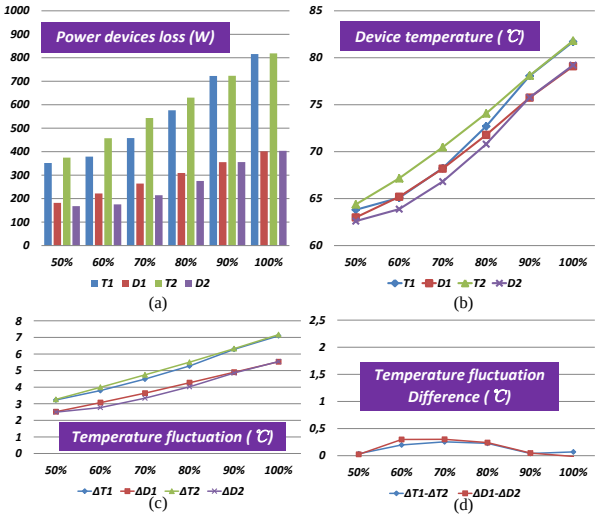


Figure 4-4 Thermal performance of single module. (a) Devices loss. (b) Devices temperature. (c) Temperature fluctuation. (d) Temperature fluctuations differences.

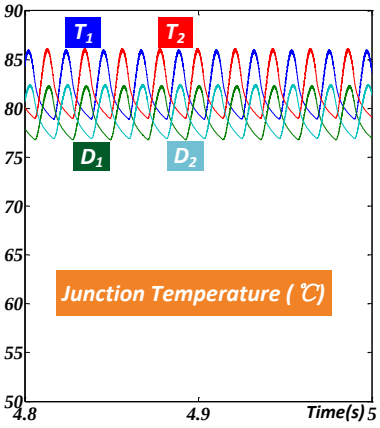


Figure 4-5 Temperature details at 100% load condition.

4.3.2. UNSUPPRESSED CIRCULATING CURRENT CONDITION

Zero sequence circulating current is flowing freely. Thus obvious circulating current can be seen as shown in Figure 4-6. Here, such kind of circulating current is represented by,

$$i_{zero} = \frac{1}{3}\left(i_{oa} + i_{ob} + i_{oc}\right) \tag{4-1}$$

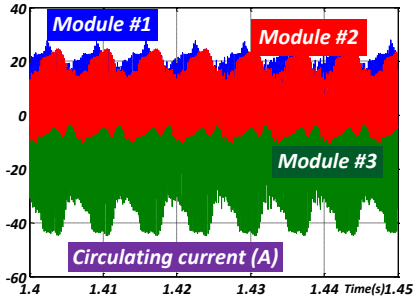
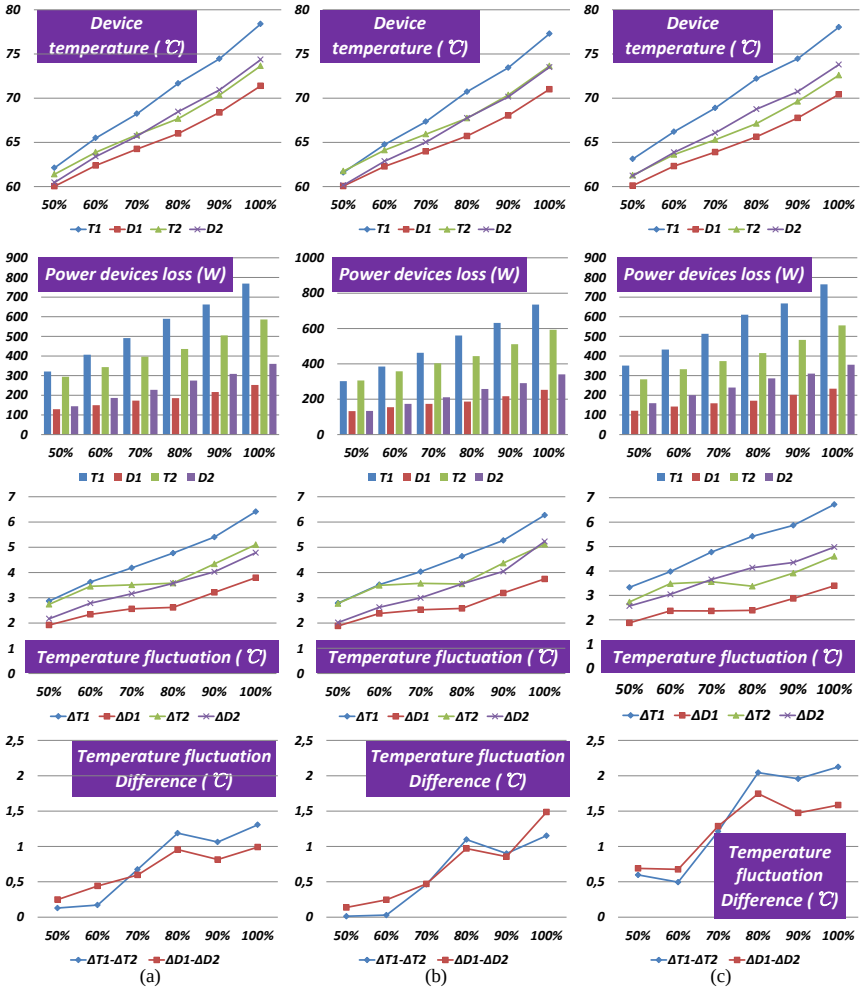


Figure 4-6 Zero sequence circulating current without suppressing.



(a) (b) (c)

Figure 4-7 Thermal performance of three DC/AC modules. (a) module #1. (b) module #2. (c) module #3.

being i_{oa}, i_{ob} and i_{oc} the three phase output current of each DC/AC module. It can be seen that there is some DC component, this is because both physical and control parameters difference will result in a small amount of active power circulating among modules.

In Figure 4-7, the analysis result is shown. Regarding power devices loss and temperature, the balanced distribution condition is broken - T_1 and T_2 present different loss and temperature. It can be seen that T_1 bears higher temperature than T_2 due to its higher loss. However, the diodes present an inverse result. D_2 becomes the victim of higher loss.

At the same time, a similar trend for temperature variation and its difference is observed as shown in Figure 4-7. Moreover, the detailed temperature information for power devices in 100% load condition is obtained as shown in Figure 4-8. It can be seen that it follows the trends shown in Figure 4-7.

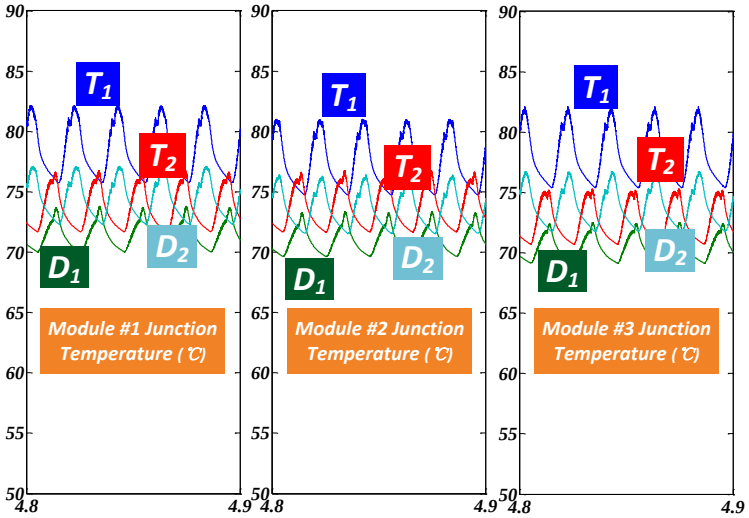


Figure 4-8 Three DC/AC modules one leg devices temperature at 100% load condition.

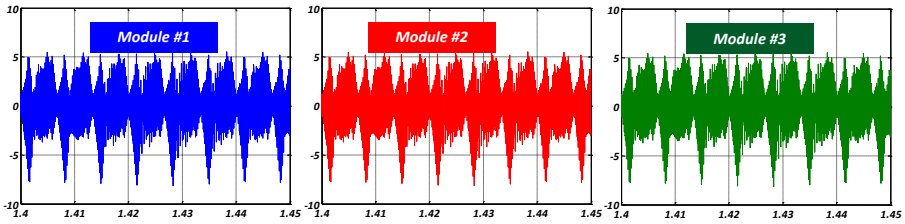


Figure 4-9 Zero sequence circulating current without suppressing.

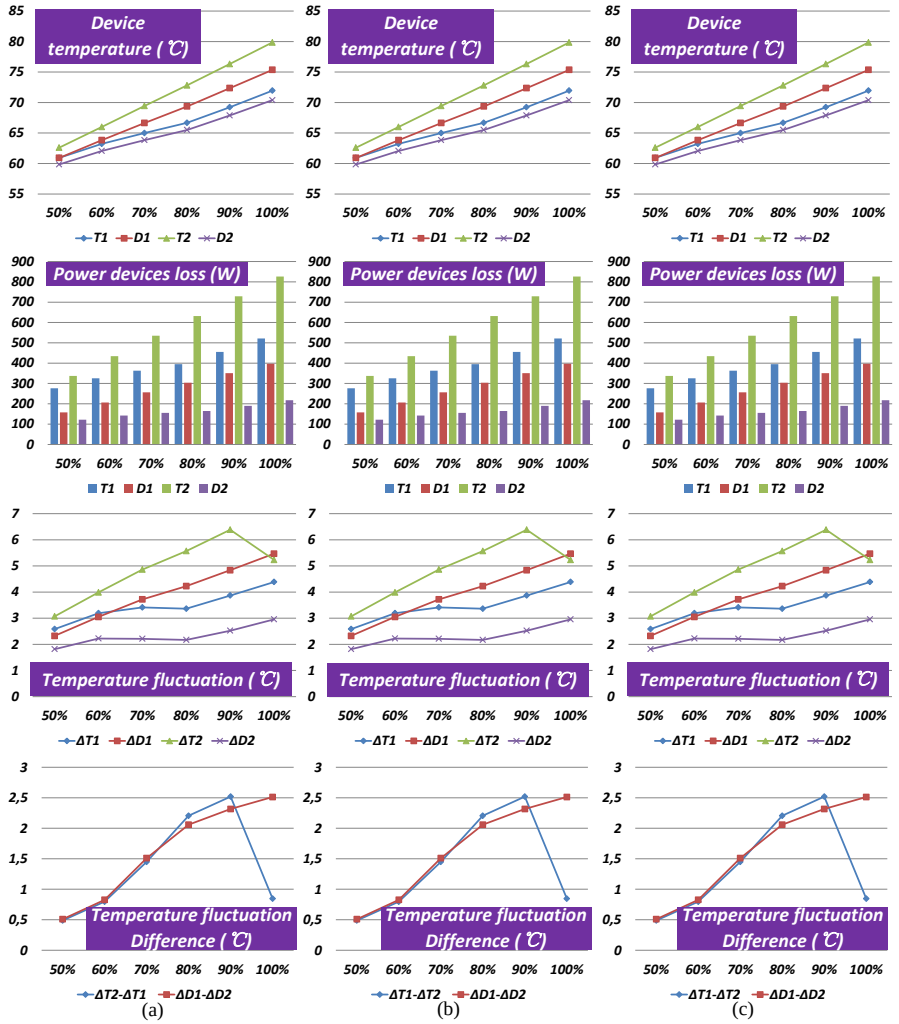


Figure 4-10 Thermal performance with suppressing circulating current. Thermal performance of three DC/AC modules. (a) module #1. (b) module #2. (c) module #3.

4.3.3. SUPPRESSING CIRCULATING CURRENT CONDITION

In order to suppress such kind of circulating current, two methods were considered – to synchronize the PWM signal and controlling the zero-vector time of the PWM modulation. From Figure 4-9, it can be seen that circulating current is highly suppressed compared with Figure 4-6. As for the temperature and loss distribution condition, it can be seen that a totally different style had been obtained. T_2 shows higher temperature than T_1 and D_1 produce more heat than D_2 as well as the temperature distribution shown in Figure 4-10.

Regarding the temperature variation amplitude, three modules share the same changing style as temperature and loss distribution, shown in Figure 4-10.

The detailed temperature information of the three modules at 100% load condition is also presented in Figure 4-11. Similarly, it follows the pattern that shown in Figure 4-10.

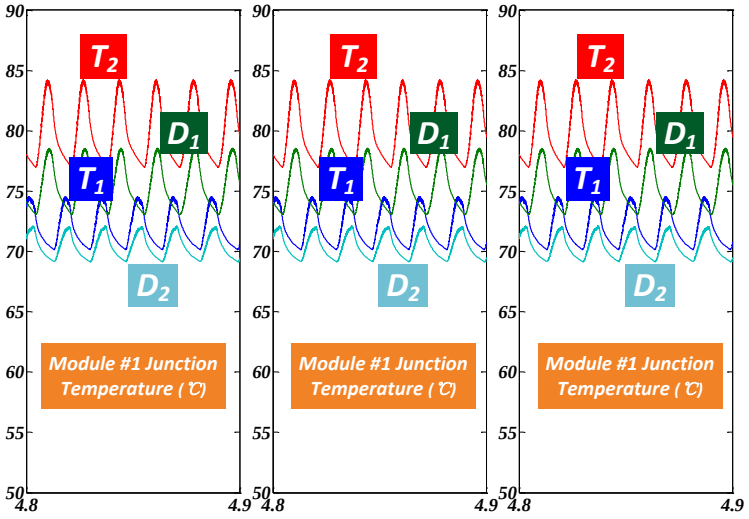


Figure 4-11 Three modules one leg devices temperature at 100% load condition with suppressing.

4.4. CONCLUSION

In this chapter, the thermal analysis is performed in order to evaluate the potential zero-sequence circulating current impact on power devices.

The conclusions are given as follows,

- Zero-sequence circulating current will increase the loss of the upper switch, down diode in each leg. A higher temperature will be observed in these two power devices.
- Suppressing control methods will suppress such kind of circulating current. However, it will change the loss distribution condition – the down switch and upper diode in each leg will suffer from high loss. As a result, they will work in a higher temperature condition.

CHAPTER 5. PRACTICAL ISSUES IN AN INDUSTRIAL PROTOTYPE

In the previous analysis, control architectures and methods, used in the modular structure shown in Figure 2-1(a), are discussed. Both mathematical model and experimental results are also presented. In this chapter, real product implementation will be considered. The structure shown in Figure 2-1(b) will be used because each module is a single, full-functional UPS system. It provides a good potential for system redundancy.

5.1. CONTROL METHODS IMPLEMENTATION IN A DIGITAL SIGNAL PROCESSOR (DSP)

In real application, control strategies for parallel and inner loop control are programmed in DSP with C language. According to [60], if the DC/AC output impedance is designed to be mainly resistive, reactive power is calculated to regulate frequency or phase angle based on the following two equations,

$$f = 50Hz - k_f * Q \tag{5-1}$$

$$\delta = \delta^* + k_\delta * Q \tag{5-2}$$

Normally, phase is obtained from PLL and derived from frequency through an integrator. So phase is related with frequency in theory. However, in digital implementation in DSP, regulating frequency and phase angle are totally different. In order to analyze the difference, it is assumed that the DSP main interruption frequency is 20kHz, *ie* 50μs. As a consequence, 2π should be divided into 400 steps to have utility cycle 20ms (50***μs****400). Thus the phase step size for normal condition is 2π/400 as shown in Figure 5-1.

First, (5-1) is used to regulate reactive power sharing. Phase step size (2π/400) is required to be modified based on reactive power. Normally, frequency will be decreased based on the output reactive power,

$$\delta(k+1) = \delta(k) + \left(50Hz - k_f Q\right) NormalStep / 50Hz \tag{5-3}$$

with k_f being the reactive power regulating coefficient, Q being the output reactive power. As a result, phase step size (2π/400) will be reduced according to (5-3). Thus in order to get 2π, it is necessary to have more steps, for instance 500, as

shown in Figure 5-1. So the output voltage period will be increase (500*50***μs***=25***ms***), which means that the output voltage frequency is regulated.

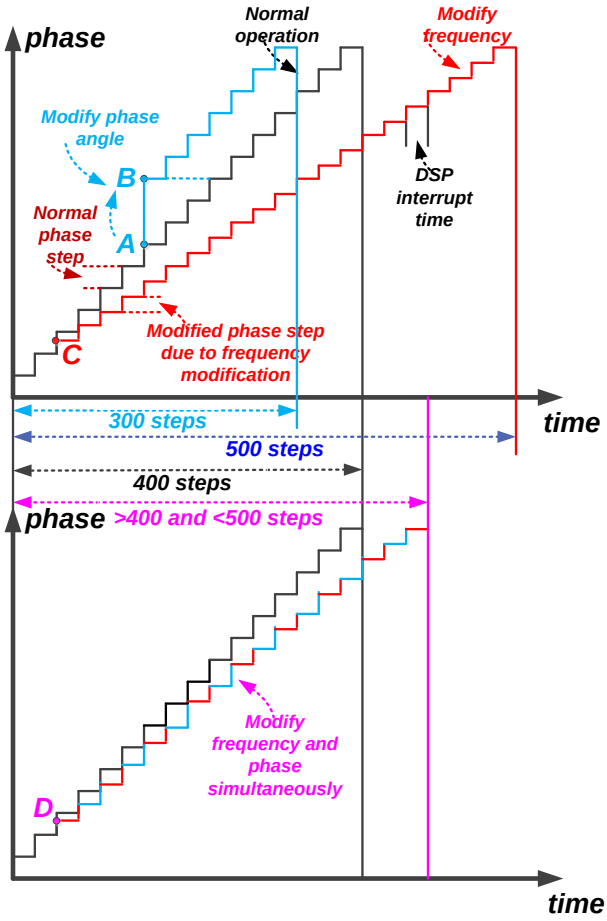


Figure 5-1 Control process for frequency regulation, phase jump and combined methods.

Then, (5-2) is considered. Phase step size (2π/400) will not be changed but the phase point will jump based on the following,

$$\delta(k+1) = \delta(k) + \left\lfloor \frac{Qk_{\delta}}{NormalStep} \right\rfloor NormalStep \tag{5-4}$$

with k_{δ} being the phase regulating coefficients. Based on output reactive power, the phase jump point number will be decided as $Qk_{\delta}/NormalStep$. If $Qk_{\delta}/NormalStep$ is not an integer value, only the integer part will be kept. Then multiplied by the *NormalStep*, the phase jump value will be decided. For example, if $Qk_{\delta}/NormalStep$

is calculated as 3, thus phase point will jump from A to B as shown in Figure 5-1. For the current cycle, the output voltage frequency will be changed because steps are reduced suddenly due to the phase jump. However, after this cycle, the frequency will be back to 50Hz since the phase step size is not changed.

It can be concluded that frequency regulation is changing the phase step size for voltage reference generation. The output voltage frequency is changed gradually until it reaches the stable value. Nevertheless, regulating phase is different. Phase step size for voltage reference generation is kept the same. Phase point will jump based on output reactive power. Abrupt frequency change can be observed and finally the frequency will move back to nominal value.

In order to enhance frequency performance, a compromised method can be derived,

$$\delta(k+1)=\delta(k)+\frac{\left(50Hz-k_f k_Q Q\right)}{50Hz}NormalStep + \left\lfloor\frac{\left(1-k_Q\right)Qk_\delta}{NormalStep}\right\rfloor NormalStep \tag{5-5}$$

Here k_Q is the reactive power divided coefficients. Reactive power is divided into two parts for regulating frequency and jump phase respectively. It seems like a kind of simple fuzzy logic. The value of k_Q depends on the frequency requirement of consumers. If a faster dynamic performance and small frequency change is desired, thus k_Q should be smaller. It means that a larger share of reactive power will be regulated by phase jump. Otherwise, k_Q should be designed as a smaller value. The frequency performance of three implementation methods is presented in Figure 5-2.

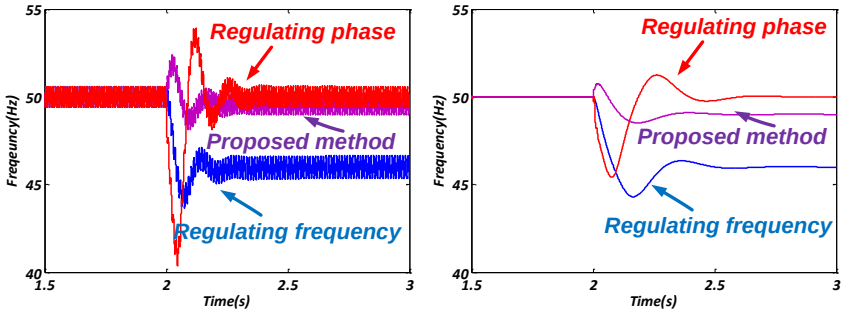


Figure 5-2 Frequency performance. (a) pPLL. (b) SOGI-PLL.

In the test, two kinds of PLL are considered, namely pPLL and SOGI-PLL. A reactive power load step is given to the system at 2***s***. pPLL is intended for single phase system while SOGI-PLL is designed for the three phase system. It can be

seen that in pPLL the compromised implementation method has a smaller frequency drop than regulating frequency but has a smaller frequency oscillation than phase jump method. Because there is a low pass filter in the pPLL structure, there exists small frequency ripples. Moreover, a similar performance can be observed while using the SOGI-PLL. In Figure 5-3, the k_Q impacts is also presented. Smaller value will result in a smaller frequency drop.

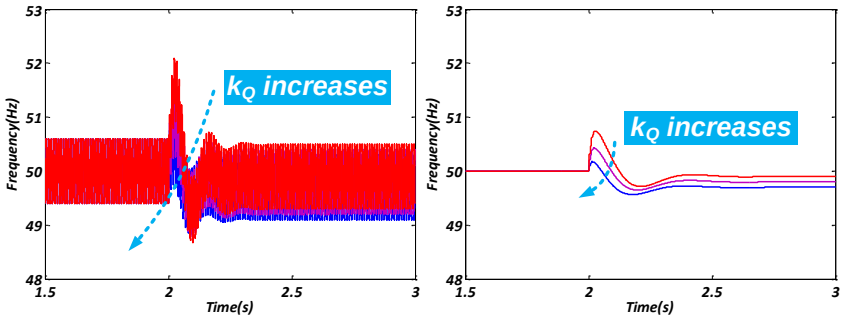


Figure 5-3 Frequency performance with variable k_Q. (a) pPLL. (b) SOGI-PLL.

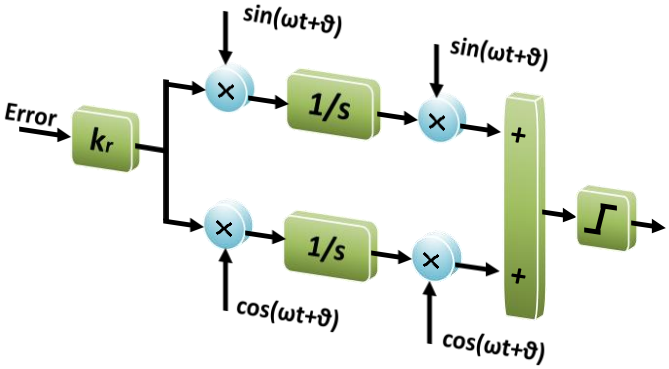


Figure 5-4 Resonant part diagram with saturation.

5.2. ANTI-WINDUP FOR DISCRETE PROPORTIONAL RESONANT CONTROLLERS

A conventional *PR* controller is considered here. And the resonant part is shown in Figure 5-4.

Hereby, two integrators are used, which are multiplied by sin and cos signal. It can be seen that there is a phase delay θ in sin and cos signals. It is used to compensate the delay in the system. There is one saturation block after the integrators to limit the output of the resonators. In case of low DC side voltage or short circuit condition, the resonators will be saturated very fast, enters deep saturation condition

and lose the capability of regulating the output of the controller. In order to create a deep saturation scenario for the PR controller, the DC voltage of the DC/AC is given a ramp from 0 to 700V. In Figure 5-5(a), it can be seen that the output voltage is still distorted when the ramp process is finished. And after some chaos cycles, the output voltage moves back to normal operation condition. In Figure 5-5(b), the DC voltage is given a step from 300V to 700V. When the DC voltage is 300V, the PR controller is kept in deep saturation condition. Once the DC voltage is 700V, the PR controller should move back to normal operation condition. However, the PR controller still stays in deep saturation condition and the output voltage is still distorted.

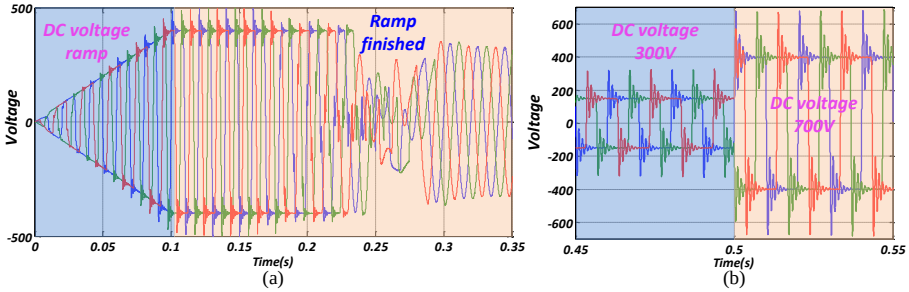


Figure 5-5 Voltage performance without anti-windup. (a DC voltage ramp. (b) DC voltage step.

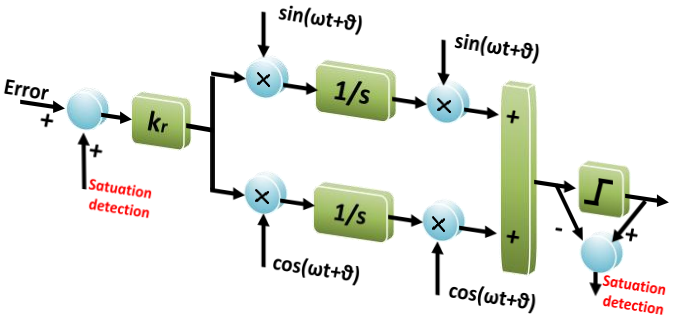


Figure 5-6 Resonators with anti-windup capability.

Thus it is necessary to avoid the saturation of the resonators, which is called anti-windup as shown in Figure 5-6. It can be seen that the output will minus the results before saturation block and give the results to the error as a feedback signal. In case of deep saturation, this method will change the direction of error, which will make the integrator working in the opposite direction. This will allow the integrators to avoid deep saturation in case of startup process. The same test is carried out to test the anti-windup performance for the PR controller as shown in Figure 5-7. DC voltage ramp and DC voltage step are used to create the PR controller deep saturation condition. It can be concluded that with anti-windup method, PR

controller can be avoided to enter deep saturation condition and a better dynamic performance is achieved.

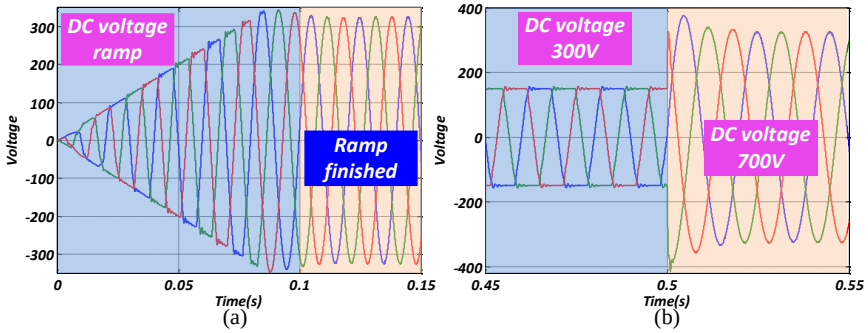


Figure 5-7 Voltage performance with anti-windup. (a) DC voltage ramp. (b) DC voltage step.

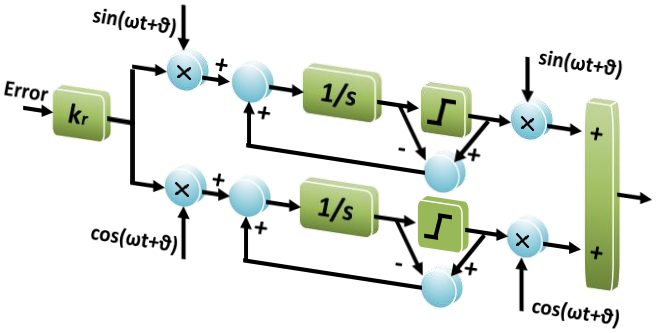


Figure 5-8 Direct anti-windup for resonators.

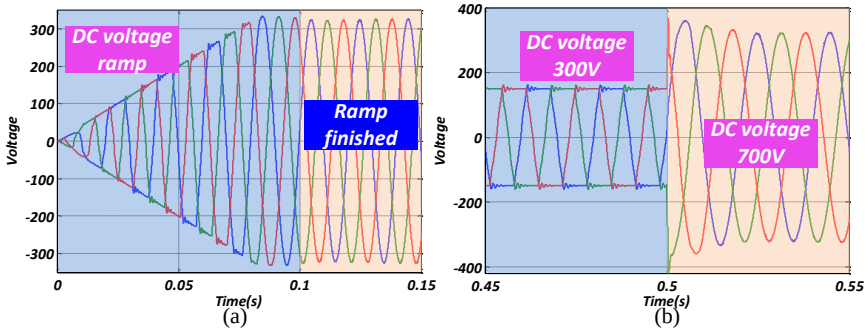


Figure 5-9 Voltage performance with direct anti-windup. (a) DC voltage ramp. (b) DC voltage step.

However, this will only limit the final output of the controllers. The condition of the two integrators is not controlled any more. Thus a direct anti-windup method can be

applied, which is shown in Figure 5-8. And the voltage control performance is shown in Figure 5-9. A similar dynamic and voltage control performance are able to be observed in Figure 5-9. Since the anti-windup is worked directly on the two integrators in the resonant part, the accuracy is improved. As a consequence, a better dynamic performance can be seen as shown in Figure 5-9.

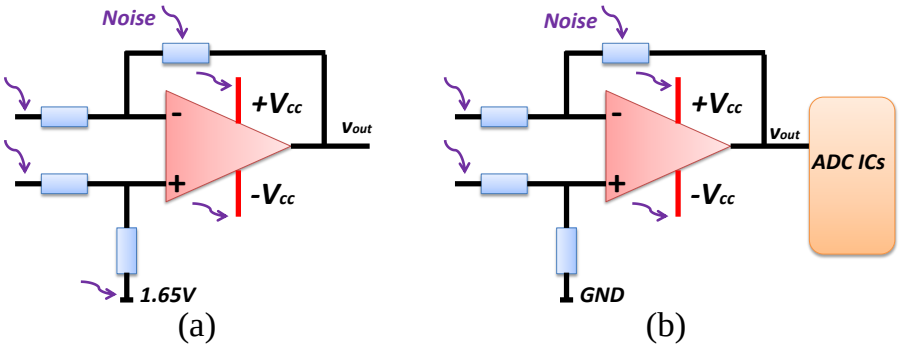


Figure 5-10 AD hardware for voltage measurement. (a) single polar. (b) bi-polar.

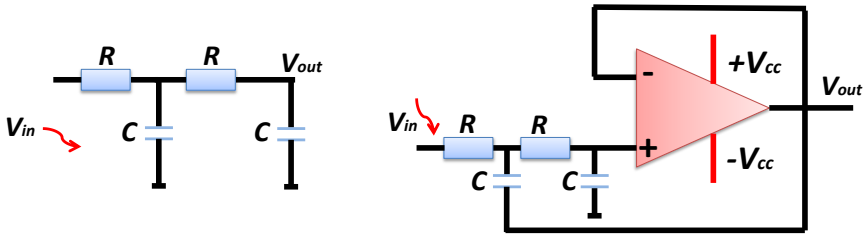
5.3. NOISE REDUCTION

For the control of a DC/AC module, another critical thing that should be taken into consideration is the ADC measurement. There are several elements that will affect the AD circuit measurement, namely PCB design style and circuit design issues. Hereby, only circuit design is discussed.

According to different kinds of AD hardware circuit, the noise will affect the AD results in different ways. Normally, there are two basic AD hardware type, namely single polar and bi-polar as shown in Fig. 5.10. In Figure 5-10(a), the differential circuit is given a 1.65V voltage offset. And the output of the AD is between 0 and 3.3V, which is more sensitive to the noise voltage amplitude. And the output is connected with the DSP directly. In such kind of circuit, there are several kinds of paths for the noise to take effect. For instance, the input of the amplifier will be polluted by the noise. On the other hand, the power supply voltage ripple will affect not only the V_{cc} but also the 1.65V voltage. Another path is the feedback loop for the amplifier.

In Figure 5-10(b), another type of AD is presented. Instead of giving a voltage offset, the output of AD will be bi-polar. Since an ADC IC is used, thus the output voltage amplitude of the AD can be increased between -15V and 15V. Thus the AD output is not easy to be polluted. And the ADC IC will get the data and send the results to DSP. However, the AD sample speed will be limited by the ADC IC. And the cost issue is also required to be considered. In these conditions, no matter what

kind of noise sources, it will result in voltage noise ripple in the AD circuit output. The noise voltage ripple is considered here.



(a) (b)

Figure 5-11 Low pass filter for AD noise. (a) passive type. (b) active type (Sallen-Key).

Thus in order to reduce the impact of the noise, both analog filter and digital filter are used in combination. There are two basic kind of analog filters considered here, namely passive and active, which is shown in Figure 5-11. Figure 5-11(a) is composed of resistor and capacitor and it is a two order low pass filter. In Figure 5-11(b), an amplifier is used to build an active low pass filter. Hereby, the capacitor is connected with the output in order to work as positive feedback, which can improve the gain performance around cut off frequency. The transfer function of these two kinds of analog filter is derived,

$$G_{passive} = \frac{1}{(RCs)^2 + 3RCs + 1} \tag{5-6}$$

$$G_{active} = \frac{A_{vp}}{(RCs)^2 + (1 - A_{vp})RCs + 1} \tag{5-7}$$

with A_{vp} being the gain of the active analog filter. The cut off frequency of these two filters is designed to be around 1kHz. Thus the R and C in Figure 5-11(a) are 51.1k and 1.5nF respectively. And the R and C in Figure 5-11(b) are 20k and 3.3nF respectively. Hereby, the active type gain is fixed to be 1, which means that the qualification factor Q is 0.5. And the performance of the filters is shown in Figure 5-12. The data is obtained from the DSP from the ADC part and plotted in Matlab. It can be seen that both filters can achieve similar filter performance.

As for the digital filters, it is implemented in DSP. When the DSP obtains the AD value, it will calculate the real voltage or current value. Thus the digital filter works with the real voltage or current value. It is designed based on the following,

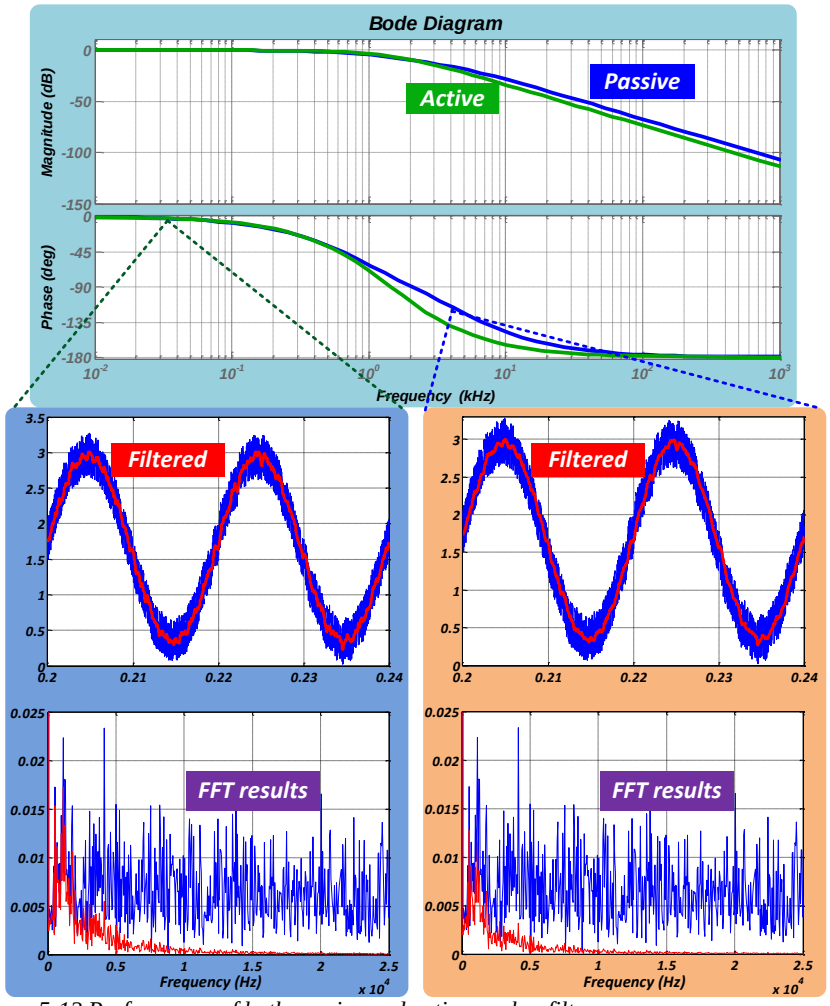
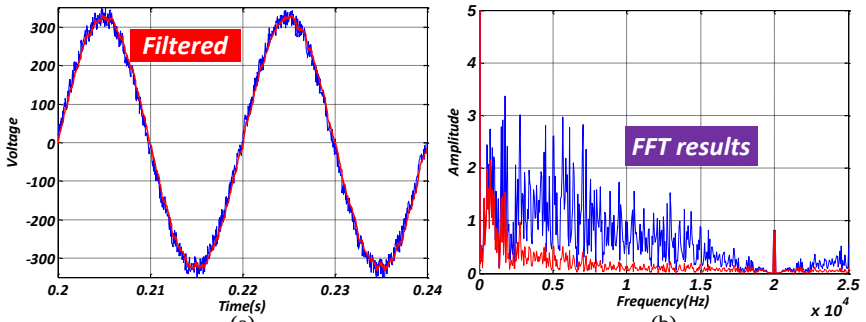


Figure 5-12 Performance of both passive and active analog filter.

$$G(s) = 1/(as + b) \tag{5-8}$$

And the performance is shown in Figure 5-13. It can be seen that the noise can be reduced. The output voltage data is stored and plotted in Matlab, which is shown in Figure 5-14. It can be seen that although the noise impact on the output voltage is reduced with the help of analog filter and digital filter, it introduces a small advanced phase angle. Thus a proper tradeoff should be made between noise filter design and output voltage performance.



(a) (b)

Figure 5-13 Digital filter performance. (a) voltage before and after filtered. (b) FFT results before and after filter.

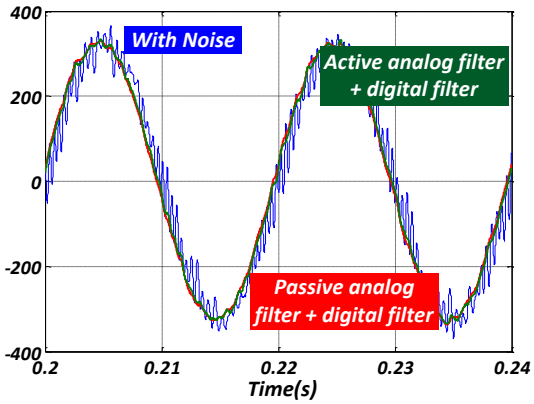


Figure 5-14 Output voltage performance with and without filtering.

5.4. PHASE LOCK LOOP IMPLEMENTATION

In UPS application, phase lock loop (PLL) is a critical element to track the utility voltage phase angle for the bypass operation, which should be carefully designed. Although the proposed UPS system is three phase, it should have the capability of operating in single phase mode. Thus in this section, both single phase PLL and three PLL are considered [122]. For single phase PLL, *pPLL* and *ePLL* is evaluated because *pPLL* is the simplest PLL for single phase while *ePLL* has a good performance regarding the frequency jump in the system. As for the three phase PLL, two are considered here, namely basic three phase and SOGI-based PLL since SOGI-based PLL has outstanding performance under grid voltage distortion condition. The four kinds of PLL structures are presented in Figure 5-15.

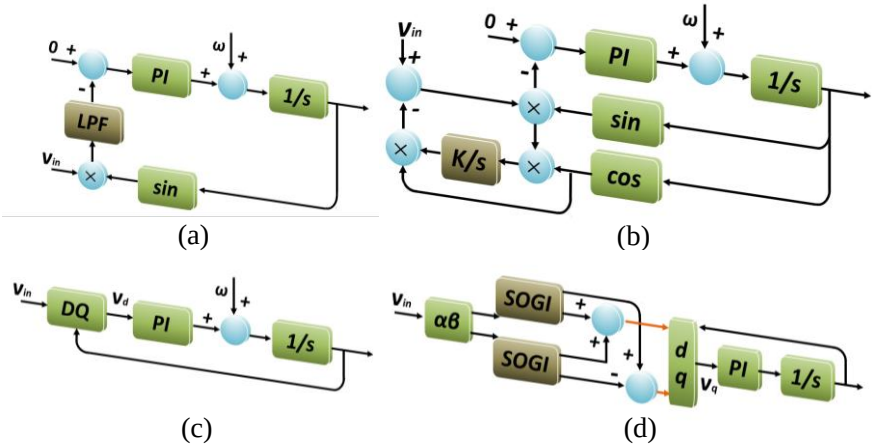


Figure 5-15 Different PLL structure. (a) pPLL. (b) ePLL. (c) basic three phase PLL. (d) SOGI-based PLL.

The analysis is based on the aforementioned four kinds of PLL. Different PLL presents different dynamic performance in case of frequency jump as shown in Figure 5-16. In the test, different PLLs are used to measure the AC critical bus voltage. Due to the low pass filter inside the PLL, *pPLL* has ripple in the frequency detect results as shown in Figure 5-16(a). In Figure 5-16(b), the result of *ePLL* is shown. It can be seen that the frequency ripple is eliminated. However, it has a poorer dynamic performance with obvious frequency oscillation. Figure 5-16(c) shows the performance of basic three phases PLL. It can be observed that its performance is outstanding in both steady and dynamic condition. Nevertheless, it doesn't have the capability of operating in single phase condition. Furthermore, the performance of SOGI-PLL is shown in Figure 5-16(d). It has no frequency ripple and the dynamic process can be accepted. However, the main drawback of SOGI based PLL is that it is too complicated. A large amount of DSP resources will be occupied by the PLL algorithm. As a result, the *pPLL* is chosen due to its simplicity, single phase capability.

Since the UPS system may work in a variable frequency scenario, such as diesel generator system, it will have the ability to track in a certain range of frequency in order to have smooth bypass process. Normally, users will give the frequency range through the human-computer interface. Then the PLL in the UPS system will operate based on the requirements.

The only way that PLL can detect the frequency is the signal before the final integrator. However, in some conditions this signal will have some ripples, which will affect the frequency judgement. For example, in pPLL there will be intrinsic frequency ripple due to the low pass filter in the control structure. And in SOGI-based PLL, in case of unbalanced three phase voltage, the frequency ripple will

come out. Thus in this condition, the frequency detection will be in chaos. In order to eliminate this negative impact, a digital Schmitt function is used to emulate the analog Schmitt circuit, which is shown in Fig. 5.17.

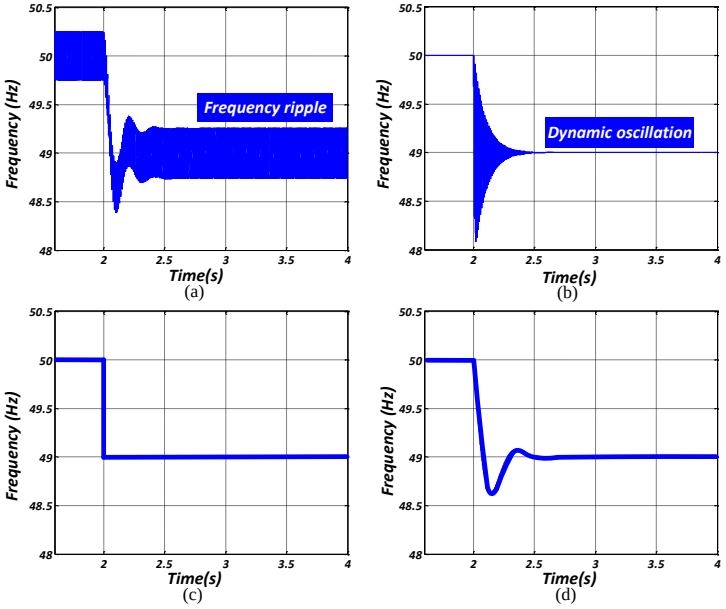


Figure 5-16 Different PLL dynamic performance in case of frequency jump. (a) pPLL. (b) ePLL. (c) basic three phase PLL. (d) SOGI-based PLL.

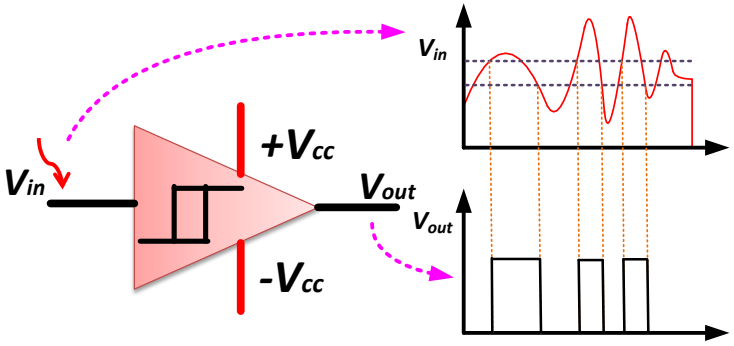


Figure 5-17 Schmitt function.

It can be seen that Figure 5-17 presents a normal positive phase Schmitt function. It is used inside the PLL structure in order to detect the frequency in a more accurate way. The mechanic is shown in Figure 5-18. Hereby the frequency change is assumed to be from 40Hz to 60Hz with around 1Hz ripple. And two different Schmitt functions (positive and negative) are employed to detect the frequency down edge and up edge. The mechanic is shown in Figure 5-18. The output logic of

the inserted the Schmitt will decide the frequency range that the users put through the human-computer interface. When the Schmitt function detects that the frequency reaches the down edge frequency, its output will step from 0 to 1. On the other hand, around the up frequency edge, the Schmitt will step from 1 to 0. Thus when both the outputs are 1, it means that now the frequency of the utility voltage is inside the range that users want. Thus the output of PLL will be delivered to the reference generation block of the UPS module. Otherwise, the PLL output will be fixed at 50Hz all the time.

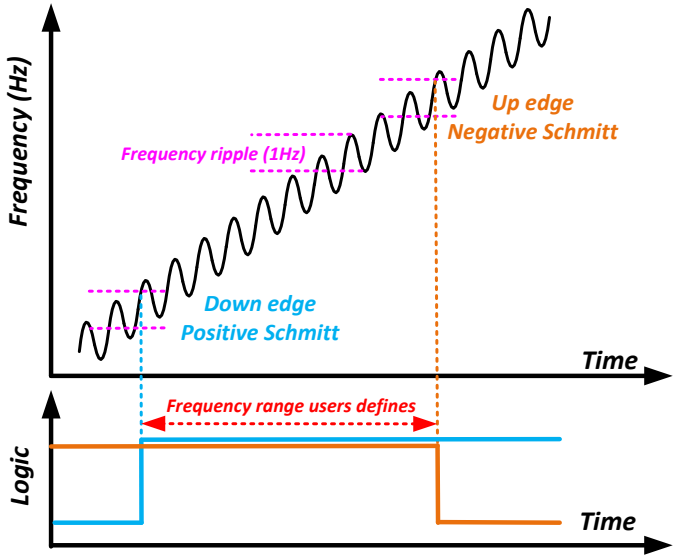


Figure 5-18 Schmitt mechanic in PLL.

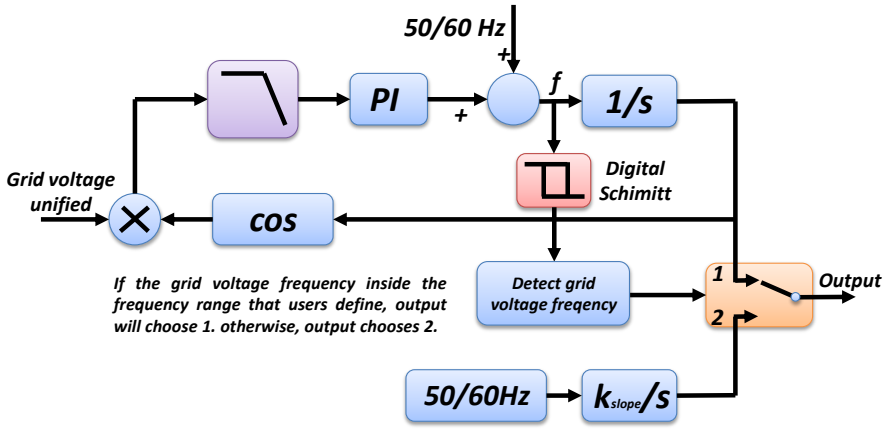


Figure 5-19 Final PLL structure based on p-PLL.

Thus the main PLL structure based on pPLL is shown in Figure 5-19. Since there are two output states in the PLL, there is another important process for the transient operation between them. The UPS system can't accept a sudden phase jump. There will be a big noise occurred in the converter if the voltage phase angle is suddenly changed. Thus a smooth transient process is mandatory. The mechanic is shown in Figure 5-20. By changing the value of k_{slope} shown in Figure 5-20, the cycle time will be changed gradually until it is very close to the output 1 in Figure 5-19. In case of that the error between the two outputs is inside an accepted smaller range, the transient will be carried out. The value of k_{slope} can be modified through human-computer interface, which means that users can be changed the transient speed by giving different values.

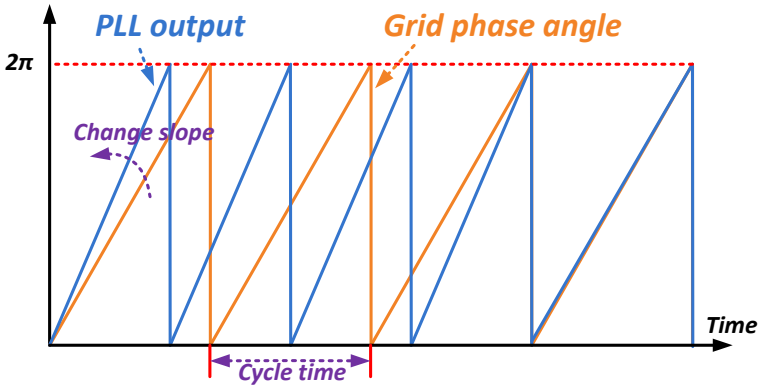


Figure 5-20 Transient mechanics between output 1 and 2 of PLL.

The final performance of the proposed PLL is shown in Fig. 5.21. In the test, the grid frequency is changed from 40Hz to 60Hz. And the frequency range that users define is between 48Hz and 52Hz, which means that if the grid frequency is inside this frequency range, the proposed PLL output will be synchronized with the grid voltage. Otherwise, it will be fixed to 50/60Hz.

In Fig. 5.21(a), when the gird frequency just reaches 48Hz, the PLL starts to track the grid voltage phase angle by changing k_{slope}. Before 4.3s, the error between grid voltage and UPS output voltage begins to decrease until it reaches around zero. And the error will be kept around zero. In Fig. 5.21(b), the grid voltage frequency reach 52Hz. It means that the proposed PLL is required to exit the synchronized condition by modifying k_{slope}.

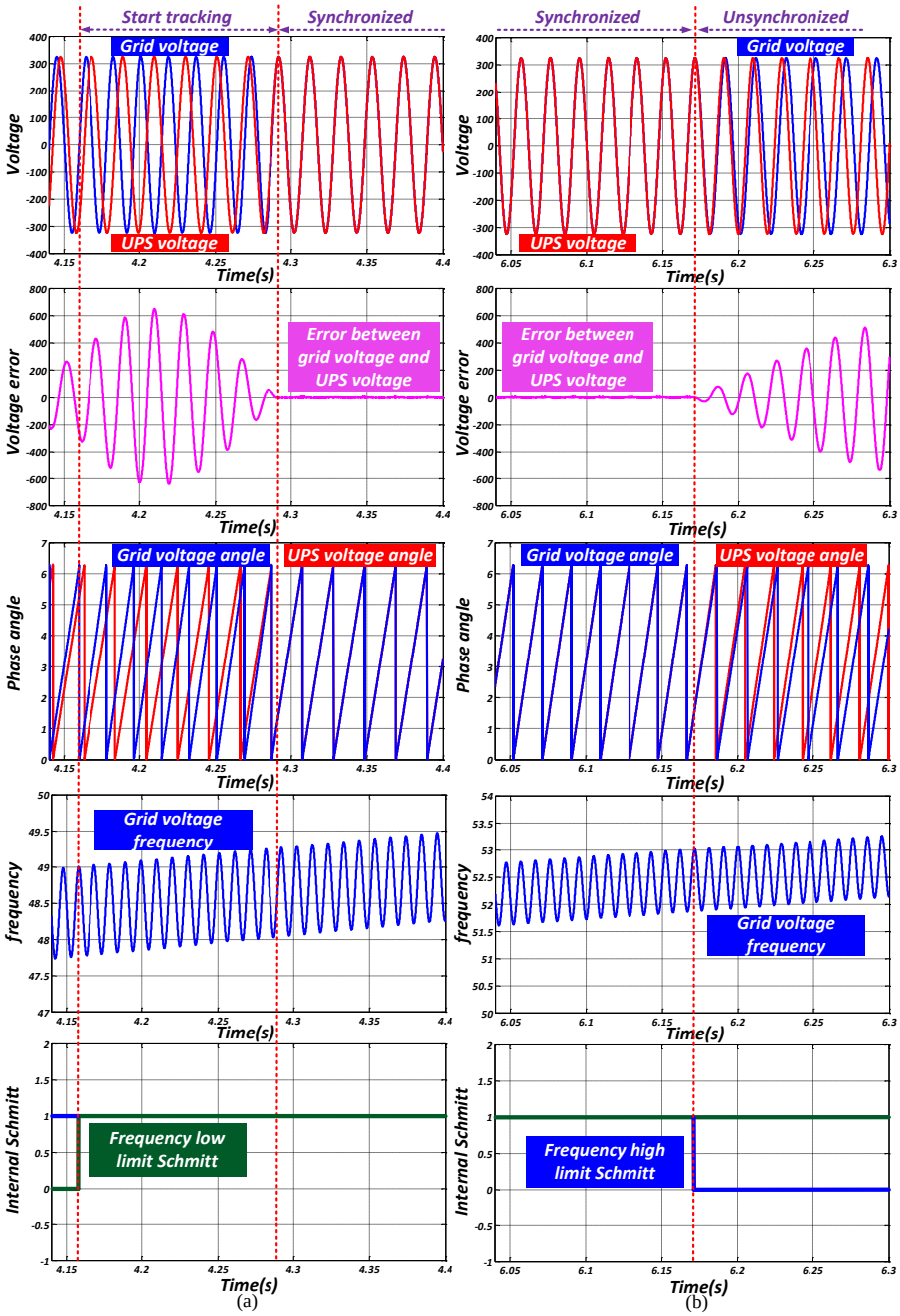


Figure 5-21 Proposed PLL performance. (a) performance from unsynchronized to synchronized condition. (b) performance of exiting synchronized.

5.5. HARDWARE OPERATING CONDITION IMPACT ON PERFORMANCE

Hardware working condition in the power block of the DC/AC module is tightly related with the performance of the DC/AC module, especially power supply part, voltage reference generation part and DSP part.

One of the main reasons that will increase the circuit temperature is the improper design of the circuit. Here a simple example is explained. During the process of the product development, the self-excited phenomenon of operational amplifier is observed. Normally, there are several reasons, namely distributed inductance and capacitance, large feedback factor, driving capacitive load directly and the unstable power supply.

(a) (b)

Figure 5-22 Final prototype of UPS module. (a) UPS module in Leaneco. (b) UPS module in Salicru.

Figure 5-22 shows the prototypes of UPS module in two companies. Figure 5-22 shows the product that has been developed in Leaneco, in which each module is rated as 35kw. This product uses the control methods that have been mentioned in Chapter 2. And in Figure 5-22(b), the prototype for single UPS module in Salicru is presented. Both prototypes use the structure shown in Figure 2.1(b)

In the DSP board in Figure 5-22(b), it is mainly responsible for the digital control, AD and whole system management. The red point marked inside the DSP part is

the point that with extremely high temperature by observing through thermal camera. Its temperature is around 100℃. Its schematic is shown in Figure 5-23. It is a voltage reference generation circuit (3.3V) for the ADC part of DSP. 3.3V is generated through an IC and in order to increase the loading capacity, a voltage follower is used to decrease the output impedance of the whole circuit as much as possible. However, this power supply becomes self-excited when the DC/AC module enters stable working condition since the OP is directly faced with capacitive load. Its improper operating condition increases its own temperature, which also affects the temperature of DSP ADC part consequently.

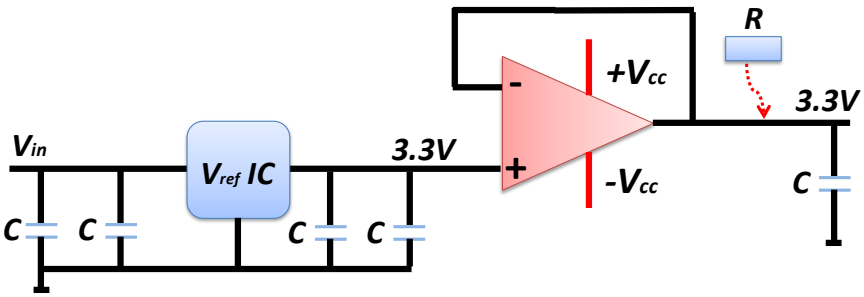
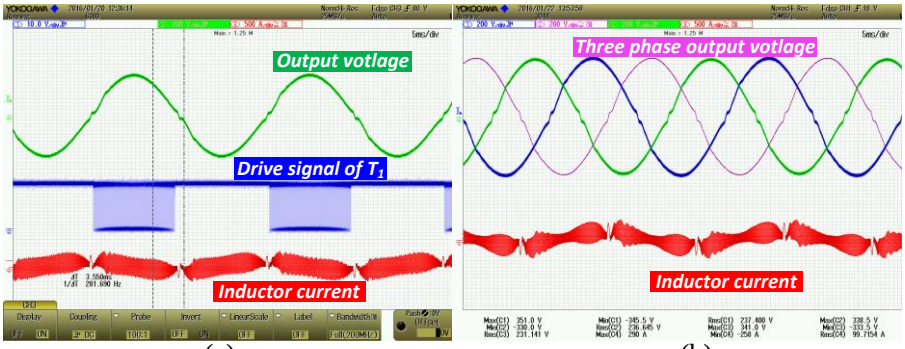


Figure 5-23 Power supply for the ADC part of DSP.

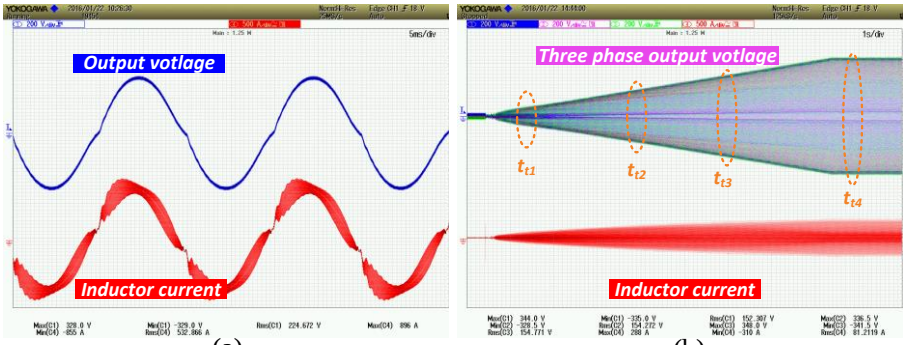
Once self-excited, the output (3.3V) becomes unstable with big voltage ripples. This has negative impact on the ADC results inside the DSP. The voltage and current value that the DSP obtains has oscillation. As a result, the current and voltage starts to have oscillation and ripples as shown in Figure 5-24(a). It can be observed that the inductor current has some small ripples and spikes. The output voltage amplitude doesn't reach the nominal value because if it is increased furthermore, there will be big voltage ripples, which will make the DC/AC module noisy and easy to be tripped to be stopped.



(a) (b)

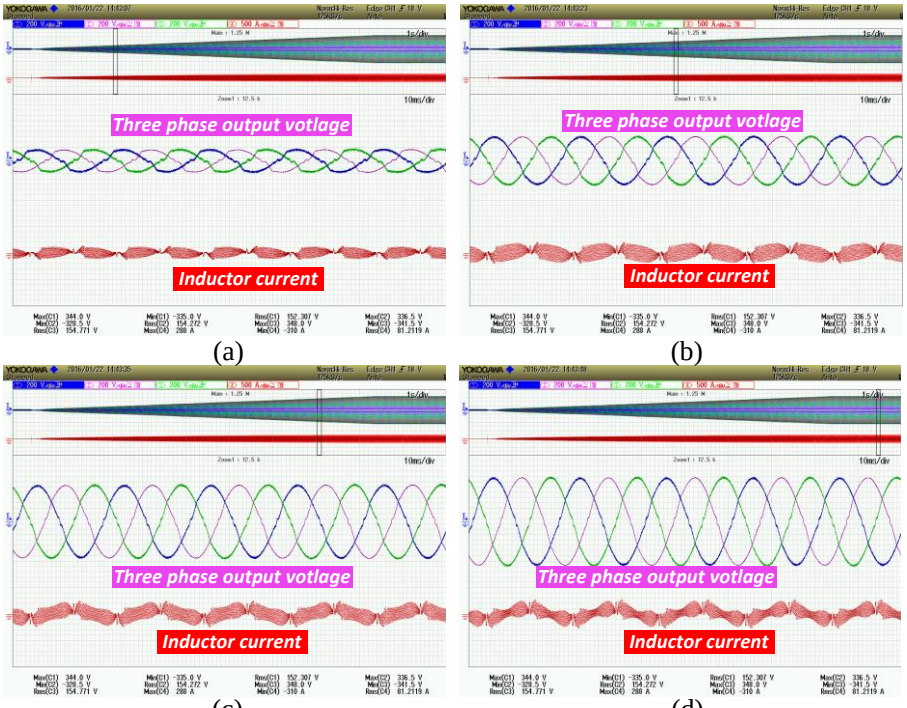
Figure 5-24 Output voltage performance. (a) output voltage in case of self-excited. (b) output voltage after improved.

In order to eliminate the self-excited condition, a resistor (around 15Ω) is inserted between the directly output of OP and the output capacitor. As a result, the circuit enters normal working condition without any oscillation. And the output voltage and inductor current can be controlled in the nominal value without any ripple or oscillation as shown in Figure 5-24(b).



(a) (b)

Figure 5-25 Test performance. (a) full load. (b) soft-start process.



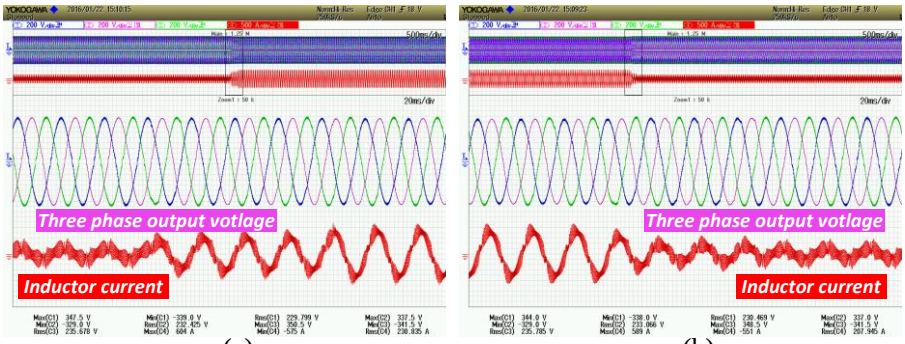
(a) (b)

(c) (d)

Figure 5-26 Soft-start details. (a) details at t_{t1}. (b) details at t_{t2}. (c) details at t_{t3}. (d) details at t_{t4}.

Further test in full load condition and soft-start process were also carried out, which is shown in Figure 5-25. In Figure 5-25(a), it can be seen that the self-excited condition is eliminated and there is no ripple or spikes in the voltage and current. Figure 5-25(b) shows the performance of soft-start and its details is shown in Figure 5-26.

On the other hand, load step test was also carried out as shown in Figure 5-27.



(a) (b)

Figure 5-27 Load step test. (a) load step up. (b) load step down.

5.6. CONCLUSION

In this chapter, some important aspects in the product development are presented. The detailed simulation and experimental results validation are presented.

The conclusion is as follows,

- Digital PR controller implantation should be paid specific attention, especially the discrete integrators.
- Noise issue is an important link for the UPS module performance. Analog filter (passive and active) and digital filter are combined together to eliminate the noise impact. However, the cut-off frequency should be designed carefully. Otherwise, it will affect the compensation for low order harmonics.
- PLL is an important issue for bypass operation of UPS module. It should take the users for into account. It should have the capability of track phase angle in a pre-defined frequency range.
- Proper hardware design is critical. In this chapter, one of the typical example, operational amplifier self-excitation, is presented.

CHAPTER 6. CONCLUSION AND FUTURE WORK

6.1. CONCLUSION

From the thesis, it can be concluded that the modular online UPS system will become more and more relevant since the distributed electrical equipment is bursting nowadays. Thus the control for a modular system is an essential element for the whole system operation. The control should have the capability of simplicity, reliability and flexibility. Considering all these aforementioned issues, the modular system design should be considered in converter topology, control and modeling, converter thermal condition and software-hardware design issues. The detail conclusions are given respectively as follows:

6.1.1. CONVERTER TOPOLOGY

As for the conventional two-level topology, it is more challenging to achieve a flexible, high performance, high power modular UPS system. Multi-level converter is receiving more and more attention. NPC converter, as one of the earliest commercialized three-level converter, is used. Regarding the power level, the single module power rate is increasing in order to have a higher power rate. Thus several cells, such as HB or FB, are used to parallel so that the power rate of a single module can be increased in an easier, faster way. This will consider not only the control of paralleling modules but also the parallel of different cells inside a single module.

6.1.2. CONTROL AND MODELLING

In high power application, several modules are required to work in parallel in order to share the total load power. Each module should bear the load in an equal way. Thus the parallel strategies are the core of the modular system. A proper trade-off should be made between reliability and performance. Since numbers of modules are connected the same AC critical bus at the same time, a monitor should exist to keep an eye on the AC critical bus voltage condition and broadcast orders to different modules. As a result, a multi-level control structure is required. In this control frame work, additional parameters, such as communication delay should be considered in order to design the control. Thus a proper mathematical model should be taken into consideration because it can represent the system in a mathematical way.

6.1.3. THERMAL ANALYSIS

Based on different parallel structure of different modules, different kinds of circulating current may occur among the modules. If the modules share the same AC side and their DC sides are isolated, the circulating current can be suppressed as much as possible by the module parallel control strategies. However, in case of the same DC and AC side, potential zero sequence circulating current will be seen, which will affect the system efficiency and result in an unbalanced loss and temperature distribution condition among the modules. Such kind of circulating current suppression requires additional control strategies, such as zero vector modulating and synchronization. However, these control strategies will affect the modulation of the module, which will change the loss and system temperature distributed condition

6.1.4. SOFTWARE-HARDWARE DESIGN ISSUES

The digital control is a small part of the total code for the product. For real products, human-interface code, protection code, monitor code, etc, that will improve the users experience is highly important. However, the resources of a DSP are limited. Thus while designing the code, efficiency, simplicity are two more critical factors to achieve reliability. As for hardware design, noise reduction issues should be taken into consideration as well as the hardware operating condition. Improper design will affect the control performance in an unpredicted way.

6.2. CONTRIBUTIONS FROM THE AUTHOR'S POINT OF VIEW

6.2.1. CONTROL FRAMEWORK FOR MODULAR ONLINE UPS SYSTEM

Based on the communication methods (CAN bus), a two-level control structure was defined, namely local level and monitor level. Local level is mainly responsible for the single module voltage, current or power regulation while the monitor level mainly aims at regulating the AC critical bus voltage quality and broadcast orders to different modules. And based on the basic concept, the two-level control structure can be simplified and the Plug'n'Play capability can be achieved, which allow the whole system to be more flexible, easier to maintain and more reliable. And based on the IEC 62040-3, the proposed control is tested and evaluated in different aspects.

6.2.2. MATHEMATICAL MODEL ESTABLISHMENT FOR MODULAR ONLINE UPS SYSTEM

Based on the proposed structure, a small signal mathematical model is established in order to analyze the system behavior. Different parameters impact on the system performance was studied through both experimental results and mathematical model, which can be a basic guide for designing such kind of system.

6.2.3. THERMAL ANALYSIS OF CIRCULATING CURRENT

In a modular system, circulating current is one of the most issues that should deserve a specific attention. It has different impact on the loss and temperature performance of different switches in different system structures and control conditions. Thermal analysis was carried out to investigate the circulating current impacts – such as loss and temperature unbalanced distribution, the nonlinearity of thermal performance in some specific load condition.

6.2.4. PRODUCT DEVELOPMENT

Some design issues during the stay in the Salicru S/A, including digital control implementation, PR controller design, modified PLL design, and noise reduction methods, were presented.

6.3. PROPOSALS FOR FUTURE RESEARCH TOPICS

6.3.1. DETAILED MATHEMATICAL MODEL FOR PLUG'N'PLAY OPERATION

- Simplify the mathematical model in order to analyze the system with more modules.
- Modify the mathematical model in order to analyze the dynamic behavior when a random module is ordered to plug in or out of the modular system.
- Improve the mathematical model accuracy in order to match the real system better.

6.3.2. IMPROVED CONTROL FOR PARALLEL SYSTEM

- Use small power rate cascaded H-bridge module to replace single bridge for each phase.
- System interface to MVDC or LVDC based on cascaded H-bridge structure considering capability of expanding the system.
- Consider parallel control based on such kind of highly modularized system.
- Module fault detection methods and solution.
- Experimental validation in respect to feasibility.

6.3.3. THERMAL ANALYSIS

- Detailed thermal model will be used of the cascaded H-bridge module.
- Module failure impact on the thermal stress of each module.
- Parallel failure impact on the thermal stress of each module.
- Improper hardware design, such as ADC, auxiliary power supply, drive circuit and so on, impact on thermal performance of each module.
- Zero sequence circulating current impact on the parallel performance.
- Experimental validation in respect to feasibility.

LITERATURE LIST OF REFERENCES

[1] T. Lee, Y. Wang, J. Li, J.M. Guerrero, "Hybrid Active Filter With Variable Conductance for Harmonic Resonance Suppression in Industrial Power Systems," *IEEE Trans. Ind. Electron.*, vol.62, no.2, pp.746-756, Feb. 2015.

[2] X. Wang, Y. Pang, P. Loh, F. Blaabjerg, "A Series-LC-Filtered Active Damper with Grid Disturbance Rejection for AC Power-Electronics-Based Power Systems," *IEEE Trans. Power Electron.*, vol.30, no.8, pp.4037-4041, Aug. 2015.

[3] Vendor Landscape: Uninterruptible Power Supply (UPS), Gamatronic,

[4] Global UPS Market Forecast & Opportunities, 2019.

[5] S. Karve, "Three of a kind [UPS topologies, IEC standard]," IEE Review, vol.46, no.2, pp.27,31, Mar 2000.

[6] S. Martinez, M. Castro, R. Antoranz, F. Aldana, "Off-line uninterruptible power supply with zero transfer time using integrated magnetics," *IEEE Trans. Ind. Electron.*, vol.36, no.3, pp.441,445, Aug 1989.

[7] H. Kim, T. Yu, S. Choi, "Indirect Current Control Algorithm for Utility Interactive Inverters in Distributed Generation Systems," *IEEE Trans. Power Electron.*, vol.23, no.3, pp.1342, 1347, May 2008.

[8] M. Azpeitia, A. Fernandez, D. Lamar, M. Rodriguez, M. Hernando, "Simplified Voltage-Sag Filler for Line-Interactive Uninterruptible Power Supplies," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.3005,3011, Aug. 2008.

[9] H. Jou, J. Wu, C. Tsai, K. Wu, M. Huang, "Novel line-interactive uninterruptible power supply," *Electric Power Applications, IEE Proceedings* -, vol.151, no.3, pp.359,364, 8 May 2004.

[10] M. Abusara, J.M. Guerrero, S.M. Sharkh, "Line-Interactive UPS for Microgrids," *IEEE Trans. Ind. Electron.*, vol.61, no.3, pp.1292, 1300, March 2014.

[11] C.C. Yeh, M.D. Manjrekar, "A Reconfigurable Uninterruptible Power Supply System for Multiple Power Quality Applications," *IEEE Trans. Power Electron.*, vol.22, no.4, pp.1361,1372, July 2007.

[12] T.J. Liang, J.L. Shyu, "Improved DSP-controlled online UPS system with high real output power," *Electric Power Applications, IEE Proceedings* -, vol.151, no.1, pp.121,127, 9 Jan. 2004.

[13] Z. Zhou, X. Zhang, P. Xu, W. Shen, "Single-Phase Uninterruptible Power Supply Based on Z-Source Inverter," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.2997,3004, Aug. 2008.

[14] G. Sousa, C. Cruz, C. Branco, L. Bezerra, R. Bascopé, "A low cost flyback-based high power factor battery charger for UPS applications," *Power Electronics Conference, 2009. COBEP '09. Brazilian* , vol., no., pp.783,790, Sept. 27 2009-Oct. 1 2009

[15] J. Park, J. Kwon, K. Ho, B. Kwon, "High-Performance Transformerless Online UPS," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.2943,2953, Aug. 2008.

[16] L. Chen, N. Chu, C. Wang, R. Liang, "Design of a Reflex-Based Bidirectional Converter With the Energy Recovery Function," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.3022,3029, Aug. 2008

[17] E. Sato, M. Kinoshita, Y. Yamamoto, T. Amboh, "Redundant High-Density High-Efficiency Double-Conversion Uninterruptible Power System," *IEEE Trans. Ind. Appl.*, vol.46, no.4, pp.1525,1533, July-Aug. 2010.

[18] A. Nasiri, N. Zhong, S. Bekiarov, A. Emadi, "An On-Line UPS System With Power Factor Correction and Electric Isolation Using BIFRED Converter," *IEEE Trans. Ind. Electron.*, vol.55, no.2, pp.722,730, Feb. 2008.

[19] R. Bascope, D. Oliveira, C. Branco, F. Antunes, "A UPS With 110-V/220-V Input Voltage and High-Frequency Transformer Isolation," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.2984,2996, Aug. 2008.

[20] R. Bascope, C. Branco, C. Cruz, E. Oliveira, G. Sousa, "Proposal of a 5kVA single-phase on-line UPS with high frequency isolation and power factor correction," *Power Electronics Conference, 2009. COBEP '09. Brazilian* , vol., no., pp.886,894, Sept. 27 2009-Oct. 1 2009.

[21] B. Chen, Y. Lai, "New Digital-Controlled Technique for Battery Charger With Constant Current and Voltage Control Without Current Feedback," *IEEE Trans. Ind. Electron.*, vol.59, no.3, pp.1545,1553, March 2012.

[22] B. Zhao, Q. Song, W. Liu, Y. Xiao, "Next-Generation Multi-Functional Modular Intelligent UPS System for Smart Grid," *IEEE Trans. Ind. Electron.*, vol.60, no.9, pp.3602,3618, Sept. 2013.

[23] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodriguez, M. Perez, J.I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol.57, no.8, pp.2553,2580, Aug. 2010.

[24] O.S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Medium voltage three-level converters for the grid connection of a multi-MW wind turbine," *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on* , vol., no., pp.1,8, 8-10 Sept. 2009.

[25] J. Holtz, N. Oikonomou, "Optimal Control of a Dual Three-Level Inverter System for Medium-Voltage Drives," *IEEE Trans. Ind. Appl.*, vol.46, no.3, pp.1034,1041, May-june 2010.

[26] J. S. Lee, K. B. Lee and F. Blaabjerg, "Open-Switch Fault Detection Method of a Back-to-Back Converter Using NPC Topology for Wind Turbine Systems," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 325-335, Jan.-Feb. 2015.

[27] M. Sharifzadeh, H. Vahedi, A. Sheikholeslami, P. A. Labbé and K. Al-Haddad, "Hybrid SHM–SHE Modulation Technique for a Four-Leg NPC Inverter With DC Capacitor Self-Voltage Balancing," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4890-4899, Aug. 2015.

[28] Zhang Xueguang, Chen Jiaming, Ma Yan, Wang Yijie and Xu Dianguo, "Bandwidth Expansion Method for Circulating Current Control in Parallel Three-phase PWM Converter Connection System," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6847-6856, Dec. 2014.

[29] M. Narimani and G. Moschopoulos, "Three-Phase Multimodule VSIs Using SHE-PWM to Reduce Zero-Sequence Circulating Current," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1659-1668, April 2014.

[30] J. C. Le Claire and G. Le Borgne, "Double boost effect topology for AC/DC converter with unity power factor," in *Proc. PESC*, 2008. IEEE, Rhodes, 2008, pp. 3199-3205.

[31] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain and A. Bakhshai, "A ZVS Interleaved Boost AC/DC Converter Used in Plug-in Electric Vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3513-3529, Aug. 2012.

[32] Uninterruptible power system (UPS) – Part 3: Method of specifying the performance and test requirements.

[33] AP. Martins, AS. Carvalho, AS. Araujo, "Design and implementation of a current controller for the parallel operation of standard UPSs," in *Proc. IECON*, 1995, vol.1, no., pp.584,589 vol.1, 6-10 Nov 1995.

[34] T. Iwade, S. Komiyama, Y. Tanimura, M. Yamanaka, M. Sakane, K. Hirachi, "A novel small-scale UPS using a parallel redundant operation system," Telecommunications Energy Conference, 2003. INTELEC '03. The 25th International, vol., no., pp.480, 484, 23-23 Oct. 2003.

[35] J.M. Guerrero, L.J. Hang, J. Uceda, "Control of Distributed Uninterruptible Power Supply Systems," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.2845,2859, Aug. 2008.

[36] J. Holtz, W. Lotzkat, K. H. Werner, "A high-power multitransistor-inverter uninterruptable power supply system," *IEEE Trans. Power Electron.*, vol.3, no.3, pp.278,285, July 1988.

[37] Y. Pei, G. Jiang, X. Yang, Z. Wang, "Auto-master-slave control technique of parallel inverters in distributed AC power systems and UPS," in *Proc. PESC*, 2004, vol.3, no., pp.2050, 2053 Vol.3, 20-25 June 2004.

[38] J.F. Chen, C.L. Chu, "Combination voltage-controlled and current-controlled PWM inverters for UPS parallel operation," *IEEE Trans. Power Electron.*, vol.10, no.5, pp.547, 558, Sep 1995.

[39] Y.J. Cheng, E.K.K. Sng, "A novel communication strategy for decentralized control of paralleled multi-inverter systems," *IEEE Trans. Power Electron.*, vol.21, no.1, pp.148, 156, Jan. 2006.

[40] X. Sun, Y.S. Lee, D. Xu, "Modeling, analysis, and implementation of parallel multi-inverter systems with instantaneous average-current-sharing scheme," *IEEE Trans. Power Electron.*, vol.18, no.3, pp.844,856, May 2003.

[41] Y.K. Cheng, T.F. Wu, Y.E. Wu, C.P. Ku, "A current-sharing control strategy for paralleled multi-inverter systems using microprocessor-based robust control," TENCON 2001. Proceedings of IEEE Region 10 International Conference on Electrical and Electronic Technology, vol.2, no., pp.647, 653, vol.2, 2001.

[42] H.M. Hsieh, T.F. Wu, Y.E. Wu, H.S. Nien, Y.E. Wu, "A compensation strategy for parallel inverters to achieve precise weighting current distribution," Industry Applications Conference, 2005. Fourtieth IAS

Annual Meeting. Conference Record of the 2005, vol.2, no., pp.954, 960 Vol. 2, 2-6 Oct. 2005.

[43] Z. Liu, J. Liu, H. Wang, "Output impedance modeling and stability criterion for parallel inverters with average load sharing scheme in AC distributed power system," in *Proc. APEC,* 2012, vol., no., pp.1921,1926, 5-9 Feb. 2012.

[44] X. Sun, L.K. Wong, Y.S. Lee, D. Xu, "Design and analysis of an optimal controller for parallel multi-inverter systems," *Circuits and Systems II: Express Briefs, IEEE Transactions on, vol*.53, no.1, pp.56,61, Jan. 2006.

[45] Z. He, Y. Xing, "Distributed Control for UPS Modules in Parallel Operation With RMS Voltage Regulation," *IEEE Trans. Ind. Electron.*, vol.55, no.8, pp.2860, 2869, Aug. 2008.

[46] T.F. Wu, Y.K. Chen, Y.H. Huang, "3C strategy for inverters in parallel operation achieving an equal current distribution," *IEEE Trans. Ind. Electron.*, vol.47, no.2, pp.273, 281, Apr 2000.

[47] S. J. Chiang, C.H. Lin, C. Y. Yen, "Current limitation control technique for parallel operation of UPS inverters," in *Proc. PESC,* 2004, vol.3, no., pp.1922, 1926 Vol.3, 20-25 June 2004.

[48] K. De Brabandere, B. Bolsens, J. Van den Keybus, A. Woyte, J. Driesen and R. Belmans, "A Voltage and Frequency Droop Control Method for Parallel Inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1107-1115, July 2007.

[49] S. K. Mishra, "Design-Oriented Analysis of Modern Active Droop-Controlled Power Supplies," *IEEE Trans. Ind. Electron.*, vol. 56, no. 9, pp. 3704-3708, Sept. 2009.

[50] E. Barklund, N. Pogaku, M. Prodanovic, C. Hernandez-Aramburo and T. C. Green, "Energy Management in Autonomous Microgrid Using Stability-Constrained Droop Control of Inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2346-2352, Sept. 2008.

[51] M. N. Arafat, A. Elrayyah and Y. Sozer, "An Effective Smooth Transition Control Strategy Using Droop-Based Synchronization for Parallel Inverters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 3, pp. 2443-2454, May-June 2015.

[52] G. Xu, D. Sha and X. Liao, "Decentralized Inverse-Droop Control for Input-Series–Output-Parallel DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4621-4625, Sept. 2015.

[53] A. P. N. Tahim, D. J. Pagano, E. Lenz and V. Stramosk, "Modeling and Stability Analysis of Islanded DC Microgrids Under Droop Control," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4597-4607, Aug. 2015.

[54] H. Han, Y. Liu, Y. Sun, M. Su and J. M. Guerrero, "An Improved Droop Control Strategy for Reactive Power Sharing in Islanded Microgrid," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3133-3141, June 2015.

[55] J. C. Vasquez, J. M. Guerrero, A. Luna, P. Rodriguez and R. Teodorescu, "Adaptive Droop Control Applied to Voltage-Source Inverters Operating in Grid-Connected and Islanded Modes," *IEEE Trans. Ind. Electron.*, vol. 56, no. 10, pp. 4088-4096, Oct. 2009.

[56] T. L. Vandoorn, B. Meersman, J. D. M. De Kooning and L. Vandevelde, "Transition From Islanded to Grid-Connected Mode of Microgrids With Voltage-Based Droop Control," *IEEE Trans. Power Sys.*, vol. 28, no. 3, pp. 2545-2553, Aug. 2013.

[57] V. Mariani, F. Vasca, J. C. Vásquez and J. M. Guerrero, "Model Order Reductions for Stability Analysis of Islanded Microgrids With Droop Control," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4344-4354, July 2015.

[58] R. Majumder, B. Chaudhuri, A. Ghosh, R. Majumder, G. Ledwich and F. Zare, "Improvement of Stability and Load Sharing in an Autonomous Microgrid Using Supplementary Droop Control Loop," *IEEE Trans. Power Sys.*, vol. 25, no. 2, pp. 796-808, May 2010.

[59] Jia Liu, Y. Miura and T. Ise, "Comparison of Dynamic Characteristics Between Virtual Synchronous Generator and Droop Control in Inverter-Based Distributed Generators," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3600-3611, May 2016.

[60] J. Guerrero, J. Matas, L. García De Vicuña, M. Castilla and J. Miret, "Decentralized Control for Parallel Operation of Distributed Generation Inverters Using Resistive Output Impedance," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 994-1004, April 2007.

[61] J. M. Guerrero, Luis Garcia de Vicuna, J. Matas, M. Castilla and J. Miret, "Output Impedance Design of Parallel-Connected UPS Inverters With Wireless Load-Sharing Control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126-1135, Aug. 2005.

[62] Y. W. Li and C. N. Kao, "An Accurate Power Control Strategy for Power-Electronics-Interfaced Distributed Generation Units Operating in a Low-Voltage Multibus Microgrid," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2977-2988, Dec. 2009.

[63] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," in IEEE Transactions on Industrial Electronics, vol. 58, no. 1, pp. 158-172, Jan. 2011.

[64] T. Dragičević, J. M. Guerrero, J. C. Vasquez and D. Škrlec, "Supervisory Control of an Adaptive-Droop Regulated DC Microgrid With Battery Management Capability," *IEEE Trans. Ind. Electron.*, vol. 29, no. 2, pp. 695-706, Feb. 2014.

[65] J. Xiao, P. Wang and L. Setyawan, "Hierarchical Control of Hybrid Energy Storage System in DC Microgrids," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4915-4924, Aug. 2015.

[66] Xiaonan Lu, J. M. Guerrero, Kai Sun, J. C. Vasquez, R. Teodorescu and Lipei Huang, "Hierarchical Control of Parallel AC-DC Converter Interfaces for Hybrid Microgrids," *IEEE Trans. Smart. Grid*, vol. 5, no. 2, pp. 683-692, March 2014.

[67] A. Milczarek, M. Malinowski and J. M. Guerrero, "Reactive Power Management in Islanded Microgrid—Proportional Power Sharing in

Hierarchical Droop Control," *IEEE Trans. Smart. Grid*, vol. 6, no. 4, pp. 1631-1638, July 2015.

[68] C. Gavriluta, I. Candela, A. Luna, A. Gomez-Exposito and P. Rodriguez, "Hierarchical Control of HV-MTDC Systems With Droop-Based Primary and OPF-Based Secondary," *IEEE Trans. Smart. Grid*, vol. 6, no. 3, pp. 1502-1510, May 2015.

[69] Xin Zhao et al., "Negative sequence droop method based hierarchical control for low voltage ride-through in grid-interactive microgrids," in *Proc. ECCE*, 2015, pp. 6896-6903.

[70] Wang Haiyun et al., "A hierarchical control of microgrid based on droop controlled voltage source converter," in *Proc, PES*, Asia-Pacific, Kowloon, 2013, pp. 1-4.

[71] J. M. Guerrero, J. C. Vásquez and R. Teodorescu, "Hierarchical control of droop-controlled DC and AC microgrids — a general approach towards standardization," in *Proc. IECON*, 2009, pp. 4305-4310.

[72] A. Micallef, M. Apap, C. Spiteri-Staines, J. M. Guerrero and J. C. Vasquez, "Reactive Power Sharing and Voltage Harmonic Distortion Compensation of Droop Controlled Single Phase Islanded Microgrids," *IEEE Trans. Smart. Grid*, vol. 5, no. 3, pp. 1149-1158, May 2014.

[73] X. Lu, J. M. Guerrero, K. Sun and J. C. Vasquez, "An Improved Droop Control Method for DC Microgrids Based on Low Bandwidth Communication With DC Bus Voltage Restoration and Enhanced Current Sharing Accuracy," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1800-1812, April 2014.

[74] F. Guo, C. Wen, J. Mao and Y. D. Song, "Distributed Secondary Voltage and Frequency Restoration Control of Droop-Controlled Inverter-Based Microgrids," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4355-4364, July 2015.

[75] Y. Gu, W. Li and X. He, "Frequency-Coordinating Virtual Impedance for Autonomous Power Management of DC Microgrid," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2328-2337, April 2015.

[76] J. Matas, M. Castilla, L. G. d. Vicuña, J. Miret and J. C. Vasquez, "Virtual Impedance Loop for Droop-Controlled Single-Phase Parallel Inverters Using a Second-Order General-Integrator Scheme," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2993-3002, Dec. 2010.

[77] J. He, Y. W. Li, J. M. Guerrero, F. Blaabjerg and J. C. Vasquez, "An Islanding Microgrid Power Sharing Approach Using Enhanced Virtual Impedance Control Scheme," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5272-5282, Nov. 2013.

[78] J. He and Y. W. Li, "Generalized Closed-Loop Control Schemes with Embedded Virtual Impedances for Voltage Source Converters with LC or LCL Filters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1850-1861, April 2012.

[79] X. Wang, Y. W. Li, F. Blaabjerg and P. C. Loh, "Virtual-Impedance-Based Control for Voltage-Source and Current-Source Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7019-7037, Dec. 2015.

[80] J. He and Y. W. Li, "Analysis, Design, and Implementation of Virtual Impedance for Power Electronics Interfaced Distributed Generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2525-2538, Nov.-Dec. 2011.

[81] S. Li, X. Wang, Z. Yao, T. Li, Z. Peng, "Circulating Current Suppressing Strategy for MMC-HVDC Based on Nonideal Proportional Resonant Controllers Under Unbalanced Grid Conditions," *IEEE Trans. Power Electron.*, vol.30, no.1, pp.387-397, Jan. 2015.

[82] A. Kuperman, "Proportional-Resonant Current Controllers Design Based on Desired Transient Performance," *IEEE Trans. Power Electron.*, vol.30, no.10, pp.5341-5345, Oct. 2015.

[83] A. Kuperman, "Proportional-Resonant Current Controllers Design Based on Desired Transient Performance," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5341-5345, Oct. 2015.

[84] A. Hasanzadeh, O. C. Onar, H. Mokhtari and A. Khaligh, "A Proportional-Resonant Controller-Based Wireless Control Strategy With a Reduced Number of Sensors for Parallel-Operated UPSs," *IEEE Trans. Power Delivery*, vol. 25, no. 1, pp. 468-478, Jan. 2010.

[85] C. Xia, Z. Wang, T. Shi and X. He, "An Improved Control Strategy of Triple Line-Voltage Cascaded Voltage Source Converter Based on Proportional–Resonant Controller," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2894-2908, July 2013.

[86] B. Singh, K. Al-Haddad and A. Chandra, "A review of active filters for power quality improvement," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 960-971, Oct 1999.

[87] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1312-1322, Nov/Dec 1996.

[88] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[89] M. Liserre, F. Blaabjerg and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281-1291, Sept.-Oct. 2005.

[90] H. Fujita and H. Akagi, "The unified power quality conditioner: the integration of series and shunt-active filters," *IEEE Trans. Power Electron.*, vol. 13, no. 2, pp. 315-322, Mar 1998.

[91] F. Z. Peng, H. Akagi and A. Nabae, "A new approach to harmonic compensation in power systems-a combined system of shunt passive and series active filters," *IEEE Trans. Ind. Appl.*, vol. 26, no. 6, pp. 983-990, Nov/Dec 1990.

[92] H. Akagi, "Trends in active power line conditioners," *IEEE Trans. Power Electron.*, vol. 9, no. 3, pp. 263-268, May 1994.

[93] H. Fujita and H. Akagi, "A practical approach to harmonic compensation in power systems-series connection of passive and active filters," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1020-1025, Nov/Dec 1991.

[94] Fang Zheng Peng, "Application issues of active power filters," *IEEE Industry Applications Magazine*, vol. 4, no. 5, pp. 21-30, Sep/Oct 1998.

[95] K. Ma, M. Liserre, F. Blaabjerg and T. Kerekes, "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 590-602, Feb. 2015.

[96] K. Ma; N. He; M. Liserre; F. Blaabjerg, "Frequency-Domain Thermal Modelling and Characterization of Power Semiconductor Devices," *IEEE Trans. Power Electron.*, vol.PP, no.99, pp.1-1.

[97] K. Ma, A. S. Bahman, S. Beczkowski and F. Blaabjerg, "Complete Loss and Thermal Model of Power Semiconductors Including Device Rating Information," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2556-2569, May 2015.

[98] K. Ma, F. Blaabjerg and M. Liserre, "Thermal Analysis of Multilevel Grid-Side Converters for 10-MW Wind Turbines Under Low-Voltage Ride Through," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 909-921, March-April 2013.

[99] ABB Application Note: Applying IGBTs, May 2007.

[100] W. Lixiang, J. McGuire, R.A. Lukaszewski, "Analysis of PWM frequency control to improve the lifetime of PWM inverter," in *Proc. ECCE*, 2009. IEEE , vol., no., pp.900,907, 20-24 Sept. 2009.

[101] ABB Hipak, IGBT Module 5SND 0800M170100, Apr 2014.

[102] SG Series UPS 10-600kVA three phase 400Vac with ultra-high efficiency eBoostTM technology, GE.

[103] Y. Zhihong, D. Boroyevich, C. Jae-Young, F.C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," *IEEE Trans. Power Electron.*, vol.17, no.5, pp.609,615, Sep 2002.

[104] T. Kawabata, S. Higashino, "Parallel operation of voltage source inverters," *IEEE Trans. Ind. Appl.*, vol.24, no.2, pp.281,287, Mar/Apr 1988.

[105] J.W. Dixon, B.T. Ooi, "Series and parallel operation of hysteresis current-controlled PWM rectifiers," *IEEE Trans. Ind. Appl.*, vol.25, no.4, pp.644, 651, July-Aug. 1989.

[106] Y. Komatsuzaki, "Cross current control for parallel operating three phase inverter," in *Proc. PESC*, 1994, vol., no., pp.943,950 vol.2, 20-25 Jun 1994.

[107] K. Matsui, Y. Murai, M. Watanabe, M. Kaneko, F. Ueda, "A pulsewidth-modulated inverter with parallel connected transistors using current-sharing reactors," *IEEE Trans. Power Electron.*, vol.8, no.2, pp.186,191, Apr 1993.

[108] Y. Sato, T. Kataoka, "Simplified control strategy to improve AC-input-current waveform of parallel-connected current-type PWM rectifiers," in *Proc. EPA*, 1995, vol.142, no.4, pp.246, 254, Jul 1995.

[109] S. Ogasawara, J. Takagaki, H. Akagi, A. Nabae, "A novel control scheme of a parallel current-controlled PWM inverter," *IEEE Trans. Ind. Appl.*, vol.28, no.5, pp.1023,1030, Sep/Oct 1992.

[110] L. Matakas, W. Kaiser, "Low harmonics, decoupled histeresis type current control of a multiconverter consisting of a parallel transformerless

connection of VSC converters," in *Proc. IAC*, 1997, vol.2, no., pp.1633,1640 vol.2, 5-9 Oct 1997.

[111] S. Fukuda, K. Matsushita, "A control method for parallel-connected multiple inverter systems," in *Proc. PEVSDP*, 1998, vol., no., pp.175, 180, 21-23 Sep 1998.

[112] R. Abe, Y. Nagai, K. Tsuyuki, H. Nishikawa, T. Shimamura, A. Kawaguchi, K. Shimada, "Development of multiple space vector control for direct connected parallel current source power converters," in *Proc. Power Conversion Conference*, vol.1, no., pp.283,288 vol.1, 3-6 Aug 1997.

[113] C. Pan, Y. Liao, "Modeling and Coordinate Control of Circulating Currents in Parallel Three-Phase Boost Rectifiers," *IEEE Trans. Ind. Electron.*, vol.54, no.2, pp.825, 838, April 2007.

[114] Z. Shao, X. Zhang, F. Wang, R. Cao, "Modeling and Elimination of Zero-Sequence Circulating Currents in Parallel Three-Level T-Type Grid-Connected Inverters," *IEEE Trans. Power Electron.*, vol.30, no.2, pp.1050,1063, Feb. 2015.

[115] D. Zhang, F. Fred Wang, R. Burgos and D. Boroyevich, "Common-Mode Circulating Current Control of Paralleled Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3925-3935, Dec. 2011.

[116] Z. Ye, P. K. Jain and P. C. Sen, "Circulating Current Minimization in High-Frequency AC Power Distribution Architecture With Multiple Inverter Modules Operated in Parallel," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2673-2687, Oct. 2007.

[117] C. T. Pan and Y. H. Liao, "Modeling and Coordinate Control of Circulating Currents in Parallel Three-Phase Boost Rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 825-838, April 2007.

[118] Yi-Hung Liao, Hung-Chi Chen, Hsiu-Che Cheng, Yu-Lung Ke and Yi-Ta Li, "A Novel Control Strategy of Circulating Currents in Paralleled Single-Phase Boost Converters With Different Power Sharing for Microgrid Applications," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1304-1312, March-April 2014.

[119] Xiaoqian Li, Qiang Song, Wenhua Liu, Shukai Xu, Zhe Zhu and Xiaolin Li, "Performance Analysis and Optimization of Circulating Current Control for Modular Multilevel Converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 716-727, Feb. 2016.

[120] T. P. Chen, "Circulating zero-sequence current control of parallel three-phase inverters," in *Proc, EPA*, 2006, vol. 153, no. 2, pp. 282-288.

[121] T. P. Chen, "Zero-Sequence Circulating Current Reduction Method for Parallel HEPWM Inverters Between AC Bus and DC Bus," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 290-300, Jan. 2012.

[122] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres and A. F. Souza, "Comparison of Three Single-Phase PLL Algorithms for UPS Applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923-2932, Aug. 2008.

APPENDICES

Appendix A. Experimental setup

The proposed control strategies are validated on a downscale parallel system controlled by a real-time control and monitoring platform in Microgrid Research Laboratories at the Department of Energy Technology, Aalborg University, as shown in Figure A1-1 and Figure A1-2, whose parameters are presented in Table A1-1.

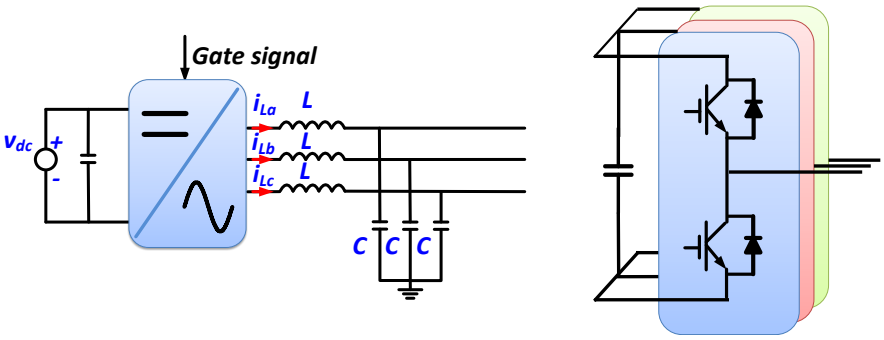


Figure A1-1 Experimental setup diagram.

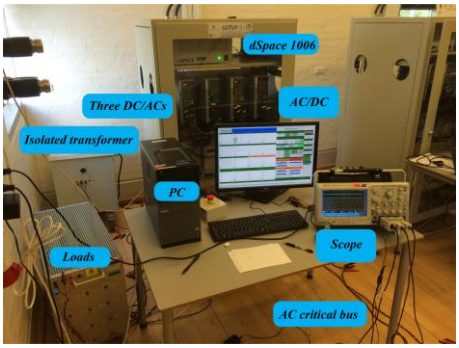


Figure A1-2 Photo of the whole system.

Table A1-1. Experimental setup parameters

DC voltage	*700V*	*Filter capacitance*	*27μF*
Switch frequency	*10kHz*	*DC/AC power rate*	*2.2kw*
Fundamental frequency	*50Hz*		
Filter inductance	*1.8mH*		

Appendix B. Control parameters

Control parameters:

Table B1-1. Control parameters for DC/AC module.

Voltage loop proportional term, k_{pv}	*0.55*	*Current loop resonant (50Hz) term, k_{rc}*	*150*
Voltage loop resonant term (50Hz), k_{rv}	*70*	*Current loop resonant (5^{th}, 7^{th}) term, k_{5rc}, k_{7rc}*	*30,30*
Voltage loop resonant (5^{th}, 7^{th}) term, k_{5rv}, k_{7rv}	*100,100*	*Virtual impedance, R_{vir}*	*2*
Current loop proportional term, k_{pc}	*1.2*	*Phase control coefficient, k_{ph}*	*0.0001*

Table B1-2. Control parameters for APF module.

DC voltage proportional term, k_{pv_apf}	*0.1*	*Reactive power proportional term*	*0.01*
DC voltage integral term, k_{iv_apf}	*750*	*Reactive power integral term*	*0.1*
Current proportional term, k_{pi_apf}	*55*		
Current integral term, k_{ii_apf}	*2360*		

Table B1-3. Control parameters for voltage amplitude recovery and phase regulation.

Voltage amplitude proportional term, k_{pv_sec}	*2.5*	*Phase regulation proportional term, $k_{p\theta\_sec}$*	*0.2*
Voltage amplitude integral term, k_{iv_sec}	*20.5*	*Phase regulation integral term, $k_{i\theta\_sec}$*	*9*

PART II THESIS REPORT SUPPORT PUBLICATIONS

Journal Paper:

[A1] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez, C. Seniger, "Modular Plug'n'Play Control Architectures for Three-phase Inverters in UPS Applications," *IEEE Trans. Ind. Appl.*, vol. PP, no.99, pp.1-1.

[A2] **Chi Zhang**, E. Coelho, J. Guerrero; J. C. Vasquez, "Modular Online Uninterruptible Power System Plug'n'Play Control and Stability Analysis," *IEEE Trans. Ind. Electron*, vol. PP, no.99, pp.1-1.

[A3] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez and E. A. A. Coelho, "Control Architecture for Parallel-Connected Inverters in Uninterruptible Power Systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5176-5188, July 2016.

Conference Paper:

[A4] **Chi Zhang**, J. M. Guerrero and J. C. Vasquez, "A simplified control architecture for three-phase inverters in modular UPS application with shunt active power filter embedded," in *Proc. of ICPE-ECCE Asia*, Seoul, 2015, pp. 413-420.

[A5] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez, E. A. Coelho and C. Seniger, "High-performance control of paralleled three-phase inverters for residential microgrid architectures based on online uninterruptable power systems," in *Proc. of APEC*, Charlotte, NC, 2015, pp. 3232-3239.

[A6] **Chi Zhang**, J. M. Guerrero, J. C. Vasquez and C. Seniger, "Modular Plug'n'Play control architectures for three-phase inverters in UPS applications," in *Proc. of ICPE-ECCE Asia*, Seoul, 2015, pp. 659-666.

[A7] **Chi Zhang**, J. M. Guerrero and J. C. Vasquez, "Thermal impact analysis of circulating current in high power modular online uninterruptible power supplies application," in *Proc. of EPE'15 ECCE-Europe*, Geneva, 2015, pp. 1-10.

[A8] **Chi Zhang**, T. Dragicevic, J. C. Vasquez and J. M. Guerrero, "Resonance damping techniques for grid-connected voltage source converters with LCL filters — A review," in *Proc. of Energy Conference (ENERGYCON)*, Cavtat, 2014, pp. 169-176.

PUBLICATION A1

(Journal paper)

Modular Plug'n'Play Control Architectures for Three-phase Inverters in UPS Applications

Chi Zhang, Josep M. Guerrero, Juan C. Vasquez, and Carsten Seniger

The paper has been published in the
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PUBLICATION A2

(Journal paper)

Modular Online Uninterruptible Power System Plug'n'Play Control and Stability Analysis

Chi Zhang, Ernane A.A. Coelho, Josep M. Guerrero, and Juan C. Vasquez

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PUBLICATION A3

(Journal paper)

Control Architecture for Parallel-Connected Inverters in Uninterruptible Power Systems

Chi Zhang, Josep M. Guerrero, Juan C. Vasquez, and Ernane A.A. Coelho

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DOI: 10.1109/TPEL.2015.2481480

PUBLICATION A4

(Conference paper)

A simplified control architecture for three-phase inverters in modular UPS application with shunt active power filter embedded

Chi Zhang, Josep M. Guerrero, and Juan C. Vasquez

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PUBLICATION A5

(Conference paper)

High-performance control of paralleled three-phase inverters for residential microgrid architectures based on online uninterruptable power systems

Chi Zhang, Josep M. Guerrero, Juan C. Vasquez, Ernane A.A. Coelho, and Carsten Seniger

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(Conference paper)

Modular Plug'n'Play control architectures for three-phase inverters in UPS applications

Chi Zhang, Josep M. Guerrero, Juan C. Vasquez, and Carsten Seniger

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PUBLICATION A7

(Conference paper)

Thermal impact analysis of circulating current in high power modular online uninterruptible power supplies application

Chi Zhang, Josep M. Guerrero, and Juan C. Vasquez

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PUBLICATION A8

(Conference paper)

Resonance damping techniques for grid-connected voltage source converters with LCL filters — A review

Chi Zhang, Tomislav Dragicevic, Juan C. Vasquez, and Josep M. Guerrero

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