Measurement, Modeling and Suppression of Substrate Noise in Wide Band Mixed-signal ICs

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Measurement, Modeling, and Suppression of Substrate Noise in Wide Band Mixed-Signal ICs

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Abstract

Ultra-Wideband (UWB) technology is expected to become one of the key main-stream communication platforms for the coming decades. At the same time, the demand for low-cost and compact implementations of wireless systems makes Complementary Metal-Oxide Semiconductor (CMOS) one of the most promising technologies for the development of such single chip UWB systems. However, UWB systems are sensitive to noise owing to the ultra wideband nature and low power spectral density of the signal. Using CMOS to implement UWB systems makes the situation even worse as it brings along another noise issue, substrate noise. To solve this problem, the substrate noise has to be characterized and subsequently efficient strategies for cancellation/suppression have to be developed. The main goal of this research work is to study substrate noise related issues in mixed-signal integrated circuits, focusing on ultra wide band (UWB) systems, and to find mitigating solutions for those issues.

To provide reliable measurement results for the validation of proposed models and noise suppression techniques, a measurement method suitable for measuring wide band substrate noise is proposed. The method relies on a passive fixture based on ohmic contacts and a layout that makes it suitable for on-wafer measurement using ground-signal-ground probes. The parasitic components affecting the measurement are investigated by EM simulations and measurements. Test chips are designed using a 0.18 μm lightly doped CMOS process to evaluate the performance of the fixture. Several practical design rules for reducing the parasitical effects are concluded based on measurement results.

An experimental impact evaluation of substrate noise on an UWB LNA has been conducted, aiming to find out the mechanism by which the substrate noise affects the UWB sensitive circuits. The measured results reveal the significant performance (noise figure) deterioration of the UWB LNA due to substrate noise issues.

A novel analytical model for the switching noise generated by individual inverters is proposed. Based on the proposed model, the spectrum envelope of the substrate noise can be predicted in the early design stage. This has been verified by the measured results from a test chip implemented using a standard 0.18 μm CMOS process. In addition, statistical methods have

been used to analyze the noise features of large scale digital blocks. The random switching activities of digital circuits leads to variable time delays and amplitude fluctuations of substrate noise, which can be equivalently modeled as multi-path fading. Therefore, the frequency selective feature of the substrate noise is modeled using the propagating delay of the digital circuits. MATLAB and SPICE simulation results have shown supports for this.

In the analysis of suppression methods both active and passive strategies are considered. Based on the substrate noise model developed in this work a novel active noise suppression technique is proposed. In this technique, an active spectrum shaping section is used to generate extra switching currents to modify the shape of the original switching noise in both time and frequency domain. The relative time delays of these switching currents to the original switching current are realized by controllable delay lines. The pulse widths and magnitudes of the switching currents are also controllable. By manipulating the extra switching currents, the spectrum of the total switching noise can be shaped to have a suppressed magnitude at desired frequencies.

In addition, analytical modeling of guard rings for substrate noise isolation in lightly doped substrates is presented. A resistive T-network is proposed to characterize the aggressor-guard ring-victim layout, and closed form expressions for the calculation of spreading resistances in the network are presented. Using this model the effects of the layout parameters can be taken into account during the pre-layout design phase, and the isolation performance of the design can be accurately predicted.

Preface

This dissertation is submitted to the Faculty of Engineering, Science and Medicine at Aalborg University in partial fulfillment of the requirements for the PhD degree. The work was carried out in the Technology Platforms Section (TPS), Department of Electronic Systems, Aalborg University.

The PhD work documented in this thesis represents the principal part of a research project "On-Chip Noise Coupling Issues for High Sensitivity, Short Range Ultra-Wide Band Communication System Implementations in Standard CMOS Technology" supported by the Danish Research Council for Technology and Production Sciences under the Grant 274-05-0491. The main goal of the project is to devise a strategy for dealing with substrate carried background noise in ultra-wideband systems. This goal is further broken into four research tasks: (1) measurement, (2) impact evaluation, (3) modeling and (4) suppression of substrate noise. During this work scientific contributions have been achieved in each of the four aspects. Here the author would like to emphasize three of them while a complete list of the scientific contributions is provided in conclusion. Firstly, an analytical model for switching noise in simple digital circuits is proposed. The model is easy to implement and provides insight into the generation and propagation of substrate noise. Secondly, a compact model of guard rings for substrate noise suppression is proposed. The model features accurate prediction of noise suppression performance of P^+guard rings. The third contribution relates to an active noise suppression method based on spectrum shaping of the switching noise. The proposed method holds great potential for integration into IP cells, which is attractive for SOC designs based on IP cells.

In addition to this thesis, the PhD work has resulted in a number of publications [1–7], which are reprinted in appendix A.

Ming Shen May 2010

Acknowledgements

My Ph.D. study and this dissertation would not have been possible without the support and encouragement from many people. I would like to take this opportunity to show my best appreciation and express my deepest gratitude to these people.

Firstly and foremost I would like to thank my main supervisor, Associate Professor Jan H. Mikkelsen, for his great supervision, encourage, and support throughout my entire Ph.D. study. I feel very fortunate to have had my research work supervised by him. Further I would like to thank my co-supervisor Tong Tian, for his great advice and guidance. His suggestions and comments have always been appreciated.

I would like to thank Professor, Dr. Techn. Torben Larson for providing me the invaluable opportunity to be a member of TPS working on challenging and interesting projects.

Moreover I want to thank Associate Professor Troels B. Sørensen from Aalborg University, Professor Erik Bruun from Technical University of Denmark and Dr. Troels S. Nielsen from Agilent for reviewing this dissertation and serving in the assessment committee.

Many thanks to all of my colleagues at TPS for their help. In particular, Ole K. Jensen deserves to be mentioned for a number of fruitful discussions.

My deepest thanks to my wife Bo for her support, encouragement and understanding throughout these years. I dedicate this dissertation to my family.

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Contents

Chapter 1

Introduction

1.1 Background

The semiconductor industry has made huge progress in the past years with rapid development of communication equipment, computing technology, and portable electronic devices. The device density, as well as the system performance are still obeying Moore's law, which states that the transistor density of integrated circuits doubles every 2 years [8]. Driven by the market demands of more powerful functionality and lower costs, technology scaling has enabled the integration of more and more functionalities on a single chip.

However, the design of mixed-signal system on chips (SoCs) faces a great number of challenges. One of the most severe challenges is from substrate noise. Since SoCs integrate sensitive analog/RF circuits on the same die with high-speed digital processing circuits, the switching noise produced by the digital circuits can easily propagate through substrate and power supply rails to the analog/RF circuits, degrading their performance. The problem remains challenging as more and more digital functionalities (more noise generated) and more efficient transmission schemes (more sensitive) are combined for the market demands. Due to the ultra wideband nature and low power spectral density of the signal, the impact of substrate noise on UWB circuits is expected to be more detrimental than narrow band circuits. To overcome these problems, the substrate noise has to be characterized and subsequently efficient strategies for cancellation/suppression have to be developed.

1.2 Origin and coupling of switching noise

The substrate noise generation and injection mechanisms of a CMOS inverter implemented in a lightly doped process may be illustrated based on Fig. 1.1, which includes

(1) power/ground contacts to bulk coupling, (2) source/drain to bulk capacitive coupling and (3) impact ionization. A lumped element circuit model of the substrate is also given in the figure.

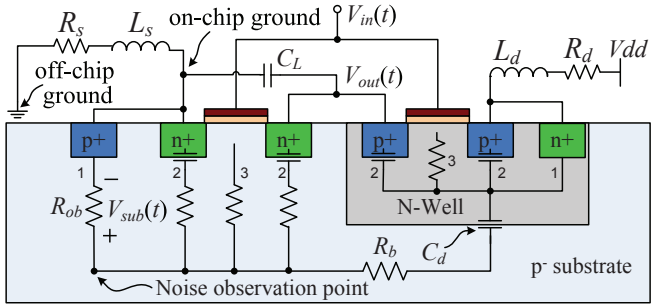

Figure 1.1: The cross-section view of a CMOS inverter stage and the equivalent circuit of the coupling mechanisms of substrate noise.

Unlike heavily doped substrates, where the substrate can be treated as a single node, the lightly doped bulk has to be modelled as a resistive network [9–11]. The N-well is modelled as one single node owing to its comparatively higher conductivity than the bulk. Among the coupling mechanisms shown in Fig. 1.1, the couplings through the power supply and ground contacts (the n^+ node of the PMOS and the p^+ node of the NMOS respectively) dominate the injection effects [9, 12]. Thus the source/drain to bulk capacitive coupling and the impact ionization are neglected in the studies of this dissertation.

Digital blocks usually have big size inverter stages to buffer outputs. When many digital blocks are integrated on the same die, there is a higher probability for these inverters to switch simultaneously. All of these switching noises are injected into the substrate or the interconnects. Fig. 1.2 shows such a propagation and coupling of the switching noise from the digital block to the sensitive analog/RF circuits. As the analog/RF circuits are sharing the same die and even the same on-chip ground, the substrate noise can be coupled either from the substrate or the power rails from digital circuit to analog/RF circuits. The coupled substrate noise could lead to a significant performance deterioration of the analog/RF circuit, such as degraded noise figures of low noise amplifiers. The main goal of this PhD project is to study substrate noise related issues in mixed-signal integrated circuits, focusing on ultra wide band (UWB) systems, and to find mitigation solutions for those issues. To reach this goal the project has been broken down into four research topics/tasks: (1) measurement, (2) impact evaluation, (3) modeling and (4) suppression of substrate noise. The relationship of the tasks is shown in Fig. 1.3. All four tasks have been pursued with UWB systems implemented using standard CMOS technologies in mind. The measurement task was to evaluate and, if needed, propose new suitable methods for conducting wide band measurements of substrate noise. Task two is to evaluate the nature of the substrate

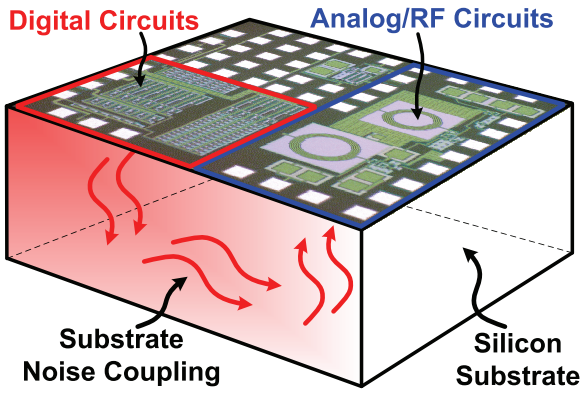

Figure 1.2: The coupling mechanisms of substrate noise from digital block to sensitive analog/RF circuits.

noise and to determine how severely it impacts UWB circuits, and the modeling task aimed to characterize the links between the substrate noise and key circuit parameters (i.e., DC supply voltage, clock frequency and circuit size) of the noise generating digital circuits. The fourth task was targeting the suppression of substrate noise and how to efficiently implement such measures.

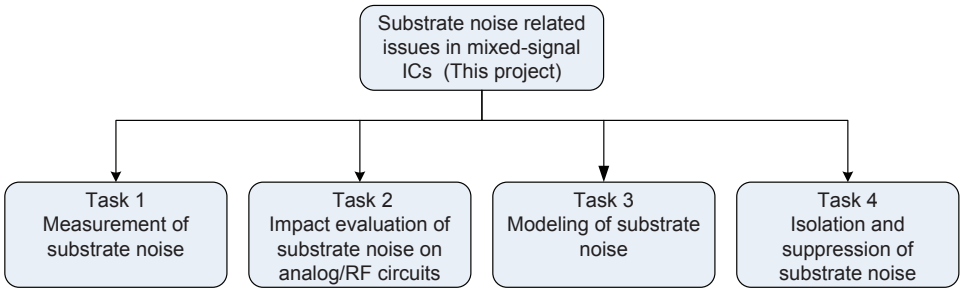

Figure 1.3: The task breakdown chart of this PhD project.

1.3 The organization of the dissertation

The work presented in this thesis deals with four different but tightly linked areas: measurement, impact evaluation, modeling and suppression of substrate noise. This is also reflected in the structure of the thesis.

Chapter 2 presents a measurement method for measuring substrate carried noise for lightly doped substrates within the UWB frequency band. The method is a passive fixture built based on ohmic contacts and suitable for on-wafer measurement using ground-signal-ground probes. The parasitic components affecting the measurement are investigated by EM simulations and measurements. Test chips are designed using

a 0.18 μm lightly doped CMOS process to evaluate the performance of the fixture. Several practical design rules for reducing the parasitical effects are concluded based on measurement results. As an example of the usability of the proposed method, switching noise measurements are presented for a switch-mode class-E PA and a digital block consisting of inverter chains.

Chapter 3 experimentally investigates the characteristics of substrate noise in a wide frequency band from DC to 10 GHz. Another aim is to evaluate the impact of substrate noise on sensitive wide band RF circuits, and to determine to what extent this is affected in the presence of substrate noise. The vehicle used for the investigation is a 1-5 GHz low-noise amplifier (LNA) for UWB systems. It is shown by the results that the substrate noise can drastically deteriorate the performance of the UWB LNA in terms of noise figure.

Chapter 4 presents two modeling methods for switching noise of simple digital circuits and large scale digital blocks, respectively. The switching noise generated by individual inverters is analytically investigated. An analytical model, named the GAP model is proposed to characterize the switching noise of individual inverters. The model is validated by both SPICE simulations and the measured results obtained from a test chip fabricated in a lightly doped CMOS process. The simulated and measured results are in good agreement with the proposed model. As the GAP is suitable for simple circuit, the modeling method based on statistic analysis for large scale digital circuits is proposed as well. The method is verified by Matlab and SPICE simulation results.

Chapter 5 presents an active suppression technique for substrate noise in mixed-signal ICs. The analytical modeling of guard rings for substrate noise isolation in lightly doped substrates is also proposed. In the proposed active suppression technique, an active spectrum shaping section is used to generate extra switching currents to modify the shape of the original switching noise in both time domain and frequency domain. The relative time delays of these switching currents to the original switching current are realized by controllable delay lines. The pulse widths and magnitudes of the switching currents are also controllable. By manipulating the extra switching currents, the spectrum of the total switching noise can be shaped to have a suppressed magnitude at desired frequencies. In the work of the analytical modeling of guard rings for substrate noise isolation, the goal is to find a simple yet accurate model describing P^+ guard rings. A resistive T-network is proposed in this work, and closed form expressions for the calculation of spreading resistance in the network are presented. Using this model the effects of the layout parameters can be taken into account during the pre-layout design phase, and the isolation performance of the design can be accurately predicted.

Chapter 6 draws conclusions and provides suggestions for the future work in substrate noise related research.

Chapter 2

Methods for Substrate Noise Measurement

2.1 Introduction

Measurement of substrate noise is a mandatory procedure needed either for the verification of noise coupling models or for the evaluation of noise strength. While it is not easy to conceptualize the coupling through the substrate, it is even more difficult to measure this noise in any real circuit. A reckless measurement of substrate noise without fine designed measurement methods could cause big measurement errors or even could lead to a completely wrong conclusion. It is known and has been reported that most energy of substrate noise is located at low frequencies. At the same time, the power spectral density of substrate noise can extend to frequency band at several GHz. As the switching speed of digital circuits increases, the power spectral density (PSD) of substrate noise moves to even higher frequencies. Thus measurement band must be wide enough to cover most of the spectral components of the substrate noise. This is especially important for analog/RF IC designers, to whom the most useful information is the power spectral density of the substrate noise. Moreover, substrate noise is usually very weak. This indicates that the measurement method should be capable of capturing weak signals without generating extra switching noise comparable to the original substrate noise.

A number of effort has been made to find substrate noise measurement methods in the past years [2, 9–11, 13–28]. The reported studies attempt to address the problem of substrate noise measurement from different perspectives. Some try to verify the coupling model of the substrate [10, 13]. Some focus on heavily doped CMOS or other integrated circuit processes [9, 14, 15]. Some investigate the waveforms or narrow band PSD of substrate noise [20] while others propose complicated circuits or devices as substrate noise sensors [16–19, 21–28]. But they can be generally categorized into two groups. One is the active methods [9, 10, 14, 16–28]. Another is the passive measurement

approaches [2, 11, 13, 15]. Active methods use active noise sensors to detect substrate noise. The sensors could be voltage comparators, transistors using back-gate voltage control and differential low noise amplifiers. Usually active methods provide a positive gain to amplify and thus observe more substrate noise. However, the use of active devices in the measurement increases the parasitical components. These parasitical components can significantly limit the measurement band. For example, the series capacitance in the measurement fixture makes it difficult to measure substrate noise close to DC. Moreover, the active measurement circuits could generate extra noise and contaminate the measured results. This is especially true when analog to digital converters or digital counters are used. For passive approaches, they usually involve the use of ohmic contacts. Since no active circuits are used the passive methods have the advantage of introducing no extra noise into the measured results. And they generally have broad measurement band because there are much less parasitical components in the fixture than that in the active approaches. However, the passive methods is usually lossy, which makes it unsuitable for the measurement of extremely low substrate noise. In the previous work few publications have investigated an appropriate wide band measurement method for measuring substrate noise in UWB systems implemented using lightly doped CMOS processes.

This chapter presents a measurement fixture suitable for measuring substrate carried noise for lightly doped substrates within the UWB frequency band. The presented method is a passive fixture based on ohmic contacts and suitable for on-wafer measurement using ground-signal-ground probes. The parasitic components effecting the measurement are investigated by EM simulations and measurements. Test chips are designed using a 0.18 μm lightly doped CMOS process to evaluate the performance of the fixture. Several practical design rules for reducing the parasitical effects are concluded based on measurement results. As an example of the usability of the proposed method, switching noise measurements are presented for a switch-mode class-E PA and a digital block consisting of inverter chains.

This chapter is organized as follows. Section 2.2 presents the proposed substrate noise measurement methods. Section 2.3 presents the verification of the proposed methods and the evaluation of the the parasitic effects in the measurement fixture. Section 2.4 presents the practical application cases of the proposed measurement methods. Section 2.5 presents an improved fixture, and section 2.6 draws the conclusion.

2.2 Proposed passive substrate noise measurement method

To experimentally investigate the substrate noise in an UWB system, the measurement setup must have a sufficiently wide measurement bandwidth. It is therefore important to avoid introducing complicated parasitic components or devices in the measurement setup, which can dramatically affect the measurement results. The presented substrate

noise measurement fixture, also refereed to as the substrate noise detector, is designed based on a modified GSG pad structure composed of two 85×85 μm ground pads and one 85×85 μm signal pad. The center-to-center distance between the signal pad and each ground pad is 150 μm. Thus, no extra fixture apart from a GSG probe is needed for the measurement of the substrate noise. The cross section view of the fixture is shown in Fig. 2.1.

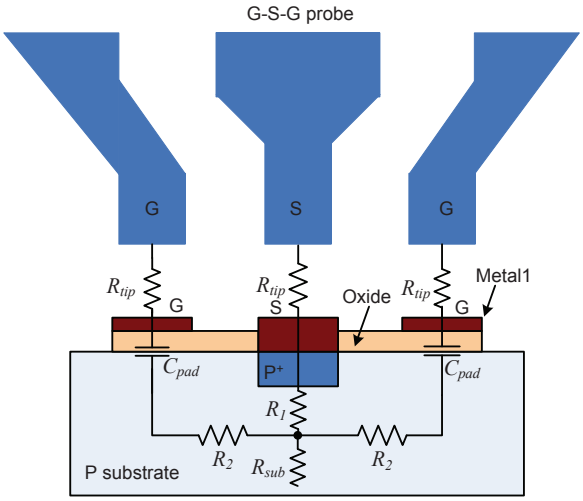

Figure 2.1: Cross-section view and the equivalent circuit of the substrate noise measurement fixture.

For simplicity only one metal layer, the Metal_1 layer, is shown here. In the actual setup all metal layers are connected to the top metal layer. Fig. 2.1 also shows the equivalent circuit model of the substrate noise measurement fixture. R_{tip} is used to model the contact resistance associated with the probing. The Metal_1 ground pad and the substrate is isolated by the oxide layer which comprises the oxide capacitance that is modeled by C_{pad}. The capacitance between the signal pad and the ground pad is significantly smaller than C_{pad} and thus neglected. It should be noticed that C_{pad} is the only reactive component in the model, and the bandwidth of the measurement fixture is closely related to its value. Its value can be approximately calculated from the oxide thickness and the pad dimensions by

$$C_{pad} = W \times L \times \frac{\varepsilon_{ox}}{t_{ox}}, \tag{2.1}$$

where W, L are the width and the length of the pad respectively, and ε_{ox} and t_{ox} are the permittivity and thickness of the oxide layer between the pads and the substrate, respectively. For lightly doped processes, the substrate can not be treated as one single node like the case is for heavily doped substrates [9]. To account for this, R_1, R_2, C_{sub} and R_{sub} are added to form a simplified network model of the substrate. R_1 and R_2 are used to model the spreading resistance of the substrate below the signal pad and

the ground pad. R_{sub} and C_{sub} are used to model the resistive and capacitive coupling between the substrate noise source and the measurement fixture. The values of R_1, R_2 and R_{sub} are difficult to precisely estimate from available parameters and are therefore derived from experimental data.

2.3 Evaluation of parasitic effects

In practical measurements of substrate noise, the substrate noise propagating from the noise source to the measurement point experiences attenuation and distortion. Distance-based substrate resistance and capacitive coupling between the substrate and the ground of the measurement setup are two key factors responsible for these effects. In order to obtain accurate measurements of the substrate noise, it is necessary to study the effects of such parasitics.

Based on the substrate noise measurement fixture in Sect. 2.2 a test chip has been designed to evaluate the effects of distance-based substrate resistance and the capacitive coupling between the substrate and Metal_1 ground. Fig. 2.2 shows the topology of the test chip.

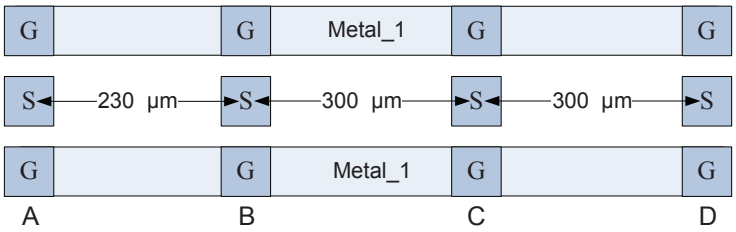

Figure 2.2: Topology of the test structure for evaluation of parasitical effects.

Four substrate noise detectors (denoted A, B, C and D) are placed with separating distances of 230, 300 and 300 μm, respectively. For each signal pad and ground pad, all the available metal layers from Metal_1 to Metal_6 are connected. Two wide metal strip lines composed of Metal_1 connect ground pads of the substrate noise detectors to produce capacitive coupling between the substrate and the ground of the measurement setup.

Fig. 2.3 shows an equivalent circuit model of the test structure. Here, there are four sub-circuit networks indicated by four dashed squares. Network 1 and 2 are models of the substrate noise detectors at port 1 and port 2, respectively. Network 3 is the model of the forward coupling network between the two measurement ports, including resistive coupling and capacitive coupling. Network 4, composed of C_{strip}, R_3 and L_{strip}, is used to model the coupling between the Metal_1 ground strip lines and the

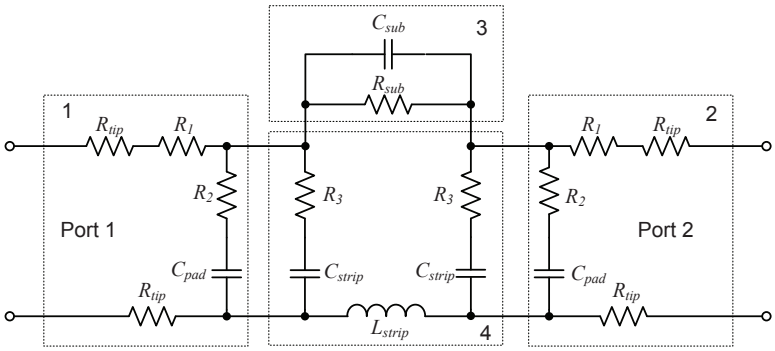

Figure 2.3: The equivalent circuit model of the test structure in Fig. 2.2.

substrate. Similar to C_{pad} in the model of the noise detector, C_{strip} can be roughly calculated from the oxide thickness and the strip dimensions. However, for the test structure in Fig. 2.2 the dimension of the ground strip is so large that the electric field between it and the substrate can not be treated as a uniform field and therefore needs more consideration. Fig. 2.4 shows the results of an EM simulation of the electric field in the oxide layer beneath the ground strips using the finite element method.

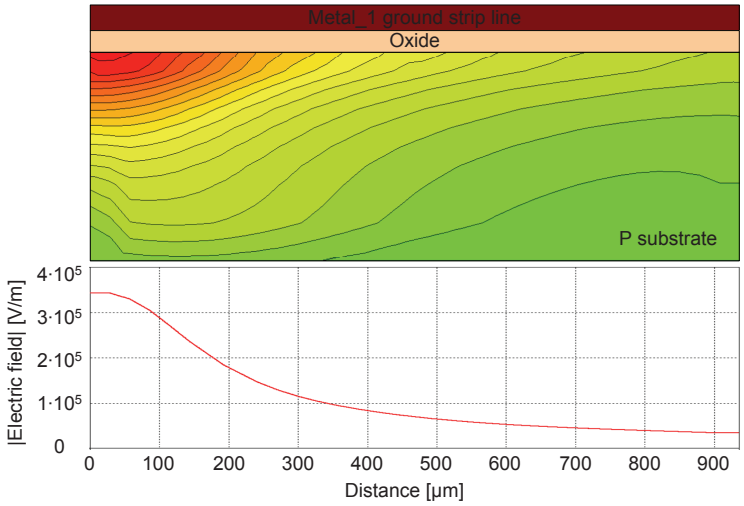

Figure 2.4: 1-D simulated electric field in the oxide layer beneath the ground strip line in Fig. 2.2.

A 6 GHz signal source is placed on the signal pad of noise detector A in Fig. 2.2 to excite the simulation. The electric field is shown using a 1-D electric field curve taken from the oxide layer beneath one of the ground strips in Fig. 2.2. It can be seen that the strength of the electric field decreases quickly as the distance between the observing point and the noise detector increases. This means that C_{strip} is over-estimated if its value is calculated using the actual length of 915 μm. From Fig. 2.4, it can be seen

Table 2.1: Parameters of the equivalent circuit in Fig. 2.3 (R_1, R_2, R_3 and R_{sub} are derived from experimental data; C_{pad} and C_{strip} are calculated based on Eq. 2.1 and simulated results in Fig. 2.4; C_{sub}, R_{tip} and L_{strip} are fitted variables).

Item	Unit	AB	BC	BD
R_{sub}	[Ω]	80	100	130
C_{sub}	[fF]	30	20	10
R_{tip}	[Ω]	3	3	3
R_1	[Ω]	140	140	140
R_2	[Ω]	40	40	40
R_3	[Ω]	60	30	10
C_{pad}	[fF]	250	250	250
C_{strip}	[pF]	1.8	2.0	2.4
L_{strip}	[nH]	1	1	1

that the electric field remains at a high level for distances of 50 μm and then drops quickly as the distance increases. Therefore, for calculating C_{pad}, the length, L, is decided as 50 μm and the width, W, is 85 μm. Then the oxide capacitance for one ground pad is calculated as 127.5 fF. Consider that two ground pads are placed in parallel, the value of C_{pad} is decided as shown in Table 2.1. Moreover, the electric field is found concentrated within a distance of 480 μm, which indicates the main area where the capacitive coupling happens. Thus it is reasonable to calculate C_{strip} according to this distance. For example, the length, L, is decided as 380 μm, subtracting $2 \times 50 = 100$ μm from 480 μm, for the case of AB. Then the C_{strip} for the case AB is calculated as 1.94 pF and finally decided as 1.8 pF due to the decreasing of the electric field. Similarly, C_{strip} for the case of BC and BD are decided as shown in Table 2.1. L_{strip} is the inductance of the strip line. Generally, the value of L_{strip} is small and 1 pH is used in the equivalent circuit. To determine the distance dependency of the substrate resistance, the DC resistance between the different signal pads of noise detector A, B, C and D are measured. The values of R_1 and R_{sub} in the equivalent circuit of Fig. 2.3 are derived based on these measurement results. Since the ground pads are not connected to the substrate, it is difficult to measure the spreading resistance between the signal pad and the ground pad. But its value can be approximated based on the measured DC resistances. The ground pads have the same dimensions as the signal pads and the central to central distance is 150 μm. So the spreading resistance of the substrate below the signal pad and the ground pad can be approximately decided as 360 Ω. Further, considering that two ground pads are connected in parallel. the spreading resistance values of R_2 and R_3 are approximated as shown in Table 2.1.

To determine the frequency dependency of the propagation effects, the test chip is studied using S-parameter measurements over 45 MHz to 10 GHz. The measured S_{21} over distances of 230 μm (AB), 300 μm (BC) and 600 μm (BD) are illustrated in Fig.

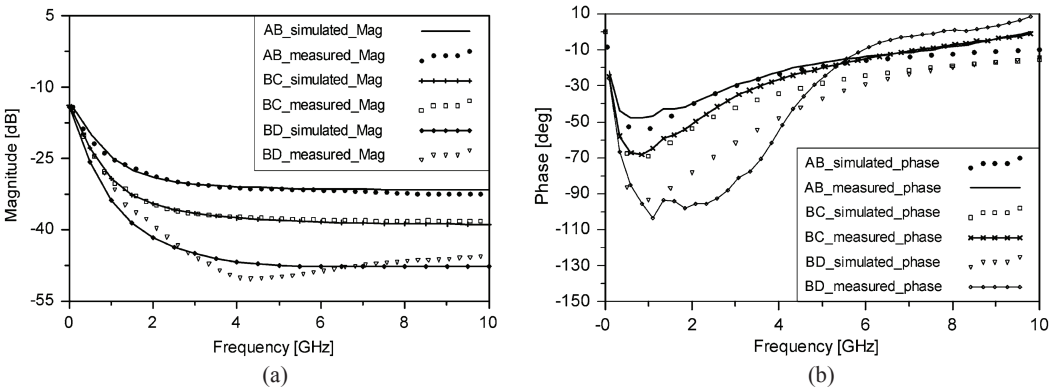

Figure 2.5: Simulated and measured (a) Magnitudes and (b) Phases of S_{21} versus frequency of the test structures in Fig. 2.2.

2.5. The simulation results of the equivalent circuit with parameters in Table 1 are also shown in Fig. 2.5. From these results the equivalent circuit model is seen to match measured data accurately, especially in case AB and BC. Relatively larger deviations are seen in case BD. For this case, the magnitude of S_{21} is around -45 to -50 dB at high frequencies, which makes accurate measurement a non-trivial task. And thus a reduced accuracy is expected over high frequencies. It is also seen in Fig. 2.5(a) that the attenuations at 45 MHz with different distances are almost identical at -14 dB. For such a low frequency, all capacitive couplings can be approximately treated as open circuit and the attenuation is mainly caused by the substrate resistance. Since the values of the substrate resistances of different distances are similar the attenuations are of course similar too. Moreover, high attenuations are observed at high frequencies. For instance, attenuations of -32, -38 and -47 dB are observed at 8 GHz for the three different cases. From Table 2.1, it is noticed that R_{sub}, C_{sub}, R_3 and C_{strip} are the only four changing variables that might be responsible for this. C_{sub} is insignificant due to its small value. Thus the different attenuations over high frequencies of three cases must be resulted from different values of R_{sub}, R_3 and the intentionally built capacitances between the Metal_1 ground strip lines and the substrate, i.e. C_{strip}. For higher frequencies, coupling through R_3 and C_{strip} to ground is more pronounced than that of low frequencies and thus the magnitude of S_{21} decrease. However, all S_{21} magnitude responses are flat over the frequency band of 3 to 10 GHz (with fluctuation less than 3 dB), which means the measurement setup can be used to measure the PSD of substrate noise even under conditions of strong parasitic effects. Considering the measured S_{21} in Fig. 2.5 and the corresponding values of R_{sub}, R_3 and C_{strip} in Table 2.1, it is seen that a larger R_3 and a smaller C_{strip} helps to decrease the loss.

Based on the findings mentioned above a number of guideline design rules for the design of practical measurement fixtures can be listed as following. The value of R_3 should be increased by reducing the dimensions of the ground pads on Metal_1 layer but keep the size of 85×85 μm on the top metal layer for measurement purpose; C_{strip} should

be minimized by reducing the Metal_1 ground around the noise detector or using the top metal layer to connect the ground pads.

2.4 Practical application example

As a practical example, the presented substrate noise measurement fixture is used to measure the switching noise generated by a switch-mode class-E PA. The class-E PA is designed in the same 0.18 μm technology as the test chip in Sect. 2.3 and hence all conclusions and design rules drawn above can be applied. While designing the substrate noise detector on the chip, several factors are taken into account. Firstly, to have a clean reference ground, the substrate noise detector's ground is closely connected to the ground pad of the DC supply. Secondly, for convenient probing, the substrate noise detector is placed at the edge of the chip with a distance of approximately 600 μm to the output stage of the class-E PA. Finally, following the design rules drawn in Sect. 2.3, to avoid large attenuations, the Metal_1 ground plane around the substrate noise detector is deleted to reduce the capacitance between the Metal_1 ground plane and the substrate. The chip photo is shown in Fig. 2.6.

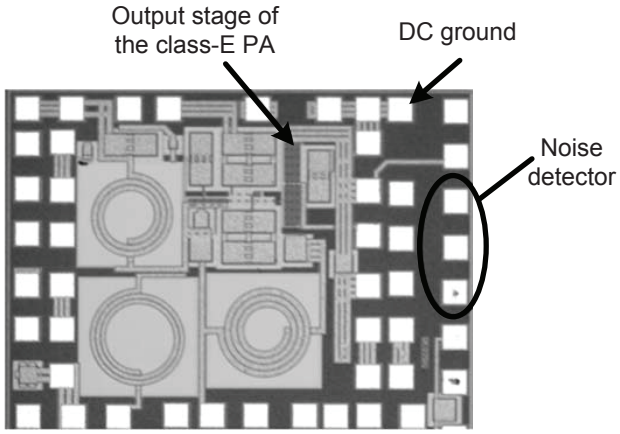

Figure 2.6: Microphotograph of the test chip consisting of a class-E PA and the substrate noise detector.

In this experiment, the PA acts as a switching noise source and the proposed measurement fixture as noise detector. When the PA is driven by high frequency signals, the generated switching noise occupies a wide frequency band, which makes it a suitable signal source to validate the wide band characteristic of the measurement fixture. The measured frequency spectrum of the switching noise generated by the PA is measured at the noise detector as shown in Fig. 2.7. It can be seen that the spectral contents of the measured substrate noise appear at 2.44, 4.88 and 7.32 GHz with magnitudes of -36, -72 and -60 dBm, respectively. The fourth harmonic at 9.76 GHz is too weak

to be measured. But the three spectral contents already cover a wide frequency band, which indicates the usability of the proposed fixture.

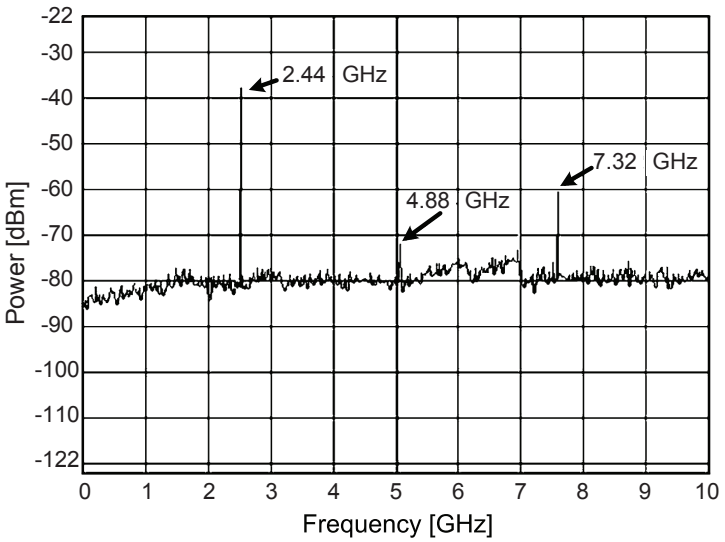

Figure 2.7: Measured frequency spectrum of the switching noise of the class-E PA measured using the proposed noise detector.

2.5 Improved passive measurement fixture

It has been shown that the measurement fixture presented in Sect. 2.2 is able to provide reliable PSD measurements over the UWB frequency band from 3 to 10 GHz. Furthermore, obvious effects of capacitive coupling are observed over 45 MHz-3 GHz. For measuring wide band switching noise in the band of 3-10 GHz or narrow band substrate noise at frequencies below 3 GHz, the fixture is applicable. But for substrate noise located from DC to 10 GHz, the present fixture is not feasible. To achieve a measurement band of DC to 10 GHz the original fixture is improved.

Fig. 2.8 shows the cross section view of the improved substrate noise measurement fixture. It can be seen that the ground pads of the fixture are connected to the substrate instead. As a result the resistive coupling is increased and even dominates the coupling between the ground pads and the substrate. The contact size and the distances between contacts determine the strength of the resistive coupling, and they should be designed based on the parameters of the process.

A test chip is fabricated using a 0.18 μm CMOS technology to verify the improved measurement fixture. Fig. 2.9 shows the microphotograph of the test chip. It consists of five improved measurement fixture aligned with central-to-cental distance of 150

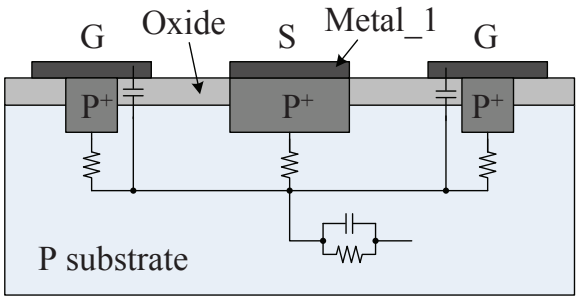

Figure 2.8: The cross section view of the improved substrate noise measurement fixture.

μm. The P^+ contacts connecting the ground pads and substrate are 10 by 10 μm. The ground pads of all fixtures are connected by two 10 μm-width Metal_6 strips. Such a narrow metal strip is used to reduce the capacitive coupling between the ground and the substrate.

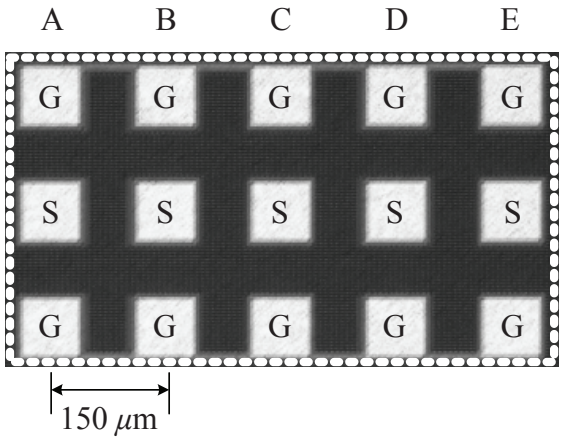

Figure 2.9: Microphotograph of the test chip for the verification of the improved substrate noise measurement fixture.

The measured S_{21}-magnitudes of the improved measurement fixture with four varying fixture-to-fixture distances are shown in Fig. 2.10.

It can be seen that for the same fixture-to-fixture distance the improved fixture has an attenuation similar to the attenuation in the original design. However, for all of the four distances, the measured magnitudes of S_{21} are flat from DC to 10 GHz, which makes the improved measurement fixture suitable for the measurement of substrate noise in such a wide frequency band.

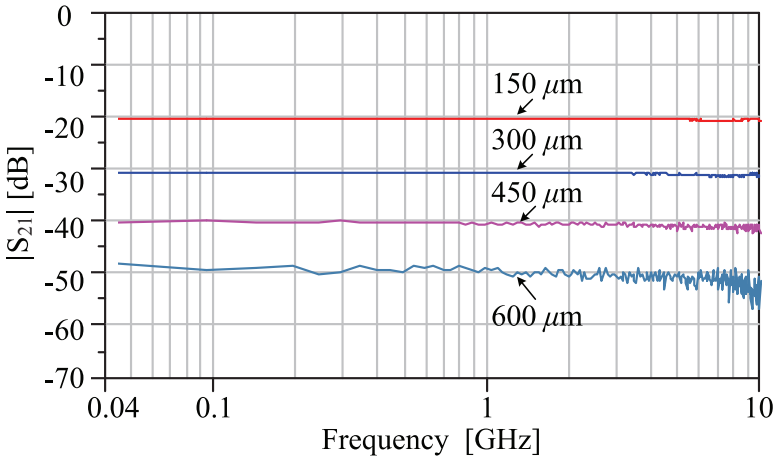

Figure 2.10: The measured magnitudes of S_{21} versus frequency with varying fixture-to-fixture distances.

2.6 Conclusion

This section presents a passive measurement fixture suitable for the measurement of substrate noise in lightly doped substrates within the UWB frequency band. The effects of the distance-based substrate resistance and the capacitive coupling between the substrate and the ground are evaluated by measurement of a test chip. An equivalent circuit model of the measurement fixture is given and shows accurate fit. The simulated and measured results show that this measurement fixture is able to provide reliable measurements over the UWB frequency band from 3 to 10 GHz. Furthermore, obvious effects of capacitive coupling are observed over 45 MHz-3 GHz. An improved fixture is proposed to reduce the capacitive coupling effects between the substrate and the ground of the measurement setup. Experimental results show that the improved measurement fixture provides flat S_{21}-magnitudes from DC to 10 GHz, which makes the improved measurement fixture suitable for the measurement of substrate noise in such a wide frequency band.

Chapter 3

Substrate Noise Impact Evaluation

3.1 Introduction

For the previously reported work on the effects of substrate noise on analogy/RF integrated circuits, almost all of them are focusing on narrow band applications [25, 29, 30]. It has not been fully investigated if substrate noise is a severe issue for wide band systems. It is also unclear how the substrate noise affects the wide band sensitive circuits. Without clear answers to these questions, going forward for modeling and suppression of substrate noise would be unmotivated.

This chapter experimentally investigates the features of substrate noise in a wide frequency band from DC to 10 GHz, and attempts to evaluate the impact of substrate noise on the performance of wide band RF circuits. The vehicle used for the investigation is a 1-5 GHz low-noise amplifier (LNA) for UWB systems [5].

This chapter is organized as follows. Section 3.2 presents the experiment setup and the design of the test chip in a 0.18 μm CMOS process for the investigation. Section 3.3 presents the discussions on the measured results. Conclusion is drawn in Section 3.4.

3.2 Experimental impact evaluation on an UWB LNA

The schematic used for the experiment is shown in Fig. 3.1. It consists of a digital block, a substrate noise detector array and an UWB LNA. The digital block plays the role of a substrate noise generator. The substrate noise detector array is the measurement fixture discussed in Chapter 2 (Fig. 2.8). It is used in the experiment for substrate noise measurements. The UWB LNA is used as a victim circuit for the experiment.

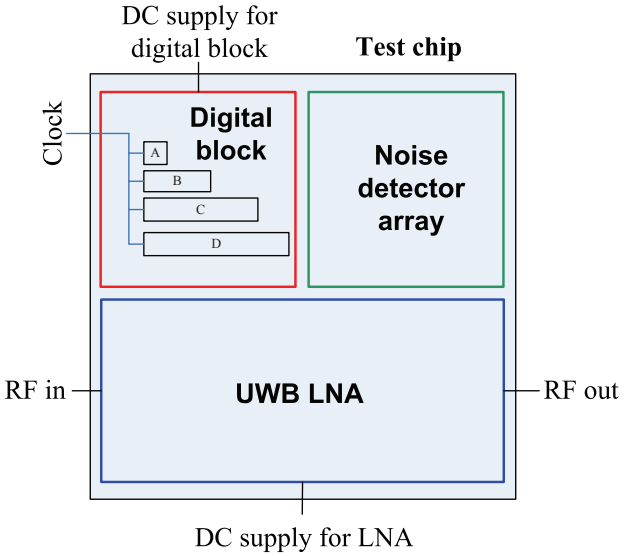

Figure 3.1: The schematic of the integrated circuit for the experiment.

The detailed schematic of the digital block consisting of four buffer chains is shown in Fig. 3.2. The buffer chain A contains six one-stage inverters.

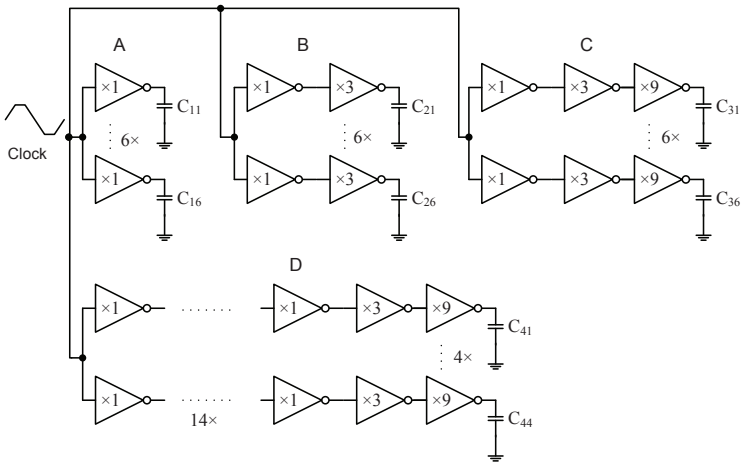

Figure 3.2: The schematic of the digital block consisting of four buffer chains for the generation of switching noise.

The width/length ratios of the NMOS and PMOS transistors of each inverter are 25 μm/0.18 μm and 50 μm/0.18 μm, respectively. The buffer chain B, C and D are multi-stage buffer chains with different stage numbers and sizing factors shown in Fig. 3.2. C_{ij} represents the parasitic capacitance at the output of each buffer chain.

Fig 3.3 shows the schematic of the UWB LNA. It is a 1-5 GHz two-stage single ended

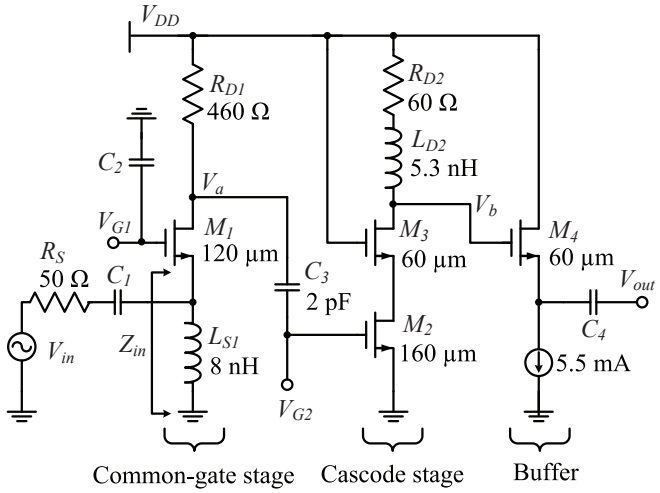

Figure 3.3: The schematic of the UWB LNA for noise impact evaluation.

amplifier with a source follower buffer for measurement purpose. In previously reported work, the study of substrate noise above 1 GHz is rare. For that reason the lower bound of the operation band in this design is set to 1 GHz aiming to obtain more results. This is done while maintaining the desired performance in the UWB band of 3-5 GHz.

3.2.1 Test chip

The fabricated test chip is shown in Fig. 3.4, and the PCB with the bonded chip for the measurements is shown in Fig. 3.5.

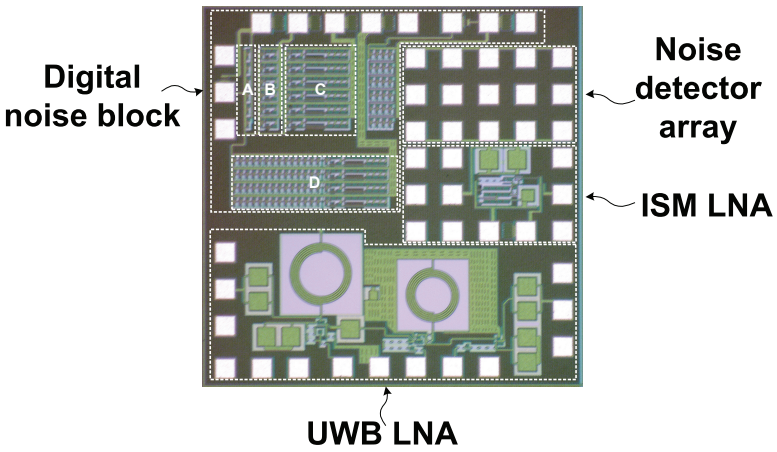

Figure 3.4: The microphotograph of the test chip.

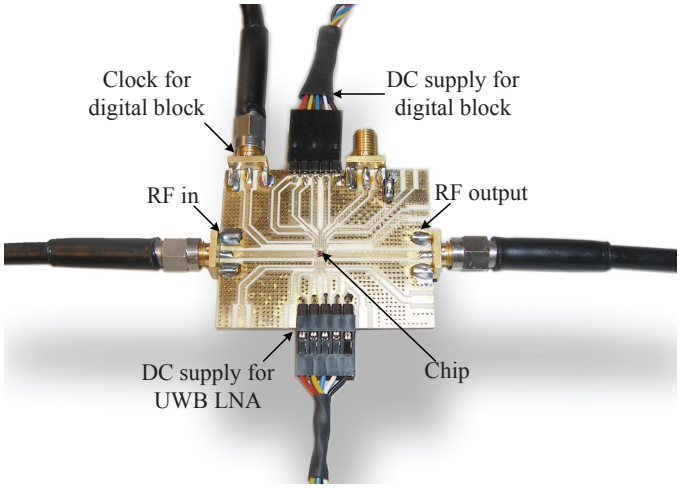

Figure 3.5: The PCB with the bonded chip for the measurements.

3.2.2 UWB LNA

The UWB LNA is measured to make sure that it has a proper overall performance. The common-gate stage and the cascode stage consume 5 mA in total at a supply voltage of 1.8 V. The simulated and measured S-parameters are shown in Fig. 3.6. It can be seen that the measured gain is 11-13.7 dB, the measured $|S_{11}|$ is less than -12 dB and the measured $|S_{22}|$ is less than -10 dB in the frequency band of 1-5 GHz. The simulated and measured noise figures are shown in Fig. 3.7 and the measured NF is 5.0-6.5 dB in 1-5 GHz. It can be seen that this UWB LNA has very good overall performance compared with previously proposed UWB LNAs [2].

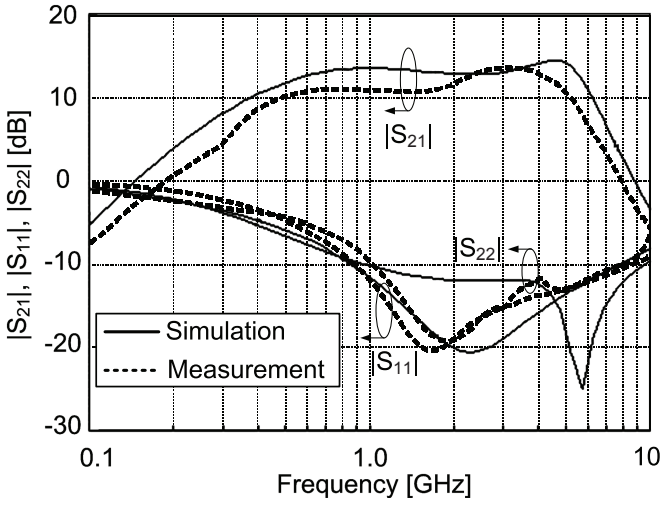

Figure 3.6: Measured and simulated S parameters versus frequency of the UWB LNA.

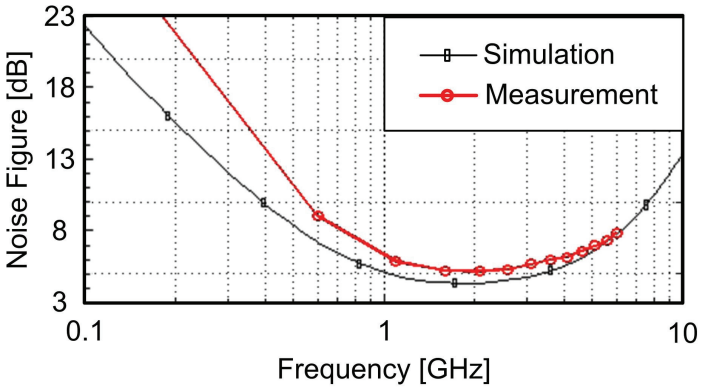

Figure 3.7: Measured and simulated noise figure versus frequency of the UWB LNA.

3.3 Results and discussion

In the experiment, square waves from a function generator Agilent 33250a are used as the clock to drive the digital block. The substrate noise due to the switching noise generated by the digital block is measured at the noise detector array as shown in Fig. 3.8(a). It can be seen that the major part of the substrate noise are located in the frequency band from DC to 2 GHz. But there are also noise tones in the frequency band up to 10 GHz with magnitudes about 10 dB higher than the noise floor. The spectrum at the RF out of the LNA is also measured when the LNA is on with a sinusoidal input of -50 dBm at 3.88 GHz (Fig. 3.8(b)). It is clear that the magnitudes of the substrate noise in 2-5 GHz are much higher than those measured at the noise detector. This indicates that the in band substrate noise coupled at the input of the LNA has been amplified by the LNA. In practical applications the magnitude of the received UWB signal could be significantly lower than the magnitude of the substrate noise as the allocated EIRP of an UWB signal is lower than -41.3 dBm/MHz [31]. The effects of the clock frequency on the substrate noise is investigated by measuring the spectrum at the RF out of the LNA, while varying the frequency of the digital clock. The measured results are shown in Fig. 3.9, zoomed in into the frequency band of 3.5-4.5 GHz for more detailed information. It can be seen that the magnitude of the substrate noise is increased when f_{clock} is increased from 10 MHz to 50 MHz. This is due to the fact that the digital circuit switches faster (generates and injects more switching noise) with a higher clock frequency. This effect will be discussed with more detail in the subsequent chapter.

Apart from the original harmonics of the substrate noise, it can be seen in Fig. 3.9 that some extra frequency components are also present. These components are caused by the intermodulation between the RF input signal and the substrate noise at the fundamental and higher order harmonics. To confirm this, the intermodulation com-

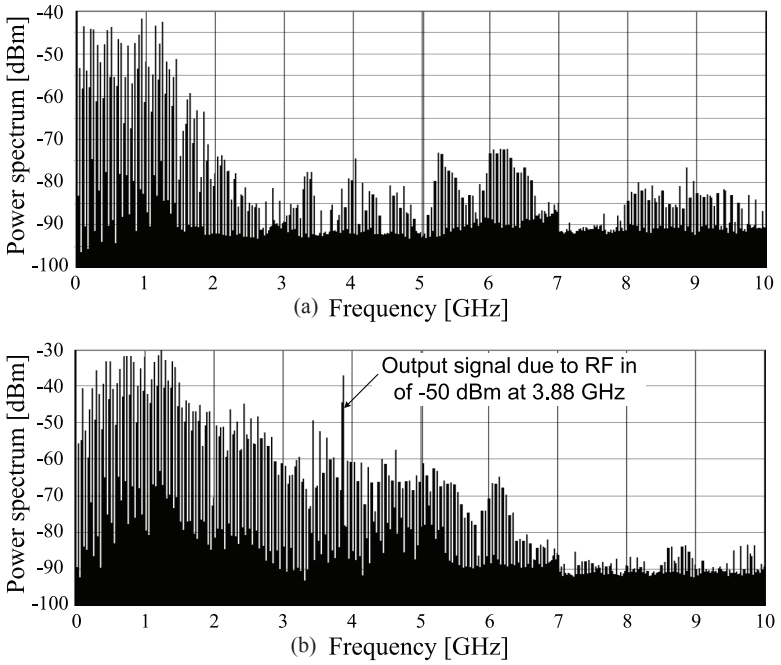

Figure 3.8: Measured power spectrum (a) from the substrate noise detector and (b) from RF out of the UWB LNA. In this measurement f_{clock} is 50 MHz and the rising and falling time of the clock is 5 ns.

ponents with two different RF input frequencies are measured and marked by circle symbols shown in Fig. 3.10. It can be seen that the noises at the harmonics of f_{clock} remain with insignificant changes, while the noise components due to intermodulation shift along with the RF input signal.

The impact of the substrate noise on the UWB LNA is studied by comparing the measured noise figure of the LNA when the digital block is turned off and turned on with three different values of f_{clock}. The measured results are shown in Fig. 3.11. It can be seen that the LNA has a smooth and flat noise figure around 6 dB in the measurement frequency band when the digital block is turned off. When the digital block is turned on, significant deterioration of the noise figure is seen. It also can be seen that the deterioration is stronger for higher f_{clock}, which is consistent with the results shown in Fig. 3.9.

3.4 Conclusion

In this chapter, the impact of substrate noise on UWB LNA is experimentally evaluated. Significant substrate noise is observed in the frequency band of DC to 10 GHz. It is shown by the results that the substrate noise can drastically deteriorate the performance

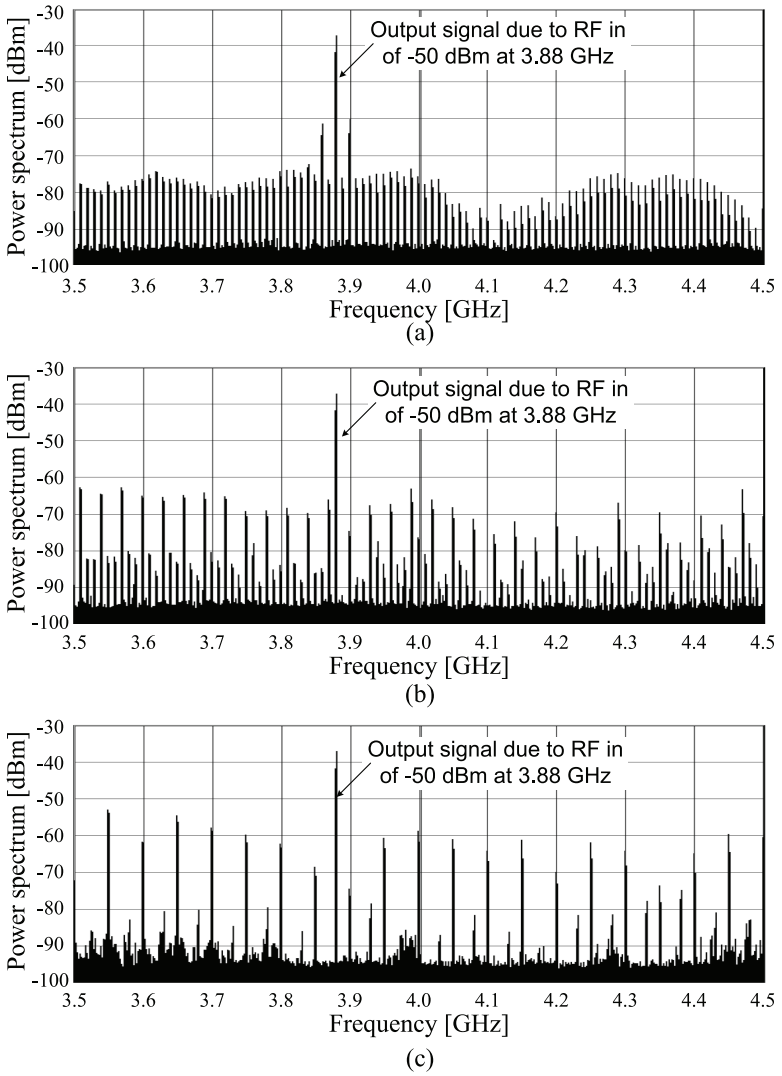

Figure 3.9: Measured power spectrum from RF out of the UWB LNA, while the digital block is driven with three different clock frequencies. The parameters for the clock are: (a) f_{clock}=10 MHz, (b) f_{clock}=30 MHz, (c) f_{clock}=50 MHz. The rising and falling time of the clocks are 5 ns for all of the three cases.

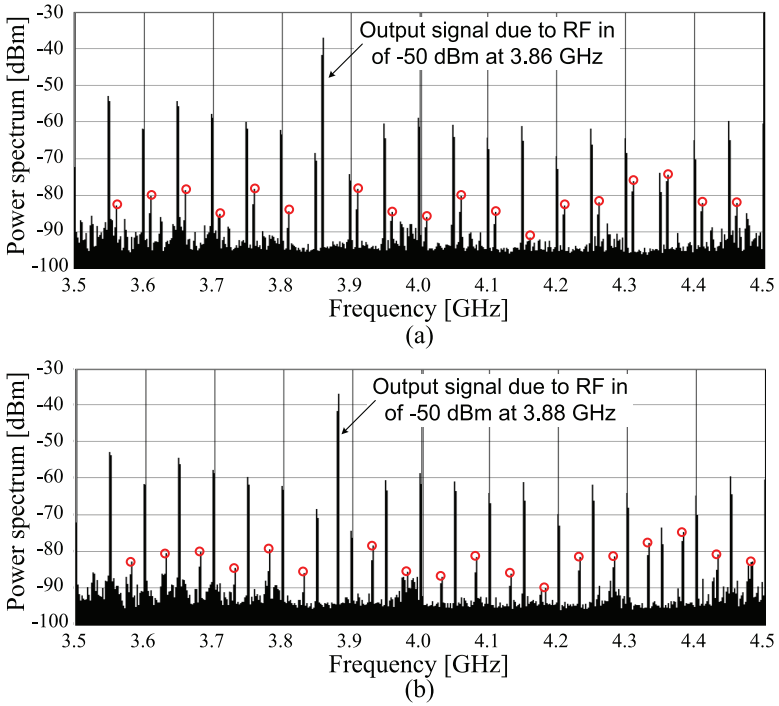

Figure 3.10: Measured power spectrum from RF out of the UWB LNA with two different RF input frequencies. The parameters for the RF input signal are: (a) f_{RF}=3.86 GHz, (b) f_{RF}=3.88 GHz. The magnitude of the RF input signal is -50 dBm. The circle symbols mark the intermodulation components.

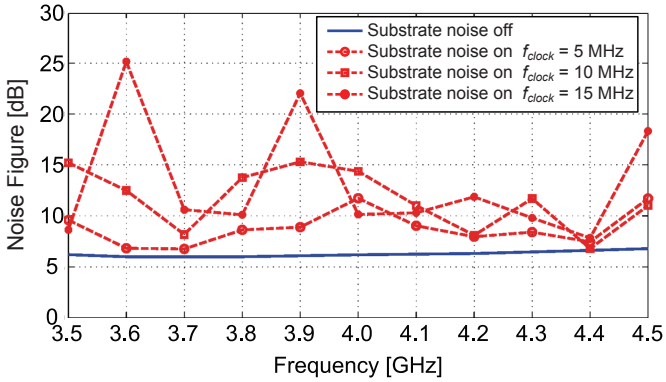

Figure 3.11: Measured noise figure versus frequency of the UWB LNA when the digital block is turned off and turned on with three different values of f_{clock}.

of the UWB LNA in terms of noise figure. The results clearly indicate the need for a good understanding of the generation and propagation of the substrate noise, as well as the need of effective approaches for reducing the substrate noise in the design of wide band mixed-signal ICs. The motivation of this PhD project to devise effective strategies for modeling and mitigating the substrate noise is also supported by the results in this chapter.

To the author's best knowledge, no similar work on wide band circuits has been presented before and the results in this chapter carry useful information for wide band mixed-signal IC designers.

Chapter 4

Analytical Modeling of Switching Noise in Lightly Doped Substrates

4.1 Introduction

Switching noise produced in digital circuits has gradually become one of the most important concerns in IC design due to higher and higher density of digital design, the need for more and more digital functionalities and the tight requirements for area in mixed-signal integrated circuits. As illustrated in Fig. 4.1, the switching noise generated by digital circuits can propagate through the substrate to reach sensitive analog/RF circuits and deteriorate their performance. A number of methods have been proposed for achieving an efficient model that is able to capture the main features of the switching noise [9–12, 26, 32–37]. For heavily doped substrates the substrate is simplified as one electrical node due to their low resistivity, and switching noise modeling methods using this simplification have been proposed [32, 33]. Featuring high resistivity and better noise isolation properties, lightly doped substrates are widely used in mixed-signal designs [12, 26, 34]. Since the resistivity of lightly doped substrates is much higher than

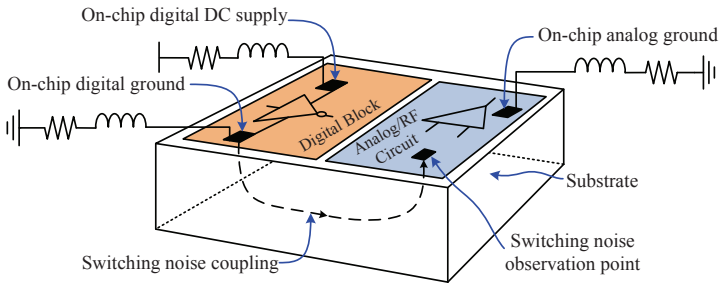

Figure 4.1: Switching noise coupling mechanism in mixed-signal circuits.

that of heavily doped substrates, the substrate can not be treated as a single electrical node. Hence, the modeling methods for heavily doped substrate are not applicable. One of the conventional ways to characterize switching noise in lightly doped substrate is to run SPICE simulations on the functional circuits in the digital block together with an extracted substrate network [9, 10]. However, such a method is computationally expensive [11]. To reduce the complexity of the simulations, approaches based on macro models have therefore been proposed [11, 12, 26, 34, 35]. In these macro models, the total switching current of a digital block is typically represented using an asymmetrical triangular waveform. Combined with an equivalent lumped element network to represent the substrate, fast generation of SPICE simulations can be achieved. However, these approaches mainly depend on simulations, and hence they suffer from the flaw of insufficient insight into switching noise generation and propagation. Another approach to switching noise modeling is to make use of analytical methods [37, 38]. Based on mathematical analysis of waveform functions characterizing the switching current and a transfer function modeling the propagation of the switching noise, closed-form expressions for the switching noise are derived [37]. This method provides more insight into the propagation of switching noise. However, the switching current source still needs to be determined by SPICE simulations, and layout extractions are still needed to find the resistances in the transfer function. To avoid the need for layout extractions, a compact model has been proposed to characterize the spreading resistance between arbitrary sized diffusion contacts on lightly doped substrates [38]. Based on this model, the transfer function describing the propagation of the switching noise can be determined. However, a feasible analytical model characterizing the switching current source is still unavailable.

This chapter presents two modeling methods for switching noise of simple digital circuits and large scale digital blocks, respectively. The switching noise generated by individual inverters is analytically investigated. An analytical model, named the GAP model is proposed to characterize the switching noise of individual inverters. The model is validated by both SPICE simulations and measured results obtained from a test chip fabricated in a lightly doped CMOS process. The simulated and measured results are in good agreement with the proposed model. The GAP is suitable only for simple circuits. To extend the usability of the GAP model to large scale circuits also, the GAP model is complimented by a statistical analysis method. The method is verified by Matlab and SPICE simulation results. This chapter is organized as follows. Section 4.2 presents the proposed GAP model for switching noise in individual inverters. The statistic model for switching noise in large scale digital circuits is present in 4.3. Section 4.4 draws the conclusion.

4.2 The GAP Model

The reason for focusing on the analysis of individual inverters is based on two facts:

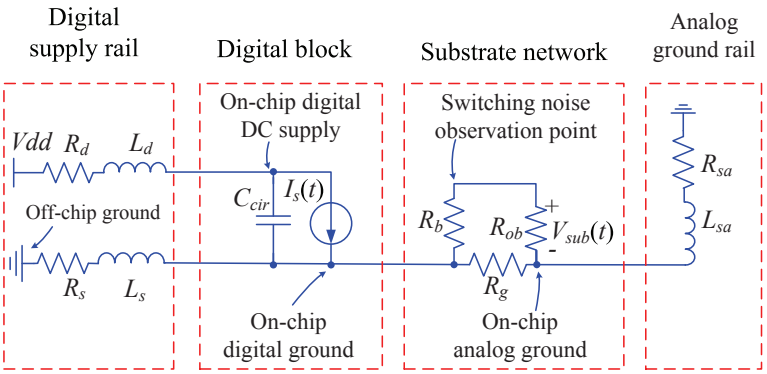

Figure 4.2: The switching noise coupling network.

(a) The inverter is a basic and often used building block in digital circuits.

(b) A typical large scale digital circuit usually contains big size inverters that act as buffers. Due to the large sizes, these inverters generate significant switching noise, and can therefor be assumed to dominant the total generation of the switching noise in the digital circuit [36].

Thus, analyzing the switching noise in an individual inverter is considered a good starting point for obtaining detailed understanding of the generation and injection of switching noise. The proposed model approximates the switching current using a Gaussian pulse (GAP) function. The key parameters in the model are derived by solving the differential equation describing the output voltage of a capacitively loaded inverter. Combining the switching current model and the transfer function, which models the propagation of the switching current, the spectrum of the switching noise can be predicted.

The simplified switching noise coupling mechanisms involved in Fig. 4.1 are illustrated by four blocks in Fig. 4.2. The digital supply rail block and the digital block in Fig. 4.2 are similar in structure to the coupling network used in [11]. In the digital block, $I_s(t)$ represents the switching current generated by the digital block. C_{cir} is the circuit capacitance between the on-chip digital DC supply and the on-chip digital ground. The substrate network block and the analog ground rail block are used to model the switching noise coupling to analog circuits. R_d and L_d are the resistance and inductance of the bonding wire and interconnect connecting the on/off-chip digital DC supply, respectively. R_s, R_{sa}, L_s and L_{sa} are the resistances and inductances of the interconnects and bonding wires connecting the off-chip ground to the on-chip digital and analog ground, respectively. R_g is the resistance between the on-chip digital and analog grounds. R_{ob} is the substrate resistor between the noise observation point and the on-chip analog ground. R_b is used to model the spreading resistance between the on-chip digital ground and the the observation point on the substrate. Based on Fig. 4.2 the

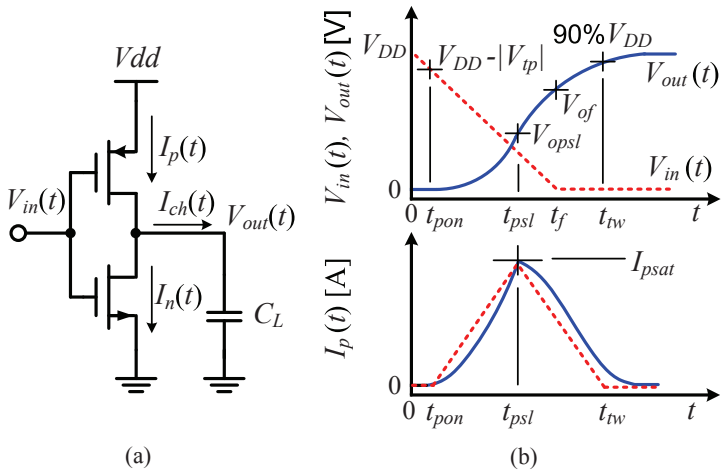

Figure 4.3: (a) The schematic of a capacitively loaded inverter, and (b) the input/output voltage (dash/solid line in the top figure) and switching current (bottom figure) of a falling input transient.

resulting noise voltage at the observation point can be derived as

$$\begin{aligned} V_{sub}(j\omega) &= H(j\omega) \cdot I_s(j\omega) \\ &= \frac{R_g R_{ob} Z_L I_s(j\omega)}{(j\omega C_{cir}(\frac{Z_L Z_{ea}}{Z_L + Z_{ea}} + Z_D) + 1)(Z_{ea} + Z_L)(R_b + R_{ob} + R_g)}, \end{aligned} \tag{4.1}$$

where $Z_D = R_d + j\omega L_d$, $Z_L = R_s + j\omega L_s$ and $Z_{ea} = R_{sa} + R_g(R_d + R_{ob})/(R_g + R_d + R_{ob}) + j\omega L_{sa}$. The procedure for finding the parameters of the transfer function, $H(j\omega)$, has been provided in previous studies [11, 37]. The remaining challenge is to find a scalable analytical model for I_s, which is also the main contribution of the presented work.

4.2.1 The switching current of an individual inverter

A typical schematic of a capacitively loaded inverter is shown in Fig. 4.3(a). Here, $I_p(t)$ is the drain current of the PMOS device, $I_n(t)$ is the drain current of the NMOS device and $I_{ch}(t)$ is the charging/discharging current. The input voltage (dash line) and output voltage (solid line) in a falling input transient of the inverter are shown in the top figure of Fig. 4.3(b). As V_{in} falls, the PMOS is turned on at time t_{pon}, and the capacitor load is charged towards a higher voltage. When $V_{out}(t)$ reaches V_{opsl} at t_{psl} and $V_{out}(t_{psl}) - V_{in}(t_{psl}) = |V_{tp}|$, where V_{tp} is the threshold voltage, the PMOS leaves the saturation region and enters the linear region. V_{of} is defined as the output voltage at the falling time t_f. The time when the output reaches 90% of the final value is defined as t_{tw}. The switching current I_p during the transient is shown by the solid line at the bottom of Fig. 4.3(b). A number of modeling approaches of the output response and switching currents in CMOS inverters have been reported [39, 40]. However, to

derive the expression of the switching current is no trivial task, and no comprehensive expressions for the switching current have been presented. To simply the analysis task, a triangular waveform is often used to model the switching current as shown by the dash line in the bottom figure in Fig. 4.3(b) [37]. The triangular model has a peak value of I_{psat} at t_{psl}, and its magnitude is zero at $t \leq t_{pon}$ and $t \geq t_{tw}$. This model is simple and accurate for estimating the Power Spectral Density (PSD) of the switching noise at low frequencies. However, this approach leads to significant estimation errors at high frequencies due to the abrupt simplifications of the switching current [11, 37]. Moreover, the expressions of the key parameters such as t_{psl} and t_{tw} are not provided. In this study, Gaussian pulse equations are used to model the switching currents. The resulting GAP model is thus described by the following equation

$$I_p(t) = \begin{cases} I_{psat} \times \exp\left[\frac{-2\pi(t-t_{psl})^2}{(1.45\times(t_{psl}-t_{pon}))^2}\right] & for\ 0 \leq t \leq t_{psl} \\ I_{psat} \times \exp\left[\frac{-2\pi(t-t_{psl})^2}{(2.0\times(t_{tw}-t_{psl}))^2}\right] & for\ t > t_{psl}. \end{cases} \tag{4.2}$$

The GAP model has the same peak current value as the triangular model at t_{psl}, and its magnitude is 10% and 20% of I_{psat} at t_{tpon} and t_{tw}, respectively. Compared with the triangular model, the GAP model has smoother transitions at the peak and bottom of the waveform. As a result, the GAP model produces less predicting errors at high frequencies. The expressions of the parameters in the GAP model are derived in the following part of this section. The expressions also can be used in the conventional triangular model.

In this study, the short circuit current during switching transients is neglected. This approximation is based on the fact that the charging/discharging currents contribute the major part of the switching current for capacitively loaded inverters in most of the present CMOS processes [39–41]. Under this assumption, the NMOS and PMOS are assumed off during a falling input transient and a rising input transient, respectively, and $I_s(t)$ only consists of $I_p(t)$ generated at the falling input transient. The discharging current generated at the rising input transient is flowing in the closed loop formed by the NMOS and C_L. Thus it has no contribution to $I_s(t)$ and is consequently neglected. Moreover, the analysis in this study is based on the well-known Square-law MOSFET model. This simplification is necessary since higher-order models are intractable for analytical manipulation. But, as shall be seen, the results derived based on the simple model are sufficiently accurate, which is shown in the measurement section. In the Square-law model the transistor drain current is expressed as

$$I_D = K_p\left[(V_{gs} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad V_{DS} < V_{Dsat} \tag{4.3}$$

$$I_D = \frac{1}{2}K_p(V_{gs} - V_t)^2 \qquad V_{DS} \geq V_{Dsat}, \tag{4.4}$$

where $V_{Dsat} = V_{GS} - V_t$, $K_p = \mu C_{ox}\frac{W}{L}$, and V_{DS}, V_{GS} are the drain-source, gate-source voltage respectively. For reasons of concise and general expressions, corresponding low-

ercase letters are used to denote voltages normalized by V_{DD} in the following analysis. For example, $v_{out}(t) = V_{out}(t)/V_{DD}$. The input voltage waveform is approximated to be a falling ramp with a falling time t_f and a slope $s_f = -1/t_f$

$$v_{in}(t) = \begin{cases} s_f \times (t - t_f) & for \quad 0 \le t \le t_f \\ 0 & for \quad t > t_f. \end{cases} \tag{4.5}$$

This approximation is widely used due to its simplicity and effectiveness [39,40]. With this t_{psl} and t_{tw} can be derived based on the expression of the output voltage, which can be found by solving the following differential equation

$$C_L \frac{dV_{out}(t)}{dt} = I_p(t), \tag{4.6}$$

where $I_p(t)$ can be replaced by Eq. (4.3) or (4.4) with corresponding terminal voltages. Categorizing the falling input transient as two cases that $v_{opsl} < v_{of}$ (relatively slow input ramp) or $v_{opsl} \ge v_{of}$ (relatively fast input ramp), the expressions for those parameters for each case are given as

Case A: $v_{opsl} < v_{of}$

$$t_{psl} = (v_{opsl} + p)/s_f, \tag{4.7}$$

where $p = V_{tp}/V_{DD}$, and v_{opsl} can be found by solving the equation

$$v_{opsl} = \frac{K_p V_{DD}}{6 s_f C_L}(v_{opsl} - 1)^3. \tag{4.8}$$

Furthermore, t_{tw} can be formed by

$$\begin{aligned} t_{tw} =& t_f + [\ln((2(1+p) - 0.1)/0.1) - \\ & \ln\left(\frac{2p + 1 + v_{of}}{1 - v_{of}}\right)] C_L/(K_p V_{DD}(1+p)), \end{aligned} \tag{4.9}$$

where v_{of} can be determined from

$$\begin{aligned} v_{of}(t) = 1 - \exp\left(\frac{K_p V_{DD}(-1-p)^2}{2 s_f C_L}\right) / \Bigg[& \frac{\exp\left(\frac{K_p V_{DD} v_{opsl}^2}{2 s_f C_L}\right)}{v_{opsl}} \\ + \sqrt{\frac{K_p V_{DD}\pi}{8 s_f C_L}} \operatorname{erf}\left(\sqrt{\frac{K_p V_{DD} v_{opsl}^2}{2 s_f C_L}}, \sqrt{\frac{K_p V_{DD}(-1-p)^2}{2 s_f C_L}}\right) \Bigg]. \end{aligned} \tag{4.10}$$

Case B: $v_{opsl} \ge v_{of}$

$$t_{psl} = t_f - \frac{2pC_L}{K_p V_{DD}(1+p)^2} + \frac{1+p}{3 s_f}, \tag{4.11}$$

$$t_{tw} = t_{psl} + \frac{\ln\left[(2(1+p) - 0.1)/0.1\right] C_L}{K_p V_{DD}(1+p)}. \tag{4.12}$$

In addition, it is easy to derive that $I_{psat} = K_p(s_f t_{psl} + v_t)^2/2$, and $t_{pon} = v_{tp}/s_f$. Since the remaining parameters in Eq. (4.2) are given by Eq. (4.7) to (4.12), the expressions for all parameters needed in the models are available.

4.2.2 Validation of the model

The proposed GAP model is verified by comparing its predictions with HSPICE simulations on the schematic in Fig. 4.3(a). A 0.18 μm CMOS process with 0.34 μm option is used for the verification. Successful verifications with different capacitive loads, transistor sizes and falling times have been conducted. For the verification shown here, the widths of the PMOS and the NMOS are 0.68 μm and 0.34 μm respectively, and both of them have the same length of 0.34 μm. The HSPICE model used in the verification is level 49. The related parameters are: $K_p = 4.75 \times 10^{-5}$, $V_{tp} = -0.66\,\mathrm{V}$, $V_{DD} = 3.3\,\mathrm{V}$ and $t_f = 5\,\mathrm{ns}$. To evaluate the model in both the case A and case B scenarios, C_L is set as 0.3 and 1 pF, respectively. It should be noted that Eq. (4.7) to (4.12) are functions of the term $K_p V_{DD}/C_L$, which means that the inverters having the same V_t, input voltages and $K_p V_{DD}/C_L$ generate switching currents with the same t_{pon}, t_{psl} and t_{tw}. Thus the example shown here represents a group of general scenarios. The simulated and modeled results for case A and case B are shown in Fig. 4.4 and Fig. 4.5, respectively.

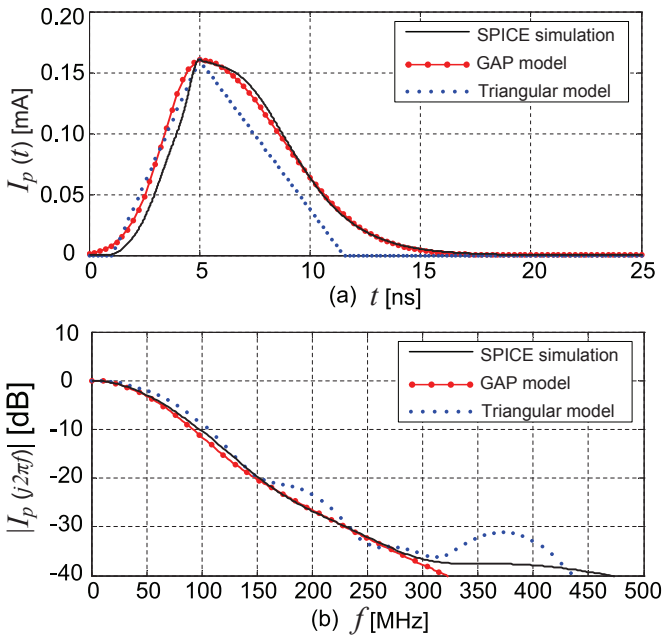

Figure 4.4: Modeled and simulated results for the capacitively loaded ($C_L = 0.3$ pF) inverter in Case A. (a) time domain, (b) frequency domain.

The normalized Fourier transforms of the switching currents are also shown. It can be

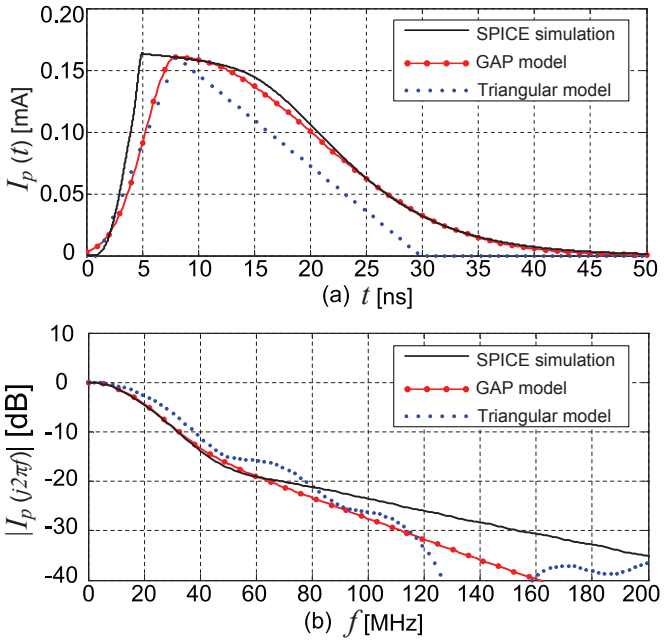

Figure 4.5: Case B: (a) The modeled and simulated switching current of the individual inverter in time domain, and (b) frequency domain. $C_L = 1$ pF in this case.

seen that both the triangular model and the GAP model match the simulation results well at low frequencies, and it is obvious that the estimation errors at high frequencies are clearly reduced in the GAP model as expected.

4.2.3 Test chip

To experimentally validate the proposed model, the model has been practically applied to predict the switching noise generated by a capacitively loaded inverter implemented using a lightly doped CMOS process (20 Ω-cm). The microphotograph of the test chip is shown in Fig. 4.6.

The PMOS and NMOS devices in the inverter are 600 μm and 300 μm wide respectively, and both transistors have the same length of 0.34 μm. The reason for using such fairly large transistors is to generate enough switching noise to enable measurements. In this case, $K_p = 0.04$, and $V_{tp} = -0.7$ V. A 20 pF capacitor is connected to the output of the inverter as a load. In the measurement, the inverter is driven using an periodic square wave signal as $V_{in}(t)$. It has a high and a low voltage level of 3.3 V and 0 V, and it is fed using a G-S-G probe connected to a signal generator. The DC supply voltage is 3.3 V, and it is fed to the on-chip digital supply and ground using DC probes. When the inverter is switching due to the square wave, the switching noise in the test chip is measured at the noise observation point using a G-S-G probe connected to a spectrum

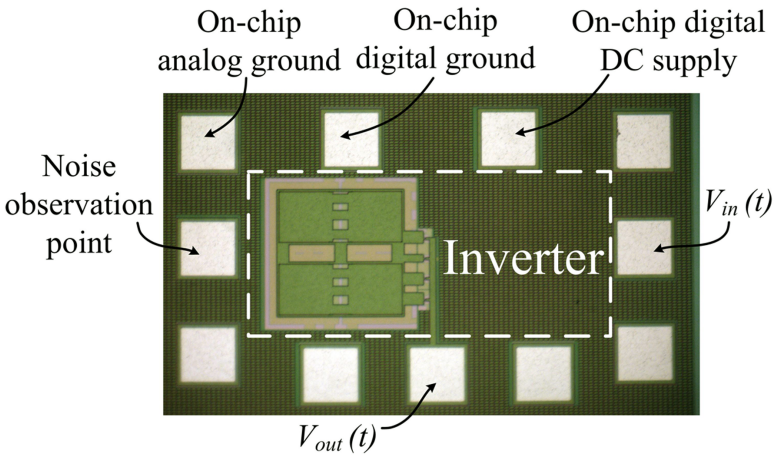

Figure 4.6: Microphotograph of the test chip.

analyzer. The observation point is an ohmic contact connected to the substrate [42]. During the measurements, the spectrum analyzer is set to have a low displayed noise floor (around -90 dBm in this case) to measure as much as possible of the low powered switching noise. Since the input signal is periodic, the switching noise is periodic as well. Thus the switching noise could be represented as a summation of harmonics in frequency domain

$$V_{sub}(j\omega) = \sum_{k=-\infty}^{+\infty} \frac{2\pi H(j\omega) I_p(j\omega)}{T} \delta(\omega - \frac{k2\pi}{T}), \tag{4.13}$$

where $I_p(j\omega)$ is the Fourier transform of $I_p(t)$ in Eq. (4.2). $H(j\omega)$ is as expressed in Eq. (4.1) and it can usually be derived based on parameters extracted from the layout and bonding wires [11, 37]. T is the period of the input signal and k is an integer. Based on Parseval's theorem, the term

$$\left| \frac{1}{T} H(jk2\pi/T) I_p(jk2\pi/T) \right|^2, \tag{4.14}$$

is the average power of the switching noise at its k(th) harmonic. In this study, $H(j\omega)$ is simplified as a purely resistive network since the measurement is on-wafer and no bonding wires and on-chip decoupling capacitors are used. Hence $H(j\omega)/T$ only effects the magnitude of the switching noise but not the spectral envelope, which is given by the term $I_p(j\omega)$. Thus the measured PSDs of the switching noise can be compared with the calculated magnitudes of the harmonics to verify the proposed model. Measurements with different signal frequencies (from 20 to 50 MHz) and different falling times have been conducted. By comparing v_{opsl} and v_{of} obtained from Eq. (4.8) and (4.10) respectively, the GAP model of case A is applicable in this test. Thus corresponding equations of case A are used for obtaining $I_p(j\omega)$. A comparison of measurement results, the triangular model and the GAP model is shown in Fig. 4.7.

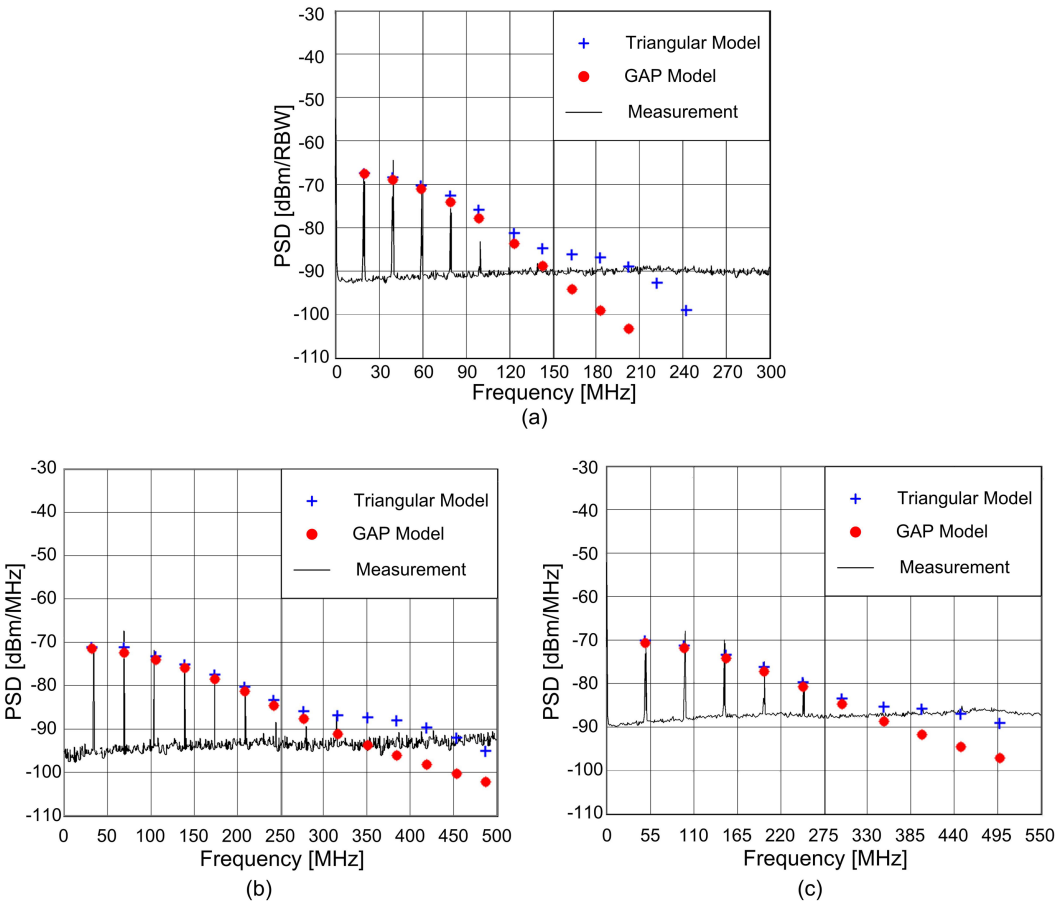

Figure 4.7: Measured PSDs and modeled harmonics of the switching noise. (a) f_{clk}=20 MHz, t_f=22 ns, RBW=500 kHz; (b) f_{clk}=35 MHz, t_f=9.3 ns, RBW=100 kHz; (c) f_{clk}=50 MHz, t_f=7.8 ns, RBW=1 MHz.

The harmonics with the highest magnitude of the models are normalized to the magnitude of the first harmonic of the measured switching noise. It can be seen that the GAP model matches the measured results quite well as it is within 4 dB for all measured switching noise components in the three cases. Moreover, the GAP model is more accurate than the triangular model at high frequencies. This is shown in Fig. 4.7(a) at the frequency of 100 MHz and Fig. 4.7(b) at the frequency of 285 MHz. For higher frequencies, the switching noise drops below the noise floor of the spectrum analyzer. But the harmonics of the triangular model are higher than the noise floor at these frequencies, which also indicates the larger estimation errors in the triangular model.

4.3 The statistic model

In large scale digital circuits, there are numerous gates switching with varying delays on the chip. For synchronized digital circuit, the switching currents are aligned at the edge of the clock with random amplitudes and random time delays. For such a scenario the substrate noise is a sum of these signals, and can not be simply modeled by a periodic switching current pulse as shown in Fig. 4.8.

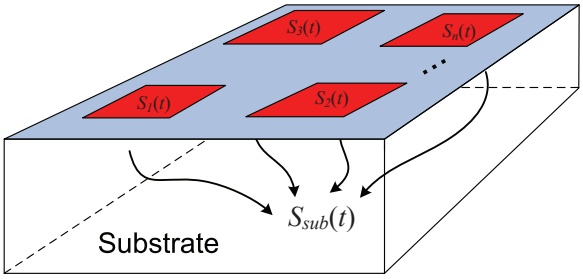

Figure 4.8: Coupling mechanism of switching noise in large scale digital blocks.

A statistic model is proposed to solve the problem. This model is based on the assumption that all switching current sources can be represented by a common pulse function yet with random magnitudes and random time delays. This assumption is based on the fact that identically sized inverters are widely used in large scale digital blocks. And the driving signal and load condition for these inverters are usually similar as well. Hence the switching currents generated by these inverters are expected to be similar to each other. Based on the assumption, the noise coupling mechanism shown in Fig. 4.9(a) in large scale digital blocks can be approximated as a multi-path coupling model with single noise source as shown in Fig. 4.9(b). In the figure, $S_u(t)$ is the mean of the switching noises, and $H_i(t)$ is the sub-transfer function describing the random attenuation and delay of the switching noises.

Using the equivalent multi-path model, the substrate noise $S_{sub}(j\omega) = S_u(j\omega) \times H(j\omega)$,

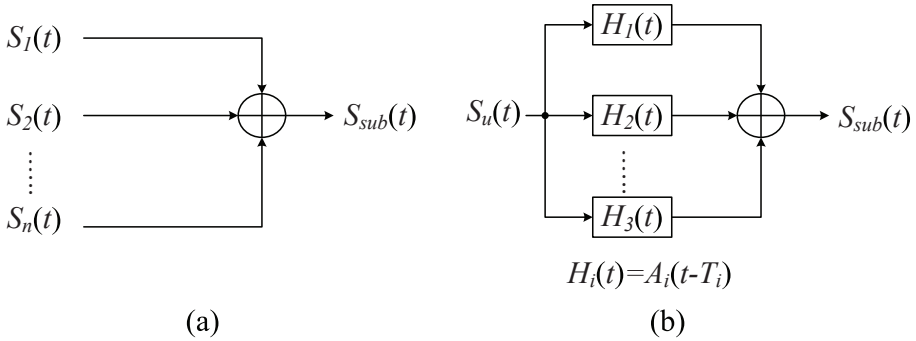

Figure 4.9: The (a) original switching noise and (b) the equivalent multi-path coupling model.

where $H(j\omega)$ is the total transfer function of the coupling. The total transfer function is expected to have frequency selective feature since the sub-transfer functions have random attenuations and delays. And the frequency bandwidth between two adjacent notches is the reciprocal of the maximal relative delay of the multiple switching current sources.

Monte Carlo simulation in Matlab is used to verify the equivalent multi-path model. Fig. 4.10(a) shows the simulated switching noise of a 10K-gate digital block with random amplitude attenuation and time delay. Its Fourier transform is shown in Fig. 4.10(b).

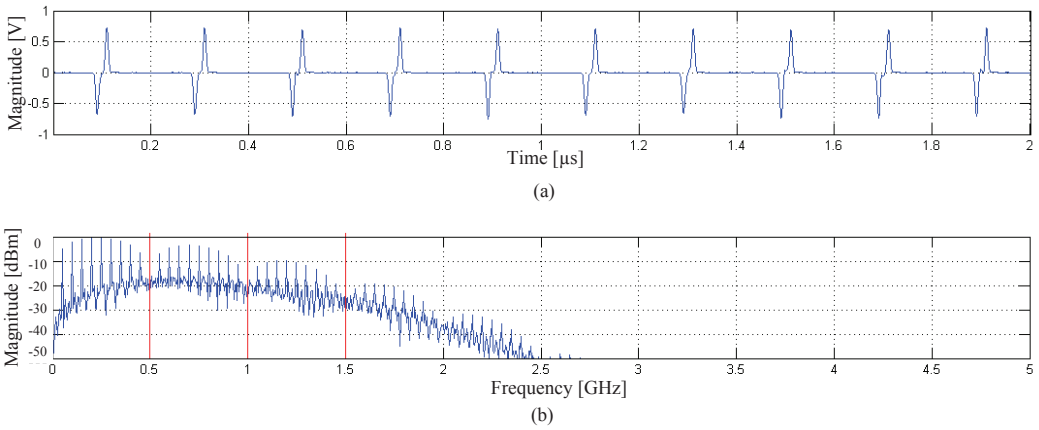

Figure 4.10: Simulated switching noise for a 10K-gate digital block with random amplitude attenuation and time delay. (a) simulated switching noise in time domain, and (b) in frequency domain.

It can be seen that the spectrum of the switching noise has a clear frequency selective feature. In this case, the maximal relative delay is 2 ns, and it is clear that the frequency

band between adjacent frequency notches is 500 MHz as expected.

The equivalent multi-path model is also verified by SPICE simulation. An inverter chain block shown in Fig. 4.11 is used for the simulation. A 0.18 μm CMOS process is used. Minimum width and length are used for all the NMOS in the inverters. PMOS in all the inverters is twice bigger than the corresponding NMOS. C_{li} represents the parasitical capacitance at the output of the inverters. Fig. 4.12 shows the PSD of the switching noise in the inverter chain block. The simulated maximal relative delay is 216 ps, and the calculated notch location is 4.6 GHz. It can be seen that the calculated notch location is consistent with the simulation results.

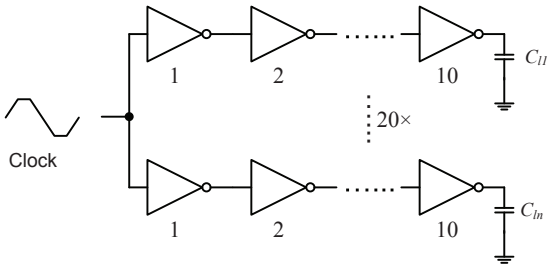

Figure 4.11: The schematic of the inverter chain block for the simulation of switching noise.

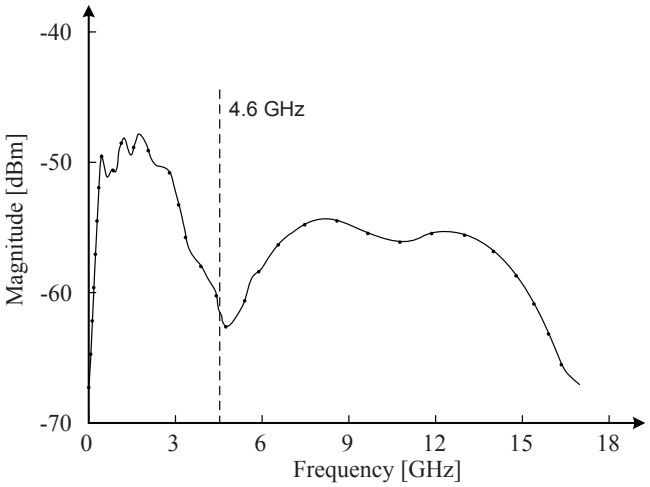

Figure 4.12: The SPICE simulation of PSD of the switching noise generated by the circuit shown in Fig. 4.11.

4.4 Conclusion

This chapter presents two modeling methods for switching noise in both small and large scale digital circuits. The novel analytical model for simple digital circuit provides a

detailed understanding of the generation and propagation of switching noise in lightly doped CMOS technologies. The spectral envelope of the switching noise can be easily predicted using the proposed model. Closed-form expressions for calculating the parameters in the conventional triangular model are also provided. The model is validated by both SPICE simulations and measurement results from a test chip fabricated in a lightly doped CMOS process. Good agreement is found between the model and simulations as well as measurement results. With this model, the simulations needed when using traditional approaches can be avoided. This can help to achieve a scalable analytical switching noise model for digital blocks. This model especially holds the advantage for estimating the switching noise when big size buffers are dominating the noise generation.

An equivalent multi-path coupling model is proposed to characterize the switching noise in large scale synchronized digital circuits. This model is capable of achieving fast results since analysis can be easily done using Monte Carlo simulation in Matlab.

Chapter 5

Substrate Noise Suppression and Isolation

5.1 Introduction

Various of methods have been proposed over time for the isolation and suppression of the substrate noise in mixed-signal ICs [43–48]. These methods can generally be divided into two categories. One is passive approaches, including physical separation, guard rings or deep N wells. The passive methods are practically feasible. However, they usually suffer the drawbacks of area consuming, uncertainty of the isolation level and high cost. The other method is active cancelation. Active cancelation is proposed to achieve a low cost yet effective substrate noise suppression. The basic idea in this method is to cancel the substrate noise at the RF area by injecting an anti-phase signal produced by an active cancelation circuit. As shown in Fig. 5.1, $V_{sno}(t)$ is the original substrate noise generated by the digital circuits. $V_{snc}(t)$ is the signal generated by the active cancelation section, and $V_{snt}(t)$ is the total substrate noise beneath the RF circuit. If $V_{snc}(t) = -V_{sno}(t)$ at a location, $V_{sno}(t)$ can be totally canceled and $V_{snt}(t)$ is reduced to zero at such location. However, the result is not as expected. Due to the fact that the signal propagation in the substrate noise is layout dependent, the location where $V_{snt}(t)$ can be reduced is significantly based on the specific layout. If the layout is not properly designed, the substrate noise could be increased other than reduced. This degrades the feasibility of the method. In addition, owing to the limited frequency band of the active cancelation circuit, this method only feasible for low frequency substrate noise suppressions.

This chapter presents a novel active suppression technique for substrate noise in mixed-signal ICs. The analytical modeling of guard rings for substrate noise isolation in lightly doped substrates is also presented. In the proposed active suppression technique, an active spectrum shaping section is used to generate extra switching currents to modify the shape of the original switching noise in both time domain and frequency domain.

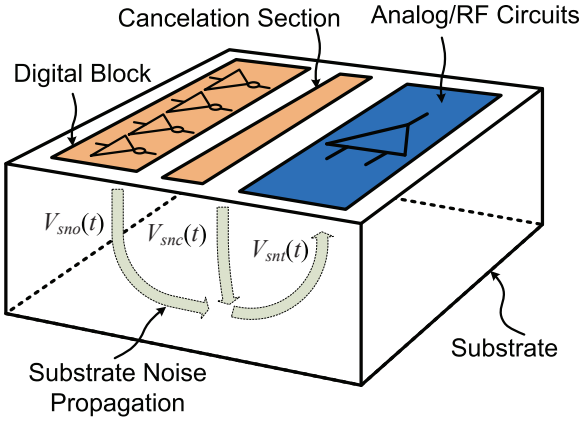

Figure 5.1: The propagation mechanism of the substrate noise from the digital block to the analog/RF block sharing the same chip, and the illustration of the proposed active suppression technique.

The relative time delays of these switching currents to the original switching current are realized by controllable delay lines. The pulse widths and magnitudes of the switching currents are also controllable. By manipulating the extra switching currents, the spectrum of the total switching noise can be shaped to have a suppressed magnitude at desired frequencies. In the work of the analytical modeling of guard rings for substrate noise isolation, the goal is to find a simple yet accurate model describing P^+ guard rings. A resistive T network is proposed in this work, and closed form expressions for the calculation of spreading resistance in the network are presented. Using this model the effects of the layout parameters can be taken into account during the pre-layout design phase, and the isolation performance of the design can be accurately predicted.

This chapter is organized as follows. Section 5.2 presents the active suppression technique for reducing of substrate noise generated by digital circuits. Section 5.3 presents the modeling and verification of P^+ guard rings in lightly doped substrates. Conclusion is drew in Section 5.4.

5.2 Active suppression of switching noise in mixed-signal integrated circuits

In the presented technique, an active cancelation section is used to generate an extra switching current. This switching current has intended relative time delay to the original switching current. The pulse width and magnitude of the switching current are also adjustable by biasing voltages. Due to the relative time delay, the extra switching current is out-of-phase to the original switching current at specific frequencies. Thus by adjusting the time delay, pulse width and magnitude of the extra switching current, the original switching current can be suppressed at desired frequencies.

Figure 5.2 shows the diagram of the active cancelation section and its connection with clock and DC supply. It comprises three subsections, the delay control unit (DCU), the width control unit (WCU) and the magnitude control unit (MCU). The MCU is used to generate the major part of the extra switching current, and the magnitude of the switching current can be controlled by the controlling voltage V_{mp} and V_{mn}. The DCU and the WCU are used to adjust the time delay and pulse width of the switching current, respectively. V_{dn} is for controlling the time delay, while V_{wn} and V_{wp} are for controlling the pulse width. The active cancelation section is driven by the same clock driving the digital circuit, so that the extra switching current can be aligned to the original switching current with the desired time delay.

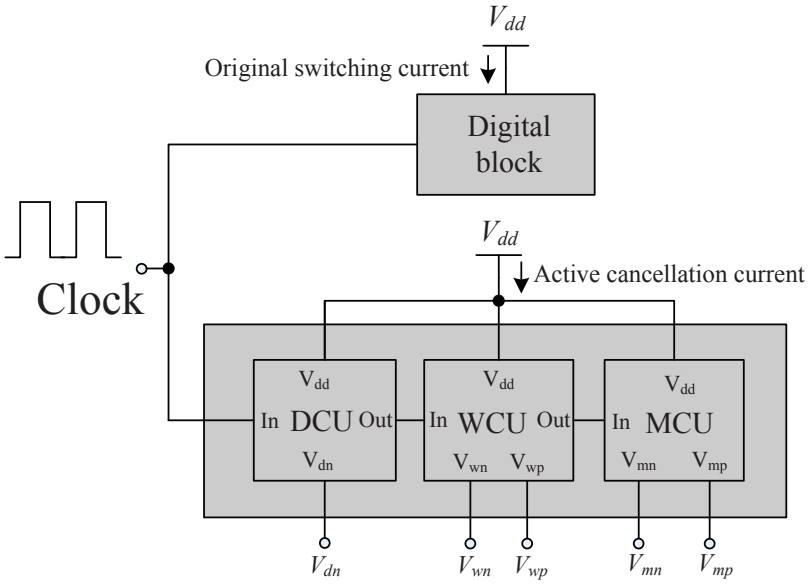

Figure 5.2: The circuit diagram of an active suppression circuit for the IC in Figure 5.1.

5.2.1 Theory

The switching current generated by a digital block could be represented by a triangular waveform. One of such current in a single cycle is shown as $I_{sno}(t)$ in Fig. 5.3 The basic idea in this study is to inject an extra current signal $I_{snc}(t)$ to cancel $I_{sno}(t)$ in desired frequency band. $I_{snc}(t)$ has a relative delay of $T_1 - T_0$. Thus the total switching current is given as

$$I_t(t) = I_{sno}(t - T_0) + I_{snc}(t - T_1), \tag{5.1}$$

and its Fourier transform is

$$I_t(j\omega) = I_{sno}(j\omega)e^{-j\omega T_0} + I_{snc}(j\omega)e^{-j\omega T_1}, \tag{5.2}$$

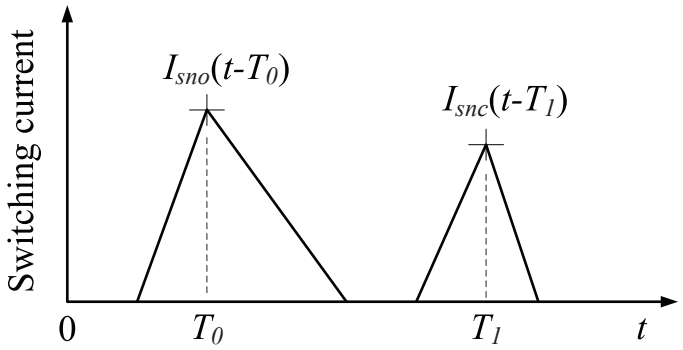

Figure 5.3: Illustration of switching currents involved in the proposed suppression method. The original switching current, I_{sno}, is combined with a cancellation current, I_{snc}, to achieve a suppression.

where $I_{sno}(j\omega)$ and $I_{snc}(j\omega)$ are the Fourier transform of $I_{sno}(t)$ and $I_{snc}(t)$, respectively. $I_t(j\omega)$ can be further written as

$$I_t(j\omega) = e^{-j\omega T_0}[I_{sno}(j\omega) + I_{snc}(j\omega)e^{-j\omega(T_1-T_0)}]. \tag{5.3}$$

At the desired substrate noise suppression frequency

$$\omega_0 = (2k+1)\pi/(T_1 - T_0) \quad for \quad k = 0, 1, 2... \tag{5.4}$$

It has

$$|I_t(j\omega_0)| = |I_{sno}(j\omega_0) - I_{snc}(j\omega_0)|. \tag{5.5}$$

Thus if I_{snc} has similar magnitude and pulse width as I_{sno}, I_{sno} could be significantly suppressed at ω_0.

5.2.2 Validation of the method in Matlab

The proposed method has been validated by Matlab simulations. One of the simulations is shown in Fig. 5.4. The original switching current $I_{sno}(t)$ is shown by the solid line in Fig. 5.4(a). It has a rising time of 100 ps and a falling time of 300 ps. Its magnitude is normalized to 1 A. The active cancelation current $I_{snc}(t)$ with three different magnitudes are also shown in Fig. 5.4(a). The active cancelation currents have the same rising and falling time as the original current. In this simulation, the desired suppression frequency is at 5 GHz. Thus the relative delay between $I_{snc}(t)$ and $I_{sno}(t)$ is set as 100 ps. Fig. 5.4(b) and Fig. 5.4(c) show the total switching current with three different cancelation currents in time domain and frequency domain, respectively. It is clear that the original switching current is significantly suppressed at the desired frequency. The -10 dB suppression band is wider than 500 MHz for all the three cases.

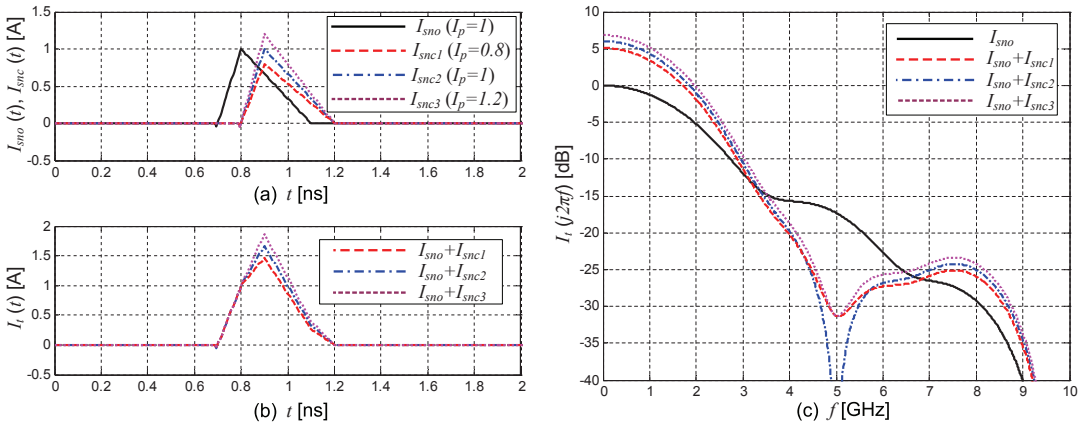

Figure 5.4: Simulated results of the suppression of substrate noise using cancelation currents with three different magnitudes.

The scenarios with different relative delays are also studied. The simulation results are shown in Fig. 5.5.

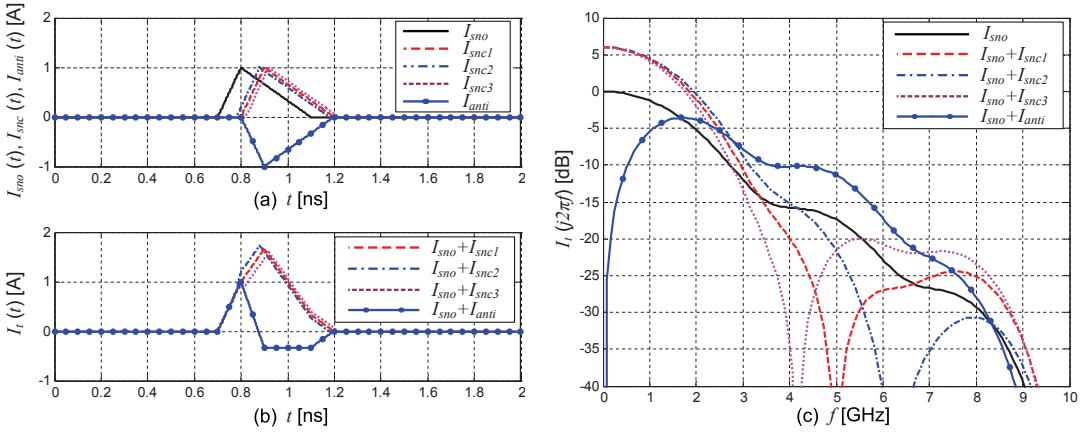

Figure 5.5: Simulated results of the suppression of substrate noise using cancelation currents with three different relative delays. The time delay between I_{sno} and I_{snc1} to I_{snc3} are 80 ps, 100 ps and 120 ps, respectively. The time delay between I_{sno} and I_{anti} is 100 ps.

The original switching current $I_{sno}(t)$ is shown by the solid line in Fig. 5.5(a). It is as the same as that in Fig. 5.4(a). The active cancelation current $I_{snc}(t)$ with three different relative delays are also shown in Fig. 5.5(a). The active cancelation currents have the same magnitudes as the original current. In this simulation, the desired suppression frequency is also at 5 GHz. Thus the desired relative delay between $I_{snc}(t)$ and $I_{sno}(t)$

is 100 ps. Fig. 5.5(b) and Fig. 5.5(c) show the total switching current with three different cancelation currents in time domain and frequency domain, respectively. The suppression of the original switching current is clear even though there are undesired offsets in the relative delay in I_{snc2} and I_{snc3}. A time-delay sensitivity demonstration of the conventional anti-phase cancelation approach with undesired time delay is also shown in Fig. 5.5. I_{anti} is the delayed anti-phase current to the original switching current. As the conventional anti-phase cancelation method does not control the time delay, the delay can varies drastically due to different circuit topologies, layouts and interconnects. In Fig. 5.5(a), the time delay of I_{anti} is set as the same as the delay of I_{snc2}. It can be seen in Fig. 5.5(c) that the magnitude of the total switching current is significantly but undesirably increased in the frequency band of 2-8 GHz, which indicates the poor application potential of the anti-phase method for UWB applications unless the timing can be well controlled.

5.2.3 Sub-blocks in the active cancelation section

One proposed delay control unit comprised of a number of delay cells (DSs) is shown in Figure 5.6. The delay cell is an inverter with controllable driving capabilities. By controlling the voltage V_{dn}, the propagation delay of the DCU can be adjusted to a desired value. The number of the delay cells is chosen based on the needed total delay time and the delay that each delay cell can introduce. But small transistors should be used in the delay cells to avoid undesired generation of significant switching currents in this subsection.

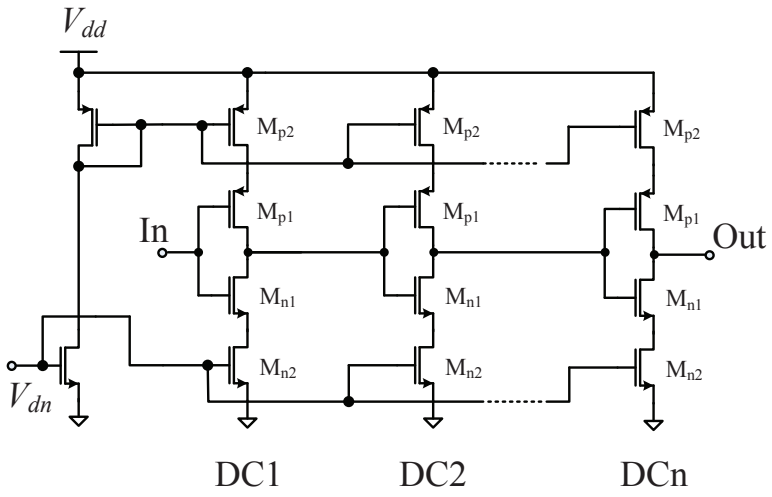

Figure 5.6: Simplified circuit of the delay control unit (DCU).

Another proposed DCU comprised of a number of inverters with tunable capacitive

loads is shown in Figure 5.7. By controlling the voltage V_{dn}, the loads of the inverters can be changed and a desired time delay can be obtained. The number of the inverters is chosen based on the needed total time delay and the delay that each inverter can introduce. Small transistors should be used in the delay cells to avoid undesired generation of significant switching currents in this subsection.

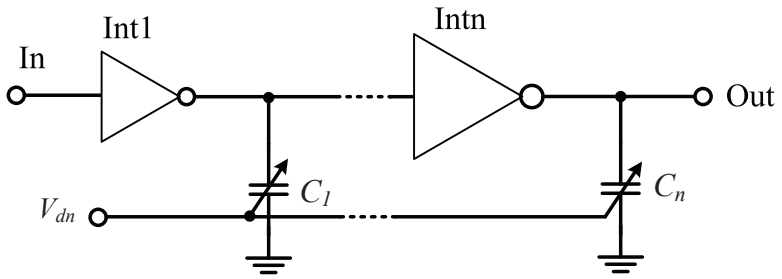

Figure 5.7: Simplified circuit of the delay control unit.

The proposed WCU comprised of one or a number of delay cells is shown in Figure 5.8. By controlling the voltage V_{wn} and V_{wp} the capacity of the WCU to drive the MCU can be adjusted. So that the slop of the input signal to the MCU at the falling or rising edge can be adjusted. As a result, the pulse width of the switching current generated by the MCU can be adjusted to a desired value. The sizes of the transistors in the WCU are chosen based on the size of the MCU and the desired pulse width of the switching current.

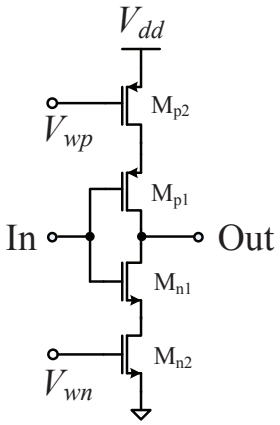

Figure 5.8: Simplified circuit of the width control unit (WCU).

Similarly, the proposed MCU comprised of one or a number of delay cells is shown in Figure 5.9. By controlling the voltage V_{mn} and V_{mp} the magnitude of the generated switching current can be adjusted. The sizes of the transistors in the MCU are chosen based on the desired magnitude of the switching current.

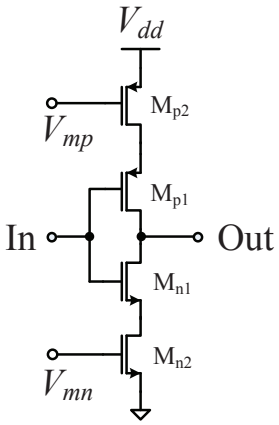

Figure 5.9: Simplified circuit of the magnitude control unit (MCU).

5.2.4 Validation of the method in SPICE

The proposed method is also validated by SPICE simulations. The schematic shown in Fig. 5.2 is used for the simulation and the schematics shown in Fig. 5.6, Fig. 5.8 and Fig. 5.9 are used for the DCU, WCU and MCU blocks, respectively. The digital block is composed of a number of inverter chains, which acts as a switching noise source. The DCU, WCU and MCU are designed based on the information of the original switching current. The controlling voltages of the units are set such that the suppressed switching noise can be achieved at desired frequencies. The simulated results with and without the active suppression are shown in Fig. 5.10 to Fig. 5.12.

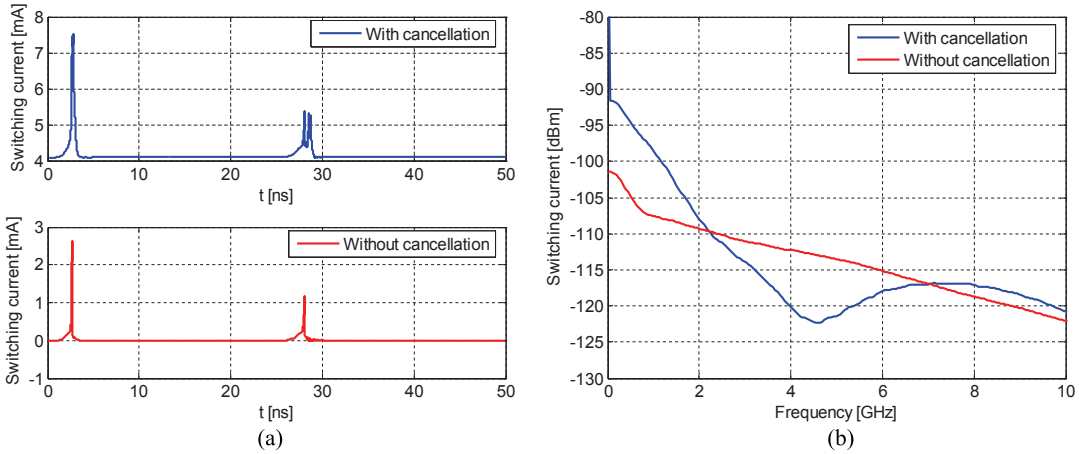

Figure 5.10: The simulated one-cycle switching current with and without active suppression in (a) time domain and (b) frequency domain. The designed relative delay in this case is 110 ps, and the desired notch frequency is 4.5 GHz.

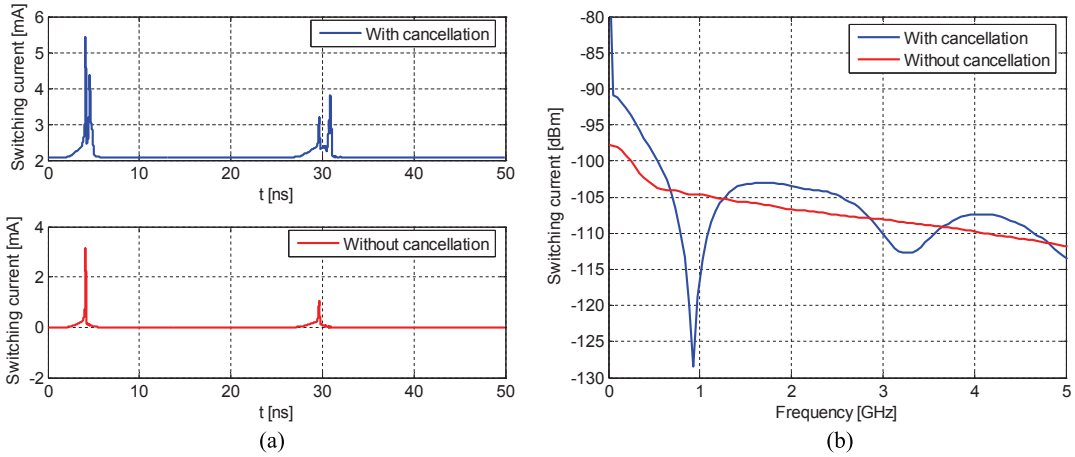

Figure 5.11: Simulated one-cycle switching current with and without active suppression in (a) time domain and (b) frequency domain. The designed relative delay in this case is 500 ps, and the desired notch frequency is 1 GHz.

The switching current without active cancelation is probed at the DC supply of the digital block, while the switching current with active cancelation is probed from the main DC supply for both the digital block and the active cancelation circuits. From the simulations, it can be seen that the switching noise at desired frequencies can be significantly suppressed. The minimal suppression is 10 dB observed in Fig. 5.10, and the best is 27 dB observed in Fig. 5.12. It is also clear that the proposed technique is valid for suppression the switching noise at least from 100 MHz to 3.3 GHz, which is attractive for different applications.

5.2.5 The mutual effects between the design of DCU, WCU and MCU

When designing the active suppression circuits it is desired and needed to have an insignificant mutual effect between the design of controlling voltages for DCU, WCU and MCU. This subsection investigates this effects using SPICE simulations. The schematic used for the SPICE simulations is the same as that in last subsection.

The performance of DCU, WCU and MCU used for the investigation are defined in Fig. 5.13. The relative time delay is defined as the peak to peak time delay between the original switching current and the cancelation current at the falling-input edge. The peak value of the cancelation current is defined as I_p and the pulse width is the time span of the cancelation current at the value of $0.1 \cdot I_p$. It should be noted that the switching current at the falling-input edge of the magnitude controlling unit is much greater than the switching current at the rising-input edge since it consists of both short circuit current and charging current [6]. Thus the greatest concern of this study

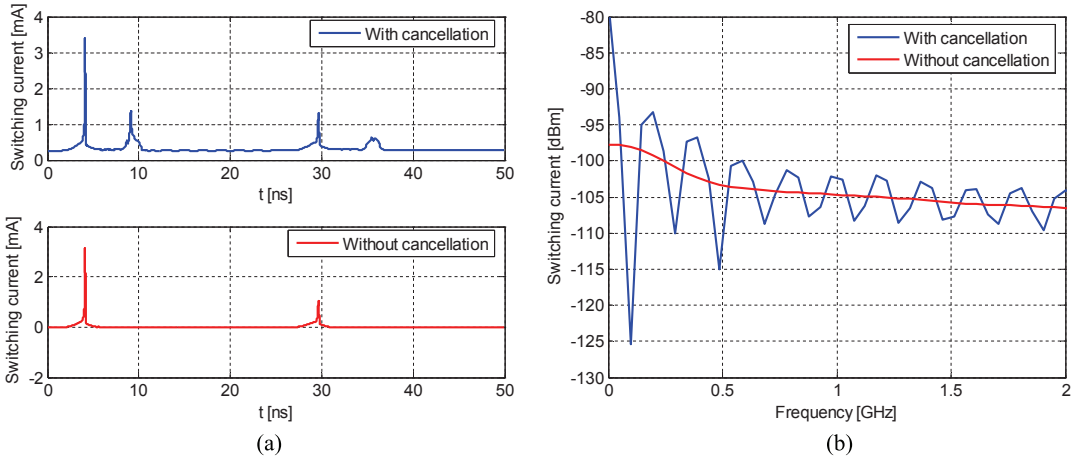

Figure 5.12: Simulated one-cycle switching current with and without active suppression in (a) time domain and (b) frequency domain. The designed relative delay in this case is 5 ns, and the desired notch frequency is 0.1 GHz.

is at the falling-input edge.

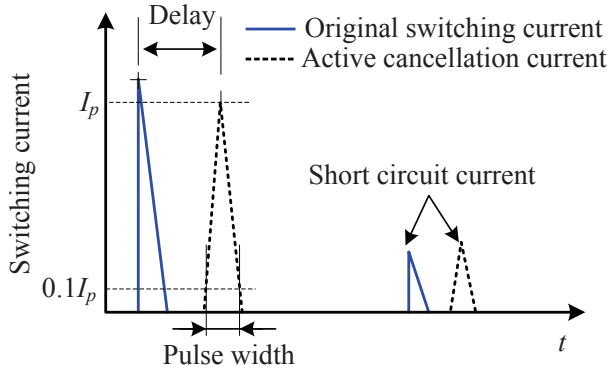

Figure 5.13: The parameter definitions in the SPICE simulation for investigating the mutual effects between the design of DCU, WCU and MCU.

Fig. 5.14 shows the simulated performance of the active cancelation circuits with different values of the control voltages for DCU, WCU and MCU.

It can be seen that V_{wn} has significant effects on the time delay when its value is small (Fig. 5.14(b)). The reason for this is that decreasing V_{wn} to a small value close to the threshold voltage greatly reduces the driving capability of the width control unit, so that increases the time delay. V_{wn} also has effects on I_p. The explanation for this can be found in Chapter 4. It has been shown that changing the value of V_{wn} changes the slope of the signal at the output of WCU (input for MCU) so that affects the magnitude

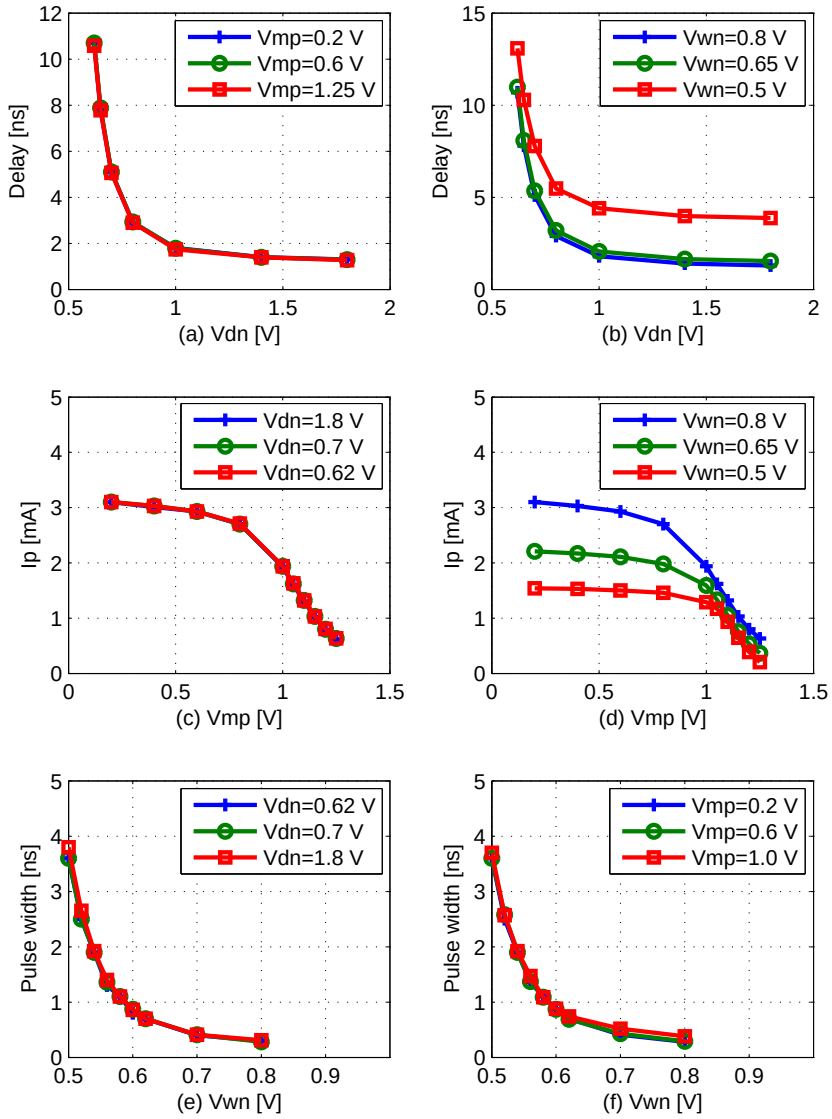

Figure 5.14: Simulated performance of the active cancelation circuit with different values of the control voltages for DCU, WCU and MCU. V_{dd} is 1.8 V, the clock frequency is 20 MHz and the rising/falling time of the clock is 5 ns. Other parameters in the simulations are: (a) V_{mn}=0.65 V, V_{wn}=0.8 V, V_{wp}=0.9 V; (b) V_{mn}=0.65 V, V_{mp}=0.2 V,, V_{wp}=0.9 V; (c) V_{mn}=0.65 V, V_{wn}=0.8 V, V_{wp}=0.9 V; (d) V_{mn}=0.65 V, V_{dn}=0.7 V, V_{wp}=0.9 V; (e) V_{mn}=0.65 V, V_{mp}=0.2 V, V_{wp}=0.9 V; (f) V_{mn}=0.65 V, V_{dn}=0.7 V, V_{wp}=0.9 V.

of the active cancelation current. Apart form V_{wn}, other control voltages are shown to have insignificant mutual effects.

Based on the SPICE simulation results, the sequence of the design for DCU, WCU and MCU can be proposed, which is design V_{wn} first, and then design V_{mp} and V_{dn}.

5.3 Compact modeling of guard rings for substrate noise isolation

To protect the sensitive analog/RF circuits from the interferences of the substrate noise, different types of guard rings and combinations with deep N-Wells have been proposed [43, 44]. Owing to the feature of low cost and easy to design, P^+ guard ring is one of the most widely used passive structures for substrate noise suppression references. Fig. 5.15 shows a typical P^+ guard ring structure used for substrate noise suppression.

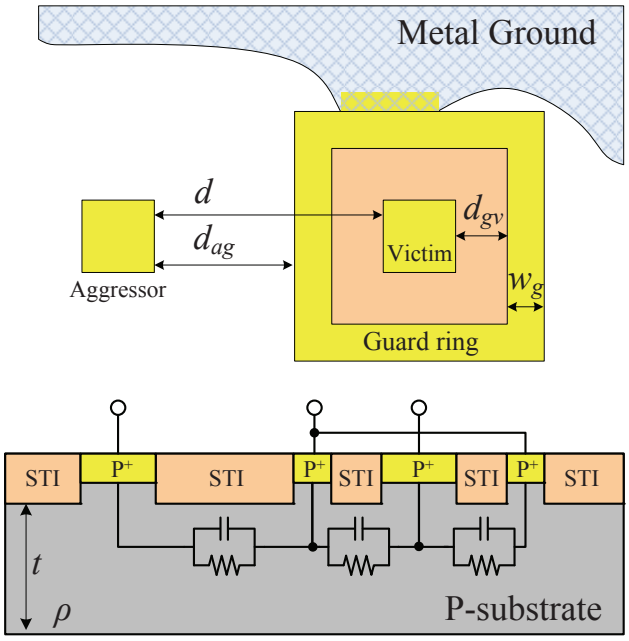

Figure 5.15: The typical layout of a P^+ guard ring used for substrate noise suppression.

Based on the fact that the coupling through diffusion areas dominates the coupling of substrate noise, the noise source and noise receiver are simplified to rectangular P^+ contacts. In the figure, the rectangular P^+ Aggressor contact represents the coupling node of the noise source generated in digital circuits. The Victim contact represents the coupling node of any sensitive analog/RF circuits. Due to the conductive substrate, the

switching noise injected at the aggressor can be coupled to the victim and deteriorate the performance of the circuit connect to it. To minimize the effect a P^+ guard ring with a width of w_g is usually put around the victim. The guard ring should be connected to the on-chip ground, so that a part of the substrate noise can be lead to ground before it reaches the victim. The noise suppression performance of the guard ring is highly dependent on the layout parameters including the aggressor-to-victim distance, guard ring-to-victim distance, guard ring width, resistivity of the substrate and the size of the aggressor and victim. Calculating the spreading resistance of contacts on substrates is a mixed-boundary value problem. The typical solutions are in integral forms or infinite series, which is less useful. A number of efforts have been made to characterize the guard rings by compact modeling of spreading resistance of contacts [38, 49–51]. However, most of the previous work are based on experiments. When a design on finite-thickness substrate, a feasible and accurate model is still unavailable.

This section presents a novel analytical model of guard rings implemented on finite-thickness substrates. The aggressor-guard ring-victim layout is modeled using a resistive T network. Equations are proposed to characterize the effects of the layout parameters on the values of the resistances in the network. The proposed model has been validated by EM simulations. A test chip in a standard 0.18 μm CMOS process is also designed for experimental verification. Good agreement between the model and the measured results is found.

5.3.1 Spreading resistance modeling of contacts and guard rings

In this subsection, the aggressor, guard ring and victim shown in Fig. 5.15 are modeled using a three-port network as shown in Fig. 5.16.

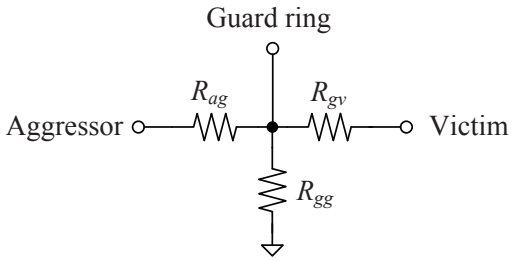

Figure 5.16: The proposed resistive T network for the modeling of the P^+ guard ring as shown in Fig.5.15.

The coupling between different ports is assumed to be purely resistive. This assumption has been widely used and it makes the analysis easier. As shown in Fig. 5.16 the resistor R_{ag} is used to model the spreading resistance between the aggressor and the guard ring. The resistor R_{gv} is used to model the resistance between the guard ring

and the victim. R_{gg} is the resistance between the guard ring and the on-chip ground reference, which results from the none-zero resistivity of the P^+ diffusion area and interconnects. In this section, the equations for calculating R_{ag} and R_{gv} are presented. The analysis is firstly conducted on circular contacts and rings since direct analysis on square contacts is difficult. Then the results are applied to square contacts and rings using simple transformations. The value of R_{gg} usually depends on the sheet resistance of P^+ diffusions and interconnects, as well as the layout. Thus a discussion on the calculation of R_{gg} for a specific layout is not so informative for other designs and consequently is not included in this study.

5.3.1.1 Spreading resistance of Rag

This subsection presents the equation of R_{ag}. The spreading resistance of a circular contact on an infinitely thick substrate is discussed first. Following this the crowding effects caused by the infinite thickness of practical substrates are discussed and a scaling factor is proposed as a mean to correct for crowding effects. In the similar way, the expression for the spreading resistance of guard rings on substrate with finite thickness is proposed. By combining the results for the circular contact and guard ring, the equation of R_{ag} is achieved.

Fig. 5.17 (a) shows the typical electric potential field of a circular contact with a radius of r_a on a uniformly doped substrate with infinite thickness. As a current is fed into the aggressor and collected from the equipotential surface at infinite, confocal ellipsoidal equipotential surfaces are built around the aggressor. Assuming zero thickness of the contact, the equipotential surfaces at the distance d from the contact can be expressed as [52]

$$V(d) = \frac{I\rho}{2r_a}\left[1 - \frac{2}{\pi}\arcsin\left(\frac{r_a}{r_a + d}\right)\right], \tag{5.6}$$

where I is the current flowing into the contact, and ρ is the resistivity of the substrate.

Thus the spreading resistance of the contact is

$$R_a = \frac{\rho}{2r_a}\left[1 - \frac{2}{\pi}\arcsin\left(\frac{r_a}{r_a + d}\right)\right]. \tag{5.7}$$

It should be noted that the equation is based on the assumption of an infinite substrate plane. But this is not the case in practical designs. Fig. 5.17 (b) illustrates the electric potential field and the current flow when the thickness of the substrate is comparable to the size of the contact. It can be seen that for the current at the near field, it is significantly constricted, and the horizontal effect is relatively unobservable. But the currents at far distances become clearly horizontal and constriction effects are

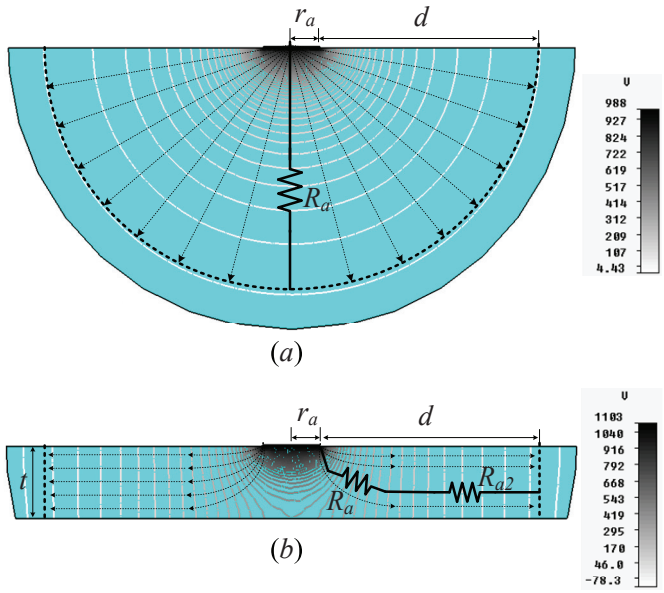

Figure 5.17: 3D EM simulation illustrating the typical electric potential field of a circular contact on (a) an infinite substrate and (b) a substrate with finite thickness.

insignificant. Based on the two different current distributions, the resistance of the contact is assumed to have two terms characterizing the near and far field resistance, respectively. The resistance at far field is simply a resistance of a ring disk, and its expression can be easily derived as

$$R_{a2} = \frac{\rho}{2\pi t} \ln\left(\frac{d + 4r_a}{4r_a}\right). \tag{5.8}$$

It is clear that Eq. (5.8) is zero if the thickness $t = \infty$. This is reasonable since the horizontal effect vanishes for an infinite substrate. It is also noticed that Eq. (5.8) is infinite if $t = 0$. This also makes sense as there is no path for the current to flow in this case.

For the near field, the expression of the spreading resistance is proposed as

$$R_a = K\frac{\rho}{2r_a}\left[1 - \frac{2}{\pi}\arcsin\left(\frac{r_a}{r_a + d}\right)\right], \tag{5.9}$$

where the current crowd effects due to the finite thickness substrate is described by the correction factor K, which has the expression of

$$K = \frac{t + r_a/\alpha}{t}. \tag{5.10}$$

Fig. 5.18 shows the value of K and normalized R_a without correction versus t/r_a. It can be seen that the normalized R_a is saturated close to 1 when t is significantly larger than r_a. This means that the effect of the thickness t is insignificant when it is greatly larger than r_a. Thus K should be close to 1 in this case. In addition, R_a without correction is zero when $t = 0$. But the real R_a should be infinite since there is no path for the current to flow horizontally, indicating that K should be infinite to correct the effect in this case. It is clear that the proposed K has the desired feature, and α determines the correction level. When α is relatively small, the correction is too much since K is not close to 1 even though t/r_a is high. It also could be an under-correction when α is relatively big and K is close to 1 even for a small t/r_a. In this study, α is set as 4, so that $K \approx 1.1$ when R_a without correction is around 0.8.

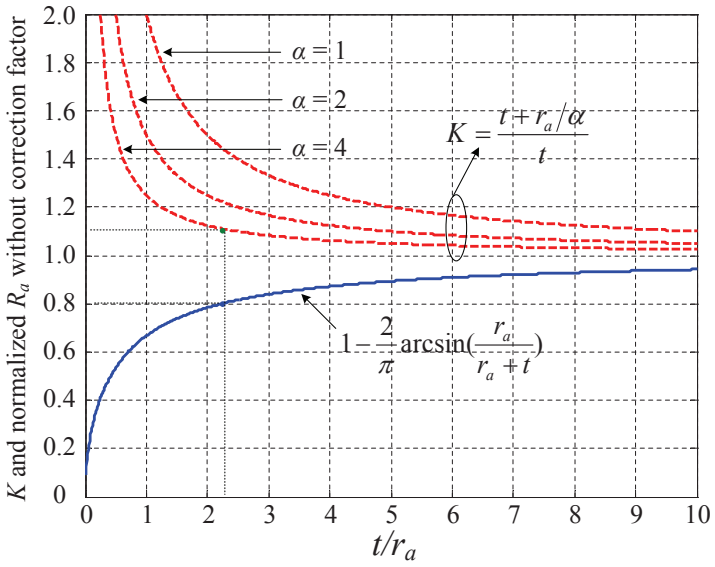

Figure 5.18: The correction factor K and normalized R_a without correction versus t/r_a.

Similarly, the electric potential field of a P^+ guard ring on an infinite substrate is shown in Fig. 5.19 (a). It can be seen that the equipotential surfaces around the guard ring is similar to that of the aggressor at far distances. But at the near field, the equipotential surfaces become confocal tube surfaces around the strip of the guard ring. Thus a simplification is proposed as shown in Fig. 5.20 for the manipulable analysis of the resistance caused by this effects. In Fig. 5.20, the spreading resistance of the guard ring consists of a near field resistance R_{g1} and a far field resistance R_{g2}. R_{g2} has a similar feature to the spreading resistance of the circular contact, and hence Eq. (5.9) can be used to calculate R_{g2}.

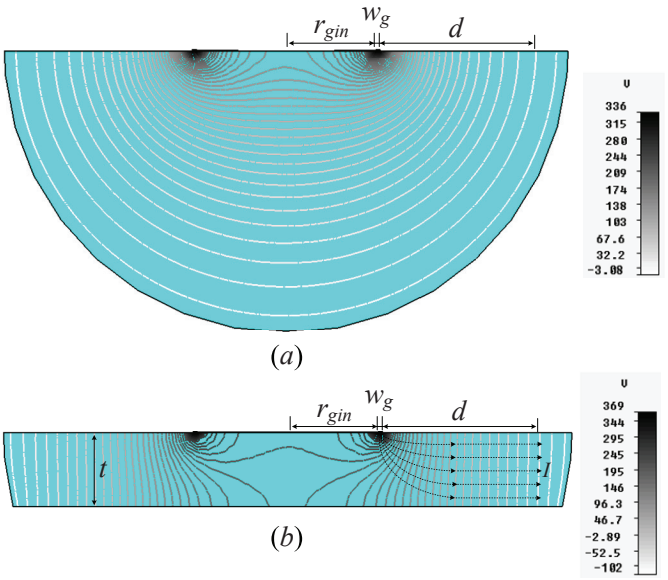

Figure 5.19: The typical electric potential field of a circular P^+ guard ring on (a) an infinite substrate and (b) a substrate with finite thickness.

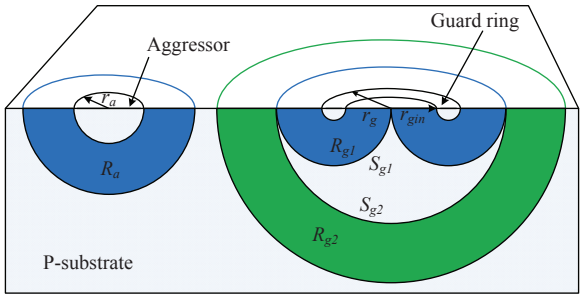

Figure 5.20: Simplified spreading resistance of the circular guard ring.

The equation for R_{g1} is derived as given below

$$R_{g1} = \frac{\rho}{(r_g + r_{gin})\pi^2} \ln\left(\frac{r_g + r_{gin}}{r_g - r_{gin}}\right). \tag{5.11}$$

This equation is derived base on an assumption of uniform current distribution in the near field. With R_{g2} given by

$$R_{g2} = K\frac{\rho}{2r_g}\left[1 - \frac{2}{\pi}\arcsin\left(\frac{r_g}{r_g + d}\right)\right], \tag{5.12}$$

and

$$K = \frac{t + r_g/4}{t}, \tag{5.13}$$

the spreading resistance of the guard ring can be found by

$$R_g = R_{g1} + R_{g2}. \tag{5.14}$$

It obvious that when $r_{gin} = 0$ the guard ring becomes a circular contact. In this case R_{g1} is found to be zero in Eq. (5.11), and R_g has the same expression as R_a as expected. It should be noticed that the current between the aggressor and guard ring is mainly constricted in the area between them [50]. This area is smaller than that in the case of standing alone contacts, and the constriction increases the spreading resistance. In this study, this constricted area is approximated as three fourth of the area for standing alone contacts. Thus R_{ag} should be 4/3 times higher, and R_{ag} in Fig. 5.16 can then be given by

$$R_{ag} = \frac{4}{3}(R_a + R_{g1} + R_{g2}). \tag{5.15}$$

5.3.1.2 Spreading resistance of Rgv

Similar to the simplification in Fig. 5.20, the simplification for R_{gv} is shown in Fig. 5.21.

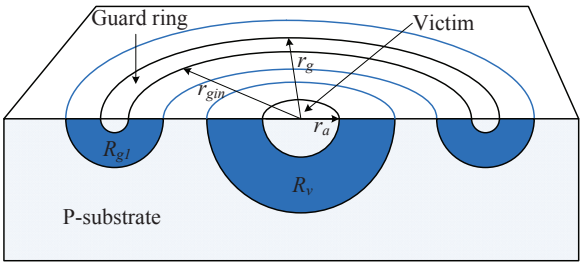

Figure 5.21: Simplified spreading resistance of the circular guard ring and victim.

Since the victim is inside the guard ring, the resistance R_{g2} in Fig. 5.20 is removed.

Using similar analysis for R_{ag}, the guard ring-to-victim resistance is given as

$$R_{gv} = R_v + R_{g1}, \tag{5.16}$$

where

$$R_{g1} = \frac{\rho}{(r_g + r_{gin})\pi^2} \ln\left(\frac{r_g + r_{gin}}{r_g - r_{gin}}\right), \tag{5.17}$$

and

$$R_a = K\frac{\rho}{2r_a}\left[1 - \frac{2}{\pi}\arcsin\left(\frac{r_a}{r_a + d_{gv}}\right)\right], \tag{5.18}$$

and

$$K = \frac{t + r_a/4}{t}. \tag{5.19}$$

It is noted that the victim and guard ring in this case are confocal and hence there is no extra current constriction as that in the case of the aggressor and guard ring.

5.3.1.3 Square contacts and guard rings

In practical applications, the aggressor, guard ring and victim are usually in rectangular shapes. To apply the results of circular contacts and guard rings to square contacts and guard rings, the square contacts are approximated using circular contacts that have the same areas. For example, for a square aggressor with a side length of L, it is approximated as a circular contact with a radius of r_a

$$r_a = \frac{L}{\sqrt{\pi}}. \tag{5.20}$$

For a square guard ring with an inner side length of L_{in} and an outer side length of L_{out}, it is approximated as a circular guard ring with the inner and outer radius of

$$r_g = \frac{L_{out}}{\sqrt{\pi}}, \tag{5.21}$$

and

$$r_{gin} = \frac{L_{in}}{\sqrt{\pi}}, \tag{5.22}$$

respectively.

5.3.2 Experiment

A test chip has been fabricated to experimentally verify the proposed model. The test chip is implemented using a standard 0.18 μm CMOS process. The parameters of the process are shown in Fig. 5.22. In the process, a 1.5-μm P-well layer is built on a

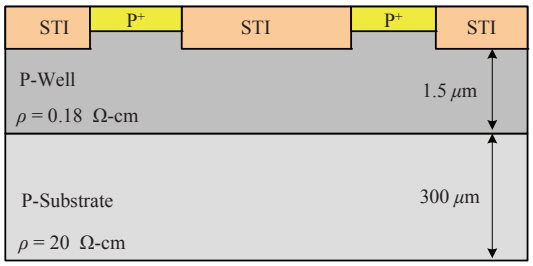

Figure 5.22: Cross section view of the 0.18 μm CMOS process used for the test.

300-μm P-substrate. It is noticed that the resistivity of the P-substrate is two orders higher than that of the P-well layer. Thus the lateral spreading resistance between P^+ contacts in the P-well layer is assumed to dominate the total spreading resistance, and the P-substrate is consequently simplified as open circuit. In this way, the P^+ contacts and guard rings designed using this process can be characterized using the proposed resistive guard ring model.

The fabricated test chip is shown in Fig. 5.23. It has a P^+ contact array and a number of guard ring test fixtures indicated by dash blocks and labeled with capital letters. The P^+ contact array consists of P^+ contact pairs with different distances and sizes.

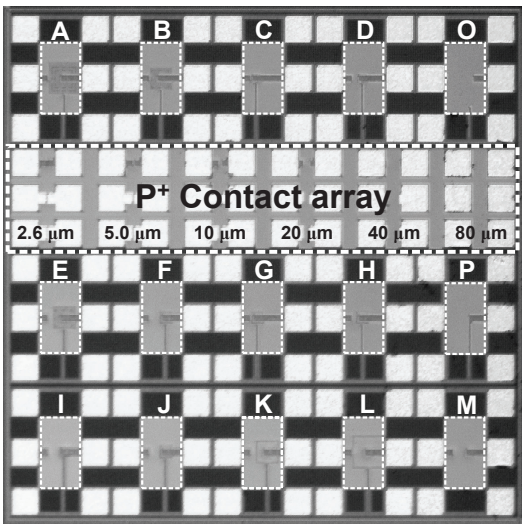

Figure 5.23: Microphotograph of the test chip.

In the experiment, The resistances of these contacts are measured using DC probes to verify the model for spreading resistance between rectangular P^+ contacts. The test fixture M has no guard ring, and it is used as a reference. Fixture O and P are the open and short fixtures for de-embedding. All the contacts in the test fixtures are square contacts with side length of 20 μm. To use the same sized contacts is due to the fact that the P^+ contact size is usually not a design parameter for substrate noise

suppression. G-S-G pads are used for both resistance and S parameter measurements.

5.3.2.1 Spreading resistance of P^+ contacts

The measured and calculated spreading resistances of P^+ contact pairs with different side lengths and distances are shown in Fig. 5.24.

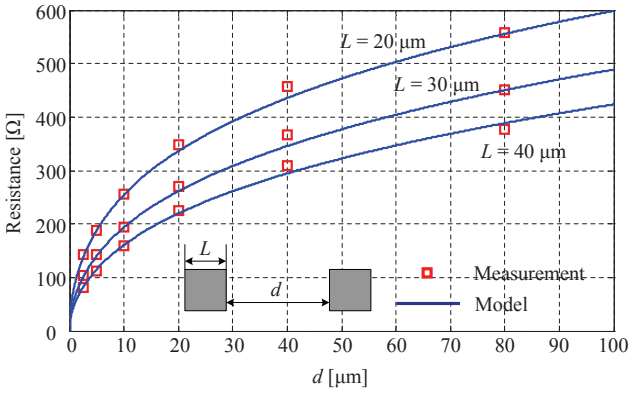

Figure 5.24: Measured and calculated resistance of P^+contacts versus distance with different side lengths.

The distance between the contacts is varying from 2.6 μm to 80 μm, and the side length of the contacts has three different values from 20 μm to 40 μm. From the results, it can be seen that the calculated results based on the proposed model match the measured results very well. The relative estimation error is less than 5% for all the results, which verifies the proposed model for the spreading resistance of P^+ contact on finite-thickness substrates.

5.3.2.2 Aggressor-to-guard ring and guard ring-to-victim resistance

The measured and calculated aggressor-to-guard ring resistance and guard ring-to-victim resistance of guard rings with varying d_{gv} are shown in Fig. 5.25.

As can be seen from the measured results, R_{gv} increases as the distance between the guard ring and the victim is increasing, and R_{ag} decreases since the distance between the aggressor and the guard ring is decreasing. It is also can be seen that the calculated results match the measured results well. The relative big estimation error is found in the results of R_{ag} when d_{gv} is 34.72 μm. In this case the guard ring is very close to the aggressor contact with a distance of 0.28 μm, which is the layout design constrain of the process. Under this condition, the current flowing from the aggressor to the guard

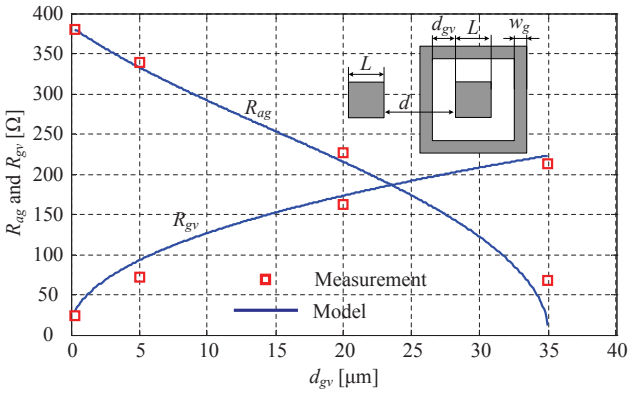

Figure 5.25: Measured and calculated aggressor-to-guard ring and guard ring-to-victim resistance versus guard ring-to-victim distance. The parameters used in this case are: $L = 20$ μm, $d = 40$ μm, and $w_g = 5$ μm.

ring is more crowed and results in an increased resistance.

The measured and calculated R_{ag} and R_{gv} of guard rings with varying aggressor-to-guard ring distances are shown in Fig. 5.26.

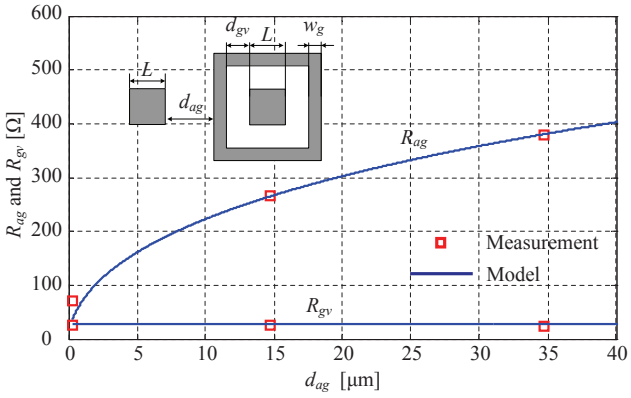

Figure 5.26: Measured and calculated aggressor-to-guard ring and guard ring-to-victim resistance versus aggressor-to-guard ring distance. The parameters used in this case are: $L = 20$ μm, $d_{gv} = 0.28$ μm, and $w_g = 5$ μm.

An excellent agreement is found between the calculated results and the measured results. It also can be seen that R_{ag} increases as d_{ag} is increasing, and a saturation effect can be observed in longer distances. The measured and calculated R_{gv} is almost constant, and the value is around 25 Ω. This is because that the guard ring is close to the victim ($d_{gv} = 0.28$ μm), and the layout of the guard ring and victim is kept as the same for all the fixtures in this test.

The guard rings designed with varying w_g are also investigated. The measured and calculated R_{ag} and R_{gv} are shown in Fig. 5.27. It can be seen that R_{ag} decreases as

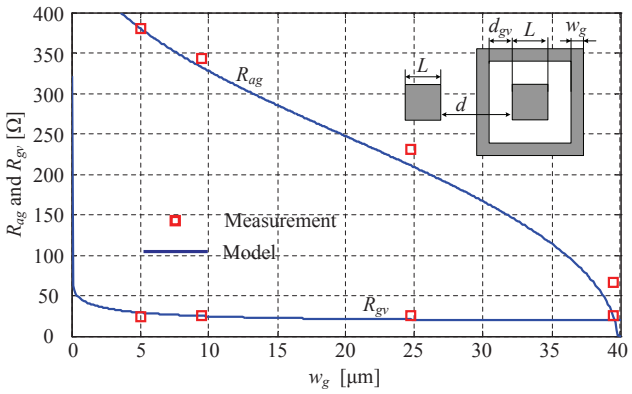

Figure 5.27: Measured and calculated aggressor-to-guard ring and guard ring-to-victim resistance versus guard ring width. The parameters used in this case are: $L = 20$ μm, $d_{gv} = 0.28$ μm, and $d = 40$ μm.

the guard ring is wider and approaching the aggressor. R_{gv} is decreasing slightly as the w_g is increasing. But it is still almost constant since the distance of the guard ring and victim is kept as the same in this test. A relative big estimation error is found when the guard ring width is 39.44 μm. In this scenario, the guard ring is very close to the aggressor ($d_{ag} = 0.28$ μm), which is similar to the case in Fig. 5.25.

The guard ring-to-ground (ground pads of the G-S-G pads) resistances are also measured, and the values are given in Table 5.1. To verify the proposed model in terms of substrate noise suppression versus frequency, the S parameters of the guard ring test fixtures are measured. S parameters calculated using the proposed T-network with measured R_{gg}, calculated R_{ag} and R_{gv} are also provided and compared with the measured results.

Fig. 5.28 shows the measured and calculated S_{21}-magnitudes of the reference fixture and guard rings with varying guard ring width.

It can be seen that the calculated results based on the proposed model match the measured results very well at frequencies below 200 MHz. Stronger coupling in the guard ring fixtures is observed at higher frequencies. This is mainly due to the parasitical capacitances between the aggressor, guard ring and victims, which are not included in this model. A decreased coupling in the reference fixture is observed at higher frequencies. This is mainly due to the aggressor-to-ground and victim-to-ground capacitances. It can be seen that the noise suppression decreases drastically when the guard ring is wide and close to the aggressor. This is because the R_{ag} decreases significantly when the guard ring is close to the aggressor. The results indicate that a wide guard ring does not improve the noise suppression and that a wider guard ring will only result in

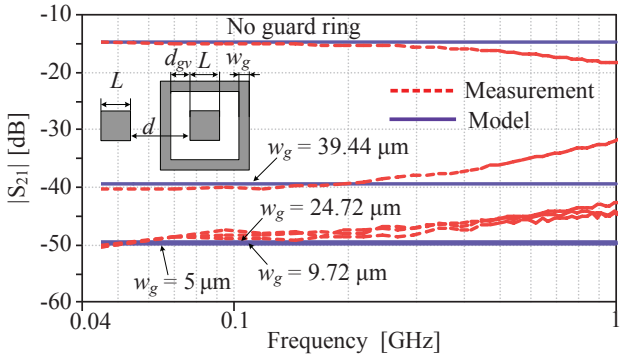

Figure 5.28: Measured and calculated S_{21}-magnitudes versus frequency with varying guard ring width. The parameters used in this case are: $L = 20$ μm, $d_{gv} = 0.28$ μm, and $d = 40$ μm.

Table 5.1: Measured and calculated resistances

	A	B	C	D	E	F	G	H	I	J	K	L
R_{ag}-measured [Ω]	66.3	66.9	70.3	267.4	230.6	343.8	68.7	209.8	379.5	338.4	226.3	67.5
R_{ag}-calculated [Ω]	26.8	29.8	46.2	265.6	211.5	325.4	38.1	202.8	375.5	328.0	215.8	30.8
R_{gv}-measured [Ω]	25.1	25.1	24.9	25.3	25.2	25.1	25.1	72.3	24.6	72.4	161.9	213.7
R_{gv}-calculated [Ω]	19.0	20.0	28.4	28.4	20.0	24.2	24.2	90.3	28.4	90.3	168.9	217.4
R_{gg}-measured [Ω]	0.58	0.59	0.92	1.25	0.63	0.93	0.63	1.75	1.10	1.86	2.67	1.26

wasted area.

The guard rings with varying guard ring-to-victim distances are also investigated. The measured and calculated S parameters are shown in Fig. 5.29.

Apart from the good agreement between the measured and calculated results at frequencies lower than 200 MHz, it also can be seen that the coupling strength increases when the distance between the guard ring and victim increases. This indicates that the guard ring should be put close to the victim to achieve a best suppression of the substrate noise.

Fig. 5.30 shows the measured and calculated S parameters of guard rings with varying aggressor-to-guard ring distances. A clear enhancement of the suppression level can be seen as the aggressor-to-guard ring distance is increasing. But the enhancement is saturated for longer distances, which is consist with the saturated aggressor-to-guard ring resistance shown in Fig. 5.26.

The measured and calculated S parameters of guard rings with varying guard ring width and aggressor-to-victim distances are shown in Fig. 5.31.

It can be seen that the suppression level is close to each other even though the guard ring widths are drastically different. And the feature is accurately predicted by the calculated results based on the proposed model.

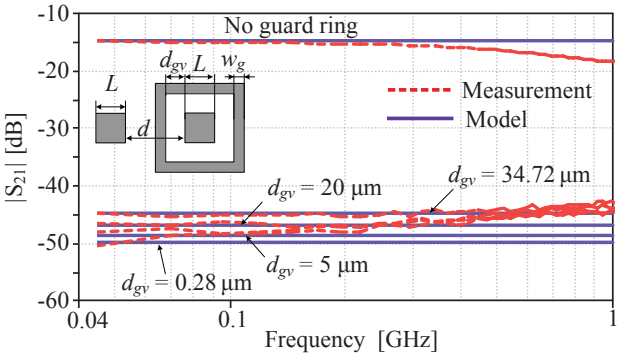

Figure 5.29: Measured and calculated S_{21}-magnitudes versus frequency with varying guard ring-to-victim distances. The parameters used in this case are: $L = 20$ μm, $w_g = 5$ μm, and $d = 40$ μm.

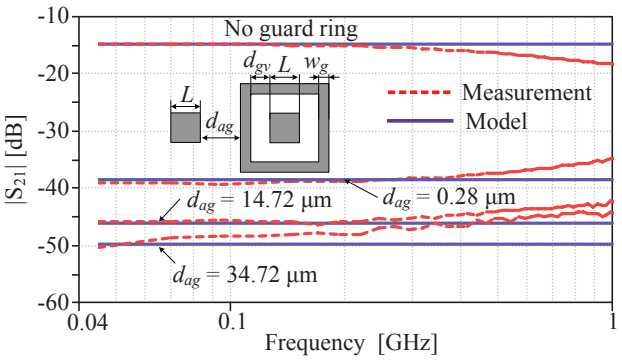

Figure 5.30: Measured and calculated S_{21}-magnitudes versus frequency with varying aggressor-to-guard ring distances. The parameters used in this case are: $L = 20$ μm, $w_g = 5$ μm, and $d_{gv} = 0.28$ μm.

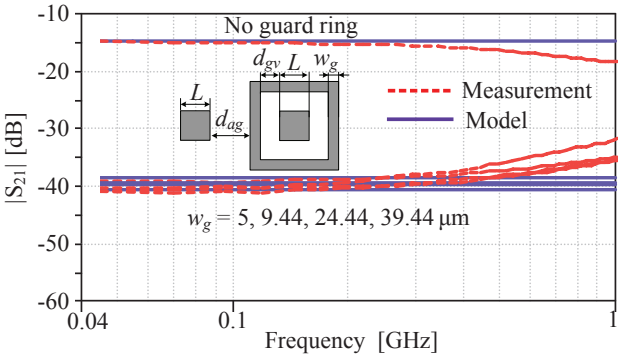

Figure 5.31: Measured and calculated S_{21}-magnitudes versus frequency with varying aggressor-to-guard ring distances and varying guard ring width. The parameters used in this case are: $L = 20$ μm, $d_{ag} = 0.28$ μm, and $d_{gv} = 0.28$ μm.

In the experiment, it can be seen that all the calculated results match the measured results for frequencies below 200 MHz. Since the major part of the substrate noise in most cases are located at the frequencies lower than a few hundreds MHz [11, 36], the proposed resistive guard ring model would be sufficient for most common practical applications. Based on the proposed model some rules of thumb for the design of guard rings with desired noise suppression level and miniaturized chip area can be concludes as below:

It is unnecessary to use a very wide guard ring. In fact a wide guard ring has the risk of even decreased noise suppression. The guard ring should be put close to the victim even as close as what the layout design constrain defines. A higher suppression can be achieved by moving the aggressor away from the victim and guard ring, but the benefit is saturated for long distances.

By assuming an achievable guard ring-to-ground resistance, a guard ring can be designed based on the proposed model to have the desired noise suppression performance. Since a zero R_{gg} is the prefect case, a relative big value should be used to have some margin. For example, an assumption of 1 Ω is much better than 10 mΩ since the later one is difficult to achieve and there might be no margin for the design.

5.4 Conclusion

This chapter presents an active suppression technique for reduce switching noise in mixed-signal ICs. The technique is based on an active section, which generates extra switching currents with desired relative delays, pulse widthes and magnitudes. The proposed method has the following advantages in nature compared to prior art.

- Lower cost. The chip area needed using this method is expected to be significantly less than when using simple physical separation. In addition, unlike deep N well isolation techniques, no extra processes are need to implement this method. All these factors make the proposed method a lower cost solution for substrate noise suppression.
- Wider applicable frequency band. Different from the architectures use in the conventional active cancelation methods, the proposed method does not modify the propagation path of the substrate noise. Thus the limited frequency band in conventional methods is not an issue in this method. Furthermore, the mechanism of the active cancelation section is as the same as the switching mechanism of ordinary digital circuit. Hence, this method is valid up to gigahertz frequencies.
- The cancelation is global for the whole chip. The active cancelation in this method is done at the source. Thus the benefit of the cancelation is available at any

location on the chip. This also eliminates the dependence on the specific layout in conventional methods.

- Higher potential of integration into standard IP cells. The conventional methods of active cancelation are analog circuits, and they are strictly based on the specific layout of the mixed-signal chip. Therefore those methods can not be applied until the layout of the chip is given, which degrades its potential to be integrated into standard IP cells. On the contrary, the active cancelation circuits in this proposal are digital circuits, and its cancelation is global for the entire chip. Thus it can be easily integrated into standard IP cells.

This chapter also presents a novel modeling method of guard rings on finite-thickness substrates. It provides a simple yet accurate prediction of R_{ag} and R_{gv} of guard rings with different layout topologies, which is helpful to estimate the noise suppression level of the guard ring and optimize the layout. The model has been validated by both EM simulations and experiments. It has been shown that this model works perfectly at frequencies of hundreds of MHz, where has the most severe substrate noises in common practical applications.

Chapter 6

Conclusion

When realizing SoCs for modern wireless applications, sensitive analog/RF circuits have to be integrated on the same chip with the digital blocks. However, these mixed-signal circuits could suffer interferences from each other. One of the most severe interferences is the impact of digital blocks on sensitive analog/RF circuits. The switching noise generated in digital blocks plays the role of a noise source. The generated noise can easily propagate to the sensitive analog/RF circuits through substrate and interconnects, and deteriorate their performance. This work focuses on four aspects of the substrate noise issues, the measurement, impact evaluation, modeling, and suppression of substrate noise. Efforts have been invested to derive an analytical switching noise model for simple digital circuit and a statistical model for large scale digital blocks. In addition, an active suppression technique for reducing switching noise in digital circuits is also proposed. A compact guard ring model for P^+ guard rings is proposed and verified by experimental results. To support the verifications of the proposed substrate noise model and noise suppression techniques, wide band substrate noise measurement fixture has been proposed. This chapter summarizes the results and contributions, as well as provides suggestions regarding the future work in this field.

Chapter 2 presents a passive fixture suitable for the measurement of substrate noise in lightly doped substrates within the UWB frequency band. The effects of the distance-based substrate resistance and the capacitive coupling between the substrate and the ground are evaluated through measurement. An equivalent circuit model of the measurement fixture is presented and measurement validation shows a good fit. The simulated and measured results show that this measurement fixture is able to provide reliable measurements over the UWB frequency band from 3 to 10 GHz. Furthermore, obvious effects of capacitive coupling are observed over 45 MHz-3 GHz. An improved fixture is proposed to reduce the capacitive coupling effects between the substrate and the ground of the measurement setup. Experimental results show that the improved measurement fixture offers a flat S_{21}-magnitude response from DC to 10 GHz, which makes the improved measurement fixture suitable for the measurement of substrate

noise in such a wide frequency band.

Chapter 3 experimentally evaluates the impact of substrate noise on an UWB LNA. Measurements show that the substrate noise can be significantly higher than the noise floor in the UWB band, and that the magnitude of the substrate noise is proportional to clock frequencies. It is also observed that intermodulation components are generated in addition to the directly coupled substrate noise. Due to the in-band harmonics of the substrate noise, the noise figure of the UWB LNA is drastically deteriorated.

Chapter 4 presents two modeling methods for switching noise in both small and large scale digital circuits. The novel analytical model for simple digital circuit, the GAP model, provides a detailed understanding of the generation and propagation of switching noise in lightly doped CMOS technologies. The spectral envelope of the switching noise can be easily predicted using the proposed model. Closed-form expressions for calculating the parameters in the conventional triangular model are also provided. The model is validated by both SPICE simulations and measurement results from a test chip fabricated in a lightly doped CMOS process. Good agreement is found between the model and simulations as well as measurement results. With this model, the simulations needed when using traditional approaches can be avoided. This can help to achieve a scalable analytical switching noise model for digital blocks. This model especially holds the advantage for estimating the switching noise when big size buffers are dominating the noise generation. In addition to the GAP model, an equivalent multi-path coupling model is proposed to characterize the switching noise in large scale synchronized digital circuits. This model is capable of achieving fast results since analysis can be easily done using Monte Carlo simulation in Matlab.

Chapter 5 presents a novel active suppression technique for substrate noise in mixed-signal ICs. The analytical modeling of guard rings for substrate noise isolation in lightly doped substrates is also presented. The proposed method has the advantages of wide applicable frequency band, global noise reducing and higher potential of integration into standard IP cells, compared with previous methods. This chapter also presents a novel modeling method of guard rings on finite-thickness substrates. It provides a simple yet accurate prediction of R_{ag} and R_{gv} of guard rings with different layout topologies, which is helpful to estimate the noise suppression level of the guard ring and optimize the layout. The model has been validated by experiments. It has been shown that this model works perfectly for frequencies up to a few hundreds of MHz. This frequency range has been shown to have the most severe substrate noises in common practical applications.

6.1 Scientific contributions

A measurement fixture for characterizing the substrate noise over the UWB frequency band has been proposed. The fixture is based on modified ground-signal-ground (GSG) pads. In addition, the effects of the parasitic capacitive coupling between the substrate and the ground of the measurement setup are evaluated and removed in an improved version of the fixture. From the measurement results the presented fixture is shown to provide a measurement band from DC to 10 GHz.

Experimental impact evaluations of substrate noise on wide band mixed-signal ICs have been carried out using a 1-5 GHz UWB LNA and a noisy digital circuit both implemented on the same substrate. This evaluation revealed the significant performance deterioration of the UWB LNA due to substrate noise issues. The results clearly indicate the need for a good understanding of the generation and propagation of the substrate noise, as well as the need of effective approaches for reducing the substrate noise in wide band mixed-signal ICs. To the author's best knowledge, no similar work has been presented before and the presented results deliver useful information for wide band mixed-signal IC designers.

A novel analytical model describing the generation and injection of switching noise in lightly doped substrates. The model provides closed-form expressions for the switching noise, which is accomplished by approximating the switching current waveform using a Gaussian pulse (GAP) function and simplifying the transfer function describing the coupling between the switching current source and substrate. The proposed model is scalable and easy to implement. Satisfactory agreement is found between the proposed model and measurement results based on a test chip implemented using a standard CMOS process.

A novel compact model of guard rings on lightly doped substrates has been proposed. This model requires no fitting factors and it is easy to use. This is accomplished by modeling the aggressor-guard ring-victim layout using a resistive T-network. Closed-form expressions for calculating the spreading resistances in the network are proposed. The model can accurately characterize the effects of the layout parameters on the noise isolation performance of the guard ring, which is useful for noise isolation enhancement or chip area miniaturization. A test chip using a standard 0.18 μm CMOS process has been fabricated for experimental verification, and an excellent agreement has been found between the model and the measured results.

A spectrum shaping technique has been proposed and preliminarily verified by mathematic analysis and SPICE simulations. In the proposed technique, an active spectrum shaping section is used to generate extra switching currents to modify the shape of the original switching noise in both time domain and frequency domain. The time delays of these switching currents relative to the original switching current are realized by

controllable delay lines with high accuracy. The pulse widths and magnitudes of the switching currents are also controllable. By manipulating the extra switching currents, the spectrum of the total switching noise can be shaped to have a suppressed magnitude at desired frequencies. Thanks to the fine-controlled delay lines, the proposed technique is robust to mismatches of magnitudes and time delays. In addition, since this technique needs no information from the substrate or layout, it holds the promising potential, for the first time, to achieve the implementation of IP cells with locally suppressed switching noise.

6.2 Future work

While novel techniques for modeling, suppression and measurement of substrate noise have been developed, there remain some issues outside the scope of this research work that may be of interest for future investigation.

Firstly, the switching noise model presented in this dissertation has covered only the CMOS on lightly doped substrate technology. While satisfactory results have been achieved for this technology, it would be interesting to evaluate the proposed techniques on heavily doped substrate with lightly doped epitaxial layer, silicon-on-insulator (SOI), and other technologies.

Secondly, the proposed active suppression technique could potentially be integrated in the design of IP cells. In this way, the substrate noise can be reduced at the very beginning of the entire design flow by setting specific design parameters in the IP cell generation. While preliminary results have been obtained to support the proposed technique, comprehensive experiments would be preferred to provide more solid verification proves. It would be interesting to apply the proposed technique into a number of typical IP cells and observe the performance.

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Appendix A

Reprint of publications

In the following pages a reprint of the publications are given in the order of appearance.

1. M. Shen, T. Tian, J.H. Mikkelsen, and T. Larsen, "A Method for Measuring Substrate Noise in the UWB Frequency Band on Lightly Doped Substrates," in *Proceedings of the IEEE 25th Norchip Conference*, Aalborg, Denmark, Nov. 2007.

2. M. Shen, T. Tian, J.H. Mikkelsen, and T. Larsen, "A Measurement Fixture Suitable for Measuring Substrate Noise in the UWB Frequency Band," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 58, no. 1, pp. 11-17, Jan. 2009.

3. M. Shen, T. Tian, J.H. Mikkelsen, O.K. Jensen, and T. Larsen, "A 1-5 GHz UWB Low Noise Amplifier in 0.18 μm CMOS," in *Proceedings of the IEEE 27th Norchip Conference*, Trondheim, Norway, Nov. 2009.

4. M. Shen, T. Tian, O.K. Jensen, J.H. Mikkelsen, and T. Larsen, "A Compact UWB Bandpass Filter With WLAN Rejection Using a Slot Ring Resonator," to appear in *Microwave and Optical Technology Letters*.

5. M. Shen, T. Tian, J.H. Mikkelsen, O.K. Jensen, and T. Larsen, "Design and Implementation of a 1-5 GHz UWB Low Noise Amplifier in 0.18 μm CMOS," submitted to *Journal of Analog Integrated Circuits and Signal Processing*.

6. M. Shen, T. Tian, J.H. Mikkelsen, and T. Larsen, "An Analytical Model for Switching Noise in Lightly Doped Substrates," submitted to *Microelectronics Journal*.

7. M. Shen, T. Tian, J.H. Mikkelsen, O.K. Jensen, and T. Larsen, "Analytical Modeling of Guard Rings on Substrates with Finite-Thickness," planned for submission to *IEEE Transactions on Electron Device*.