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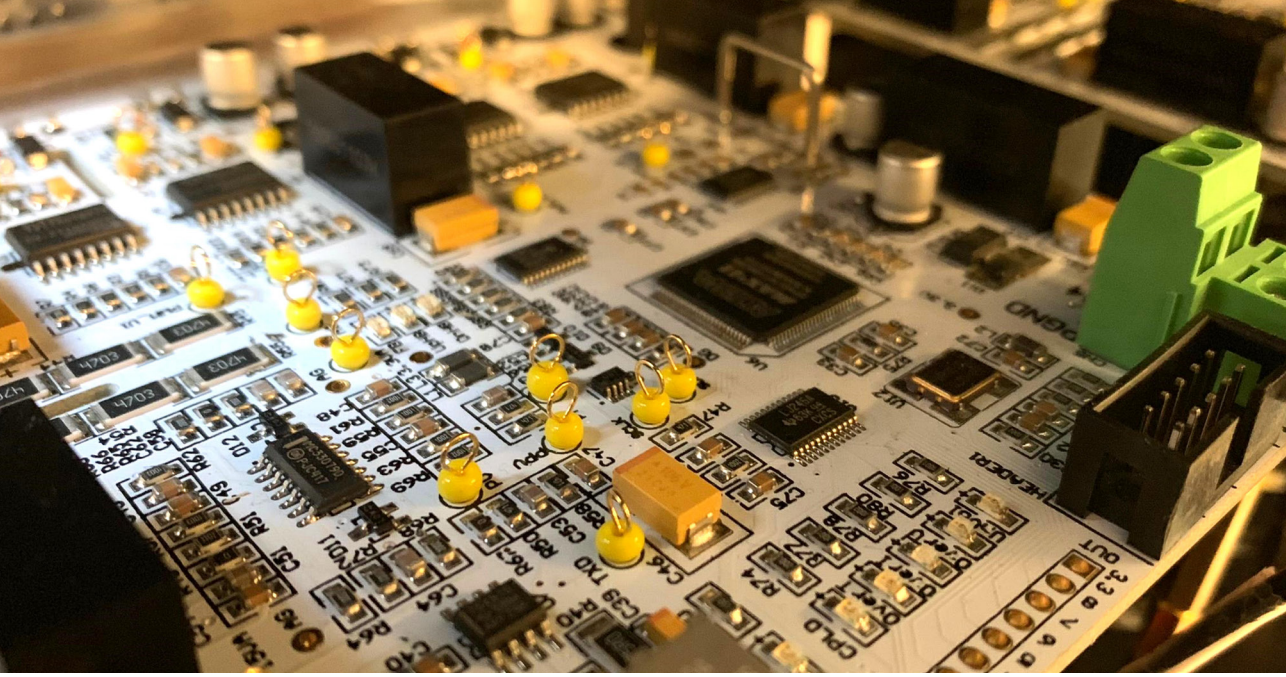

MISSION PROFILE BASED CONTROL AND RELIABILITY IMPROVEMENT STRATEGIES OF MODULAR MULTILEVEL CONVERTERS

BY
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Mission Profile Based Control and Reliability Improvement Strategies of Modular Multilevel Converters

Ph.D. Dissertation

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Abstract

Modular multilevel converters (MMCs) are typically composed of hundreds of power devices and capacitors. Its fast-growing application and complexity call for much more attention and research need on its reliability performance. Given its different topology from conventional two- or three-level converters, how to effectively improve the reliability of the MMC has not been sufficiently studied. In order to cope with these issues, this thesis firstly studies a sub-module (SM) based reliability testing scheme of the MMC and then proposes reliability improvement strategies from a control perspective. Two condition monitoring strategies for SM capacitors are also introduced and validated experimentally.

In order to illustrate the limitations of existing SM based testing schemes, an overview of existing testing emulators is given. Based on the challenges, this Ph.D. project proposes a mission profile emulator for power modules in the MMC. By integrating an auxiliary SM based voltage stabilizer, the testing scheme is applicable to mimic practical current profiles and switching profiles. Meanwhile, due to the decoupling between the voltage of DC power supply and the high voltage of SM capacitors, the power rating and voltage rating of the used power supply in the current source are both significantly reduced. In order to facilitate the implementation of this setup, a guideline regarding the selection of control parameters and hardware parameters is provided. Simulation and experiment results validate the effectiveness of the proposed mission profile emulator.

Capacitor voltage balancing control offers an internal conduction loss balancing mechanism among SMs. An analytical evaluation validates that the balanced conduction loss distribution is independent of the control, modulation and loading conditions of the MMC. However, due to parameter mismatch and the low switching frequency operation of the MMC, switching losses are not evenly distributed among SMs. Thus, a power loss balancing control is proposed in this project. The switching loss differences among SMs can be reduced to less than 25%.

For MMCs connected to the grid, stringent grid codes are supposed to be fulfilled during the operation. In order to limit the output current THD

within a specific range, a relatively high switching frequency has to be employed for MMCs with a relatively small number of SMs considering conventionally fixed carrier frequency. Large switching losses can be generated for heavy loading conditions for high voltage rating power devices. In this regard, this Ph.D. project proposed an adaptive control to dynamically adjust the carrier frequency according to the loading conditions of the MMC. The carrier frequency boundaries regarding the output current THD and SM capacitor voltage ripple are first explored. Based on the results, the lowest allowable switching frequency can be applied to the MMC while meeting the requirements of output current THD and SM capacitor voltage ripple. A mission profile-based reliability evaluation is conducted to illustrate the impact of the proposed method on the efficiency, thermal stress, and lifetime of the MMC. A case scenario based on a 15 kVA three-phase MMC is also studied experimentally. The observed power loss reduction of power devices validates the effectiveness of the proposed method.

Capacitors are one of the components prone to failure in power electronic converters. When it comes to the MMC, the reliability concern about SM capacitors is much more serious since they typically account for over 50% and 80% of the volume and weight of one SM, respectively. Since the capacitor ages with time, as one of the means to improve reliability, condition monitoring of SM capacitors is important regarding the reliable operation of the MMC. Due to high voltage rating, film capacitors are typically applied in the MMC. One of the end-of-life criteria of film capacitors is typically 5-10% capacitance drop. The tiny capacitance change poses a challenge for the condition monitoring (CM) of film capacitors. In order to enhance the monitoring accuracy, two CM methods are proposed in this Ph.D. project. Firstly, it is based on the DC-side start-up of the MMC. An RC charging circuit formed during the start-up process can be utilized to extract the capacitance values. The impacts of diode tolerance and degradation, bleeding resistor tolerance and time delay are discussed. Experimental validation is provided in the end.

The second condition monitoring method takes full advantages of the SM voltage sensor range. The monitoring accuracy can be significantly improved. The precondition is that the capacitance of the reference SM should be known beforehand by applying existing CM methods but with more accurate sensors or extra measurement circuits. For comparison, an accuracy analysis is conducted. Practical considerations regarding the implementation of these proposed methods are discussed, namely the detection of reference SM capacitance and the impact of the proposed method on the operation of the MMC. Experiments based on capacitors with small capacitance differences (e.g., from 0% to 3.2%) show that the proposed method can achieve the objective of capacitor monitoring with enhanced accuracy, less computational burden, and loading-independent characteristics.

Resumé

Modulære multilevel konvertere (MMCs) er almindeligvis sammensat af hundredvis af effektelektroniske komponenter og kondensatorer. Deres stadig stigende anvendelse og øget kompleksitet kræver stor opmærksomhed og forskningsbehov, i forbindelse med deres evne til at operere pålideligt. I betragtning af de forskellige konventionelle konverter topologier på henholdsvis to og tre niveauer er de ikke blevet forsket tilstrækkelig i forbindelse med en effektiv forbedring af modulære multilevel konverteres pålidelighed. For at overkomme de nuværende problemstillinger undersøges pålideligheden af sub-moduler indledningsvist i dette projekt og der foreslås udfra dette pålidelighedsforbedringer fra et kontrol perspektiv. To tilstandsovervågningsstrategier for SM-kondensatorer introduceres og valideres eksperimentelt.

For at illustrere begrænsningerne i eksisterende SM-baserede testanordninger, gives der en oversigt over eksisterende testemulatorer. Udfra de nuværende problemstillinger baserer dette Ph.D. projekt en operativ profil emulator for effektelektroniske moduler i modulære multilevel konvertere. Ved at integrere en ekstra SM-baseret spændingsstabilisator er testanordningen i stand til at efterligne strømprofiler og tilstandsprofiler af kontakterne. Samtidigt kan der som følge af afkobling mellem DC-strømforsyningens spænding og den høje spænding af SM-kondensatoren, kan både effekten of spænding reduceres betydeligt i den anvendte strømforsyning. For at lette implementeringen af denne opsætning angives der retningslinjer for valg af både kontrolparametre og hardwareparametre. Effektiviteten af den foreslåede operations profil emulator valideres gennem simuleringer og eksperimentelle resultater.

Gennem afbalanceringskontrol af kondensator spændingen opstår muligheden for en balance mekanisme af det indre ledningstab mellem submoduler. Gennem analytisk evaluering valideres det at den afbalancerede ledningstabsfordeling er uafhængig af styring, modulering og belastningstilstand for modulære multilevel konvertere. Tabet i kontakterne fordeles dog ikke jævnt mellem sub-modulerne, hvilket skyldes en uoverensstemmelse mellem parametrene kontaktstyringsfrekvens af modulære multilevel konvertere. Derfor præsenteres en balance kontrol af effekttabet i dette projekt,

hvor forskellene i effekttabet som er grundet tilstandsændringer i kontakterne reduceres til mindre end 25%

For netforbundet modulære multilevel konvertere gælder der strenge net betingelser, som skal overholdes under operation. For at begrænse udgangsstrømmens THD til at være indenfor et specificeret område, skal der anvendes en relativ høj tilstands skifte frekvens for modulære multilevel konvertere med relativ lavt antal sub-moduler, hvor der anvendes en konventionel fast bærefrekvens. Store tab ved tilstandsskift opstår ved store lasttilstande for effektenheder som opererer ved høje spændinger. Derfor præsenterer dette Ph.D. projekt en tilpassende kontrolstrategi til at justere bærefrekvens i forhold til den modulære multilevel konverters lasttilstand. Indledningsvist undersøges bærefrekvensens grænseværdier med hensyn til udgangsstrømmens THD og ripple spændingen af sub-modul kondensaterne. Udfra disse resultaterne kan den lavest tilladelige switching frekvens påføres MMC'en kravende om udgangsstrømmens THD og spændings ripplen af sub-moduls kondensaterne stadig overholdes. En pålideligheds evaluering, som er baseret på operations profiler, er udført for at illustrere hvilken indflydelse den foreslået metode har på effektiviteten, det termiske stress og livstiden af MMC'en. Et case baseret scenario hvori en 15 kVA tre-faset MMC testes eksperimentelt. Gennem reduktionen i det observerede effekttab af effektenhederne valideres effektiviteten af den foreslået metode.

Kodensatorer er en af de komponenter, som indgår i effektkonverterer, som er tilbøjelig til at svigte. I tilfældet hvor disse SM-kondesatorer indgår i modulære multilevel konverteres er dette pålidelighedsproblem langt mere alvorligt, da kondensatorne udgør mere end 50% af volumen og 80% af vægten af et SM. En af de måder hvorpå pålideligheden kan forbedres er gennem tilstandsovervågning af SM kondensatorne, som vil give indblik i den forringet tilstand i takt med at kondensatorne ældes og som kan sikre en pålidelig drift af modulære multilevel konvertere. Som et resultat af de høje operationsspændinger anvendes der ofte filmkondensatorer i modulære multilevel konvertere. Et ofte anvendt livstidskriterie for filmkondensatornes er et fald i dens kapacitans i størrelsesordenen 5-10%. Denne forholdsvis lille kapacitansændring udgør en udfordring ift. tilstandsovervågning og for at forbedre nøjagtigheden af tilstandsovervågningen præsenteres to metoder i dette Ph.D. projekt. Den første metode er baseret på DC-sidens opstart af den modulære multilevel konverter. I opstartsprocessen kan RC opladnings kredsløbet udnyttes til at angive størrelserne af kapacitanserne. Indflydelserne af diodetolerancer og komponentforringelse gennem ældning, diskuteres blødningsmodstandstolerance og tidsforsinkelse. Der gives i slutning en eksperimentel validering.

Den anden tilstandsovervågningsmetode drager fuld fordel sub-modulets spændingssensor interval. Nøjagtigheden af tilstanden kan forbedres markant, hvis kapacitansen af reference sub-modulet er kendt op forhånd. Dette gøres

ved at anvende allerede eksisterende tilstandsovervågningsmetoder men hvor der enten anvendes sensorer med større nøjagtighed eller der påføres et ekstra målekredsløb. Praktisk overvejelser ift. implementering af de foreslåede metoder diskuteres, især hvordan reference kapacitansen af SM og hvilken indvirkning denne metode har på den modulære multilevel konverters virkemåde. Der udføres eksperimenter med kondensatorer, hvor kapacitans forskellene er forholdsvis lille (f.eks. fra 0% til 3,2%). Disse eksperimenter viser at den foreslåede metode er i stand til at nå målet ift. en forbedring af nøjagtigheden af tilstandsovervågning af kondensatorer og samtidig opnå mindre beregningsbyrde og bedre belastningsuafhængige egenskaber.

Preface

This Ph.D. thesis is a summary of the outcomes from the Ph.D. project entitled "Mission Profile Based Control and Reliability Improvement Strategies of Modular Multilevel Converters". This Ph.D. project is mainly supported by Department of Energy Technology, Aalborg University, Denmark and Otto Mønsteds Fond. Special acknowledgement is given to the Center of Reliable Power Electronics (CORPE).

First of all, I would like to take this opportunity to express my deepest gratitude to my supervisor, Professor Huai Wang, for his valuable, insightful and patient guidances and discussions during my Ph.D. study. I would also like to thank my co-supervisor Professor Frede Blaabjerg for his consistent advices, support and encouragement. I am really honored to have the opportunity to work with them.

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Last but not least, I would like to express my sincere gratitude to my family for their unconditional love, support and understanding all the way. They have been always encouraging me to find my own path in life to make me who I am today.

Zhongxu Wang
Aalborg University, October 20, 2019

Contents

Part I

Report

Chapter 1

Introduction

This chapter presents the background and motivation of the Ph.D. project. The research questions and objectives are discussed. Then, the outline of the Ph.D. thesis is presented to show the flow of this research work.

1.1 Background and Motivation

Modular multilevel converter (MMC) is a hot research area in power electronics. Nevertheless, majority of the studies focus on the topology configurations [1, 2], circulating current control[3], voltage control algorithms [4–6], and modulation strategies [7–10]. In practical applications, such as high-voltage direct current (HVDC) transmission [11, 12], offshore wind farms [13, 14] and variable speed drive [15–17], major challenges are: 1) fulfilling stringent reliability requirements while limiting the cost of the MMC system during the design phase in terms of thousands of main components including insulated gate bipolar transistors (IGBTs) and sub-module (SM) capacitors; 2) enhancing the reliability/availability of the MMC system in operation in terms of degradation of main components caused by severe operation environments or mission profiles. Therefore, in 2016, we started the MMC reliability research with two planned Ph.D. research topics, which focus on "design and verification" and "control and monitoring" of the MMC, respectively, according to the power electronics reliability triangle as shown in Fig. 1.1. This presented Ph.D. thesis focuses on the latter one.

The scope of power electronics reliability includes three major aspects. The analytical analysis is to understand the failure mechanism of power electronic products from the physics point of view [19]. Design and verification is to design the reliability and to ensure sufficient robustness of power electronics during the initial design phase [20]. The control and monitoring is targeting to ensure reliable operation of the power electronic system under

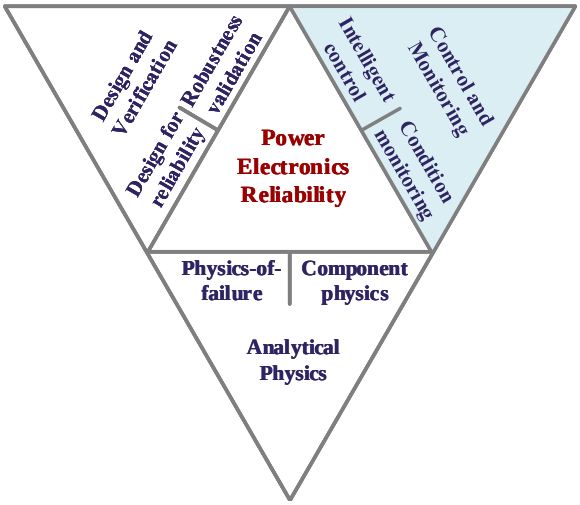

Fig. 1.1: Scope of power electronics reliability [18].

particular mission profiles [21, 22]. It means that not only hardware design but also more intelligence should be introduced into future products [18]. This Ph.D. project focuses specifically on the third aspect of the reliability triangle, namely control and monitoring, to enhance the reliability of the MMC. As a matter of fact, reliability is the probability that a system can properly function under a particular loading conditions and within a specific period of time [23]. Therefore, accordingly, attention can be paid to three research directions in order to improve the reliability/availability of the MMC. Firstly, enhancing the physical strength of components or choosing proper components can prolong the lifetime of converter given specific loading conditions. Secondly, relieving the stresses that components are subject to can extend the serving time of the system as well considering the same hardware implementation. Once the components and their stresses are determined, the third option is to conduct preventive maintenances that can push the potential of all major components in the system close to their limits.

In this regard, this Ph.D. project will focus on three major research topics to achieve the above objectives. The first topic is an SM based mission profile emulator of the MMC. It provides an experimental platform for the two Ph.D. research activities. Meanwhile, by exploring practical electro-thermal stresses that major components are exposed to with a down-scaled laboratory prototype, the testing scheme is able to assist a proper selection of components in the design phase of the MMC. The second part of the Ph.D. project is reliability-oriented control strategies, which are able to actively improve the reliability of the MMC system in operation from a control perspective.

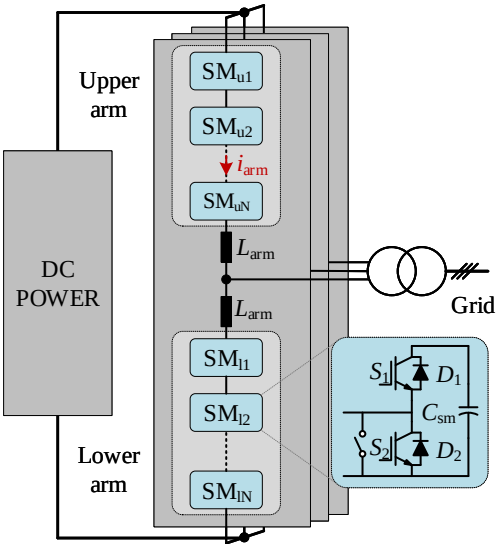

Fig. 1.2: A typical three-phase modular multilevel converter. Source:[J4]

By regulating the current, voltage, switching frequency, modulation and so on, thermal stresses of major components can be reduced or balanced to prolong the reliability and availability of the system as a whole. The last topic is condition monitoring (CM). By evaluating the health status of components to take preventive actions prior to the occurrence of failures, condition-based maintenance can be achieved instead of routine-based schedule to replace aged SMs. Thus, less repair time, lower maintenance cost and longer reliable operational time can be achieved. More detailed explanation of the three research topics are given in the following.

At the beginning of this Ph.D. project, a mission profile emulator which aims to provide an experimental platform for both Ph.D. project research activities will be explored. As we all know, for power electronic converters, mission profile is a combination of stresses that a converter is subject to during its service life [24]. This might involve electrical stresses like current and voltage, internal thermal stresses like junction temperatures [25], and environmental factors like ambient temperature and wind speed for wind power generation applications [24, 26]. Different mission profiles might contribute to different loading conditions and stresses of the components in the system and finally different reliability performance of the converter. Therefore, mission profiles have to be taken into account when conducting the reliability research of a power electronic converter. In this regard, a hardware platform that is capable of emulating practical operation conditions of a converter is very important for experimental validations to mission profile-related relia-

bility research. When it comes to the MMC specifically, an MMC mission profile emulator instead of a three-phase MMC is recommended for experimental validations since the MMC typically operates under high power and high voltage conditions (e.g., several hundreds of Megawatts power level and several hundreds of kilovolts DC bus voltage level [27]). A large testing facility, which is costly and time-consuming to build, is needed if the whole MMC is tested with full power [28]. The modular structure enables that the testing of the MMC can be based on one or a small number of SMs [29] compared with conventional converters, which are typically based on the whole converter, a phase leg or a valve [30]. In other words, the large power requirement in the conventional converter testing is not required for the MMC any more. Thus, an MMC mission profile emulator can facilitate the experimental validation of the reliability research being conducted in the two Ph.D. projects.

Regarding the second research topic, the reliability-oriented control focuses on power modules in the MMC only. For power modules, bond wire lift-off, solder joint fatigue and bond wire heel cracking are recognized as major failure mechanisms and are affected by a variety of stresses, such as voltage, temperature, vibration, humidity, cosmic radiation etc. [31]. Among them, thermal cycling (e.g., temperature swing) has been revealed as one of the most critical failure causes [32]. It is driven by the mismatch of coefficients of thermal expansion between different materials (e.g., between Aluminum bond wires and Silicon chips [33]). Physical disconnection between layers with different materials leads to the wear-out of power devices after a certain number of thermal cycles. When it comes to power modules in the MMC, especially in applications like renewable energy generation (e.g., offshore wind power generation) and motor drives, complicated and variable operation/environmental conditions (i.e., mission profiles) of the converter can directly change the loading of power devices [18]. Severe variable thermal stresses involved in this process can quickly cause the wear-out of the power devices. Therefore, in order to extend the serving time of the power modules, one straightforward and effective way is to reduce the thermal stresses that components are subject to. According to a project called LEISIT conducted in the 1990s, both the reduction of the junction temperature swing amplitude and average junction temperature can extend the life span of a power module, in which the reduction of temperature variation is more effective [32]. This relationship between temperature and lifetime offers an opportunity to enhance the reliability of the converter through reliability-oriented control methods. The above objective can be achieved by re-distributing power losses and further regulating the junction temperature of the power module through applying different strategies like modulations [34], manipulating switching frequency [35], reactive power control [36], circulating current control [37] etc in conventional power converters. Since limited research on the

reliability-oriented control is conducted for the MMC, similar ideas will be part of the research focus of this Ph.D. project.

As an alternative, condition monitoring (CM) can also increase the availability of power electronic converters by scheduling preventive maintenances with less operational cost and longer reliable operational time. Condition monitoring is a process of collecting health status data of a physical system [38]. Preventive maintenance of the monitored system can be scheduled to avoid the occurrence of catastrophic failures once the threshold of particular monitored parameters is reached. It can be seen that two major steps are involved in the process of the CM, namely identifying degradation indicators of failures and detecting physical states of them [22]. For power modules, various device parameters have been identified as the degradation precursor, such as on-state voltage [39], on-state resistance [40], switching transition [41], threshold gate voltage [42, 43], thermal resistance [44], short-circuit current [45], case temperature [46] etc. Nevertheless, the challenge lies in the detection of the above signals. Extra measurement circuits and sensors (e.g., voltage, current or thermal sensors) are usually required in the hardware implementation. These methods might be applicable to conventional two-level converters with a limited number of components to be monitored. However, when it comes to MMC-based applications typically with a large number of SMs, condition monitoring may not be a feasible research direction to go due to: 1) the majority of possible methods for power module condition monitoring need calibrations, hardware sensors, or invasive components as revealed from the above literatures; 2) the increased complexity and the failure of additional sensors and circuits may have impact on the operation of the MMC system; 3) wear-out issue of power modules can be addressed by properly sizing and control based on existing extensive studies. Therefore, this Ph.D. thesis will not focus on the condition monitoring of power modules but limit its scope to the condition monitoring of another major components, namely SM capacitors which account for 50% and 80% of the total volume and weight of an SM [48].

Due to features like high voltage rating, self-healing and excellent ripple current performance, metalized polypropylene film (MPPF) capacitors are typically applied in the MMCs [49]. Its dominant failure mechanisms include moisture, corrosion, and dielectric loss [50]. They will lead to the the wear-out of MPPF capacitors with time. However, there are still lack of capacitor lifetime models that distinguish different failure mechanisms due to electrical, thermal, and humidity aspect stresses, which make the lifetime prediction results in the design phase a relatively high-degree of uncertainty. Condition monitoring of SM capacitors are thus recommended during the operation of MMCs to compensate the shortcomings of lifetime prediction. The reduction of capacitance and increase of equivalent series resistance (ESR) are two typical characterization involved in the process of degradation [51]. The

main principles for the estimation of capacitance and ESR always involve the measurement of voltage and current of the capacitor as summarized in [21]. For MMCs, SM capacitor voltage sensors are typically required in the system for capacitor voltage balancing control and can be used to measure the capacitor voltage. It is also possible to calculate the SM capacitor current from the arm current measured by a current sensor and switching signals. The key lies in how to make full use of these signals to estimate the capacitance or ESR easily and accurately.

In summary, based on the above discussions, this Ph.D. project will focus on the MMC mission profile emulator at the beginning, and then will explore the possibilities of reliability-oriented control strategies for power modules and condition monitoring strategies for SM capacitors in the MMC.

1.1.1 MMC Mission Profile Emulator

Among plenty of components in the MMC system, power devices are regarded as one of the most reliability-critical parts [53]. It has been known that thermal stresses (e.g., junction temperature variation and mean junction temperature) have a great impact on the reliability of power devices [54]. Thus, it is of great necessity to carry out the reliability-related testings in the laboratory and in practical applications. In order to see the electro-thermal stress that power semiconductors are subject to, a mission profile emulator is proposed in this project.

However, the power rating of MMC can rate at Megawatt level. The high voltage and high current operation condition challenges the design and implementation of the testing setup. In addition, it is also significant to maintain key reliability features of SMs as the one in practice, especially the junction temperature of power devices [55, 56]. One straightforward way to meet the above demands is to conduct the testing based on a mission profile emulator, in which the current going through the devices, the switching pattern and the capacitor voltages (blocking voltage of the IGBTs) [57] of an SM can be mimicked. Specifically, the following requirements or mission profiles as shown in Fig. 1.3 are supposed to be mimicked:

- **Current profile**: The arm current of the MMC should be emulated and it is supposed to be applicable to the arm current with DC bias and low harmonic components [58].
- **Switching profile**: Should be able to apply switching profiles with a wide range of switching frequencies (e.g., from kHz to several hundreds Hz or even lower [59]).
- **Voltage profile**: Voltage profile refers to the SM capacitor voltage, which is the blocking voltage of power devices. It should be the same as the SM in practice to emulate the switching losses of devices.

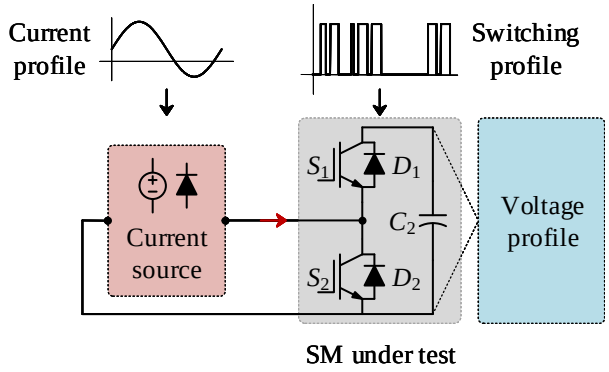

Fig. 1.3: Concept of one SM based testing scheme.

In addition, the current source in Fig. 1.3 is generally achieved by an DC/AC converter, in which a DC power supply is typically required [60]. In order to extend the application scope of the emulator and to facilitate the testing, two requirements in terms of the power supply used in the current source also need to be carefully considered.

- **Reduced voltage rating**: High voltage rating of SMs poses a great challenge to the power supply and the power devices in the current source with much higher voltage ratings. Series connection of power devices is required when this concern is not properly handled and it is not preferable in practical applications.
- **Reduced power rating**: SMs might rate at Megawatt level in practice and the same power rating is required for the power supply if no proper testing topology is used. Thus, power rating of the DC power supply is supposed to be well coped with.

1.1.2 Reliability-Oriented Control of MMCs

In order to improve the reliability performance of the whole MMC system, most existing methods focus on redundancy [61] and periodic preventive maintenance [62]. In addition, the reliability can also be improved from a control point of view. By changing the behavior of components, the thermal stress can be relieved but with no or minor impact on the control performance of the system. Fig. 1.4 lists the possible control variables affecting the thermal stresses of the MMC components.

Reference [63] evaluated the influence of a series of parameters (e.g., circulating current with first- and second-order harmonics and DC offset voltage) on the power loss redistribution among devices and phases. Conclusions show that negligible amounts of total power loss difference in the devices

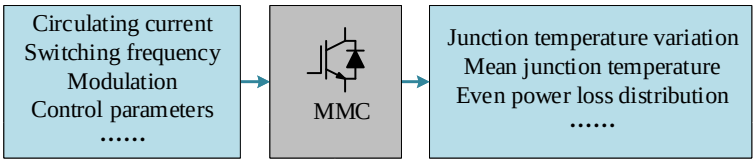

Fig. 1.4: Possible parameters for reliability improvement of MMCs.

can be obtained and its inability of regulating the junction temperature. A thermal balancing control embedded in the capacitor voltage balancing algorithm is proposed in [64]. By introducing one temperature loop, simulation results present that the thermal stresses among devices can be balanced. However, the challenge lies in the junction temperature estimation, which can not be accurately implemented in practice [65]. Additionally, the capacitor voltage is also utilized to achieve the sub-module level thermal balancing control, which might be caused by SM capacitor parameter mismatch [66] and low switching frequency of the MMC. By adjusting the average SM capacitor voltage, the switching losses of SMs can be redistributed and the junction temperature of different devices can be regulated [67]. Even though the aforementioned methods contribute to the reduction of thermal stress and reliability improvement of the power devices in the MMC, further research still need to be conducted.

1.1.3 Capacitor Condition Monitoring of MMCs

Besides reliability-oriented control, condition monitoring is another tool to increase the availability of power converters. According to field operation experience, unpredicted failures of key components can cause a shutdown of the whole system. If immediate access to the converter cannot be achieved, such as offshore wind farm applications [68], it might lead to considerable financial loss [38]. Nevertheless, by means of monitoring the health status of key components, the possibility of catastrophic failures can be reduced by identifying the abnormal behavior and severe degradation of key components in advance. Then preventive maintenances can be scheduled to further reduce the operation and maintenance cost [69].

As mentioned in Section 1.1, the condition monitoring strategy will only focus on the SM capacitors in the MMC system. For conventional two-level converters, CM methods can generally be divided into two categories as summarized in [21], namely hardware based method (e.g., voltage or current sensor) and advanced algorithm based method. However, when it comes to MMCs, the large amount of SMs (e.g., can be hundreds in HVDC applications) makes it not preferable to integrate extra measurement circuits into each SM because of the considerably increased cost and reliability concern.

Therefore, existing CM methods for MMCs are mainly achieved without additional hardwares. The SM capacitor voltage sensors and the arm current sensors have to be made full use of.

Several state-of-the-art research on the CM of capacitors in the MMC are proposed. By taking full advantage of the bleeding resistor inside SMs, reference [70] proposes an CM method based on the RC discharging curve. This method is easy to implement with light computational load. However, the impact of auxiliary power on the capacitance estimation accuracy is not evaluated since SMs in the MMC normally are self-powered by their local capacitors. Additionally, several approaches based on Kalman filter [71], band-pass filter [72], and recursive least square algorithm [73] are proposed for MMC-based applications. Similar to the reference SM based method in [74], all of them estimate the SM capacitance from the SM voltage ripple. However, the major limitation of these methods is the monitoring accuracy. In general, the SM voltage ripple is limited within 10% of its rated voltage. It means that only one tenth of the voltage sensor range can be fully utilized for the CM purpose. Considering 5% capacitance drop of MPPF capacitors at the end-of-life, the detectable voltage change used for CM is only 0.5% of the voltage sensor range. Given the commonly-used voltage sensor accuracies (e.g., 0.1% or 0.3%) in the market, the aforementioned methods might fail to work. Moreover, the voltage ripple amplitude decreases with the drop of the power loading of the MMC [75], and the monitoring accuracy can be further impaired.

Therefore, in order to address the aforementioned limitations, cost-effective, computational-light condition monitoring methods targeting MPPF capacitors with small capacitance drop are explored in this Ph.D. project. Special attention will be paid to the accuracy enhancement of the CM method.

1.2 Project Objectives and Limitations

1.2.1 Research Questions

Based on the above introduction and research motivations regarding various reliability issues of the MMC, the overall question of this Ph.D. project is: ***How to improve the reliability performance of modular multilevel converters by control and condition monitoring?*** More specifically, the following three research subquestions are to be explored:

- How to emulate the operation conditions of MMCs with a minimum viable down-scaled laboratory prototype used for model validation and testing?
- How to improve the reliability performance of MMCs from a control point of view?

- How to conduct no additional hardware-based, cost-effective and computational light condition monitoring for MMCs?

1.2.2 Research Objectives

Once the above research questions are identified, more detailed research objectives are summarized below,

- Mission profile emulator for MMCs
  In order to provide an experimental platform for both Ph.D. project research activities and to facilitate the reliability-related testings of SMs in practice, this Ph.D. project will explore an SM-based mission profile emulator by taking full advantage of the modular structure of the MMC. It should be able to mimic the key electro-thermal features of a practical SM, such as current profiles and switching profiles. Moreover, solutions to reduce the power rating and voltage rating of the power supply used in current source will be explored in order to facilitate the hardware implementation of the mission profile emulator.

- Reliability-oriented control of MMCs

  By taking full advantages of the control freedoms mentioned in Fig. 1.4, this Ph.D. project will explore reliability-oriented control strategies to mitigate the thermal stresses that power modules are subject to. With the knowledge of major stresses, the reliability of the MMC system might be improved by, such as reducing the junction temperature swings, evenly re-distributing the power losses among SMs and so on. At the meantime, the overall system performance, such as efficiency, should better remain unchanged and not deteriorated.

- Condition monitoring for SM capacitors in MMCs
  For the purpose of preventive maintenance with less operation cost and longer reliable operation time, many condition monitoring strategies are proposed for DC-link capacitors in conventional two-level converters. However, it is a challenge to apply them directly to the MMC with many SMs in terms of the involved cost, computational load and reliability issues. In this regard, easy-implemented, computational-light and cost-effective condition monitoring methods will be explored in this Ph.D. project. Meanwhile, considering the small capacitance drop of commonly used film capacitors in the MMC, special attention will be paid to enhancing the monitoring accuracy. Enhancing the richness of degradation precursors and even the way to collect them will contribute to better condition monitoring results and give a bigger picture of the health status of the monitored capacitors from different perspectives.

1.2.3 Project Limitations

The Ph.D. project focuses on the reliability improvement strategies for the MMC, especially from a control and condition monitoring point of view. However, several limitations exist in this project:

- The mission profile emulator considers only the testing of power semiconductors. The electro-thermal behavior and reliability of SM capacitors, which are also one major component prone to failure in the MMC, are not evaluated.
- Due to the existence of DC component in the arm current, thermal stresses of power devices inside one SM are inherently imbalanced. The proposed power loss balancing control focuses only on the sub-module level imbalance instead of the component level.
- Special operation modes are required for the proposed condition monitoring strategies for SM capacitors in this Ph.D. project. CM methods being conducted without special operation modes would be better.

1.3 Thesis Outline

The outcomes of this Ph.D. project are documented by the Ph.D. thesis, which is composed of two main parts, namely Part I-report with six main chapters and Part II-related publications.

Chapter 1 is the introduction of this project with the research background and motivation presented. The project objectives and its limitations are discussed as well. Chapter 2 proposes an SM based mission profile emulator to conduct the testing of the power semiconductors in the MMC. Experimental validation is demonstrated. Chapter 3 and Chapter 4 focus on the reliability improvement strategies from a control perspective. The power loss balancing control is presented in Chapter 3 followed by the adaptive frequency control of MMCs in Chapter 4. Chapter 5 introduces two capacitor condition monitoring strategies for MMCs. Their basic operation principles, flowcharts and practical considerations of implementation and experimental validations are provided. Chapter 6 concludes the project with future research perspectives.

1.4 List of Publications

The publications from this Ph.D. project and their relevance to the chapters are shown in Table. 1.1.

Journal Papers

Table 1.1: Related publications for each chapter published in the thesis.

Chapter No.	Relevant Publications
1	-
2	J1, C5
3	C1, C2, C3
4	C4
5	J3, J4
6	-

J1. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "A viable mission profile emulator for power modules in modular multilevel converters" *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11580-11593, Dec. 2019.

J2. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "A multi-port thermal coupling model for multi-chip power modules suitable for circuit simulators" *Microelectronics Reliability*, vol. 88-90, no. 5, pp. 519-523, Sep. 2018.

J3. **Z. Wang**, Y. Zhang, H. Wang, and F. Blaabjerg, "Capacitor condition monitoring based on the DC-side start-up of modular multilevel converters" *IEEE Trans. Power Electron.*, under review, 2019.

J4. **Z. Wang**, Y. Zhang, H. Wang, and F. Blaabjerg, "A reference sub-module based capacitor condition monitoring method for modular multilevel converters" *IEEE Trans. Power Electron.*, under review, 2019.

Conference Papers

C1. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "An analytical essential switching loss estimation method for modular multilevel converters with nearest level modulation" in *Proc. IEEE IECON*, pp. 762-767, Oct. 2017.

C2. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "Submodule level power loss balancing control for modular multilevel converters" in *Proc. IEEE ECCE* , pp. 5731-5736, Sep. 2018.

C3. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "Balanced conduction loss distribution among SMs in modular multilevel converters" in *Proc. IEEE ECCE Asia*, pp. 3123-3128, Oct. 2018.

C4. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "Mission profile based adaptive carrier frequency control for modular multilevel converters for medium voltage applications" in *Proc. IEEE ECCE Asia*, pp. 1848-1853, Aug. 2019.

C5. **Z. Wang**, H. Wang, Y. Zhang, and F. Blaabjerg, "A minimum viable mission profile emulator for IGBT modules in modular multilevel converters" in *Proc. IEEE APEC*, pp. 313-318, Mar. 2019.

Chapter 2

Mission Profile Emulator for Power Modules in MMCs

In order to provide an experimental platform for the two planned Ph.D. research activities and to facilitate the reliability-related testings of a practical sub-module (SM) in the laboratory, this chapter presents a mission profile emulator for power modules in modular multilevel converters (MMCs) to mimic their thermal stresses and to explore the feasibility for reliability testing as well as thermal model validation. The emulator is able to apply real and practical current profiles and switching profiles to the SM under test. Meanwhile, significantly reduced voltage and power requirements for the dc power supply used in the current source can extend the application scope of this testing setup in terms of the testing of higher voltage rated power devices.

2.1 Background

Power devices are regarded as one of the components prone to failure in power electronic systems as reported in an industry survey [76]. As the key components, the massive application of power modules might introduce reliability concerns to the operation of MMC systems. As electro-thermal stress is an important mechanism resulting in fatigue and failure for power semiconductors [32], the reliability testing of the MMC, especially from a electro-thermal point of view, is pretty important for both laboratory validation and testing prior to field operations of the MMC.

In order to reduce the required resources [29], SM based testing is greatly recommended given that all SMs applied are the same in hardware due to the modular structure of the MMC. To meet the requirements mentioned

above, a viable mission profile emulator based on a full-bridge converter and an auxiliary SM is proposed in this Ph.D. project. Its topology and modulation algorithm are presented. For comparison, several existing SM based testing solutions are introduced. In addition, issues regarding the practical implementation of the mission profile emulator, such as control and hardware parameter selection, the carrier frequency selection for the voltage stabilizer, and the impact of current ripple on the power loss, are discussed. Finally, experimental validations are given.

2.2 Existing SM Based Testing Solutions

The state-of-the-art SM based solutions are introduced in this section to illustrate the challenge of SM testing. Their major advantages and limitations are summarized in Table 2.1.

Table 2.1: Comparison between the proposed mission profile emulator and other testing schemes when the rated SM voltage is 2 kV. Source: [J1]

Testing capabilities		Proposed	[77]	[60]	[78]	[29]
DC power supply voltage		Wide range	545 V	$>$ 2 kV	= 2 kV	—
Switching profile	High switching frequency	√	√	√	√	√
	Low switching frequency	√	√	√	×	×
Current profile	DC current	√	√	√	√	×
	Second-order current	√	√	√	√	×

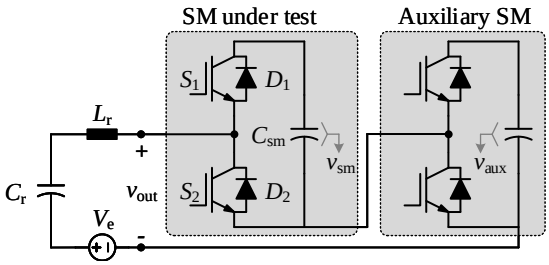

Fig. 2.1: Dual SM based resonant testing scheme.

- Dual SM based resonant testing scheme [29]

  Resonance between the inductor L_r and capacitor C_r generates a sinusoidal current as shown in Fig. 2.1. It can be used as the arm current to stress the SM under test. By switching the auxiliary SM in opposition with the SM under test, DC component of the two SM voltages (i.e., v_{sm} and v_{aux}) are canceled and only doubled AC voltages exist in the

output voltage v_{out}. A smaller inductor L_{r} can thus be applied in this setup to fulfill the same arm current ripple requirement of the MMC. However, the resonant circuit can only generate sinusoidal current and is not able to mimic the DC component in the arm current of MMCs.

- Dual half-bridge SM based testing scheme [78]

  As shown in Fig. 2.2, one half-bridge SM is used to mimic the grid side voltage of the MMC system. The SM under test regulates the current going through the inductor L_{c}. However, the setup focuses more on the electrical characteristics of the MMC instead of the thermal performance. It is not applicable to low switching frequency mission profiles (e.g., nearest level modulation (NLM)), where undesirable harmonics might be introduced into the arm current.

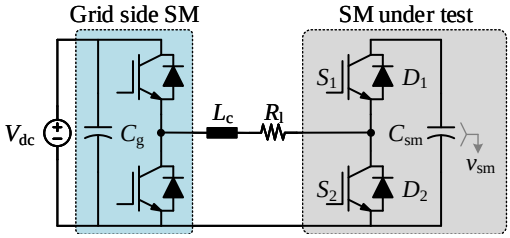

Fig. 2.2: Dual half-bridge SM based testing scheme.

- Full-bridge current source based testing scheme [60]

  A full-bridge converter is employed as the current source as shown in Fig. 2.3. It is utilized to track the current profile, where both dc current and low switching profiles can be applied. Nevertheless, the voltage V_{dc} of the DC power supply has to be higher than the voltage v_{sm} of the SM under test, which restrains its application, especially for high-voltage power semiconductors.

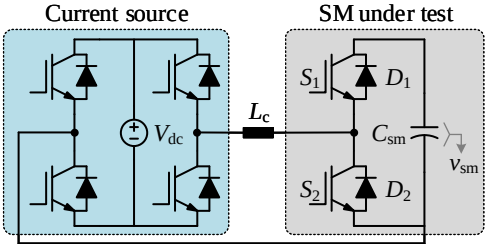

Fig. 2.3: Full-bridge current source based testing scheme.

- Full-bridge current source dual SM based testing scheme [77]

Reference [77] takes advantage of a reverse-connected auxiliary SM as shown in Fig. 2.4. By proper control, the power supply voltage V_{dc} can be as low as one fifth of the voltage v_{sm} of SM, and the test capability is correspondingly improved. SMs with five times higher blocking voltage can be tested in this setup. However, it should be noted that the power supply voltage and the voltage of the SM under test are still coupled with each other. The voltage V_{dc} of the power supply can not be selected independently and should be high enough.

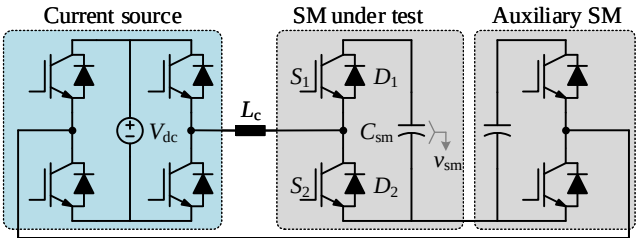

Fig. 2.4: Full-bridge current source dual SM based testing scheme.

2.3 Topology and Control Scheme

Topology, working principle and control strategy of the proposed SM based mission profile emulator are studied in this section. Several design guidelines regarding the control and hardware parameter selection are discussed. Besides, how the current ripple and voltage ripple affect the conduction losses and switching losses of the power devices is investigated. A case study is demonstrated to validate the above analysis.

2.3.1 Topology of Mission Profile Emulator

The proposed mission profile emulator consists of four major parts: namely current source, coupling inductor L_c, SM under test, and a voltage stabilizer as shown in Fig. 2.5.

The detailed circuit diagram is shown in Fig. 2.6. The specific function of the four parts are summarized as given below:

- **Current source**: The current source aims to track the current profile of the SM under test in order to keep the same stress as the SM in a practical MMC. It should be able to mimic a DC-bias, fundamental, and second-order harmonics of the arm current. Proportional integral (PI) controller or proportional resonant (PR) controller can be applied to the current control [79].

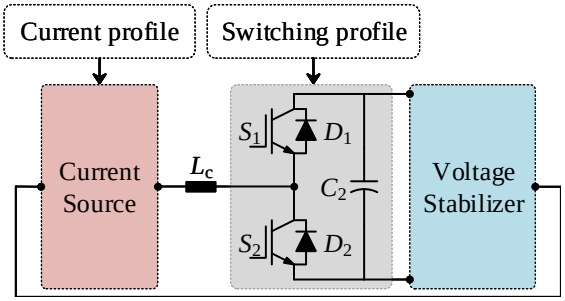

Fig. 2.5: Simplified circuit diagram of the proposed mission profile emulator. Source: [J1]

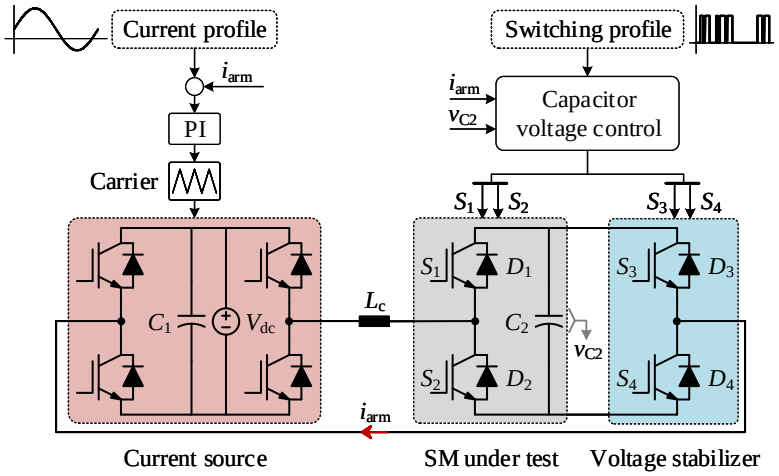

Fig. 2.6: Detailed circuit diagram of the mission profile emulator (i_{arm} is the arm current, v_{C2} is the voltage of capacitor C_2, L_c is the coupling inductor and V_{dc} is the voltage of the DC power supply). Source: [J1]

- **Coupling inductor** L_c: Coupling inductor ensures reactive power flow within the setup to greatly reduce the power rating requirement of the DC power supply. The only active power dissipation in this emulator is the power loss of the system.
- **SM under test**: SM under test is controlled by the switching profile, which cannot be interfered by other controls with extra switching actions.
- **Voltage stabilizer**: By properly regulating the two auxiliary power devices S_3 and S_4, the voltage stabilizer is able to keep the voltage v_{C2} of capacitor C_2 stable at the average voltage of the SM under test. Therefore, almost the same switching loss behavior as in practice can be achieved for SM under test. Note that capacitor C_2 is different from

the capacitor applied in the practical SM. The capacitor C_2 serves to maintain the blocking voltage of the power devices only to obtain the similar switching loss behavior as the power devices in real SMs. In addition, S_3 and S_1 share the same gate signal obtained from the switching profile. They are complementary to the gate signals of S_2 and S_4. Fig. 2.7 shows the ideal current paths in the SM under test.

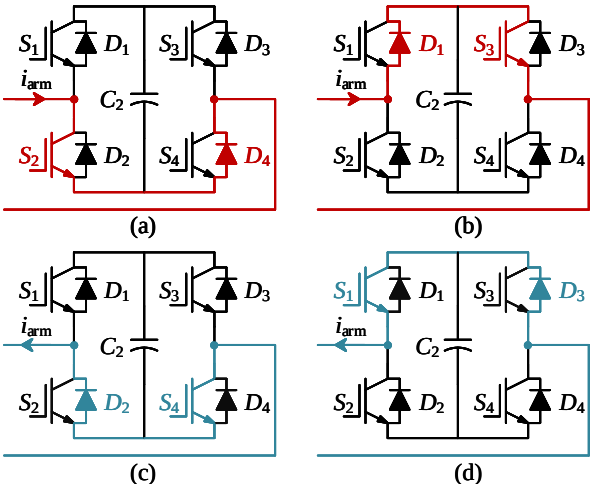

Fig. 2.7: Ideal current paths in the SM under test and the voltage stabilizer. (a) Bypass state of SM with a positive current; (b) Insert state of SM with a positive current; (c) Bypass state of SM with a negative current; (d) Insert state of SM with a negative current. Source: [J1]

As it can be seen, the capacitor C_2 is not inserted into the main current path regardless of the switching profile and the current profile. This feature offers two major advantages:

- Since there is always a current path inside the SM under test without passing through the capacitor C_2, the current profile is thus decoupled with the switching profile. Different practical switching profiles can thus be tested based on the proposed mission profile emulator.
- DC power supply voltage V_{dc} is decoupled with the high voltage across the capacitor C_2. It means that the voltage of DC power supply can be as low as possible theoretically under the condition that the coupling inductor L_c is properly designed accordingly. The reduced voltage requirement of the power supply greatly facilitate the test of SMs rated at high voltage.

2.3.2 Control of Mission Profile Emulator

Two main control targets are involved in this part, namely the arm current control and the capacitor voltage control as shown in Fig. 2.6. The current profile can be achieved by a PI controller or a PR controller and is not further discussed in this section. As for the capacitor voltage control, it is essential to the switching loss emulation of SM under test. The voltage of the capacitor C_2 grows in practice due to turn-on delays, which are necessary to avoid short circuit faults between the IGBT devices in the same half-bridge leg. Fig. 2.8 shows how the turn-on delays can get C_2 charged by the non-ideal current paths. Consequently, the capacitor voltage v_{C2} might deviate from its rated value, especially when a high frequency switching profile is applied. Thus, a capacitor voltage controller is necessary. As the SM under test is strictly regulated by the switching profile, thus the voltage stabilizer has to take the responsibility. Two cases are taken into account regarding different switching mission profiles.

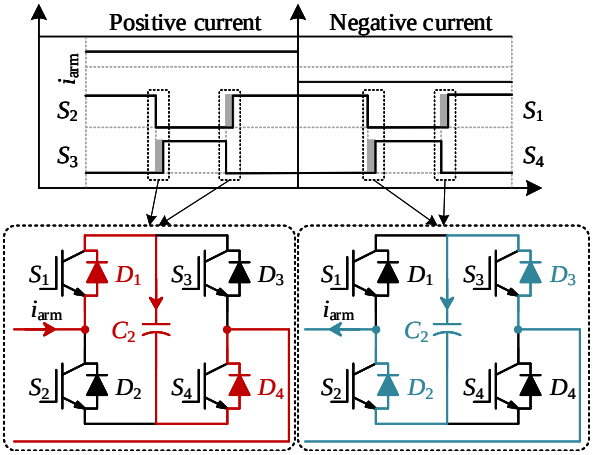

Fig. 2.8: Non-ideal current paths during the turn-on delays. Source: [J1]

- **High Switching Frequency Mission Profile**

  Regarding high switching frequency applications like mission profiles from Phase Shifted Carrier (PSC) modulation, the capacitor voltage control can be achieved by introducing an dynamic adjustment to the original voltage reference as shown in Fig. 2.9. By doing so, the same actual switching frequency can be applied to the power devices in SM under test and the two auxiliary IGBTs with similar switching loss.

- **Low Switching Frequency Mission Profile**

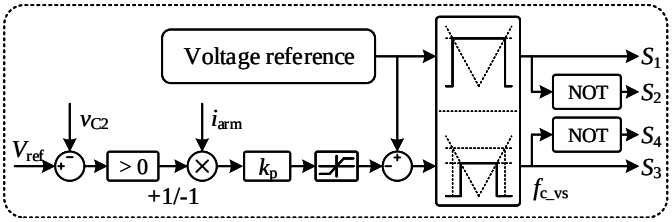

Fig. 2.9: Capacitor voltage control for high switching frequency mission profiles (V_{ref} is the voltage reference of the capacitor voltage control, f_{c_vs} is the carrier frequency used in the voltage stabilizer, and k_p is the control gain). Source: [J1]

Compared with the control method in Fig. 2.9, less switching transitions can be utilized to control the SM capacitor voltage when the switching profile has low equivalent switching frequency. Thus, the method shown in Fig. 2.10 is proposed. By combining the original switching profile with additional high switching frequency signals, the gate signals for S_3 and S_4 can be obtained. Moreover, it can be seen from Fig. 2.10 that, in some cases, the gate signals of S_3 and S_4 are the same as the original switching profile even after the logic operation, Thus, these additional switching signals are ineffective and are not able to change the capacitor voltage v_{C2}.

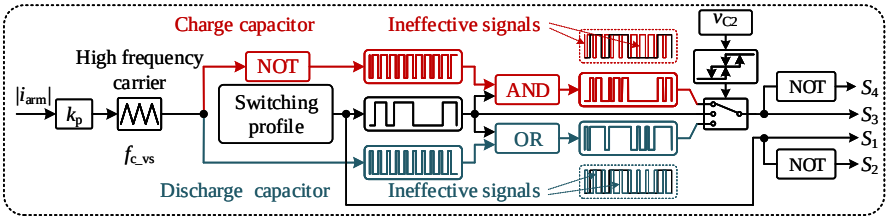

Fig. 2.10: Capacitor voltage control for low switching frequency mission profiles. Source: [J1]

2.3.3 Control and Hardware Parameter Selection

In order to meet testing requirements, three major types of components used in the mission profile emulator, namely the power modules, coupling inductor L_C and power supply V_{dc} needs to be sized accordingly.

- **Control Parameter**

As it can be seen in Fig. 2.9 and Fig. 2.10, the control gain k_p that needs to be well tuned since it determines the current ripple to a great extent. First of all, the current ripple is given as

$$\Delta I = \frac{V_{C2}}{L_c} T_a = k_a \left| i_{arm} \right|, \tag{2.1}$$

where V_{C2} refers to the capacitor voltage of C_2; L_c refers to the coupling inductance; k_a is the constant current ripple ratio, which limits the current error caused by the proposed capacitor voltage control; T_a defines the duration of the additional switching action. The duty ratio introduced by T_a is equal to $k_p \left| i_{arm} \right|$

$$T_a f_{c\_vs} = \frac{k_a \left| i_{arm} \right| L_c f_{c\_vs}}{V_{C2}} = k_p \left| i_{arm} \right|, \tag{2.2}$$

where f_{c_vs} refers to the carrier frequency used in the voltage stabilizer and k_p is defined as the proportional gain to limit the current ripple

$$k_p = \frac{k_a L_c f_{c\_vs}}{V_{C2}}. \tag{2.3}$$

By using (2.3), the current error caused by the capacitor voltage control can be limited within $k_a \times 100\%$ of the actual current.

- **IGBT Modules**

It is recommended that all IGBT modules in the current source and the voltage stabilizer are supposed to have higher voltage and current ratings than that of the SM under test. A series of potential SMs with different ratings can be tested by the mission profile emulator. Meanwhile, longer lifetime than the SM under test can be expected for the current source and voltage stabilizer without frequent hardware modification. Moreover, independent cooling system are supposed to be used to avoid thermal coupling with the SM under test.

- **Coupling Inductor L_c and DC Power Supply**

The coupling inductor L_c and the power supply interacts with each other. The maximum inductance L_{c_max} is determined by the dynamic current tracking performance. The current response should be fast enough to mimic the current profile. By analyzing all possible current variations caused by different reasons as shown in Fig. 2.11, the following relationship holds

$$\begin{cases} \Delta i_{arm\_c} = \dfrac{V_{dc}}{L_c} T_{c\_vs} \\ \Delta i_{ref} = \dfrac{d i_{arm}}{dt} T_{c\_vs} \\ \Delta i_{arm\_a} = k_a i_{arm} \\ \Delta i_{arm\_d} = \dfrac{V_{C2}}{L_c} T_d \\ \Delta i_{arm\_c} \geq \Delta i_{ref} + \Delta i_{arm\_a} + \Delta i_{arm\_d}, \end{cases} \tag{2.4}$$

where Δi_{arm_c}, Δi_{ref}, Δi_{arm_a}, and Δi_{arm_d} refer to the current changes caused by the power supply, current reference, capacitor voltage control, and turn-on

delay, respectively; V_{dc} refers to the voltage of the DC power supply; T_{c_vs} is the period of the carrier in the current source; T_d defines the duration of the turn-on delay.

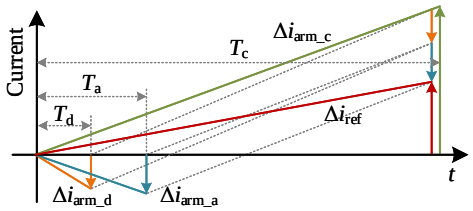

Fig. 2.11: Current changes caused by the DC power supply (Δi_{arm_c}), current reference (Δi_{ref}), turn-on delay (Δi_{arm_d}), and capacitor voltage control (Δi_{arm_a}) in one carrier period. (T_d is the period of the turn-on delay, T_a is the period of the additional switching actions for capacitor voltage control, and T_c is the duration of one carrier period.) Source: [J1]

The maximum allowed inductance is

$$L_{c\_max} = \frac{V_{dc} T_{c\_vs} - V_{C2} T_d}{\left(k_a I_0 + \sqrt{\omega^2 T_{c\_vs}^2 + k_a^2} I_1 + \sqrt{4\omega^2 T_{c\_vs}^2 + k_a^2} I_2\right)}. \tag{2.5}$$

The requirement of an arm current ripple caused by the Pulse Width Modulation (PWM) decides the minimum inductance L_{c_min} as

$$L_{c\_min} = \frac{T_{c\_vs} V_{dc}}{4 I_{r\_max}}, \tag{2.6}$$

in which I_{r_max} refers to the current ripple amplitude caused by the PWM.

- **Switching Profile Classification**

Capacitor voltage change caused by two factors (i.e., the turn-on delay and the additional switching actions) decides the classification of the mission profile. The turn-on delays always charge the capacitor C_2 by

$$\Delta v_{C2\_d\_i} = \frac{1}{C_2} \int_{t}^{t+T_d} |i_{arm}| dt \approx \frac{T_d}{C_2} |I_{arm\_i}|, \tag{2.7}$$

where C_2 is the capacitance; $\Delta v_{C2\_d\_i}$ refers to the voltage increase caused by the i-th turn-on delay; T_d refers to the duration of turn-on delay; I_{arm_i} is the current amplitude during the turn-on delay. Due to a short period of delay, constant current is assumed.

Additional switching actions introduced by the capacitor voltage control can either charge or discharge the capacitor C_2 as

$$\Delta v_{C2\_a\_i} = \frac{1}{C_2} \int_{t}^{t+T_{a\_i}} |i_{arm}| dt \approx \frac{k_a L_c}{C_2 V_{C2}} |I_{arm\_i}|^2, \tag{2.8}$$

where $\Delta v_{\text{C2\_a\_i}}$ is the voltage change caused by the i-th additional switching action in the time interval of $T_{\text{a\_i}}$.

Combining (2.7) and (2.8), the capacitor voltage variation in one fundamental period is

$$\begin{aligned}\Delta V_{\text{C2\_in/de}} &= \sum_{i=0}^{N_{\text{a}}} \Delta v_{\text{C2\_a\_i}} \pm \sum_{i=0}^{N_{\text{DUT}}} \Delta v_{\text{C2\_d\_i}} \\ &\approx \frac{f_{\text{c\_vs}}}{f_1} \frac{k_{\text{a}} L_{\text{arm}}}{C_2 V_{\text{C2}}} \overline{|i_{\text{arm}}|^2} \pm \frac{f_{\text{e\_DUT}}}{f_1} \frac{T_{\text{d}}}{C_2} \overline{|i_{\text{arm}}|},\end{aligned} \tag{2.9}$$

where $\Delta V_{\text{C2\_in/de}}$ refers to the voltage change in one fundamental period; N_{a} is equal to $f_{\text{c\_vs}}/f_1$; N_{DUT} is the number of the switching transitions of the SM under test in one fundamental period, which is equal to $f_{\text{e\_DUT}}/f_1$ determined by the mission profile; f_1 is the fundamental frequency, which is 50 Hz in this case study; $f_{\text{c\_vs}}$ refers to the carrier frequency applied in the voltage stabilizer; $f_{\text{e\_DUT}}$ refers to the equivalent switching frequency of the DUT; $\overline{|i_{\text{arm}}|^2}$ and $\overline{|i_{\text{arm}}|^2}$ are the average of $|i_{\text{arm}}|^2$ and $|i_{\text{arm}}|$ in one fundamental period.

The time taken to obtain a certain capacitor voltage change ΔV_{C2} is

$$T_{\text{in/de}} = \frac{\Delta V_{\text{C2}}}{f_1 \Delta V_{\text{C2\_in/de}}}, \tag{2.10}$$

When a minimum $T_{\text{in/de}}$ is set to ensure an reasonable performance of the capacitor voltage control, the carrier frequency obtained from the above equations is the threshold to distinguish different mission profiles.

2.3.4 Practical Considerations

MMC has excellent current harmonic performance due to its high equivalent switching frequency [80]. Thus, the current ripple caused by the PWM might contribute to different conduction loss behavior of the power devices in the SM under test and should be evaluated. Moreover, the capacitor voltage v_{C2} is controlled to be a constant, which is different from the practical SM voltage with ripples. Therefore, the absence of voltage ripple might lead to different switching loss behavior of the power devices and is supposed to be assessed as well. Two case studies based on a full-scale MMC system and the propose mission profile emulator are discussed. Their system parameters are listed in Table 2.2.

- **Impact of Current Ripple on the Conduction Losses**

By linearizing the on-state voltage of the power devices as $V_{\text{on}} = V_{\text{on\_0}} + R_{\text{on}} |i_{\text{arm}}|$ with $V_{\text{on\_0}}$ being the on-state zero-current voltage drop and R_{on}

Table 2.2: Main parameters of IGBTs used in full-scale MMC and the mission profile emulator. Source: [J1]

MMC system	Full-scale	Mission profile emulator
Power rating	30 MVA	-
DC link voltage	50 kV	-
SM number per arm N	20	-
SM capacitor voltage	2.5 kV	300 V
Power module	5SNA_1200G450350	F4_50R12KS4
V_{on_0}	1.5 V	1.9 V
R_{on}	0.52 mΩ	31.6 mΩ

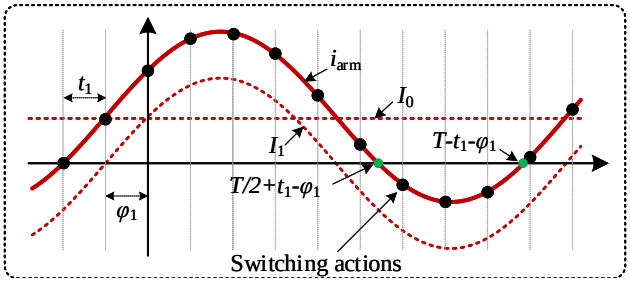

Fig. 2.12: Ideal arm current waveform with DC circulating current and simplified evenly-distributed switching actions. Source: [J1]

being the equivalent on-state resistance, the sum of the conduction losses of the four semiconductors can be evaluated in one fundamental period as

$$\begin{aligned} P_{\text{con\_sm}} &= \frac{1}{T}\int_{-t_1-\varphi_1}^{T/2+t_1-\varphi_1} V_{\text{on}}\,|i_{\text{arm}}|dt + \frac{1}{T}\int_{T/2+t_1-\varphi_1}^{T-t_1-\varphi_1} V_{\text{on}}\,|i_{\text{arm}}|dt \\ &= P(I_0, I_1) + P(I_{\text{r\_max}}) \end{aligned} \tag{2.11}$$

where T refers to the fundamental period; t_1 is shown in Fig. 2.12; $P(I_0, I_1)$ is the conduction loss independent of the current ripple, and $P(I_{\text{r\_max}})$ is the conduction loss caused by the current ripple.

The maximum conduction loss error introduced by the ripple current is

$$\frac{P(I_{\text{r\_max}})}{P(I_0, I_1)} \leq \frac{P_{\text{max}}(I_{\text{r\_max}})}{P(I_0, I_1)} = e_{\text{con\_max}}, \tag{2.12}$$

Considering the main device parameters listed in Table 2.2, the maximum conduction loss error is below 0.1% for both scenarios as shown in Fig. 2.13. Thus, the current ripple impact on the conduction loss is negligible.

- **Impact of Voltage Ripple on the Switching Losses**

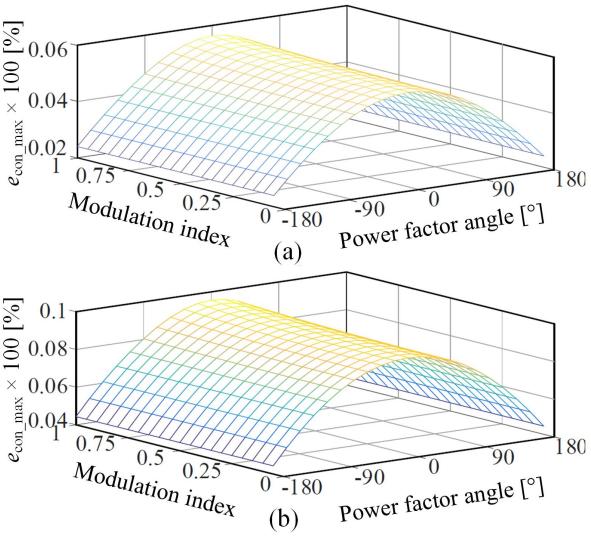

Fig. 2.13: Maximum conduction loss error introduced by the current ripple: (a) Full-scale MMC and (b) Mission profile emulator. Source: [J1]

Since the blocking voltage of IGBTs is a constant voltage of C_2 without including voltage ripple, its effect on the switching loss of the SM has to be assessed. The switching energy of the power devices is

$$E_{\text{sw}}(i_{\text{arm}}, v_{\text{sm}}, T_{\text{j}}) = E_{\text{sw}}(i_{\text{arm}}, V_{\text{ref}}, T_{\text{ref}})[1 + K_{\text{T}}(T_{\text{j}} - T_{\text{ref}})]\frac{v_{\text{sm}}}{V_{\text{ref}}}, \tag{2.13}$$

in which $E_{\text{sw}}(i_{\text{arm}}, V_{\text{ref}}, T_{\text{ref}})$ is the curve-fitted switching energy obtained from the data-sheet provided information under the junction temperature T_{ref} and the blocking voltage V_{ref}, v_{sm} refers to the actual SM capacitor voltage, K_{T} is a constant temperature coefficient, and T_{j} is the junction temperature.

Assuming an even distribution of switching actions of IGBTs in one fundamental period, the total switching loss of IGBTs and diodes ($E_{\text{sw\_on}}$, $E_{\text{sw\_off}}$ and $E_{\text{sw\_rec}}$) is calculated as $\sum E_{\text{sw\_x}}(i_{\text{arm}}, v_{\text{sm}}, T_{\text{j}})$. Thus, the switching energy error caused by omitting voltage ripple in one fundamental period is

$$e_{\text{sw}} = \frac{\sum_{1}^{N_{\text{s}}} \sum E_{\text{sw\_x}}(i_{\text{arm}}, v_{\text{sm}}, T_{\text{j}}) v_{\text{sm\_ripple}}}{\sum_{1}^{N_{\text{s}}} \sum E_{\text{sw\_x}}(i_{\text{arm}}, v_{\text{sm}}, T_{\text{j}}) v_{\text{sm}}}, \tag{2.14}$$

where N_{s} is the number of switching transitions in one fundamental period.

Figs. 2.14 show that the maximum switching loss error is within 1.5% by ignoring the SM voltage ripple (e.g., 10% in this case study). Thus, a constant

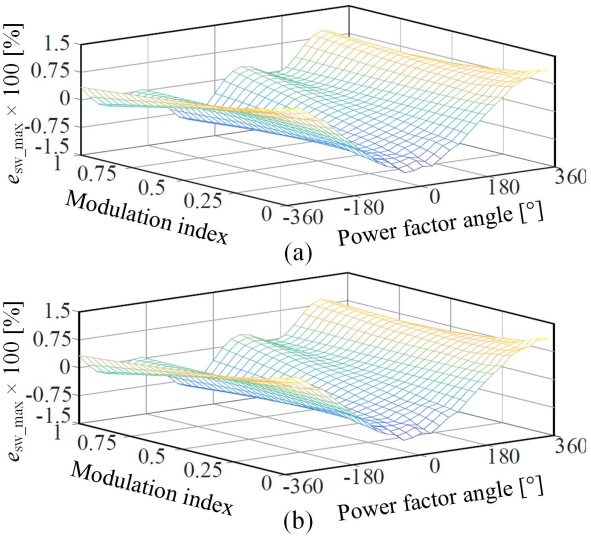

Fig. 2.14: Maximum switching loss error introduced by the absence of the SM voltage ripple: (a) Full-scale MMC and (b) Mission profile emulator. Source: [J1]

capacitor voltage is a reasonable solution in the mission profile emulator from the switching loss point of view.

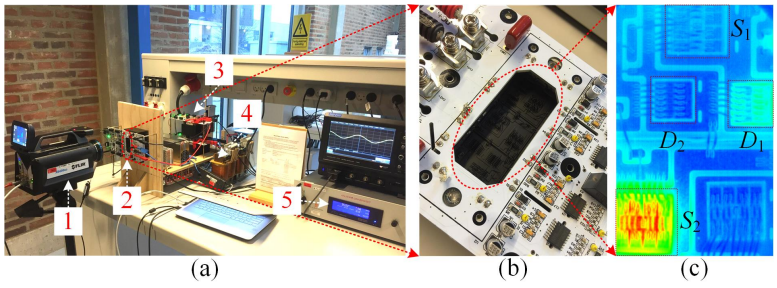

Fig. 2.15: Experimental setup of the proposed mission profile emulator: (a) photo of the setup, (b) photo of the SM with black painted IGBT module, (c) thermal distribution of the devices in the SM under test (1: Thermal Camera, 2: Device Under Test, 3: Current source and the voltage stabilizer, 4: Inductor, and 5: Power Supply.)). Source: [J1]

2.4 Mission Profile Emulator Demonstration

In order to validate the proposed mission profile emulator, an experimental setup is built as shown in Fig. 2.15 with the main system parameters being listed in Table 2.3. Three full-bridge IGBT modules from Infineon are

employed. One module serves to carry out the current source. Another two serve as the SM under test and the voltage stabilizer, respectively, at the half-bridge status in order to avoid the thermal coupling between the two half-bridges. First of all, the capacitor voltage control strategies are validated based on two mission profiles (i.e., high and low switching frequencies). Then, two capabilities, AC power cycling testing and electro-thermal model validation, that the emulator has are demonstrated.

Table 2.3: Main experimental parameters of the mission profile emulator. Source: [J1]

Parameter	Value
DC power supply voltage V_{dc}	40.0 V
Average capacitor voltage V_{C2}	300.0 V
Coupling inductor L_c	1.5 mH
Capacitor C_2	1.4 mF
DC current amplitude I_0	10.0 A
Fundamental current amplitude I_1	20.0 A
Current ripple radio k_a	0.05
Carrier frequency of current source f_{c_cs}	6.0 kHz
Carrier frequency of voltage stabilizer f_{c_vs}	1.5/2.0 kHz
Equivalent frequency of DUT f_{e_DUT}	1.5/0.1 kHz
Fundamental frequency f_1	50 Hz
Turn-on delay T_d	2.0 us
Ambient temperature T_{amb}	20 °C
IGBT module	F4_50R12KS4

2.4.1 Capacitor Voltage Control

The experimental results of the capacitor voltage control in high and low switching frequency mission profile applications are shown in Fig. 2.16 and Fig. 2.17, respectively. It should be noted that the capacitor voltage v_{C2} should be charged to its required steady state voltage (e.g., in this case study, the voltage is 300 V) in the start-up process. Afterwards, the emulator can start to work normally. Therefore, it can be observed that the capacitor is charged gradually from zero to 300 V at the beginning. It takes roughly 2.5 and 7.5 seconds in the two cases. The time difference is caused by the ineffective signals as discussed in Fig. 2.9, where the extra switching transitions are the same as the gate signal from the original mission profile. In the zoom-in Fig. 2.16(b) and Fig. 2.17(b), the current profile is emulated very well with limited ripples and the capacitor voltage stabilizes at around 300 V, which is the targeted value in terms of the average voltage of SM under test. Additionally, the modulation pattern shown in Fig. 2.9 can be clearly observed, where the turn-on delays and turn-off leads are embedded into S_3 to regulate the capacitor voltage compared with S_1. From Fig. 2.10, additional high frequency switching actions are inserted when the capacitor voltage control

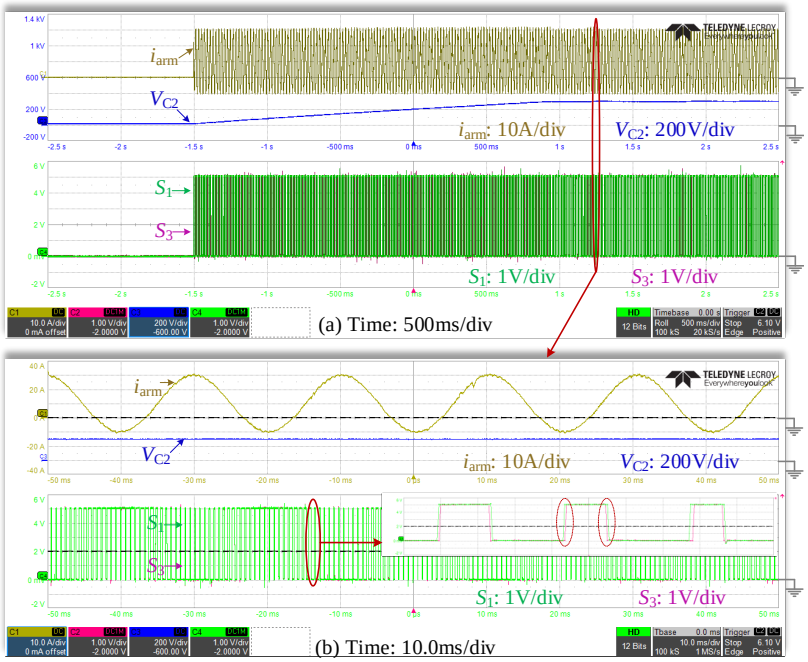

Fig. 2.16: Experimental waveforms of the arm current, the capacitor voltage and the gate signals with DUT operating with phase shifted carrier modulation. Source: [J1]

is enabled to limit the voltage within a certain band.

2.4.2 AC Power Cycling Testing

The proposed mission profile emulator is able to carry out AC power cycling testing [54], where the power semiconductors are stressed under more practical loading conditions than conventional DC power cycling testing. Several major testing indicators, namely the cycle period, the junction temperature variation, and the mean junction temperature can be adjusted in terms of different testing requirements accordingly.

Experimental results of the junction temperature response of the four power devices in a half-bridge SM are shown in Fig. 2.18. It can be seen that different temperature variations can be achieved by changing the power loading levels (0.9 kW, 1.8 kW, and 2.7 kW at 0, 20, and 40 minutes respectively). Meanwhile, the average junction temperature increases slightly as well. Increasing the switching frequency and the blocking voltage of the power devices can also pose higher stress to accelerate the power cycling testing.

In order to show the impact of cycle period on the temperature variation, a

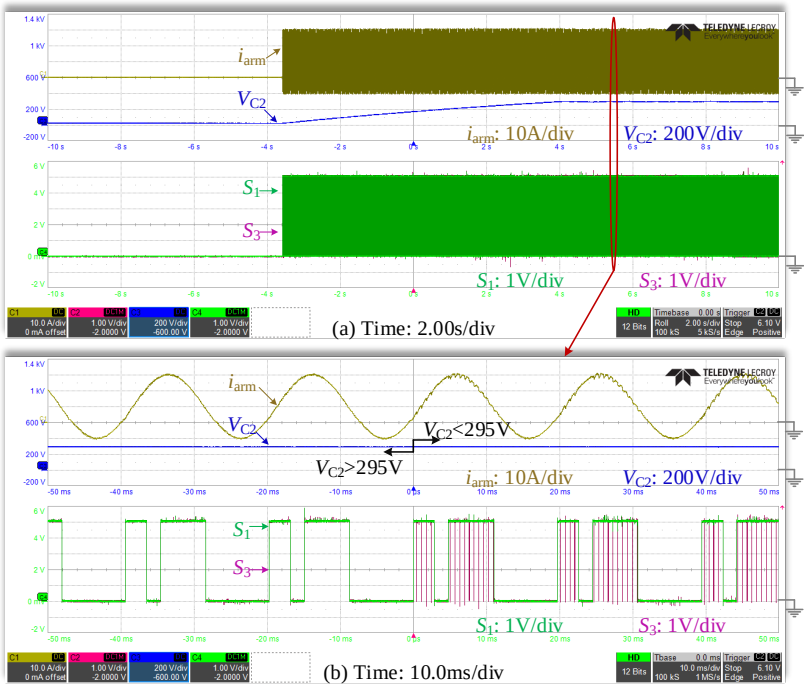

Fig. 2.17: Experimental waveforms of the arm current, the capacitor voltage and the gate signals with DUT operating with nearest level modulation. Source: [J1]

series of experimental results regarding different temperature cycle frequencies are shown in Fig. 2.19. It can be seen that the junction temperature swing increases with the drop of the applied fundamental frequency. Additionally, due to the uneven thermal distribution among the power devices in the SM, S_2 expects to be the first device reaching the end-of-life.

2.4.3 Electro-Thermal Model Validation

Thermal model provided by the manufacturer cannot be used directly to accurately estimate the junction temperature of power devices due to the following reasons:

- The cooling systems of the actual SMs may be different from the one which the thermal impedance of the power module is characterized in the data-sheet. Thus, in this case, the thermal model has to be rebuilt and validated [81].
- Data-sheets normally provide a Foster model instead of Cauer model of the power devices. However, since Foster model does not have physical

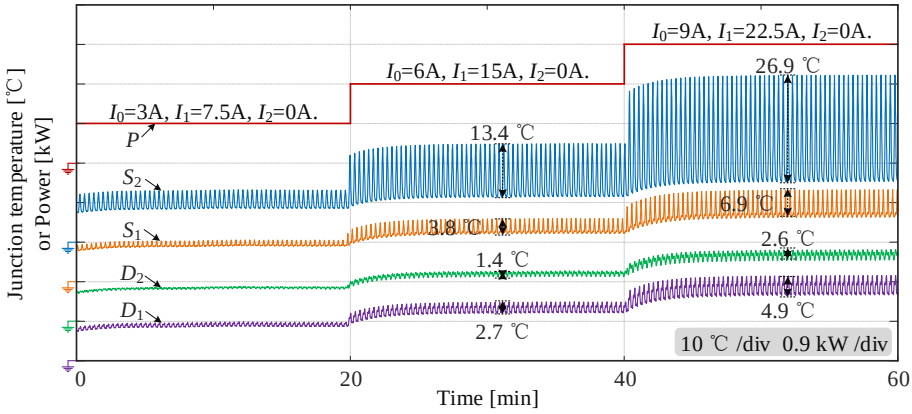

Fig. 2.18: Measured junction temperatures of four DUTs under different power levels in 60 minutes with the cycle period being 20 s. (The arm current profile consists of three parts, namely the DC, fundamental, and the second-order components with their amplitudes being I_0, I_1, and I_2, respectively.) Source: [J1]

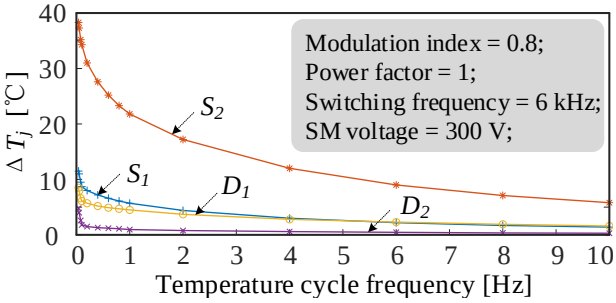

Fig. 2.19: Junction temperature variation of the four power devices tested under different temperature cycle frequencies. Source: [J1]

meaning, different Foster models cannot be connected in series directly. For example, the Foster models of the power device and its heat-sink cannot be connected.

- Thermal coupling effects are not considered by the thermal model from data-sheet, especially for multi-chip modules, where different power devices interact with each other through the shared baseplate and the heat-sink.

Thus, a complete thermal model from the junction to the ambient via the thermal grease and heat-sink has to be rebuilt and validated in order to achieve a more realistic junction temperature estimation. The proposed mission profile emulator can be used to fulfill the above target for power devices in MMCs.

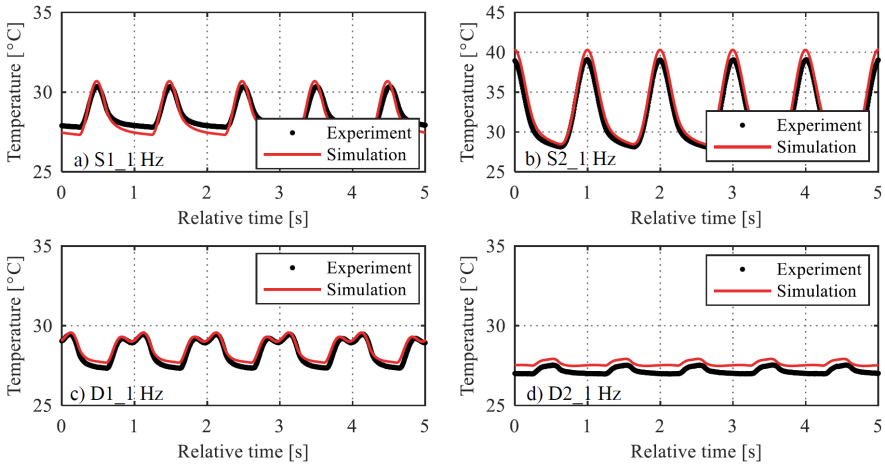

Fig. 2.20: Measured and simulated waveforms of the steady state junction temperature of the four devices with the frequency being 1 Hz. (a) S_1, (b) S_2, (c) D_1, and (d) D_2. Source: [J1]

Fig. 2.20 shows the simulation and experiment results of the steady-state temperature of all four devices. The average junction temperature estimation error is up to 0.6 °C for the four devices. The most stressed device is S_2 in this case study, where the power is transferred from the DC side to the AC side of the MMC. The reason is the existence of an inherent DC bias in the arm current. Thus, it can be seen that the thermal imbalance among devices might limit the lifetime of the whole SM.

Fig. 2.21 presents the junction temperature of the most stressed device S_2. Various fundamental frequencies are applied ranging from 50 Hz to 0.1 Hz. It can be seen that the temperature variation from simulations are in well agreement with the experimental results with the maximum error being 0.9 °C when the frequency is 1 Hz. The temperature error of the mean junction temperature decreases from 1.5 °C to 0.2 °C when the frequency changes from 50 Hz to 0.1 Hz.

2.5 Summary

In this chapter, a viable mission profile emulator for power modules in the MMC has been proposed with three main parts, namely a current source, SM under test, and voltage stabilizer. A full bridge converter serves as the controlled current source for current profile emulation. An auxiliary SM, serving as the voltage stabilizer, is employed to keep a constant blocking voltage for power devices in order to achieve similar switching losses as in practice. A coupling inductor allows reactive power flow inside the emulator.

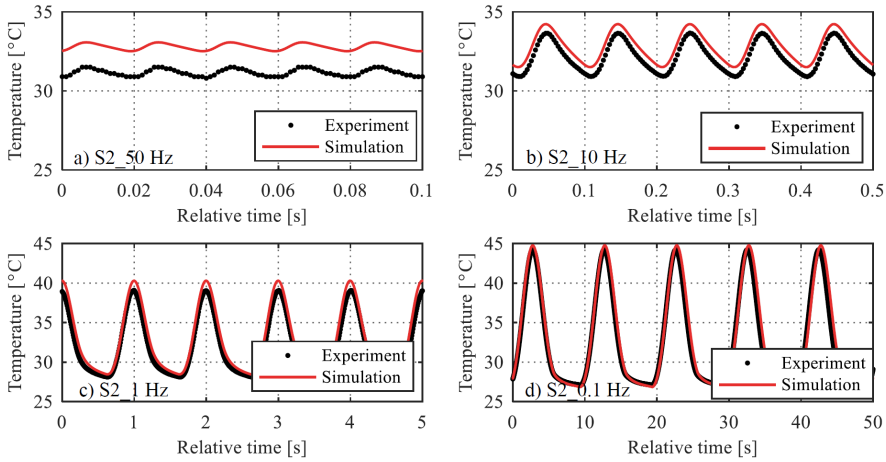

Fig. 2.21: Measured and simulated waveforms of the steady state junction temperature of the device S_2 under different current frequencies. (a) 50 Hz, (b) 10 Hz, (c) 1 Hz, and (d) 0.1 Hz. Source: [J1]

The proposed mission profile emulator has the following advantages:

- Current profile is decoupled with the switching profile, which means that a wide range of practical current profiles and switching profiles can be applied in this emulator.
- The power rating requirement of the DC power supply is greatly reduced due to the reactive power flow in this setup. The active power that the power supply needs to deal with is the power losses of the emulator only.
- The voltage rating of the power supply is independent of the voltage of SM under test.

In addition, two capacitor voltage control methods for high and low switching frequency mission profiles are proposed to regulate the blocking voltage of power devices. The control parameter selection and hardware component sizing (e.g., IGBT modules, coupling inductor and power supply) of the mission profile emulator are discussed. To differentiate switching profiles, a classification method is given by assessing the time consumed for a certain capacitor voltage change. The impact of extra current ripples on the conduction losses and the absence of voltage ripples on the switching losses are evaluated. The results show that the maximum errors are 0.1% and 1.5%, respectively, which are negligible. The performance of capacitor voltage control is experimentally demonstrated. Two other potential applications of the mission profile emulator (e.g., AC power cycling testing and electro-thermal

model validation) are presented to show the effectiveness and functionalities of the emulator. In summary, the above merits of the proposed mission profile emulator lay a good foundation for the two planed MMC reliability-related Ph.D. research projects in the past three years.

Chapter 3

Power Loss Balancing Control of MMCs

3.1 Background

As the backbone of the power system, high power MMC generally requires high reliability to secure its continuous operation throughout the service life. In order to meet the reliability requirement, much attention is given to the power semiconductors, which are the major component in the MMC and also one of the most fragile components in the system [76]. Due to the modular structure, one commonly used methods is a redundant design [82]. Failed SMs can be replaced by a healthy one immediately after failure occurs. The redundant resign can ensure high availability of the system. In addition, enhancing the reliability through control method is an alternative to relieve the thermal stress of key components. It is able to extend the lifetime of SMs by adjusting and balancing the thermal stress among the different SMs. For example, regulating the junction temperature variation [83] and the mean junction temperature amplitude [84] might extend the lifetime of the power semiconductors.

Instead of the direct junction temperature control [85, 86], regulating the power losses [35] is an alternative method to achieve the same objective as mentioned in [87], where the concept of power routing is proposed. Conduction losses and switching losses are the major loss source involved in this process. Regarding the MMC specifically, the capacitor voltage balancing control provides a conduction loss balance mechanism among SMs. This feature facilitates the thermal control and the cooling system design of the SM. Detailed explanations on how the voltage balancing control contributes to power loss balancing are discussed in this chapter. However, it is not applicable for

the switching loss. Due to the different current that switching actions are subject to, significant switching loss variations can be observed among SMs. Especially when it comes to the application of high blocking voltage power semiconductors in the MMC (e.g., HVDC), the switching loss mismatch deteriorates due to the higher average switching loss per pulse compared to low voltage rated devices. This is also the reason that the switching losses account for a large proportion of the total loss even though the equivalent switching frequency is as low as several hundreds Hertz. In that regard, the power loss balancing control in this project focuses on distributing the switching losses. By integrating a power loss control loop into the capacitor voltage control, a power loss balancing control can be achieved. Simulations based on a 30 MVA three-phase MMC is conducted.

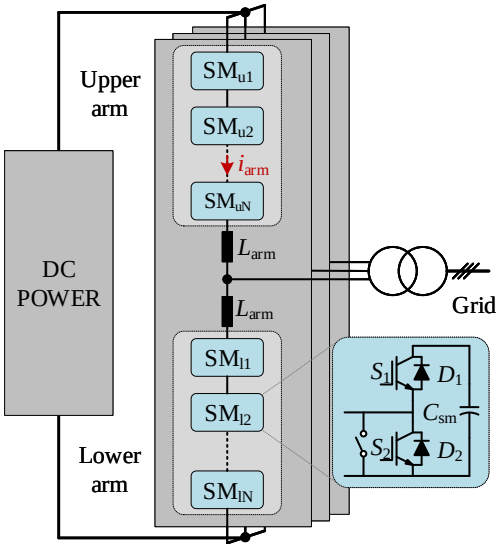

Fig. 3.1: A typical three-phase MMC with half-bridge SM. Source: [C2]

3.2 Balanced Conduction Loss Distribution among SMs in MMCs

3.2.1 Conduction Loss Estimation

The capacitor voltage balancing control provides an internal power loss balance mechanism for power semiconductors in the SM [65], especially in terms of the conduction losses. However, no existing research has validated it analytically. In order to clearly see how this phenomenon occurs, the conduction losses of IGBTs and diodes in one SM are explored in the following.

The average conduction loss of IGBTs and diodes in one fundamental period T can be expressed as

$$\begin{cases} P_{S_2/D_1} = \dfrac{1}{T}\displaystyle\int_0^T \left(V_{\mathrm{S/D}} i_{\mathrm{p}} + R_{\mathrm{S/D}} i_{\mathrm{p}}^2\right) S_i dt \\ P_{S_1/D_2} = \dfrac{1}{T}\displaystyle\int_0^T \left(V_{\mathrm{S/D}} i_{\mathrm{n}} + R_{\mathrm{S/D}} i_{\mathrm{n}}^2\right) (1 - S_i)\, dt \end{cases} \tag{3.1}$$

where $V_{\mathrm{S/D}}$ and $R_{\mathrm{S/D}}$ refer to the on-state zero current voltage and on-state resistance of IGBT and diode, respectively; i_{p} and i_{n} define the positive and negative part of the arm current, respectively; S_i is the gate signal of the i-th SM, which is equal to 1 or 0 and is complementary for the two IGBTs in one SM as shown in Fig. 3.1.

Then the total conduction loss of one SM in one fundamental period can be calculated as

$$\begin{aligned} P_{\mathrm{total}} = &\frac{1}{T}\int_0^T \left(V_{\mathrm{D}} i_{\mathrm{p}} + R_{\mathrm{D}} i_{\mathrm{p}}^2 + V_{\mathrm{S}} i_{\mathrm{n}} + R_{\mathrm{S}} i_{\mathrm{n}}^2\right) dt \\ &+ \frac{1}{T}\int_0^T \left(\Delta V i_{\mathrm{arm}} + \Delta R i_{\mathrm{arm}} \left|i_{\mathrm{arm}}\right|\right) S_i dt \end{aligned} \tag{3.2}$$

where $\Delta V = V_{\mathrm{S}} - V_{\mathrm{D}}$ and $\Delta R = R_{\mathrm{S}} - R_{\mathrm{D}}$.

The SM capacitor voltages are always kept balanced in steady-state operation of MMCs. It means that the voltage changes caused by charging (through (D_1)) and discharging (through S_1) of the capacitors are equal in one fundamental period. Thus, the following relationship holds

$$\begin{cases} \Delta U^+ = \displaystyle\int_0^T \frac{i_{\mathrm{p}}\,(1 - S_i)}{TC_i} dt = \Delta U^- = \int_0^T \frac{i_{\mathrm{n}}\,(1 - S_i)}{TC_i} dt \\ i_{\mathrm{p}} = \dfrac{|i_{\mathrm{arm}}| + i_{\mathrm{arm}}}{2}, i_{\mathrm{n}} = \dfrac{|i_{\mathrm{arm}}| - i_{\mathrm{arm}}}{2} \end{cases} \tag{3.3}$$

where $\Delta U^{+/-}$ are the SM capacitor voltage increase and decrease; C_i is the capacitance of the i-th SM; i_{arm} is the arm current.

Replacing i_{p} and i_{n} by i_{arm}, (3.3) can be simplified as

$$\int_0^T i_{\mathrm{arm}} S_i dt = \int_0^T i_{\mathrm{arm}} dt. \tag{3.4}$$

By substituting (3.4) into (3.2), the average conduction loss of one SM in one fundamental period can be re-expressed as

$$\begin{aligned} P_{\mathrm{total}} = &\underbrace{\frac{1}{T}\int_0^T \left(V_{\mathrm{D}} i_{\mathrm{p}} + R_{\mathrm{D}} i_{\mathrm{p}}^2 + V_{\mathrm{S}} i_{\mathrm{n}} + R_{\mathrm{S}} i_{\mathrm{n}}^2\right) dt}_{P_{\mathrm{com1}}} \\ &+ \underbrace{\frac{1}{T}\int_0^T \left(\Delta V + \Delta R k\right) i_{\mathrm{arm}} dt}_{P_{\mathrm{com2}}} + \underbrace{\frac{1}{T}\int_0^T \Delta R i_{\mathrm{arm}} \left(|i_{\mathrm{arm}}| - k\right) S_i dt}_{\Delta P_i} \end{aligned} \tag{3.5}$$

where P_{com1} and P_{com2} are the common conduction losses, which are same for all SMs and regardless of the gate signals. ΔP_i is the conduction loss related to gate signals of the i-th SM, which means that it is different for different SMs; k is a constant related to the arm current.

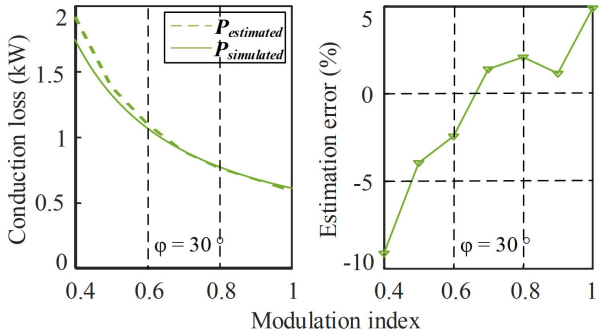

Fig. 3.2: The total conduction loss and the estimation error of an SM at $\varphi = 30^{\circ}$. Source: [C3]

By estimating ΔP_i with $P_{\max}(k)$ in the following equation, the total conduction loss of SMs can be estimated.

$$|\Delta P_i| \leq \left| \frac{\Delta R}{T} \int_0^T |i_{\text{arm}}(|i_{\text{arm}}| - k)| dt \right| = P_{\max}(k), k = \frac{\int_0^T |i_{\text{arm}}|^2 dt}{\int_0^T |i_{\text{arm}}| dt} \tag{3.6}$$

$$P_{\text{total}} = P_{\text{com1}} + P_{\text{com2}} + P_{\max}(k). \tag{3.7}$$

Fig. 3.2, Fig. 3.3, and Fig. 3.4 show the estimated and simulated conduction loss of one SM and the corresponding error. It can be seen that the estimation errors are within 5% for different modulation indexes and power factor angles when the modulation index is larger than 0.5, which can cover the typical operating range of the MMC.

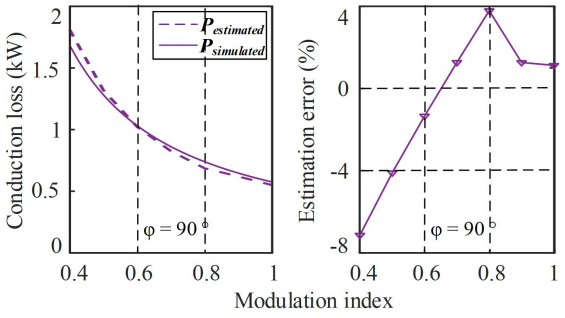

Fig. 3.3: The total conduction loss and estimation error of an SM at $\varphi = 90^{\circ}$. Source: [C3]

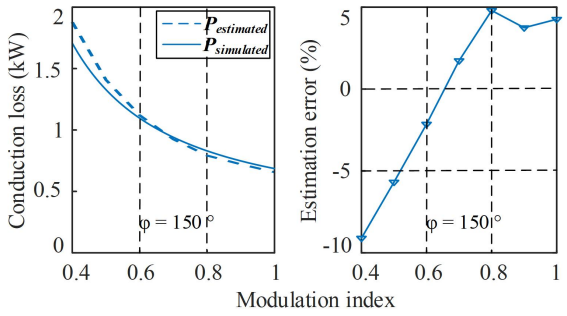

Fig. 3.4: The total conduction loss and the estimation error of an SM at $\varphi = 150^{\circ}$. Source: [C3]

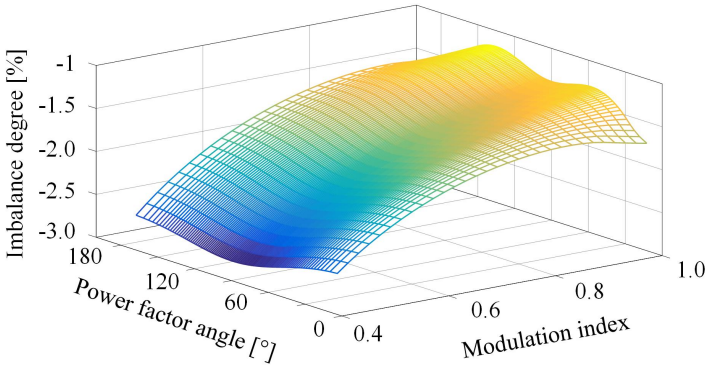

Fig. 3.5: Conduction loss imbalance degree with different operating conditions. Source: [C3]

From (3.7), it can be seen that all SMs share common conduction losses as P_{com1} and P_{com2}. Their differences lies in ΔP_i, which can be used to evaluate the imbalance degree of conduction loss among SMs. Fig. 3.5 presents the imbalance degree of conduction losses among SMs with different operating conditions, which is defined as $\Delta P_i / P_{\text{total}} \times 100\%$. It can be sen that the imbalance degree is less than 4% when the modulation index ranges from 0.4 to 1. The impact of different parameters between IGBT and diode is also evaluated and shown in Fig. 3.6. The conduction loss imbalance degree among SMs is less than 3% in terms of two times value difference between V_{S} and V_{D} as well as R_{S} and R_{D}. So far, the following two conclusions can be drawn from the above analysis:

- P_{total} can be used to estimate the total conduction loss of SMs in the MMC with the information of on-state semiconductor characteristics and the arm current information only.
- Conduction losses among SMs are balanced regardless of the modu-

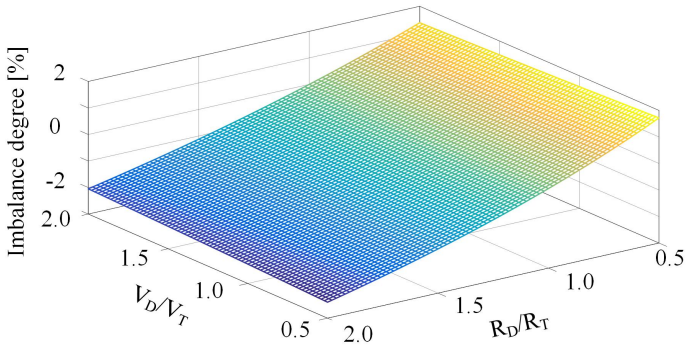

Fig. 3.6: Conduction loss imbalance degree regarding parameter difference between IGBT and diode. Source: [C3]

lation, operation condition, and the capacitor parameter mismatch as long as SM capacitor voltages are well balanced.

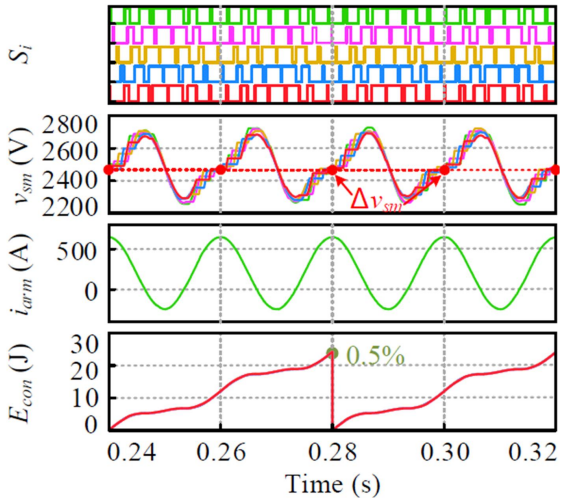

Fig. 3.7: Simulation results of the MMC with PSC: waveforms of gate signals, SM voltages, arm current, and accumulated conduction losses of five SMs. Source: [C3]

3.2.2 Case Study: Three-Phase MMC Based Simulation Validation

In order to validate the above analysis, simulations are carried out based on the power module 5SNA-1200G450350 from ABB. As the balanced power

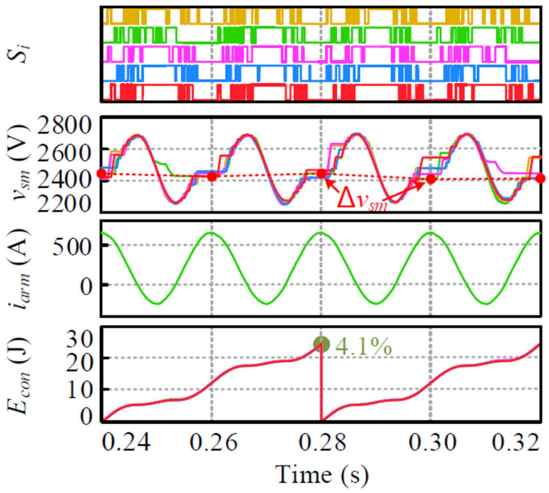

Fig. 3.8: Simulation results of the MMC with LSC: waveforms of gate signals, SM voltages, arm current, and accumulated conduction losses of five SMs. Source: [C3]

loss distribution is independent of the modulation methods, three commonly used modulation methods, namely phase-shifted carrier (PSC) modulation, level-shifted carrier (LSC) modulation and nearest level modulation (NLM) are applied respectively as shown in Fig. 3.7, Fig. 3.8, and Fig. 3.9. It can be seen that all SM capacitor voltages are well balanced at 2500 V but with different voltage variations for different modulation methods. Even though the average conduction losses for SMs are similar being 23.9 J, 24.2 J, and 24.2 J for PSC, LSC and NLM, respectively, the imbalance degree grows from 0.5%, 4.1% to 5.8%. The reason is that the capacitor voltage balancing performance gets worse from PSC to NLM. It can be seen that the SM capacitor voltage increase and decrease are not equal and the difference in one fundamental period are getting larger and larger. This makes the assumption in (3.3) can not be fully met any more. Nevertheless, the small imbalance degree still validate the balanced conduction loss among SMs with a negligible impact from the modulation method and capacitance mismatch.

3.2.3 Case Study: MMC Emulator Based Experimental Validation

Experimental validations are conducted based on the mission profile emulator as shown in Fig. 2.6. One PSC based mission profile and two NLM based mission profiles are applied as the switching profile. By measuring the on-state voltage of the IGBTs and diodes as shown in Fig. 3.10, the accumulated conduction losses of the whole SM are presented in Fig. 3.11.

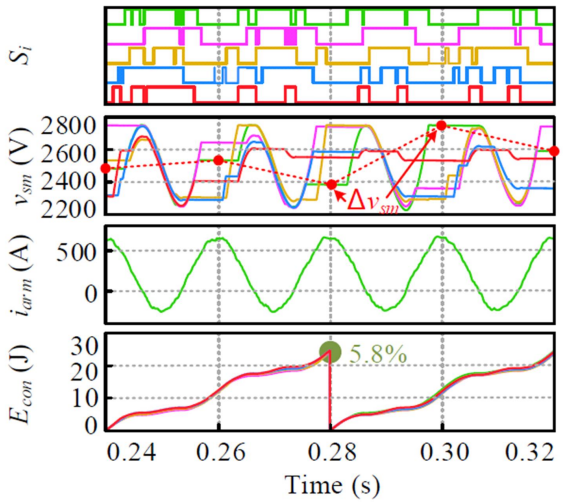

Fig. 3.9: Simulation results of the MMC with NLM: waveforms of gate signals, SM voltages, arm current, and accumulated conduction losses of five SMs. Source: [C3]

The average total conduction loss of one SM from simulations are 0.2332 J, 0.2333 J and 0.2316 J for PSC, NLM1 and NLM2, respectively. The variation is 0.7%. By contrast, the experimentally measured accumulated conduction energy losses are 0.2464 J with the variation as low as 0.3%. It can be seen that the imbalance degree of the conduction losses with different modulations are pretty small and it validates the above conclusion. Moreover, the estimated conduction loss by the proposed method is 0.2296 J. Compared with the simulated and experimental results, the error is 1.4% and 6.8%, respectively.

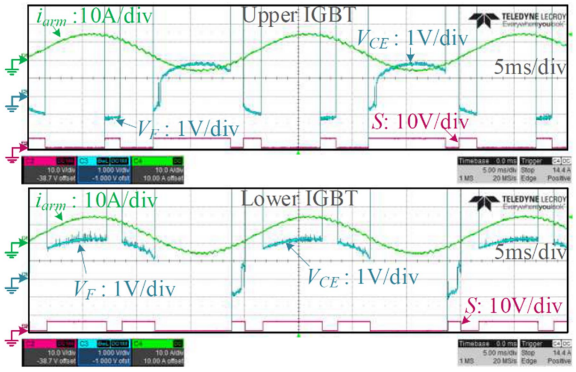

Fig. 3.10: Experimental waveforms of the arm current, the on-state voltage and the gate signal of upper and lower IGBTs in one half-bridge SM. Source: [C3]

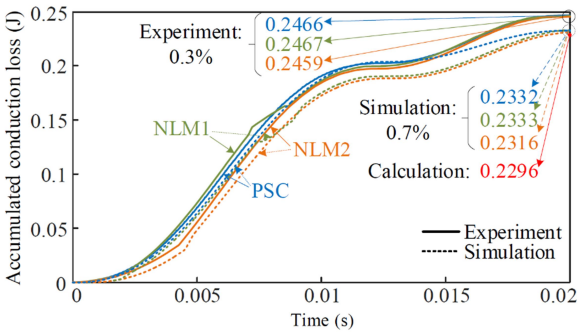

Fig. 3.11: Accumulated simulated and experimental conduction losses of one SM with three different modulation methods. (The percentage numbers express the conduction imbalance degree) Source: [C3]

3.3 Imbalanced Switching Loss Distribution among SMs in MMCs

Different from the conduction losses, the switching losses of the active devices among the SMs have much more differences. The reason comes from two folds, namely the low switching frequency characteristic and also parameter mismatch. Detailed explanations are given in the following.

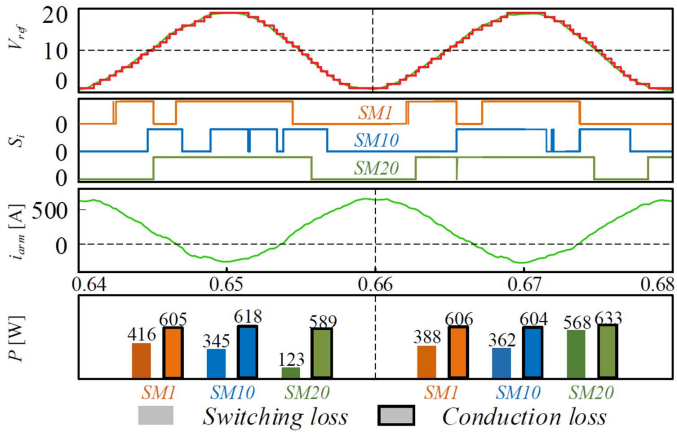

Fig. 3.12: Voltage references for the upper arm, the gate signals for SM_1, SM_{10} and SM_{20}, the arm current, and the power losses including the switching losses and the conduction losses. Source: [C2]

3.3.1 Low Switching Frequency

MMC can operate at very low switching frequency (e.g., as low as several times of the fundamental frequency with the nearest level modulation (NLM)). In this case, different switching transient corresponds to different arm currents and switching losses.

Fig. 3.12 shows the simulated power losses of a three-phase 30 MW MMC with 20 identical SMs per arm. For simplification, only the power loss of three SMs are shown. It can be seen that the average switching losses of the three SMs are 416 W, 345 W and 123 W in one fundamental period, respectively. The difference is as large as 300% (e.g., taking 123 W as the reference). Even regarding the same SM, taking the 20-th SM (SM20) in the arm for example, the switching loss changes from 123 W to 568 W in two consecutive periods. This comes from the low switching frequency, which cannot evenly be distributed in one fundamental period. However. the average conduction loss difference among SMs are below 5% with its value being 600 W all the time. The results indicate that an internal balancing mechanism exists for the conduction loss, but it is not the case for the switching losses.

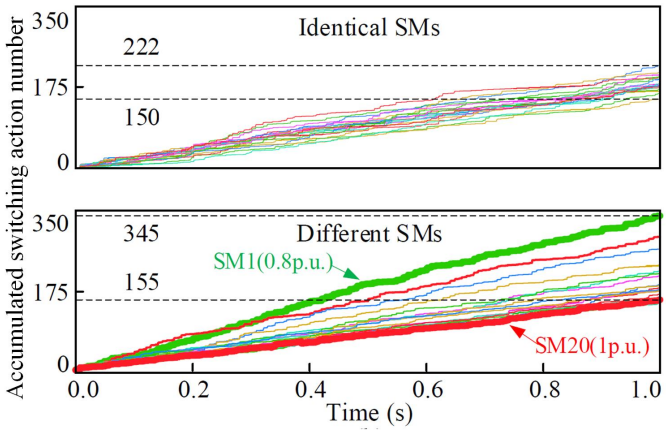

Fig. 3.13: Accumulated switching frequency of 20 SMs with the NLM. (Upper sub-figure: identical SMs, and lower sub-figure: SMs with different capacitances). Source: [C2]

3.3.2 Parameter Mismatch

There are different sources of parameter mismatches in a MMC. For example, the manufacturing tolerance of power semiconductors can contribute to various on-state voltages, which affect the conduction loss of the SM. The different performance of the cooling system can lead to different case temperatures among SMs. It can further result in varied junction temperature of power devices and power losses. Moreover, the SM capacitance tolerance,

in practice, can be as large as 20% of its rated value [64]), plus the impact of degradation, the SM capacitance difference can deteriorate the power loss imbalance in the MMC.

Examples are given in Fig. 3.13, in which two case studies with identical SMs and different SMs (i.e., different SM capacitor value) are presented. Regarding the accumulated switching action number with time, it can be seen that the maximum switching frequency difference of 72 Hz can be achieved by the MMC with identical SMs. For the MMC with different SMs, the switching difference rises to 190 Hz, where the capacitance mismatch ranges from 1.6 mF to 2.0 mF. Therefore, the capacitance mismatch can worsen the switching frequency spread among SMs and further the uneven loss distribution [66].

3.4 Power Loss Balancing Control of MMCs

A capacitor voltage sorting algorithm determines the actual switching action of one SM, thus by modifying the inputs (e.g., the capacitor voltage) of the capacitor voltage sorting algorithm is able to influence the switching loss. The idea of the proposed power loss balancing control (PLBC) is to achieve the objective below: SMs with higher switching loss tend to keep the current switching status from further increasing the loss [C2]. Instead, SMs with lower switching loss take the duty to track the voltage reference for control purpose [C2]. Specifically, the PLBC enhances the probability of changing the gate status of the SM with lower switching loss by adding an adjustment to the real capacitor voltage v_{sm} [C2]. The adjustment is decided by the arm current direction, the previous status of the SM, and the switching loss information [C2]. Detailed control scheme is shown in Fig. 3.14.

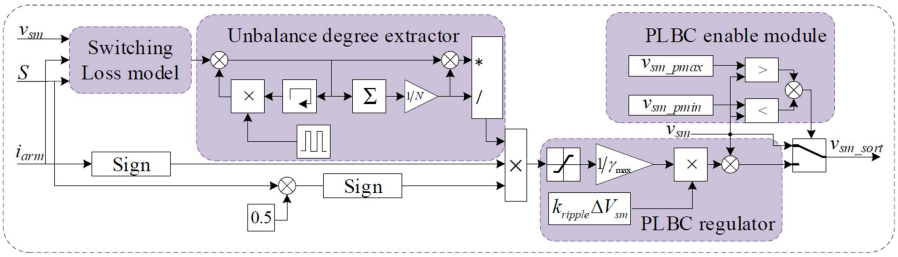

Fig. 3.14: Submodule level power loss balancing control (PLBC) scheme. Source: [C2]

3.4.1 Switching Loss Model

The switching energy of power semiconductors are current, voltage and temperature dependent and their relationships can be found in the data-sheet

provided by the manufacturer. By curve-fitting the data-sheet information through a second-order polynomial, the switching energy can be obtained with certain blocking voltage and junction temperature given as [88]

$$E_{\mathrm{sw}}\left(i_{\mathrm{arm}}, T_{\mathrm{ref}}, V_{\mathrm{ref}}\right) = a_2 i_{\mathrm{arm}}^2 + a_1 \left|i_{\mathrm{arm}}\right| + a_0, \tag{3.8}$$

where a_2, a_1 and a_0 are the curve-fitted coefficients of the data-sheet information, i_{arm} refers to the arm current, and V_{ref}, T_{ref} are the blocking voltage and the junction temperature given in the data-sheet, respectively. The switching loss under practical operating conditions is [89]

$$E_{\mathrm{sw}}\left(i_{\mathrm{arm}}, T_{\mathrm{j}}, V_{\mathrm{sm}}\right) = \frac{V_{\mathrm{sm}}}{V_{\mathrm{ref}}} E_{\mathrm{sw}}\left(i_{\mathrm{arm}}, T_{\mathrm{ref}}, V_{\mathrm{ref}}\right)\left[1 + K_{\mathrm{T}}\left(T_{\mathrm{j}} - T_{\mathrm{ref}}\right)\right], \tag{3.9}$$

where V_{sm} refers to the average SM capacitor voltage, T_{j} is the junction temperature, and K_{T} is the curve-fitted temperature coefficient.

3.4.2 Imbalance Degree Extractor

Rather than the real power loss difference, the power loss imbalance degree among SMs is the focus of the proposed power loss balancing control. Thus, an imbalance degree extractor is implemented to achieve the objective. It is defined as the maximum power loss difference divided by the average power loss among SMs. To simplify the analysis, the following relationship is assumed: $E_{1\_\Sigma\mathrm{sw}} > E_{2\_\Sigma\mathrm{sw}} = E_{3\_\Sigma\mathrm{sw}} = ... = E_{\mathrm{N}\_\Sigma\mathrm{sw}}$. The average accumulated switching energy and the imbalance degree γ are

$$E_{\Sigma\mathrm{sw\_avg}} = \frac{E_{1\_\Sigma\mathrm{sw}} + (N-1)\, E_{2\_\Sigma\mathrm{sw}}}{N} \tag{3.10}$$

$$\gamma = \frac{\max\left(E_{\mathrm{i}\_\Sigma\mathrm{sw}}\right) - \min\left(E_{\mathrm{i}\_\Sigma\mathrm{sw}}\right)}{\min\left(E_{\mathrm{i}\_\Sigma\mathrm{sw}}\right)} = \frac{E_{1\_\Sigma\mathrm{sw}} - E_{2\_\Sigma\mathrm{sw}}}{E_{2\_\Sigma\mathrm{sw}}} \tag{3.11}$$

The output y_1 of the imbalance degree extractor for SM_1 can be derived as (3.12). In terms of practical cases where the SM number is normally large [90], the output can be simplified into γ, which is in general around 1.

$$y_1 = \frac{\Delta E_{1\_\Sigma\mathrm{sw}}}{E_{\Sigma\mathrm{sw\_avg}}} = \frac{E_{1\_\Sigma\mathrm{sw}} - E_{\Sigma\mathrm{sw\_avg}}}{E_{\Sigma\mathrm{sw\_avg}}} = \frac{(N-1)\,\gamma}{\gamma + N} \approx \gamma \tag{3.12}$$

It can be seen that the output of the imbalance degree extractor is γ, which can be used to evaluate the power loss imbalance among SMs and used for power loss balancing control.

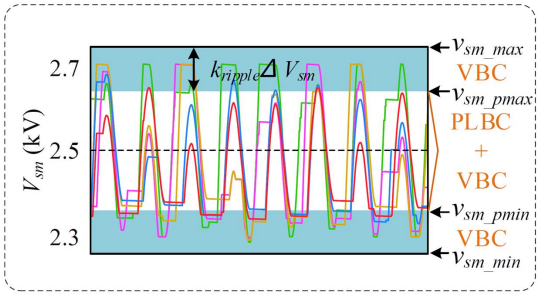

Fig. 3.15: Operating principle of the PLBC enable module (shown in Fig. 3.14). Source: [C2]

3.4.3 PLBC Regulator and Enable Module

The PLBC regulator aims to achieve two tasks. One is to adjust the threshold of the saturation function and the sensitivity of the PLBC to the imbalance degree changes according to different ($\pm\gamma_{\max}$). The other is to weight the power loss balancing control and the capacitor voltage balancing control (VBC) through changing k_{ripple}, which determines the maximum output of the PLBC regulator. Note that capacitor voltage control has the top priority compared with the power loss balancing control, which aims to optimize the operation of the MMC. Therefore, the output of PLBC should not be as aggressive as the capacitor voltage control. Otherwise, the divergence of the actual capacitor voltage and worse overall switching loss performance might be caused.

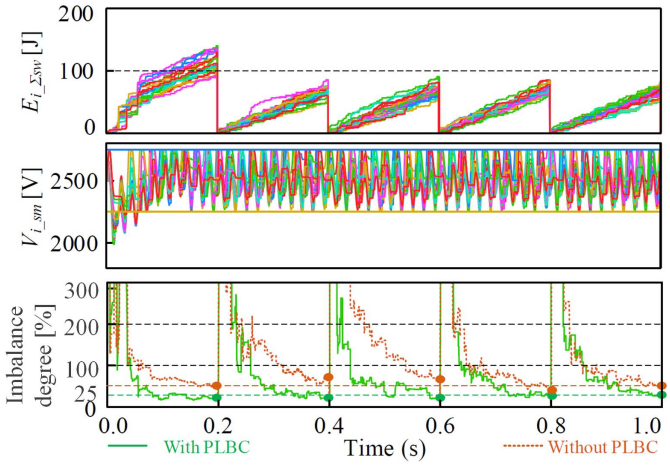

Fig. 3.16: Simulation results under pure active power transfer in a 20 SMs per arm MMC (50 kV/30 MVA): accumulated switching energy without PLBC, SM voltage, and the imbalance degree. Source: [C2]

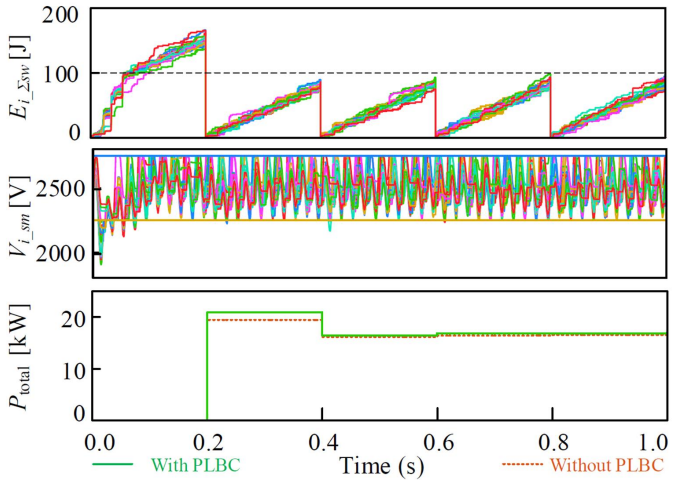

Fig. 3.17: Simulation results under pure active power transfer in a 20 SMs per arm MMC (50 kV/30 MVA): accumulated switching energy with PLBC, SM voltage, and total power loss. Source: [C2]

As for the PLBC enable module, it is set to leave a certain control margin for the voltage balancing control (VBC). When the SM capacitor voltage exceeds the thresholds, the power loss balancing control is disabled with the capacitor voltage balancing control functioning only.

Table 3.1: Simulation parameters of the three-phase MMC.

Power rating	30 MVA	DC link voltage	50 kV
SM number per arm N	20	Arm inductance	13 mH
SM capacitance	2 mF	Modulation index	0.8

3.4.4 Simulation Validation

The effectiveness of the proposed power loss balancing control is verified based on a 50 kV/30 MVA three-phase MMC with 20 SMs per arm as shown in Table 3.1. The simulation results are shown in Fig. 3.16 to Fig. 3.19. Under the unity power factor condition, the switching energy spreads among SMs and it can be observed in Fig. 3.16 and Fig. 3.17. Without implementing the power loss balancing control, the imbalance degree remains higher than 50%. By applying the PLBC, it drops to 25%. Meanwhile, the value of capacitor voltage ripple remains the same as 10 % of the rated voltage, which is guaranteed by the PLBC enable module.

In contrast, when a pure reactive power is transferred by the MMC, the

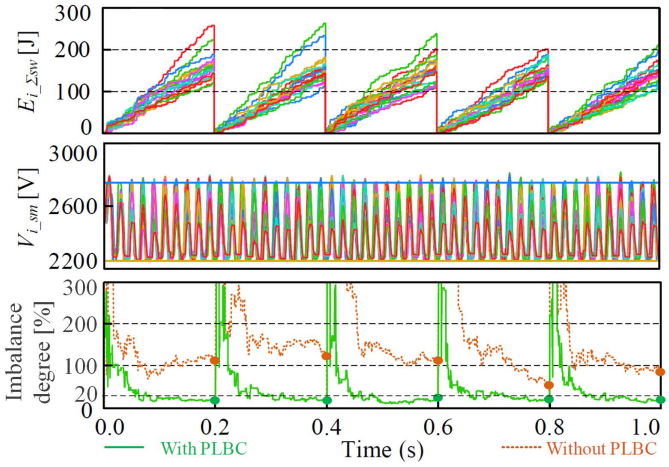

Fig. 3.18: Simulation results under pure reactive power transfer in a 20 SMs per arm MMC (50 kV/30 MVA): accumulated switching energy without PLBC, SM votlage, and the imbalance degree. Source: [C2]

power loss imbalance among SMs becomes more severe than the pure active power case as illustrated in Fig. 3.18. The maximum imbalance degree is higher than 100 %, which means that certain SM dissipates more than two times the switching loss of the other SMs. By applying the PLBC, the imbalance degree is reduced to under 20 % as it is shown in Fig. 3.19. The reduced power loss imbalance can balance the thermal stress among SMs and avoid hot spots and weakest links in the MMC. Moreover, it can also improve the cooling system design.

3.5 Summary

This chapter studies the power loss distribution among SMs in the MMC. An internal conduction loss balancing mechanism formed by the SM capacitor voltage balancing is explored. It is independent of the switching gate signals, operation condition, the modulation techniques and the parameter mismatch of the MMC as long as the capacitor voltages are balanced. The switching loss imbalance among SMs are discussed as well. Two major reasons are the low switching frequency operation and the parameter mismatch. Based on this phenomenon, an active power loss balancing control is proposed by estimating the switching losses and the imbalance degree among SMs. Simulation results show that the imbalance degree among SMs can be reduced to below 25% for unity power factor conditions and 20% for zero power factor conditions.

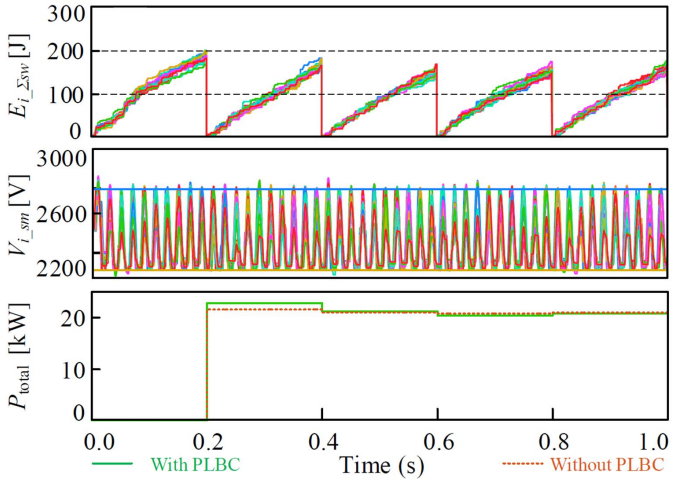

Fig. 3.19: Simulation results under pure reactive power transfer in a 20 SMs per arm MMC (50 kV/30 MVA): accumulated switching energy with PLBC, SM voltage, and total power loss. Source: [C2]

Chapter 4

Adaptive Carrier Frequency Control of MMCs

4.1 Background

When the modular multilevel converter (MMC) is employed as a grid-side converter, stringent grid code regarding the output current and voltage harmonics has to be met during its operation. However, the output current and voltage THD are loading-dependent, namely the lighter the loading is, the higher the output current THD is supposed to be, given the same modulation strategy and output filter. In order to ensure the output THD within a specific limit, a relatively high equivalent switching frequency has to be applied to the converter for a wide range of power loading conditions with fixed switching frequency. However, for MMCs where high voltage rated power semiconductors are applied, the high switching frequency can generate large amount of switching loss in heavy loading conditions due to the high average switching energy per pulse for high voltage power devices.

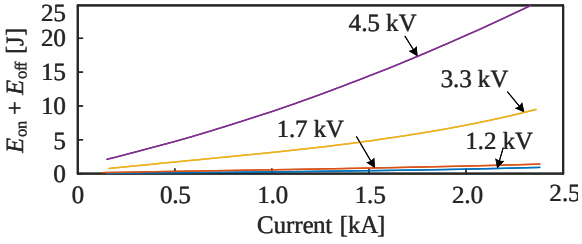

Fig. 4.1: Switching energy loss for different voltage rating power devices from Infineon (4.5 kV: FZ1200R45KL3-B5, 3.3 kV: FZ1200R33HE3, 1.7 kV: FZ1200R17HP4-B2, 1.2 kV: FZ1200R12HE4).

Fig. 4.1 shows the switching energy losses per pulse for devices with different voltage rating and for the same current rating. A significant switching loss increase can be observed for 4.5 kV devices compared with 1.2 kV devices. Thus, MMCs with high voltage rating power devices are in general rather sensitive to the switching frequency. It is also the reason why the switching loss still accounts for a large proportion of the total power loss of MMCs even though the switching frequency is as low as several hundreds Hertz [91] [64]. Therefore, optimization of the switching frequency is beneficial to reducing the power loss and thermal stress of power devices in the MMC, and further enhancing the reliability of the whole system. As a matter of fact, the conduction losses, as mentioned in the previous chapter, is mainly dominated by the loading conditions and is independent of the modulation techniques for the MMCs [92]. There is a little room for the power loss and thermal stress reduction regarding the conduction losses. Thus, more attention is paid to the switching loss reduction in this chapter for reliability improvement of the MMCs, especially for medium power and voltage applications where the SM number per arm is relatively low. In this case, the phase-shifted carrier modulation strategy is typically applied with a high switching frequency, which can be optimized accordingly.

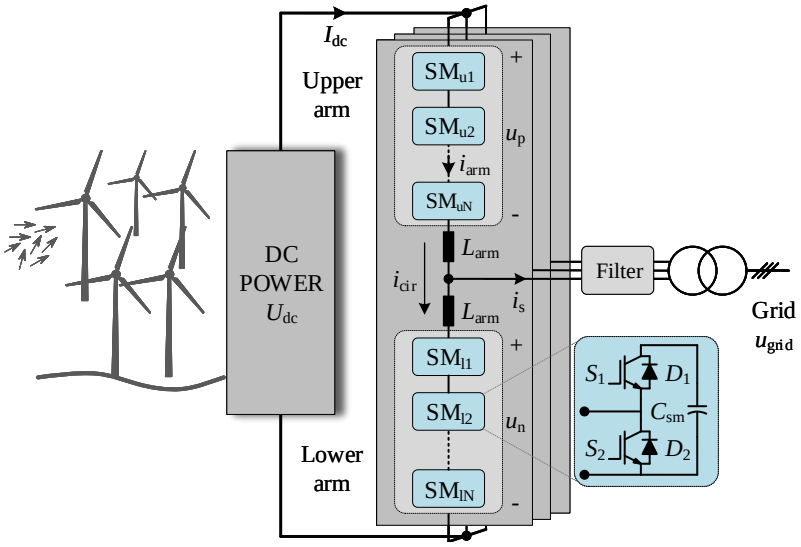

Fig. 4.2: A typical three-phase MMC converter connected to grid.

In order to achieve the aforementioned objectives, the switching frequency boundary has to be specified with respect to particular requirements, such as output current THD and the SM capacitor voltage ripple. Simplified MMC models are thus required in this process and the three-phase MMC circuit is

shown in Fig. 4.2.

4.2 Impact of Carrier Frequency on Harmonics and Capacitor Voltage Ripple

4.2.1 Output Current Harmonics

The three-phase MMC can be simplified as shown in Fig. 4.3. The output currents are driven by the output voltage of the MMC and the grid voltage. Therefore, the impact of the carrier frequency on the harmonics of the output current can be evaluated by conducting the Double Fourier Series analysis to the output voltage of the MMC as below.

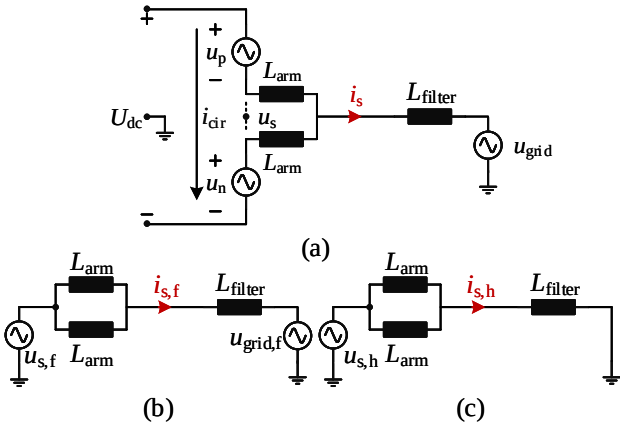

Fig. 4.3: Simplified MMC model. (a) One-phase MMC model; (b) Circuit model for the fundamental component of the output current; (c) Circuit model for the harmonic component of the output current with an ideal grid condition. (i_{cir} is the circulating current, L_{arm} is the arm inductance, L_{filter} is the filter inductance, and $u_{s,f/h}$, $i_{s,f/h}$, and $u_{grid,f/h}$ are the fundamental or harmonic components of the converter output voltage and current, and the grid.) Source: [C4]

$$
\begin{cases}
u_s = \dfrac{1}{2}\left(u_n - u_p\right) = H(u_s)_f \cdot \cos\left(\omega_1 t\right) + H(u_s)_{a,b} \\
\qquad \times \cos\left(\left(Na\omega_c + b\omega_1\right)t + \dfrac{Na\theta + b\pi - \pi}{2}\right) \\
H(u_s)_f = \dfrac{mU_{dc}}{2} \\
H(u_s)_{a,b} = \dfrac{2U_{dc}}{a\pi N} \sin\left[\dfrac{(Na+b)\,\pi}{2}\right] \\
\qquad \times J_b\left(\dfrac{mNa\pi}{2}\right) \cos\left(\dfrac{Na\theta + b\pi - \pi}{2}\right)
\end{cases}
\tag{4.1}
$$

where u_{s} is the converter output voltage; u_{p} and $u_{\mathrm{n}}$are the upper and lower arm voltage, respectively; $H(u_{\mathrm{s}})_{\mathrm{f}}$ is the amplitude of the fundamental component; $H(u_{\mathrm{s}})_{a,b}$ is the amplitude of the harmonic components with the order identified by a and b; U_{dc} is the DC link voltage; N is the SM number per arm; J_b is the Bessel function of the first kind; ω_c is the angular frequency of the triangle carrier; θ is the angular displacement between the carriers of the upper arm and lower arm; m is the modulation index.

The amplitude of the fundamental output current can be calculated according to the power delivered by the MMC as

$$H(i_{\mathrm{s}})_{\mathrm{f}} = \frac{2S}{3H(u_{\mathrm{s}})_{\mathrm{f}}}. \tag{4.2}$$

where S is the apparent power and $H(i_{\mathrm{s}})_f$ is the amplitude of the fundamental component of the output current.

The harmonics in the output current, as shown in Fig. 4.3 (c), are driven by the corresponding harmonics of u_{s} if an ideal grid condition is assumed. Its amplitude is

$$H(i_{\mathrm{s}})_{a,b} = \frac{H(u_{\mathrm{s}})_{a,b}}{\omega_{a,b}\left(L_{\mathrm{arm}}/2+L_{\mathrm{filter}}\right)}, \tag{4.3}$$

where $H(i_{\mathrm{s}})_{a,b}$ is the amplitude of harmonic components in the output current with the order identified by a and b.

Based on (4.2) and (4.3), the Total Harmonic Distortion (THD) of the output current is

$$THD\left(i_{\mathrm{s}}\right) = \frac{\sqrt{\sum_{a=1}^{\infty}\sum_{b=-\infty}^{\infty} H\left(i_{\mathrm{s}}\right)_{a,b}^{2}}}{H(i_{\mathrm{s}})_{\mathrm{f}}}. \tag{4.4}$$

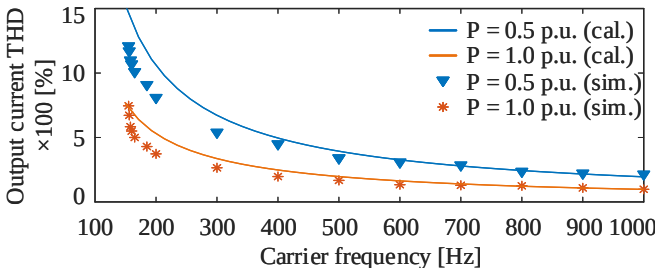

Fig. 4.4: The simulated and calculated relationship between the carrier frequency and the output current THD at different power loading conditions. Source: [C4]

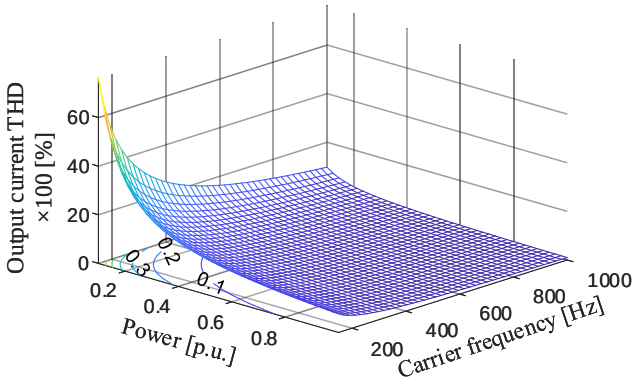

Fig. 4.5: The calculated relationship between the output current THD, carrier frequency, and power loading with unity power factor.

It can be seen from Fig. 4.4 that the analytical model for output current THD evaluation agrees well the simulation results based on the system parameters listed in Table 4.1, especially when the applied carrier frequency is high. With the increase of the carrier frequency and the power loading, the output current THD gets smaller. The calculated relationship of the three parameters are shown in Fig. 4.5. Based on the figure, the contour line with a constant THD can be readily obtained showing the relationship between the power loading and the carrier frequency.

Table 4.1: Main system parameters for the case study.

Power rating P	15 MVA	Dc link voltage U_{dc}	20 kV
SM number per arm N	8	Arm inductance L_{arm}	4.1 mH
SM voltage U_{sm}	2.5 kV	SM capacitance C_{sm}	3.0 mF
Modulation index m	0.9	Case temperature T_{c}	40 °C

4.2.2 Capacitor Voltage Ripple

The capacitor average voltage is decided by the DC bus voltage and SM number per arm. However, the capacitor voltage ripple changes with respect to different power loading conditions and carrier frequencies. Omitting the harmonics in the arm current, their impact can be evaluated by the detailed

expression of the SM capacitor voltage as

$$\begin{cases} u_{\mathrm{cap,p},i} = U_{\mathrm{sm}} + \dfrac{1}{C_{\mathrm{sm}}} \displaystyle\int \left[\left(\begin{array}{l} \frac{1}{2} - \frac{m}{2} \cos\left(\omega_1 t\right) + \\ K_{a,b} \cos\left(\omega_{a,b} t + \alpha_{\mathrm{p},a,b}\right) \end{array} \right) \left(i_{\mathrm{cir}} + \frac{1}{2} i_{\mathrm{s}} \right) \right] \\ K_{a,b} = \displaystyle\sum_{a=1}^{\infty} \sum_{b=-\infty}^{\infty} \frac{2}{a\pi} \sin\left[\frac{(a+b)\,\pi}{2} \right] \times J_b\left(\frac{ma\pi}{2} \right) \\ \omega_{a,b} = a\omega_{\mathrm{c}} + b\omega_1 \\ \alpha_{\mathrm{p},a,b} = a\theta + a\,(i-1)\,\dfrac{2\pi}{N} + b\pi \end{cases} \tag{4.5}$$

where $u_{\mathrm{cap,p},i}$ is the capacitor voltage of the i-th SM in the upper arm; U_{sm} is the average SM capacitor voltage; C_{sm} is the SM capacitance.

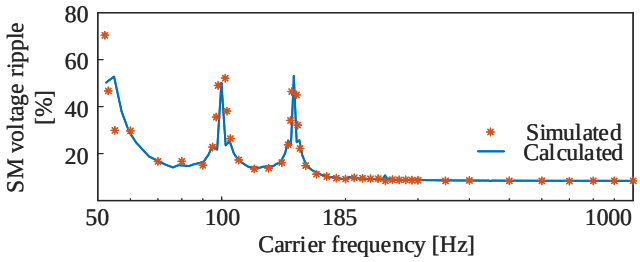

Fig. 4.6: Simulated and calculated SM voltage ripple (derived from 4.7) with different carrier frequencies. Source: [C4]

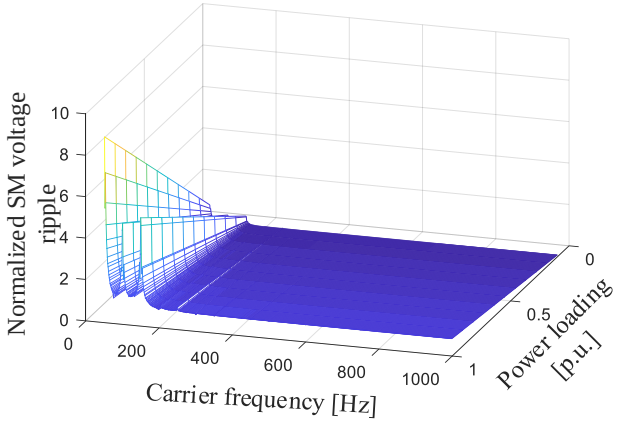

Fig. 4.7: The calculated relationship between the capacitor voltage ripple, carrier frequency, and power loading with unity power factor.

Fig. 4.6 shows the simulated and the calculated capacitor voltage ripples

with different carrier frequencies, and they are in good agreement with each other. Moreover, voltage divergence can be observed when the carrier frequency is the integer times of the fundamental frequency (i.e., 50 Hz, 100 Hz and 150 Hz) and should be avoided in practical applications. Meanwhile, carrier frequencies lower than 185 Hz can contribute to higher capacitor voltage ripple and carrier frequencies higher than 185 Hz have limited impact on the voltage ripple. The relationship among the normalized SM voltage ripple, carrier frequency, and the power loading is shown in Fig. 4.7.

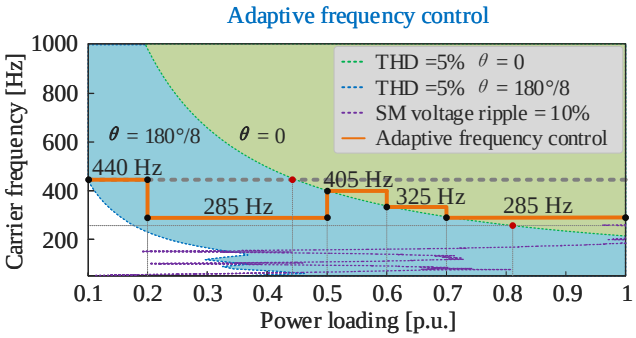

Fig. 4.8: Carrier frequency selection strategy according to the power loading, output current THD, and capacitor voltage ripple. Source: [C4]

4.3 Adaptive Carrier Frequency Control and Reliability Evaluation

4.3.1 Adaptive Carrier Frequency Control

Based on the above analysis, the carrier frequency boundary regarding a particular output current THD and capacitor voltage ripple requirement (e.g., THD of the output current is less than 5%, and the voltage ripple is less than 10% of the average voltage) can be obtained as shown in Fig. 4.8. The dotted blue and green lines refer to the minimum carrier frequency ensuring the output current THD within 5% with and without shift between the upper and lower carriers, respectively. Note that the phase shift between upper and lower carriers can greatly improve the THD performance of the output current with the doubled equivalent switching frequency of the converter [10]. The purple line corresponds to the carrier frequency for 10% SM capacitor voltage ripple. The solid orange line is the optimized carrier frequency according to different loading conditions. It can be seen that higher frequency is needed for a lower loading condition. By contrast, conventional modulation is using a fixed carrier frequency, which is 440 Hz in this case study, in

order to meet the requirements mentioned above. The fixed carrier frequency is indicated by the gray dotted line.

Ideally, the carrier frequency can be optimized and chosen continuously according to the power loading change. However, discrete carrier frequencies determined by predefined power loading intervals is more practical in terms of the implementation of the control. Therefore, the power loading range is divided into ten intervals in accordance with a 10% power loading change and a particular carrier frequency will be allocated to each power interval. More specifically, in order to meet the capacitor voltage ripple requirement, the main integer carrier frequencies (e.g., 100 Hz, 150 Hz, 200 Hz, and 250 Hz), which can cause a high SM voltage divergence, must be avoided, and the carrier frequency is set to be higher than 250 Hz with a sufficient margin. Thus, the minimum carrier frequency of 285 Hz corresponding to $P_{\text{load}} = 0.7$ p.u. and $\theta = 0$ is chosen for the power loading range of 0.7 - 1.0 p.u.. 325 Hz and 405 Hz are used in the loading range of 0.6 - 0.7 p.u. and 0.5 - 0.6 p.u. respectively with $\theta = 0$ as well. When the power loading goes down further, a phase shift angle ($\theta = \pi/N$ regarding even SM number per arm) between the upper arm carrier and lower arm carrier has to apply to prevent the output current THD from being higher than 5%. Meanwhile, the output current THD is greatly reduced and a lower carrier frequency can be expected under this condition. A low frequency 285 Hz same as the one used in the power range 0.7 - 1.0 p.u. is applied for the power interval 0.2 - 0.5 p.u., and 440 Hz for the power loading lower than 0.2 p.u..

4.3.2 Power Loss and Thermal Stress Evaluation

In order to see how the proposed adaptive carrier frequency can improve the reliability of the MMC, a series of evaluations are conducted based on the flow chart in Fig. 4.9, including the power loss modeling and the thermal stress estimation, mission profile modeling, and the reliability evaluation.

- **Power Loss Estimation**

In order to estimate the power loss with different carrier frequencies, a full-scale MMC based simulation model instead of an analytical method is applied in order to better taking the impact of switching actions into account. By conducting discrete simulations with different power loading conditions, the power losses and thermal stresses of major components are obtained in order to build a curve-fitted model. There are three major components dissipating power in the MMC system, namely power semiconductors, SM capacitors and arm inductors. The conduction loss and switching loss of power devices can be obtained from the data-sheet and be applied in PLECS easily. As for the capacitor and inductor, their power losses can be calculated by the

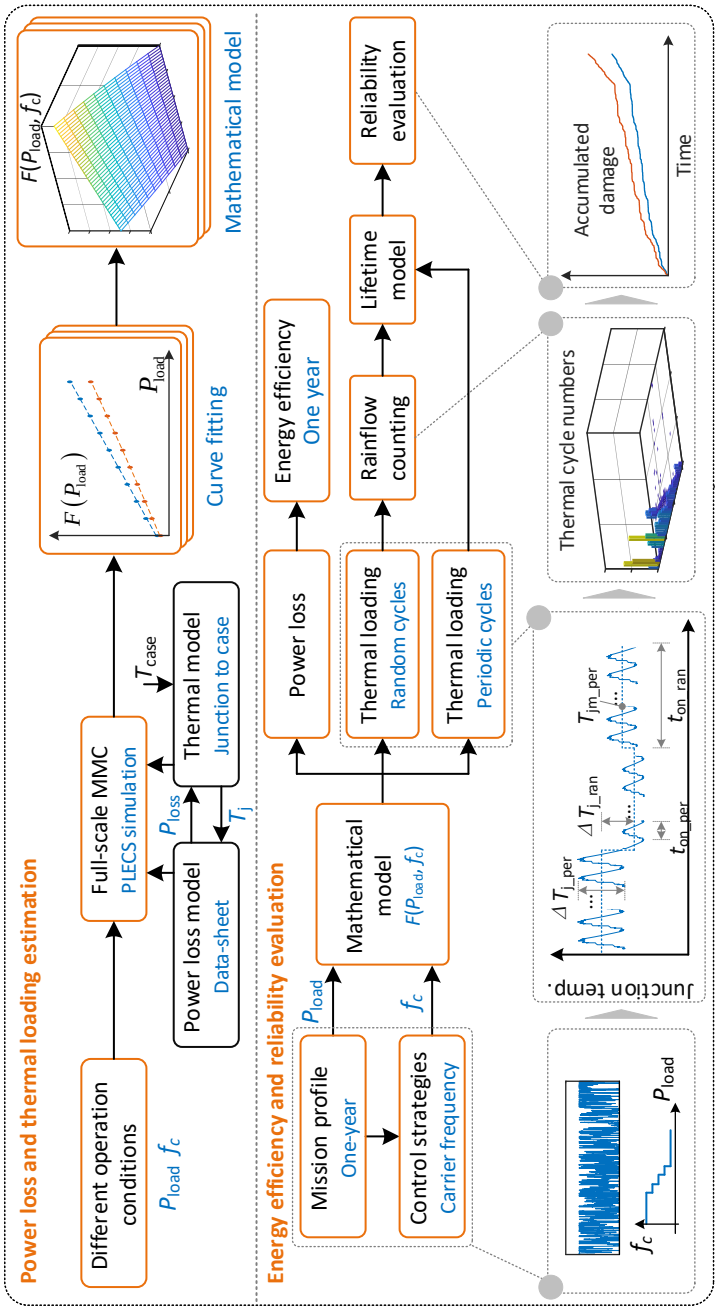

Fig. 4.9: Flow chart of mission profile based reliability evaluation of power modules in the MMC system.

following equations as

$$\begin{cases} R_{\text{ESR\_cap}}(n) = R_{\text{s}} + \dfrac{\tan\delta_0}{2\pi n f_1 C_N} \\ P_{\text{loss\_cap}} = \sum I^2_{\text{cap,rms}}(n) R_{\text{ESR\_cap}}(n) \end{cases} \tag{4.6}$$

where $R_{\text{ESR\_cap}}$ and $I_{\text{cap,rms}}$ are the ESR and rms current of one capacitor at the n-th harmonic; $P_{\text{loss\_cap}}$ is the power loss of one capacitor; C_{N} is the rated capacitance; R_{s} and $\tan\delta_0$ are series resistance and dielectric dissipation factor, respectively; f_1 is fundamental frequency, which is 50 Hz in this case study.

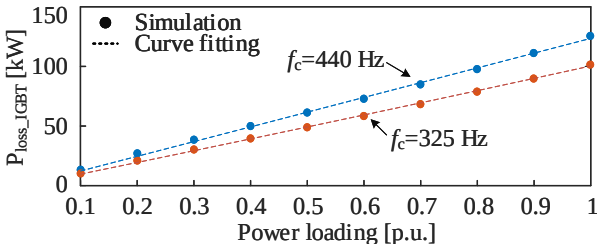

Fig. 4.10: The simulated and curve fitted power losses of all power semiconductors in the MMC under different power loading conditions. Source: [C4]

Arm inductors in the MMC are typically dry-type air-core reactors . Due to the absence of iron core, only the winding ac resistance loss caused by the skin and proximity effect needs to be considered [93]. The power loss of arm inductor is [94]

$$P_{\text{loss\_Larm}} = R_{\text{wdc}} \left(I^2_{\text{arm,dc}} + \sum F_{\text{R}}(n) I^2_{\text{arm,rms}}(n) \right) \tag{4.7}$$

where $P_{\text{loss\_Larm}}$ is the power loss of one arm inductor; R_{wdc} is the dc resistance of the inductor winding; $I_{\text{arm,dc}}$ is the dc component of the arm current; $I_{\text{arm,rms}}(n)$ is the rms value of the arm current at the n-th harmonic; $F_{\text{R}}(n)$ is the ac-to-dc winding resistance ratio. Expressions for R_{wdc} and F_{R} can be referred like given in [94].

Fig. 4.10 and Fig. 4.11 show the total power losses of all power semiconductors (i.e., IGBT and diode) in the MMC under different power loading conditions and carrier frequencies. Their relationship can be curve fitted either by first-order or the second-order polynomials as

$$\begin{cases} F\left(P_{\text{load}}\right) = a_1 P^2_{\text{load}} + a_2 P_{\text{load}} + a_3 \\ F\left(f_{\text{c}}\right) = a_4 f_{\text{c}} + a_5, \end{cases} \tag{4.8}$$

where F refers to the power loss; P_{load} is the power loading, which is normalized with a range of [0-1]; f_{c} is the carrier frequency; a_i $(i = 1...5)$ are constants obtained by curve fitting.

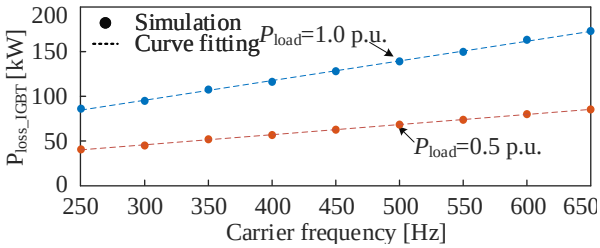

Fig. 4.11: The simulated and curve fitted power losses of all power semiconductors in the MMC under different carrier frequencies. Source: [C4]

- **Thermal Stress Estimation**

Similarly, the thermal stress of the power devices can be evaluated as well through simulations by integrating in the simulations the thermal model provided by the manufacturer of the devices. In Fig. 4.12 and Fig. 4.13, the mean junction temperature and the junction temperature variation amplitude with different power loadings and carrier frequencies can be observed and curve fitted according to (4.8). It can be clearly seen that the uneven thermal stress distribution among the four power devices exists for a typical half-bridge SM. S_2 is most stressed in terms of both temperature variations and mean junction temperature in this case.

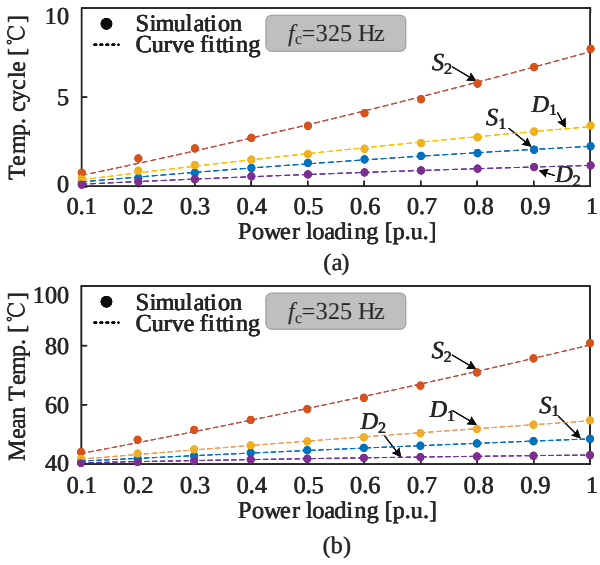

Fig. 4.12: The simulated and curve fitted junction temperature of the power semiconductors under different power loading conditions. (a) Junction temperature cycle amplitude and (b) Mean junction temperature.

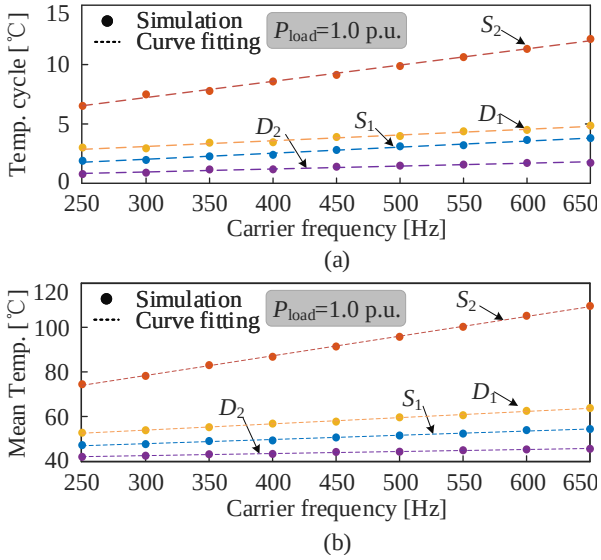

Fig. 4.13: The simulated and curve fitted junction temperature of the power semiconductors under different carrier frequencies. (a) Junction temperature cycle amplitude and (b) Mean junction temperature.

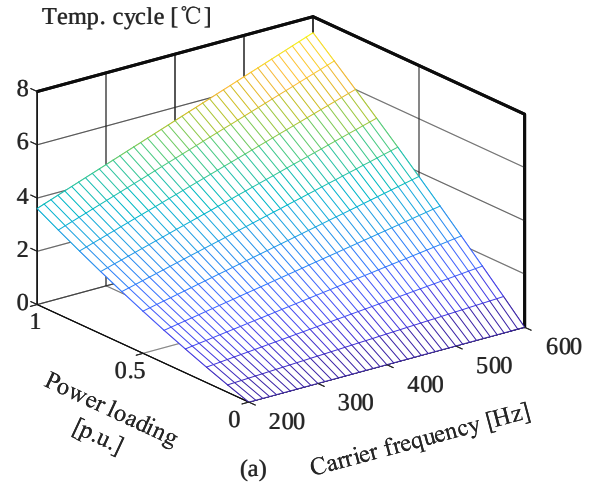

Fig. 4.14: Relationship between the junction temperature cycle amplitude, carrier frequency, and the power loading.

- **Mission Profile Modeling**

Since $F(x)$ shows a proportional relationship with the carrier frequency, a mathematical model describing the relationship between $F(x)$, the power loading, and the carrier frequency is

$$F\left(P_{\text{load}}, f_{\text{c}}\right) = \frac{F(P_{\text{load}})_{@440\text{Hz}} - F(P_{\text{load}})_{@325\text{Hz}}}{440 - 325} \times (f_{\text{c}} - 325) + F(P_{\text{load}})_{@325\text{Hz}}, \tag{4.9}$$

where $F(P_{\text{load}})_{@325\text{Hz}}$ and $F(P_{\text{load}})_{@440\text{Hz}}$ are the curve-fitted polynomial under the carrier frequency of 325 Hz (1.0 p.u.) and 440 Hz (0.5 p.u.), respectively. Fig. 4.14 shows the relationship among the junction temperature cycle amplitude ΔT, the power loading P_{load}, and the carrier frequency f_{c}. Similar results can be obtained for the mean junction temperature T_{m} and the system power loss P_{loss}. They can be further used in the mission profile based efficiency and reliability evaluation.

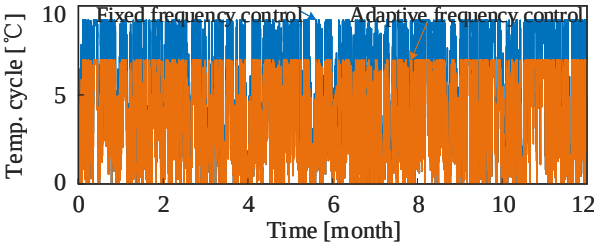

Fig. 4.15: Junction temperature variation comparison between the proposed adaptive control and the conventional control. Source: [C4]

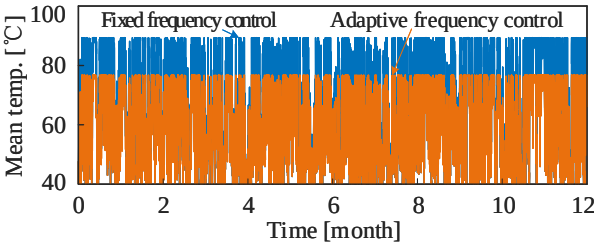

Fig. 4.16: Mean junction temperature comparison between the proposed adaptive control and the conventional control. Source: [C4]

With the help of the mathematical model, a one-year power loading mission profile can be modeled into the junction temperature and power loss mission profiles as shown in Fig. 4.15 to Fig. 4.17. Temperature drops of 2.3 °C and 12.4 °C can be observed for the proposed method regarding the

junction temperature cycle and the mean junction temperature, respectively. Meanwhile, the accumulated power loss reduction throughout the year can be as large as 21% when the carrier frequency can be changed dynamically as illustrated in Fig. 4.18. The reason for large power loss reduction comes from the high average switching energy of the high blocking voltage power semiconductors. The switching frequency decrease can contribute to a lower power dissipation and still be in the specifications of the MMC converter.

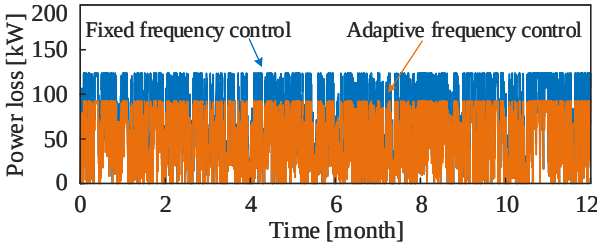

Fig. 4.17: Power loss comparison between the proposed method and the conventional control method. Source: [C4]

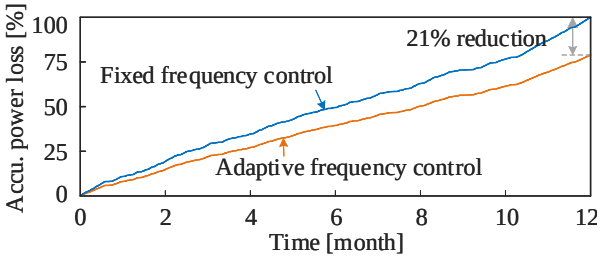

Fig. 4.18: Annual accumulated power loss comparison between the proposed adaptive control and the conventional control. Source: [C4]

4.3.3 Reliability Evaluation

Once the thermal loadings are obtained, the reliability of the power semiconductors can be evaluated for the proposed method and conventional control method. By applying the rain-flow counting [95, 96], the instantaneous junction temperatures can be analyzed in terms of thermal cycles. The Miner's rule [97] and empirical lifetime model developed from testings can be employed to estimate the annual lifetime consumption of the two methods.

$$D = \sum_{i=1}^{k} \frac{n_i}{N_{fi}}, \tag{4.10}$$

where D is the damage caused by cycles at different stress levels; k refers to the stress levels included in the thermal stress profile. n_i is the number of cycles for a particular stress condition (e.g., ΔT_j and T_jm); N_{fi} is the number of cycles to failure at the i-th stress. Note that the impact of different thermal stresses on the damage is assumed to be independent of the time it happens.

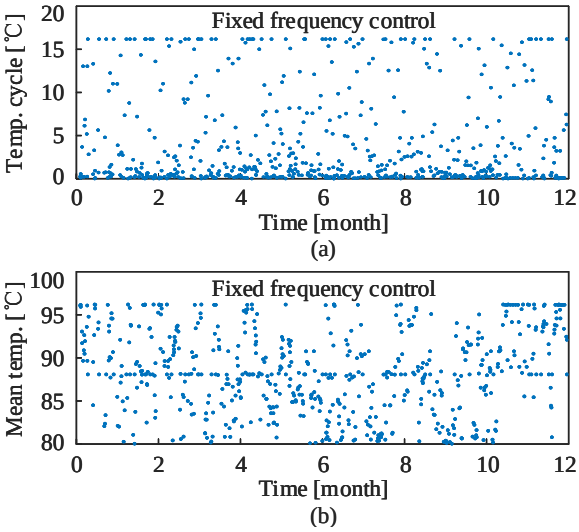

Fig. 4.19: Rain-flow counting results of the junction temperatures with fixed carrier frequency control. (a) Junction temperature cycle and (b) Mean junction temperature.

Thus, the impact of repetitive thermal stresses on the power semiconductors can be evaluated by [98]

$$N_f = A\left(\Delta T_\mathrm{j}\right)^{\alpha} \cdot \exp\left(\frac{E_a}{k_b T_\mathrm{jm}}\right), \tag{4.11}$$

where N_f is the number of cycles to failure under particular stress condition; $A = 3.025 \times 10^5$, $\alpha = -5.039$, $E_a = 9.891 \times 10^{-20}$ J, and k_b is the Boltzmann constant; ΔT_j and T_jm are the junction temperature variation and the mean junction temperature in unite of Kelvin. As shown in Fig. 4.9, the thermal loading are divided into two categories, namely the random cycles and periodic cycles. The random cycles are caused by the power loading variations and ambient temperature changes. The periodic cycles are caused by the fundamental frequency power loss variation with a fixed cycle period. The number of periodic cycles is fixed during one sampling period of the mission profile, and do not need to do the Rainflow counting analysis. As for the random cycles, the Rainflow counting results plotted in chronological order based on the ending time of thermal cycles are shown in Fig. 4.19 and Fig. 4.20, including the junction temperature cycle amplitude ΔT_j, and

the mean junction temperature T_{jm}. It can be seen that the maximum junction temperature random cycle amplitude of the adaptive frequency control is about 4 °C lower than the fixed frequency control, and the mean junction temperatures decrease to around 4 °C for the adaptive frequency control. As it is expected, taking the most stressed power component S_2 for example, the relieved thermal stress resulting from the adaptive frequency control will cause less damage (12% as can be seen in Fig. 4.21) during the one-year mission profile, and have a longer lifetime expectation than the fixed frequency control.

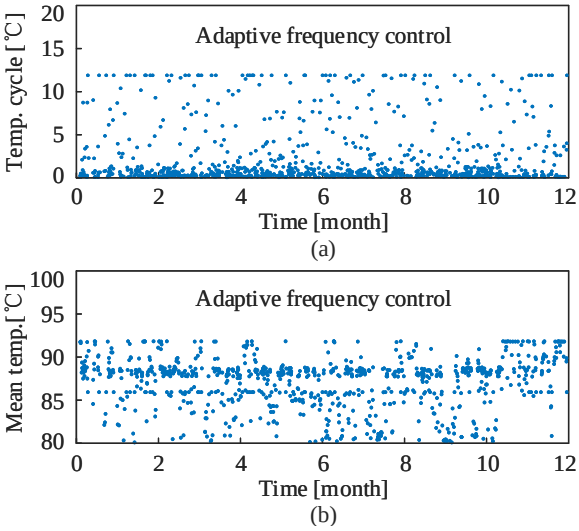

Fig. 4.20: Rain-flow counting results of the junction temperatures with adaptive carrier frequency control. (a) Junction temperature cycle and (b) Mean junction temperature.

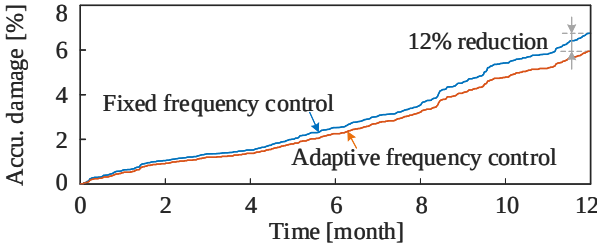

Fig. 4.21: The accumulated damage of the power devices comparison between the proposed method and conventional method. Source: [C4]

A comprehensive comparison between the two control methods is shown in Fig. 4.22. It can be clearly observed that by utilizing adaptive frequency control, the carrier frequency, circulating current ripple amplitude, thermal

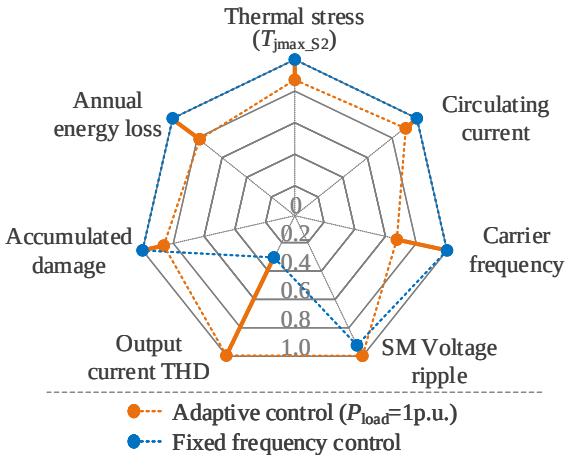

Fig. 4.22: Comprehensive comparison of an MMC performance when applying the proposed method and the conventional method.

stress of the power devices, annual energy loss of the MMC system, and the accumulated damage of the power devices are all reduced compared with the conventional fixed frequency control. Meanwhile, at the cost of other system performance, the output current THD and the SM voltage ripple both increase but it is still within an allowable limit.

Table 4.2: Experimental parameters of the three-phase MMC.

Power rating P	15 kW	DC link voltage U_{dc}	900 V
SM number per arm N	4	Arm inductance L_{arm}	4 mH
SM voltage U_{sm}	225 V	SM capacitance C_{sm}	1.5 mF
Modulation index m	0.71	Ambient temperature T_a	24 °C

4.4 Case Study: Three-Phase MMC Based Experimental Validation

The effectiveness of the proposed adaptive carrier frequency control is validated based on a three-phase 15-kVA MMC platform as shown in Fig. 4.23. Each arm has 4 SMs with IGBT module F450R12KS4 from Infineon, two 400 V capacitors connected in parallel, and one bleeding resistor. Other main system parameters are listed in Table 4.2. According to the proposed control method, a series of power loading conditions and carrier frequencies are chosen as shown in Fig. 4.24 and Table 4.3 when the output current THD

is set to 5%. Note that the phase shift between the upper arm and the lower arm carriers is always applied in the experiments.

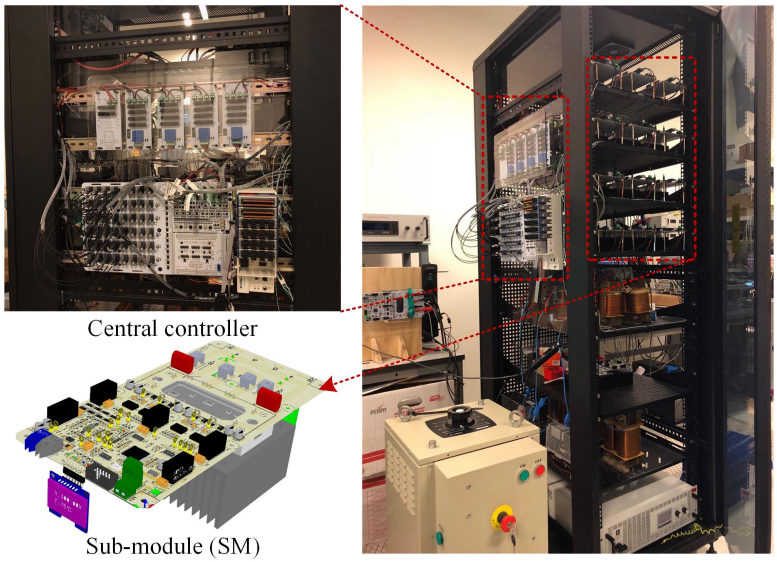

Fig. 4.23: Experimental platform of 15-kVA three-phase MMC with a sub-module overview.

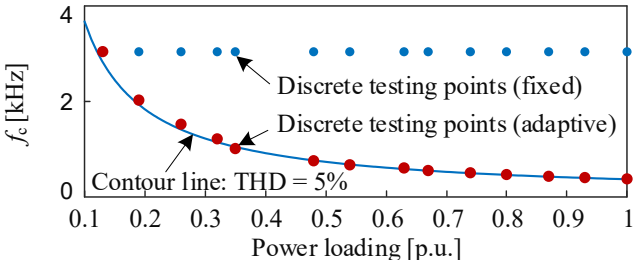

Fig. 4.24: Relationship between carrier frequency and power loading conditions with the output current THD being 5%.

4.4.1 Output Current THD and SM Voltage Ripple

According to Table 4.3, a series of operating conditions are tested based on the three-phase MMC platform. Fig. 4.25 shows the output current THD performance with different control strategies. As it can be expected, the current THD gradually goes down from 5.6 % to 1.86 % with the increase of the power loading from 0.13 p.u. to 1.0 p.u. when a fixed carrier frequency (i.e., 3045 Hz) is applied. By contrast, the measured current THD is always

Table 4.3: Discrete testing points for experimental validation.

P_{load} [p.u.]	1.00	0.93	0.87	0.80	0.74	0.67	0.63
f_c [Hz]	380	408	435	471	508	555	609
P_{load} [p.u.]	0.54	0.48	0.35	0.32	0.26	0.19	0.13
f_c [Hz]	675	760	1015	1218	1523	2030	3045

around a constant value (i.e., 5.6%) under a wide range of power loading by applying a changeable carrier frequency dynamically. Even though 5.6 % is a bit higher than the targeted THD 5.0%, the experimental results still validate the THD analysis.

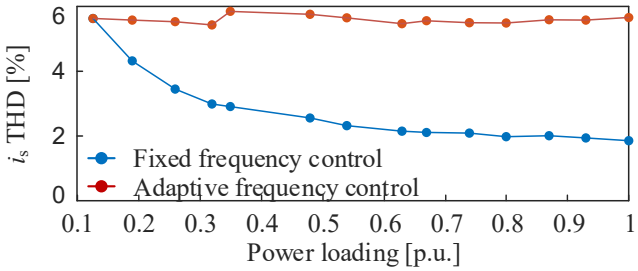

Fig. 4.25: Experimental results for different control schemes: output current THD.

As it can be seen from Fig. 4.26, the measured SM voltage ripples gradually grow as the power loading goes up, but are basically unchanged when different carrier frequencies are applied. The experimental results agree with both the analysis and the simulation results.

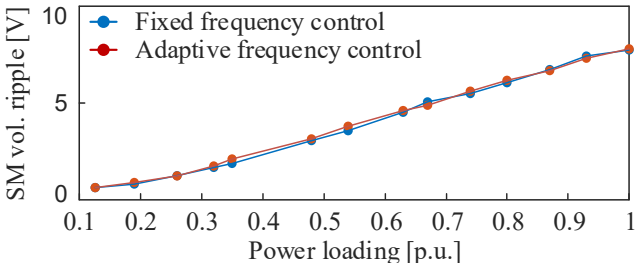

Fig. 4.26: Experimental results for different control schemes: SM voltage ripple (half of peak-to-peak value).

4.4.2 Power Loss

In order to see how the power loss of the whole MMC system behaves with different control strategies, several main components in the system are tested. One SM and one arm inductor in the upper arm of Phase A are tested. By scaling with the number of specific components, the total power loss of the MMC system can be evaluated.

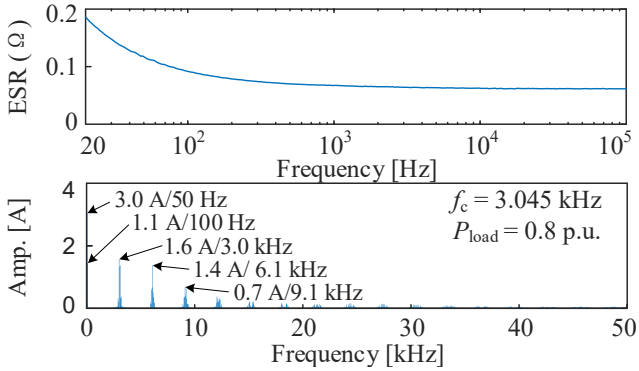

Fig. 4.27: The measured ESR and the current going through the SM capacitor.

Specifically, the power losses of one SM as a whole and the arm inductor are tested by the power analyzer PPA4500. As for SM capacitor, its equivalent series resistance (ESR) and current are measured, respectively. By summarizing the power losses at all harmonic frequencies, the power loss of one capacitor can be obtained as [99]

$$P_{\text{loss\_Cap\_1}} = 2\sum_{i=1}^{200} \widehat{I}_i^2 \text{ESR}_i, \tag{4.12}$$

where $P_{\text{loss\_Cap\_1}}$ is the power loss of capacitor in one SM (two capacitors in parallel in one SM in this setup), $\widehat{I}_i$ and $\text{ESR}_i$is the Root Mean Square (RMS) of the capacitor current and the ESR of the capacitor at the i-th harmonic. Note that 200 harmonics, namely up to 10 kHz harmonic frequency, are taken into account for the loss calculations in terms of 50 Hz fundamental frequency. Fig. 4.27 shows the tested ESR of the capacitor and its current harmonic distribution. By applying (4.12), a slight power loss increase can be observed in Fig. 4.28 for SM capacitors due to the introduced extra current harmonics. Comparatively speaking, more power is dissipated by the arm inductor and the power loss is almost doubled when employing the proposed control method as shown in Fig. 4.29. It should be noted that the practical MMC utilizes dry-type air-core reactors instead of iron-core inductor in this setup. Thus, the losses related to iron-core don't exist in practical applications.

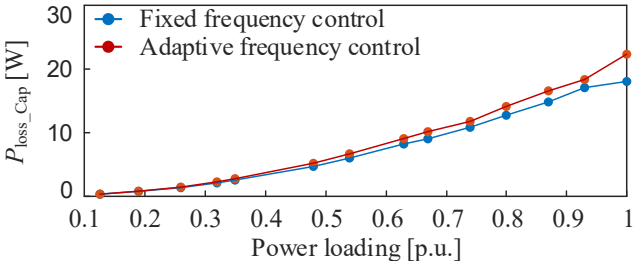

Fig. 4.28: Experimental power loss of all sub-module capacitors in the MMC.

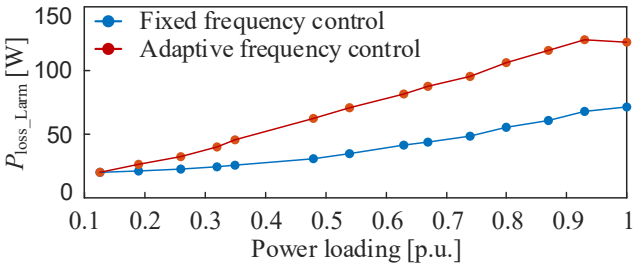

Fig. 4.29: Measured power loss of all arm inductors in the three-phase MMC.

Moreover, to discharge the SM capacitor while the system shuts down, SM capacitors are paralleled with a 12 kΩ bleeding resistor in this setup, and its power loss can be calculated by

$$P_{\text{loss\_Rb\_1}} = \frac{U_{\text{sm}}^2}{R_{\text{b}}} = \frac{225^2}{12000} = 4.22\text{W}, \tag{4.13}$$

where $P_{\text{loss\_Rb\_1}}$ is the power loss of the bleeding resistor in one SM, and R_{b} is the resistance of the bleeding resistor.

The power loss of power semiconductors in one SM is

$$P_{\text{loss\_IGBT\_1}} = P_{\text{loss\_SM\_1}} - P_{\text{loss\_Cap\_1}} - P_{\text{loss\_Rb\_1}}, \tag{4.14}$$

where $P_{\text{loss\_IGBT\_1}}$ and $P_{\text{loss\_SM\_1}}$ are the power losses of all power semiconductors in one SM and one SM as a whole.

Fig. 4.30 shows the power consumed by 24 SMs in total and the adaptive frequency control has a positive impact on the loss reduction being around 10% and most of them come from the power dissipation of power modules as shown in Fig. 4.31. More specifically, as it can be seen from Fig. 4.32, the power dissipation of the power semiconductors account for over 80% of the total SM power loss with the percentage of the bleeding resistor and the capacitor being around 13% and 3%, respectively. The reduced power loss

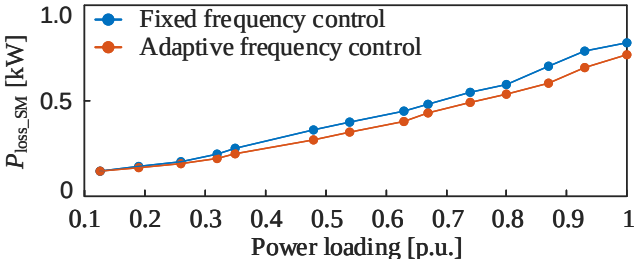

Fig. 4.30: Measured power loss of all SMs in the three-phase MMC.

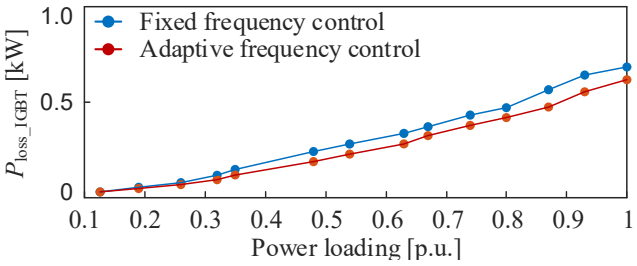

Fig. 4.31: Measured power loss of all power semiconductors in the MMC.

and thermal stress will contribute to a better reliability performance of the power semiconductors.

It can also be seen from Fig. 4.28 and Fig. 4.29 that higher THD caused by the lower carrier frequency can lead to higher power losses for the passive components. In this case study, the power loss from capacitors account for about 3% of the total power loss of the system. In practical applications, due to features like high voltage rating, excellent ripple current performance, and high stability [48, 50, 100], metalized polypropylene film (MPPF) capacitors are normally used instead of aluminum electrolytic capacitors in this setup. Thus, the lower ESR of the MPPF capacitors can push the percentage of power dissipated by SM capacitors further down from 3% to below 0.5% of total power loss [101].

However, when it comes to the system efficiency, merely slight increase can be seen for the proposed method as shown in Fig. 4.33. In this case study, the power loss of the arm inductors at unity power loading is almost doubled from 71 W to 122 W when the adaptive frequency control is applied as shown in Fig. 4.29. Accordingly, the power loss contribution from arm inductors accounts for 8% and 13% of the total system power loss with the two control methods. It causes the situation that the overall efficiency of the MMC system with adaptive frequency control is only slightly higher than that with fixed frequency control. In practice, high voltage power semiconductors present lower average conduction losses and higher average switch-

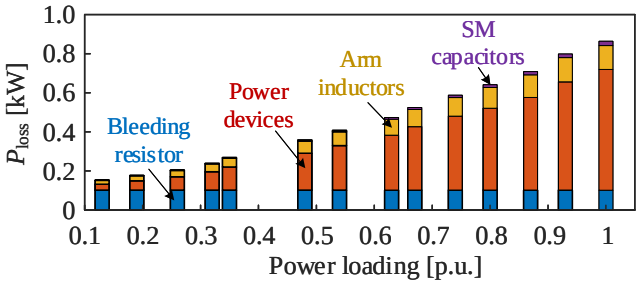

Fig. 4.32: Measured power loss comparison among different components.

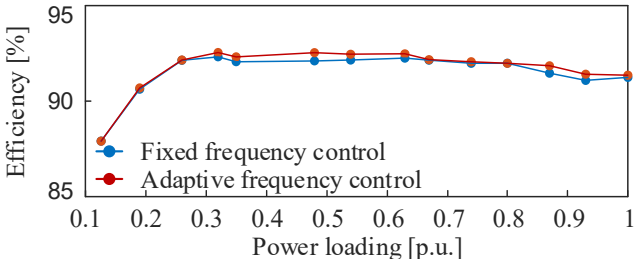

Fig. 4.33: Experimental results: overall efficiency of the MMC system.

ing losses. It means that more power loss reduction of power semiconductors can be achieved by applying the adaptive frequency control for high voltage rating power semiconductors and a higher efficiency can be expected as well.

4.5 Summary

In this chapter, an adaptive carrier frequency control is proposed to improve the reliability performance of power semiconductor and to enhance the energy efficiency of the MMC system. By exploring the carrier frequency boundary while meeting specific output current THD and SM voltage ripple requirements, the carrier frequency of the MMC can be dynamically adjusted according to the loading conditions. Its impact on the power loss, thermal stress, and lifetime of the power semiconductors is evaluated. Case study based on a 15-kVA three-phase MMC prototype validates the effectiveness of the proposed method in achieving power loss reduction of the power semiconductors.

Chapter 5

Condition Monitoring of Capacitors in MMCs

This chapter studies condition monitoring (CM) strategies for SM capacitors in the MMC. By taking full advantage of the hardware characteristics of the MMC, two CM strategies have been proposed. One is based on a DC-side soft start-up. Another is based on a reference SM with known capacitance and use that for CM. Both approaches are easy to be implemented with light computational load.

5.1 Background

Besides the power semiconductors, sub-module (SM) capacitors are the other major components in MMCs. Of all kinds of capacitors, metalized polypropylene film (MPPF) capacitors stand out and are typically applied in MMCs [49] because of the features like high voltage rating and self-healing. However, the capacitance drop caused by degradation is inevitable. In general, a 5% capacitance reduction is regarded as a criterion of the end-of-life for MPPF capacitors [50]. Most existing condition monitoring methods [71–74] for MMC are targeting electrolytic capacitors, which typically have 20% capacitance drop at the end-of-life. The large value drop will not pose severe challenge to the accuracy of the measurement hardware, such as current sensors and voltage sensors and the above methods work well. However, when it comes to MPPF capacitors with merely 5% capacitance change, the monitoring accuracy of the CM method will be a large concern from a practical application point of view. Therefore, in order to enhance the monitoring accuracy, two capacitor CM methods are proposed in this Ph.D. project. One is based on the DC-side start-up process of the MMC, and the other one is

based on a reference SM as [74] but with greatly improved accuracy.

5.2 DC-Side Start-Up Based Condition Monitoring

5.2.1 Operation Principle

All capacitors need to get charged to the average SM voltage to avoid inrush current at the instant of the start of the MMC. One straightforward way is to use the start-up resistor [10] as shown in Fig. 5.1(a). In this case, an RC charging circuit formed by the resistor R_s and SM capacitors can be utilized to conduct the condition monitoring. By turning on switch S_1 and turning off switch S_a, all SM will be charged by the DC bus and the three-phase MMC can thus be simplified as Fig. 5.1(b).

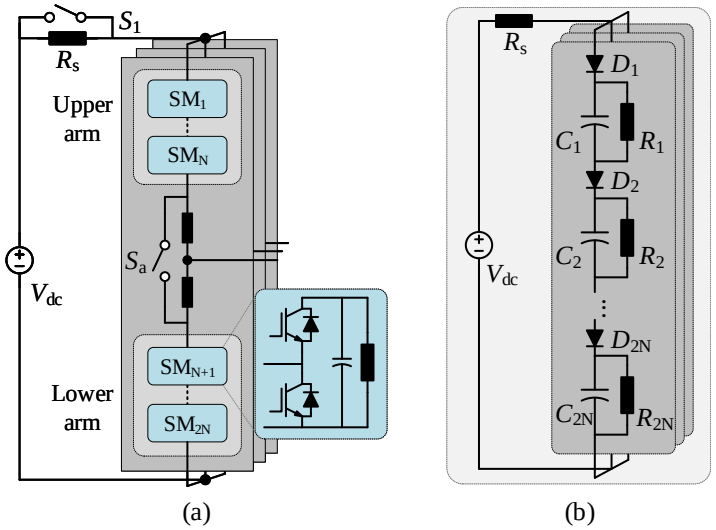

Fig. 5.1: Circuit simplification of the MMC during its start-up. (a) Three-phase MMC, (b) Equivalent three-phase MMC during DC-side start-up, (c) Equivalent single-phase MMC during DC-side start-up. Source: [J3]

In this case, the MMC can be simplified as Fig. 5.1(b). When it comes to the phase current and SM capacitor voltages in a specific phase, a single-phase circuit as shown in Fig. 5.2(a) can be achieved with a tripled start-up resistance. The impact of all series-connected diodes can be taken into account by introducing a constant voltage source V_d and an on-state resistor R_d [103]. Therefore, the three-phase MMC can be simplified into Fig. 5.2(b)

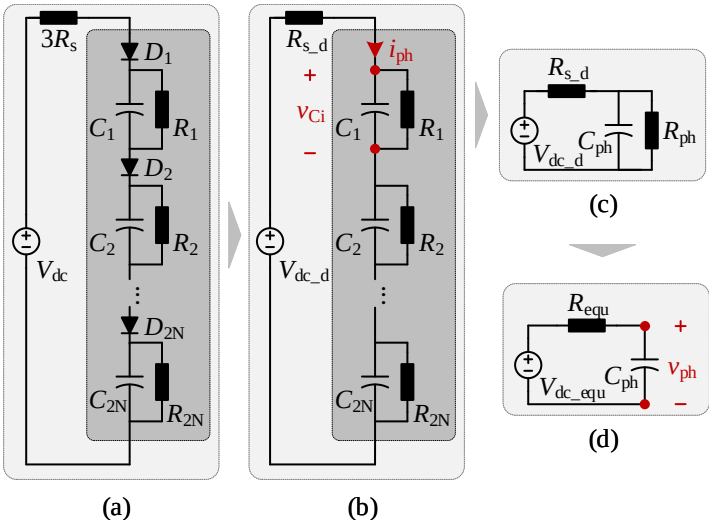

Fig. 5.2: Circuit simplification of the MMC during its start-up. (a) Equivalent single-phase MMC during DC-side start-up, (b) Equivalent single-phase MMC with linearized diode model, (c) Equivalent MMC circuit regarding the same phase current, and (d) Equivalent MMC circuit regarding the same phase capacitor voltage. Source: [J3]

and further into Fig. 5.2(c).

$$\begin{cases} R_{\text{s\_d}} = 3R_{\text{s}} + 2NR_{\text{d}}, V_{\text{dc\_d}} = V_{\text{dc}} - 2NV_{\text{d}} \\ R_{\text{ph}} = \sum_{i=1}^{2N} R_i, \dfrac{1}{C_{\text{ph}}} = \sum_{i=1}^{2N} \dfrac{1}{C_i} \end{cases} \tag{5.1}$$

where $R_{\text{s\_d}}$, R_{s}, $V_{\text{dc\_d}}$ and V_{dc} refer to the equivalent start-up resistance and equivalent DC bus voltage with/without considering the diodes; R_{ph} and C_{ph} are the equivalent phase resistance and capacitance; R_i and C_i are the resistance and capacitance of the i-th SM; N is the SM number per arm.

The voltage of the equivalent phase capacitor C_{ph} in Fig. 5.2(c) can be derived as given in (5.2) according to Fig. 5.2(d).

$$\begin{cases} v_{\text{ph}} = V_{\text{dc\_equ}} \left(1 - \exp(\dfrac{-t}{\tau_{\text{equ}}})\right) \\ V_{\text{dc\_equ}} = \dfrac{R_{\text{ph}}}{R_{\text{ph}} + R_{\text{s\_d}}} V_{\text{dc\_d}}, R_{\text{equ}} = \dfrac{R_{\text{ph}} R_{\text{s\_d}}}{R_{\text{ph}} + R_{\text{s\_d}}} \end{cases} \tag{5.2}$$

where $\tau_{\text{equ}} = R_{\text{equ}} C_{\text{ph}}$ is the equivalent time constant; $V_{\text{dc\_equ}}$ and R_{equ} are the equivalent DC voltage and resistance seen from the terminals of C_{ph}.

So far, the phase current i_{ph} can be obtained by

$$i_{\text{ph}} = \frac{V_{\text{dc\_d}} - v_{\text{ph}}}{R_{\text{s\_d}}} = \frac{V_{\text{dc\_d}}}{R_{\text{ph}} + R_{\text{s\_d}}} \left(1 + \frac{R_{\text{ph}}}{R_{\text{s\_d}}} \exp(\frac{-t}{\tau_{\text{equ}}})\right) \tag{5.3}$$

where i_{ph} is the phase current.

All series-connected SMs share the same phase current calculated above. Therefore, the following equation holds for a specific SM

$$C_i \frac{dv_{C_i}}{dt} + \frac{v_{C_i}}{R_i} = i_{\text{ph}}, \tag{5.4}$$

where v_{C_i} is the voltage across the i-th SM capacitor. By substituting (5.3) into (5.4), the SM voltage is estimated as

$$\begin{cases} v_{C_i} = A_1 R_i \left(1 - \exp(\frac{-t}{\tau_i})\right) + \frac{A_2 \tau_{\text{equ}} R_i}{\tau_{\text{equ}} - \tau_i} \left(\exp(\frac{-t}{\tau_{\text{equ}}}) - \exp(\frac{-t}{\tau_i})\right) \\ A_1 = \frac{V_{\text{dc\_d}}}{R_{\text{ph}} + R_{\text{s\_d}}}, A_2 = \frac{R_{\text{ph}}}{\left(R_{\text{ph}} + R_{\text{s\_d}}\right) R_{\text{s\_d}}} V_{\text{dc\_d}} \end{cases} \tag{5.5}$$

in which $\tau_i = R_i C_i$ is the time constant of i-th SM. The transient SM voltage response is dominated by τ_{equ} as τ_i is far larger than τ_{equ} in practical MMC applications [70]. Therefore, (5.5) can be rewritten if a short period of time (e.g., several τ_{equ}) is applied

$$\begin{cases} v_{C_i} = K_1 + \frac{K_2}{\tau_{\text{equ}} - \tau_i} \\ K_1 = A_1 R_i \left(1 - \exp(\frac{-t}{\tau_{\text{rated}}})\right) \\ K_2 = A_2 \tau_{\text{equ}} R_i \left(\exp(\frac{-t}{\tau_{\text{equ}}}) - \exp(\frac{-t}{\tau_{\text{rated}}})\right) \end{cases} \tag{5.6}$$

in which $\tau_{\text{rated}} = R_{\text{rated}} C_{\text{rated}}$ is the rated time constant. Based on the above analysis, the capacitance of the i-th SM can thus be calculated by

$$C_i = \left. \frac{\tau_{\text{equ}}}{R_i} - \frac{K_2}{\left(v_{C_i} - K_1\right) R_i} \right| \quad t = n\tau_{\text{equ}} \tag{5.7}$$

A flowchart is given in Fig. 5.3 to show how the whole CM process is implemented.

5.2.2 Practical Considerations

Several practical issues have to be taken into account regarding the implementation of the proposed method.

- Impact of Diode Tolerance and Degradation

  Due to the manufacturing tolerance and aging of components, the voltage source and on-state resistance in the diode are subject to change with time. However, given their relatively small values compared with the DC bus voltage, their impacts are negligible.

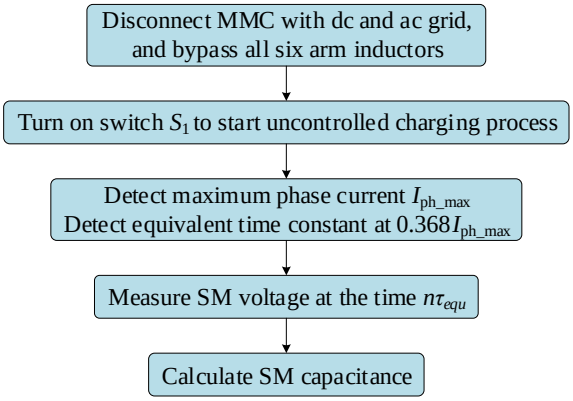

Fig. 5.3: Flowchart of the DC-side start-up based capacitor condition monitoring. Source: [J3]

- R_{s_d} Measurement

  Since all SM capacitors are in a short-circuit state at the instant of the start, R_{s_d} can thus be calculated as

$$R_{s\_d} = \frac{V_{dc\_d}}{I_{ph\_max}}. \tag{5.8}$$

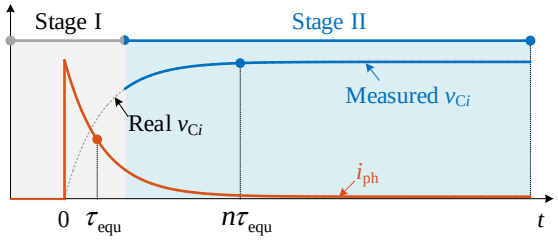

Fig. 5.4: Data sampling during the start-up process of the MMC (Stage I: SM control board is not powered on and Stage II: SM control board is powered on.). Source: [J3]

- SM Voltage Measurement

  In practice, SMs are self powered by its own capacitors [104]. In this case, the SM control board will not work and measure its voltage before the capacitor voltage is higher than the threshold of its auxiliary power supply. As shown in Fig. 5.4, v_{C_i} is not measurable at stage I as the SM controller is powered off. At stage II, the SM control board is powered on and the SM voltage can be measured for the condition monitoring.

It should be noted that the phase current can be measured throughout the start-up process.

Table 5.1: Main system parameters for the MMC used in the case study.

Parameter	Value	Parameter	Value
Power rating S_{rated}	300 MVA	DC bus voltage V_{dc}	300 kV
SM capacitance C_{rated}	5.0 mF	SM number per arm N	150
Bleeding resistor R_{rated}	12 kΩ	Start-up resistor R_{s}	1 kΩ
Diode zero-current voltage V_{d}	1.6 V	Diode on-state resistance	1.6 mΩ

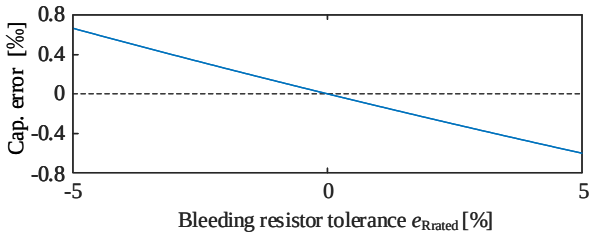

Fig. 5.5: The impact of bleeding resistor tolerance on capacitance estimation. Source: [J3]

- Impact of Bleeding Resistor Tolerance

  Since the rated bleeding resistance is utilized to estimate the SM capacitance instead of its real value, certain errors might be introduced due to the bleeding resistor tolerance. Its impact is thus evaluated based on a 300 MVA three-phase MMC system with its main parameters listed in Table 5.1. By introducing ±5% variation to R_{rated}, its impact on the capacitance estimation can be evaluated and it is shown in Fig. 5.5. It can be seen that the error is within 0.08%, which is very small and can be completely neglected.

- Impact of Time Delay

  Time delays might result from signal sampling and communication. For example, the current sampling frequency can affect the estimation accuracy of the τ_{equ}, which is equal to 50 ms in this case study when considering the same start-up resistor and SM capacitor mentioned above. In terms of a typical 20 kHz current sampling rate, the sampling delay is about 0.05 ms and introduces 0.1% error to τ_{equ}.

Table 5.2: Combination of capacitors to mimic the SM degradation. Source: [J3]

[uF]	C_0	C_1	C_2	C_3	C_4	C_5	C_{sum}	%
C_{rated}	1640	10	10	22	22	22	-	-
Cap1	*	*		*	*	*	1716	0.00%
Cap2	*	*	*	*	*		1704	0.70%
Cap3	*	*		*	*		1694	1.28%
Cap4	*	*	*	*			1682	1.98%
Cap5	*	*		*			1672	2.56%
Cap6	*	*	*				1660	3.26%
Cap7	*	*					1650	3.85%
Cap8	*						1640	4.43%

Table 5.3: The rated capacitances and the tested capacitances obtained by LCR meter at 20 Hz.

	C_{sm1}	C_{sm2}	C_1	C_2	C_3	C_4	C_5
C_{rated} [uF]	820	820	10	10	22	22	22
C_{real} [uF]	731	732	9.9	9.8	20.4	20.3	20.5
Tolerance [%]	-10.9	-10.7	-1.0	-2.0	-7.3	-7.7	-6.8

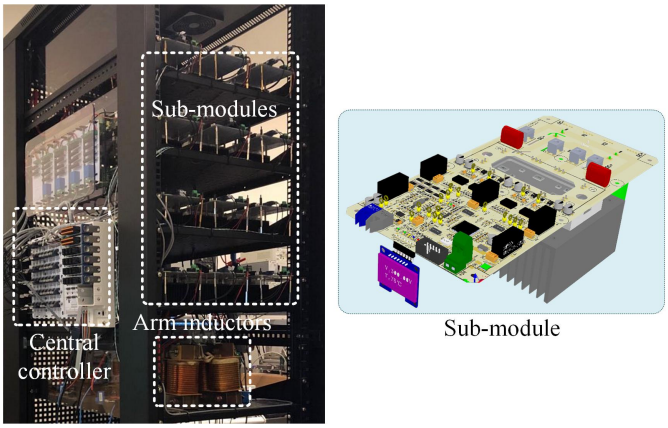

Fig. 5.6: Experimental platform of 15-kVA three-phase MMC with a sub-module overview. Source: [J3]

5.2.3 Experimental Validation

A series of capacitor combinations listed in Table 5.2 are used to validate the proposed method based on a 15-kVA three-phase MMC as shown in Fig. 5.6. The experimental results in Fig. 5.7(a) show that the phase current jumps to its maximum value being about 4.8 A at the instant of the start, then decreases exponentially to around zero. At the same time, SM capacitor voltage

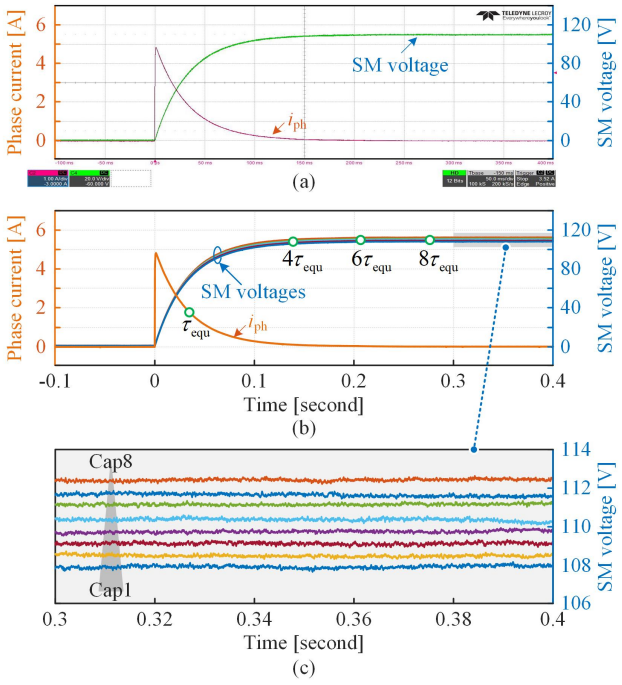

Fig. 5.7: Experimental results of phase current and SM voltage under different capacitor aging levels (see Table 5.2). (a) Experimental waveform from oscilloscope screen-shot; (b) SM voltages and phase current with different capacitors; (c) Zoom-in SM voltages shown in (b). Source: [J3]

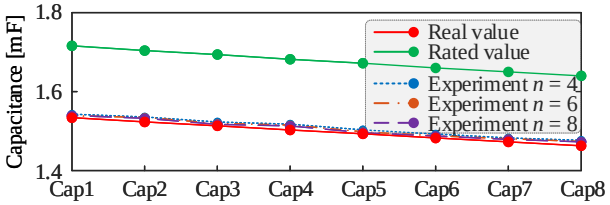

Fig. 5.8: Comparison between measured, real and rated SM capacitances at different time points $n\tau_{\text{equ}}$ ($n = 4, 6, 8$) (see Fig. 5.7 (b)). Source: [J3]

increases and stabilizes at around 112.5 V. Testing results with different capacitors are shown in Fig. 5.7(b) and (c). It can be observed that a lower steady-state SM voltage can be achieved when its capacitance is higher.

As for the measured capacitance shown in Fig. 5.8, a constant error of around 10% as shown in Fig. 5.9 can be observed due to the manufacturing tolerance, which are tested by an LCR meter and listed in Table 5.3. Excluding the impact of tolerance, the estimation error is within 1% as shown in Fig. 5.10. Since the capacitance change is treated as the indicator of capacitor

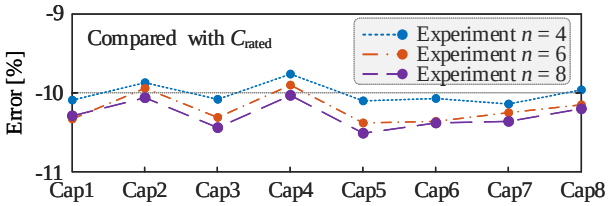

Fig. 5.9: The capacitance estimation error compared with the rated capacitances for different experiments. Source: [J3]

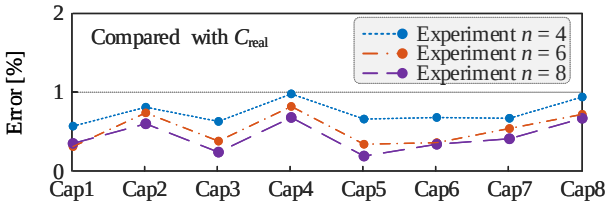

Fig. 5.10: The capacitance estimation error compared with the real capacitances for different experiments. Source: [J3]

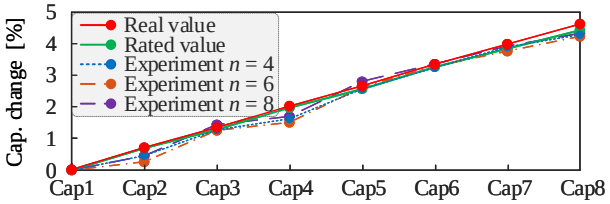

Fig. 5.11: Comparison between the percentage of capacitance change for the measured, real and rated capacitances at different time points $n\tau_{equ}$ ($n = 4, 6, 8$). Source: [J3]

degradation rather than its absolute value, the value drop percentage is thus shown in Fig. 5.11. It can be seen that the trends for the capacitance drop of the rated value and real value can both be well captured by the proposed method.

5.3 Reference Submodule Based Condition Monitoring

5.3.1 Operation Principle

The core idea of the reference sub-module based (RSB) condition monitoring method is that the monitored SM shares the same gate signal with the reference SM, whose value is known by being tested by a specific measure-

ment circuit. Under this condition, the voltage difference between the two SMs can only be caused by the their capacitance difference due to the series connection. The original RSB method is based on the SM voltage ripple difference as shown in Fig. 5.13 with the following relationship

$$C_{\mathrm{m}} = \frac{\Delta v_{\mathrm{ref}}}{\Delta v_{\mathrm{m}}} C_{\mathrm{ref}}, \tag{5.9}$$

where C_{ref}, C_{m}, Δv_{ref} and Δv_{m} are the capacitance and the peak-to-peak voltage of the reference and monitored SMs. However, the small voltage ripple amplitude (e.g., less than 10% of the rated value) makes it not sensitive to the capacitor degradation and leads to low monitoring accuracy.

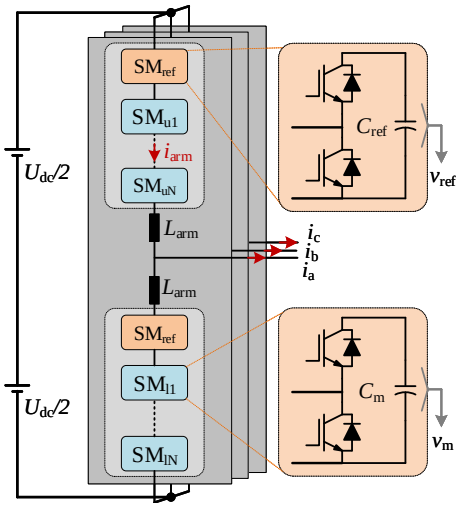

Fig. 5.12: A three-phase MMC system with six reference SMs used for the condition monitoring (i_{a}, i_{b} and i_{c} are the three phase output currents; v_{m} and v_{ref} are the voltages of the monitored SM and the reference SM.). Source: [J4]

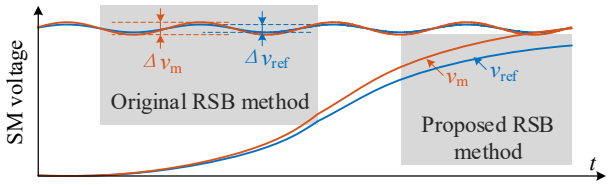

Fig. 5.13: SM voltages used for condition monitoring in the original and proposed RSB methods. (Δv_{ref}, Δv_{m}, v_{ref}, and v_{m} are the peak-to-peak voltages and the real voltages of the reference SM and the monitored SM.) Source: [J4]

By contrast, the proposed RSB method takes full advantage of the whole SM voltage range by charging the monitored SM from zero to its rated voltage

as shown in Fig. 5.13. Regarding the same measurement hardware and accuracy, the proposed method can achieve ten times higher accuracy than the original method with

$$v_{\mathrm{ref/m}} = \frac{1}{C_{\mathrm{ref/m}}} \int S_{\mathrm{m}} i_{\mathrm{arm}} dt, \tag{5.10}$$

where v_{ref}, v_{m} are the voltage of the reference and monitored SMs; i_{arm} is the arm current; S_{m} is the gate signal. Since the two SMs are charged from zero voltage, the instantaneous voltages can be used directly to obtain the monitored capacitance throughout the whole CM process given as

$$C_{\mathrm{m}} = \frac{v_{\mathrm{ref}}}{v_{\mathrm{m}}} C_{\mathrm{ref}}. \tag{5.11}$$

It can be seen that no complicated calculations or controls are involved in this process. Since the two SMs can always be charged to their rated voltage during the CM process, it means that the proposed RSB method is independent of the loading conditions of the MMC. Meanwhile, the utilization of instantaneous voltages further simplifies the implementation of the proposed method. To better illustrate the whole procedure of implementing the proposed CM method, a flowchart is given in Fig. 5.14.

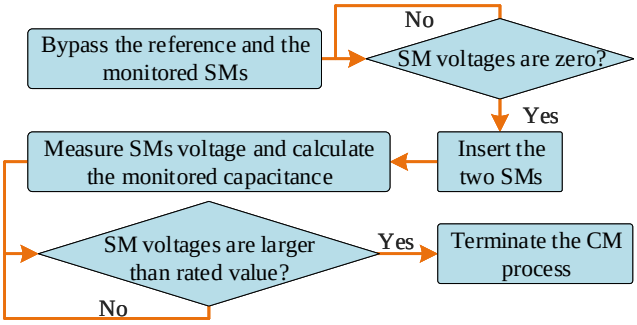

Fig. 5.14: Flowchart of the proposed RSB condition monitoring method. Source: [J4]

5.3.2 Two Potential Simplified Reference SM Topologies

Several equipotential points exist in the MMC system, where two or more different SMs share the same voltage level. In this case, different SMs can actually share one capacitor through proper hardware connection. This feature offers an opportunity to do the capacitor condition monitoring with reduced number of reference SM and specifically designed capacitance measurement circuit.

- **Three Reference SMs based RSB Method**

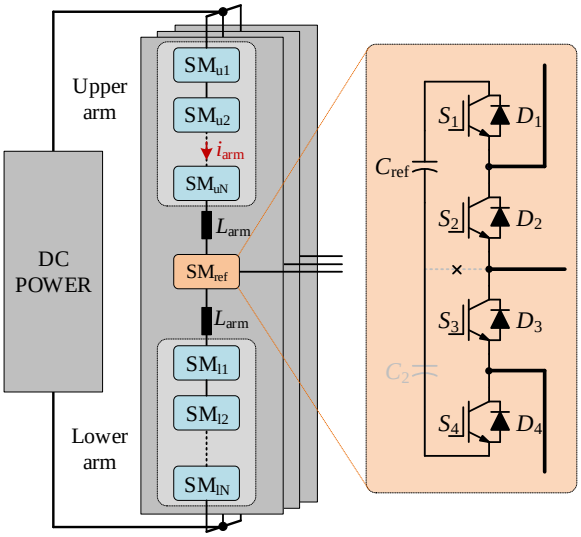

Fig. 5.15: A three-phase MMC system with three reference SMs for capacitor monitoring.

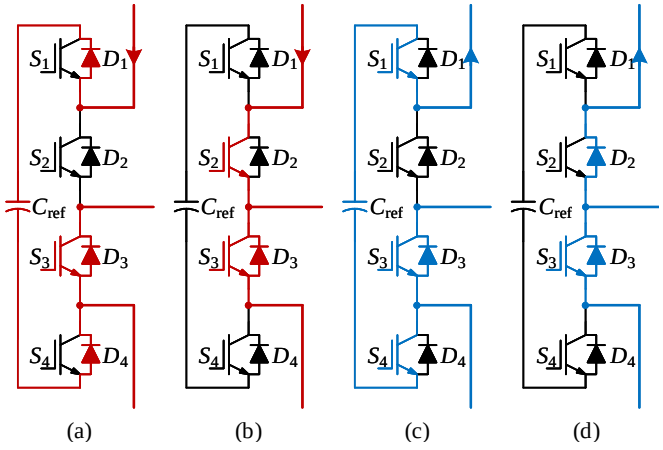

Fig. 5.16: Arm current path when the reference SM functions as a SM in the upper arm: (a) Inserted state with positive arm current, (b) Bypassed state with positive arm current, (c) Inserted state with negative arm current, and (d) Bypassed state with negative arm current.

By integrating the SMs connected to the AC output in the upper arm and lower arm, only one capacitor and one corresponding capacitance measurement circuit are needed for each phase with the modified reference SM as shown in Fig. 5.15. Since it is based on two conventional half-bridge SMs, no hardware modification besides reconnecting the two SMs is needed. By a proper control, the modified reference SM can be regarded as an SM either

Table 5.4: Available switching states of the reference SM.

S_1	S_2	S_3	S_4	SM state	belong to
off	on	on	on	Bypass	Upper arm
on	off	on	on	Insert	Upper arm
on	on	off	on	Insert	Lower arm
on	on	on	off	Bypass	Lower arm
off	on	on	off	Bypass	No arm

in the upper arm or in the lower arm.

The output states of the reference SM are listed in Table 5.4. Specifically, when the lower two IGBTs are turned off (S_3 and S_4), the reference SM functions as an SM in the upper arm. By switching the upper two complementary IGBTs (S_1 and S_2) on and off, the reference SM can be inserted and bypassed respectively. Similarly, by controlling the upper two devices being in the on-state all the time, the reference SM will be connected in series with the other SMs in the lower arm. One example of the arm current path is given in Fig. 5.16 when the reference SM is connected to the upper arm. Therefore, the proposed reference SM can be shared by the upper and the lower arms with merely one capacitor and corresponding capacitance measurement circuit for the reference SM.

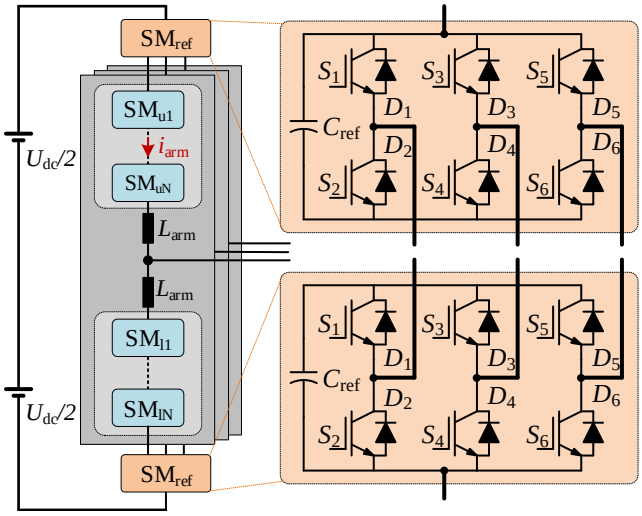

Fig. 5.17: A three-phase MMC system with two reference SMs for capacitor monitoring.

- **Two Reference SMs based RSB Method**

Sub-modules connected to positive and negative DC bus can share one common capacitor as shown in Fig. 5.17. Three conventional half-bridge SMs in three phases are connected through the capacitor terminals. By doing so, a reference SM shared by three phases is built, and only two reference SM capacitors needs to be accurately detected in the whole MMC system. In fact, as can be seen, the reference SM actually turns into a three-phase converter. The control of each SM is independent and remains the same as separate SMs. Therefore, by proper control, the reference SM can be inserted into one of the three phases at one time and helps to monitor the other SMs in the arm it belongs to. For example, when S_1 is turned off, S_3 and S_5 are turned on, the upper arm reference SM can be inserted into phase A.

It should be noted that the reference SM connected to positive and negative DC bus are inversely connected and their gate signals should be inversely applied as well. Besides, when the reference SM functions as a normal SM shared by three phases, the voltage ripple of this capacitor will be extremely low compared to other SMs.

5.3.3 Accuracy Analysis

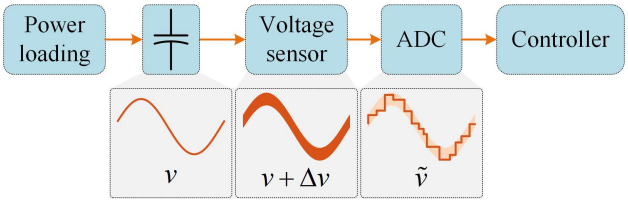

Fig. 5.18: Impact of the sensor and ADC accuracy on the voltage measurement. Source: [J4]

The accuracy of the measurement system greatly determines the accuracy of the condition monitoring. For the proposed RSB capacitor condition monitoring method, two major measurement components, namely the voltage sensor and the analog-to-digital converter (ADC), are involved in the SM voltage detection as shown in Fig. 5.18. In order to quantify their impacts, the relationship between the measured SM voltage and the real voltage is defined as

$$\tilde{v} = \text{floor}\left(\frac{v+\Delta v}{dv}\right) dv, \tag{5.12}$$

where v and $\tilde{v}$ are the real voltage and the measured voltage, which are $\Delta v_{\text{ref/m}}$ and $\Delta\tilde{v}_{\text{ref/m}}$ for the original RSB method, and $v_{\text{ref/m}}$ and $\tilde{v}_{\text{ref/m}}$ for the proposed RSB method as shown in Fig. 5.13; floor (x) outputs the greatest integer equal to or less than its input; Δv is the voltage measurement error caused by the voltage sensor. It belongs to $[-\varepsilon_s V_s, +\varepsilon_s V_s]$, where ε_s and V_s are the the accuracy and voltage range of the sensor, respectively. dv is the

minimum SM voltage resolution of the ADC. Assuming that the SM rated voltage is equal to V_s, the actual voltages used for the two RSB methods are

$$\begin{cases} v_{\text{ref}} = V_{\text{rated}}, v_{\text{m}} = \dfrac{v_{\text{ref}}}{1 - d_{\text{cap}}} \\ \Delta v_{\text{ref}} = p_{\text{v}} V_{\text{rated}}, \Delta v_{\text{m}} = \dfrac{\Delta v_{\text{ref}}}{1 - d_{\text{cap}}} \\ dv = \dfrac{V_{\text{rated}}}{2^B} \end{cases} \tag{5.13}$$

where p_{v} is the SM voltage utilization percentage for the CM; B is the bit-resolution of the ADC; d_{cap} is the capacitance drop percentage.

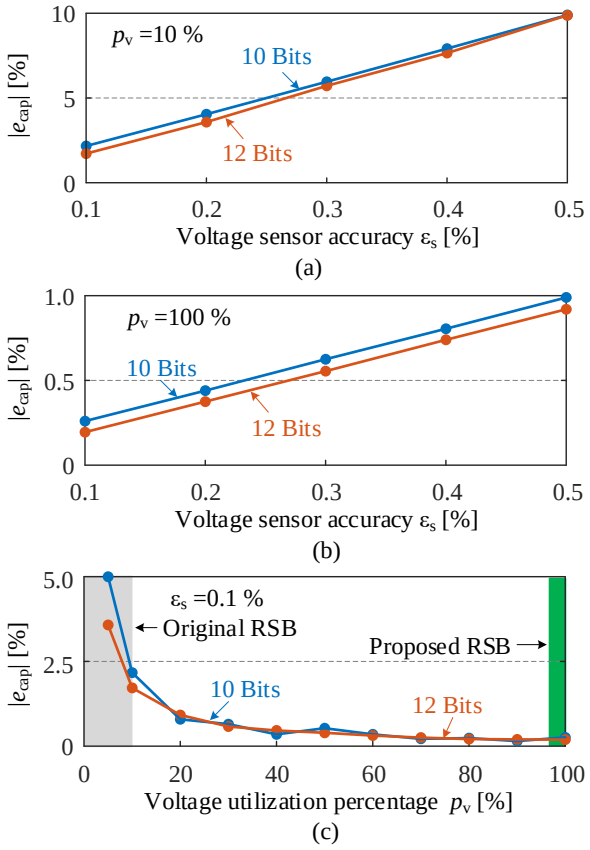

Fig. 5.19: Comparison of the capacitance estimation error between the original and the proposed RSB CM methods regarding different voltage sensor accuracy, ADC resolution, and SM voltage utilization rate. (a) Original RSB CM method, (b) Proposed RSB CM method, and (c) Voltage utilization percentage. Source: [J4]

Meanwhile, the error of the capacitance monitoring e_{cap} is

$$e_{\text{cap}} = \left(\frac{\tilde{C}_{\text{m}}}{C_{\text{m}}} - 1 \right) \times 100\%, \tag{5.14}$$

where C_{m} and $\tilde{C}_{\text{m}}$ are the real and the measured SM capacitances.

Combining (5.11)-(5.14), the accuracy comparison results between the two RSB methods are shown in Fig. 5.19. In terms of the same voltage sensor accuracy (e.g., 0.1%), the proposed RSB method can achieve an accuracy of 0.26% with voltage sensor range utilization rate being 100% as shown in Fig. 5.19(b). By contrast, the original RSB method estimates the capacitance based on the peak-to-peak voltage of the SM, an error as large as 2.2% (10 bits) can be observed in Fig. 5.19(a) considering a typical 10% voltage utilization rate p_{v}. In addition, it can be seen that the worse the voltage sensor accuracy is, the larger the capacitance detection error will be. The impact of the voltage utilization rate on the monitoring accuracy is further illustrated in Fig. 5.19(c). It can be seen that the capacitance estimation error decreases inversely proportionally with the increase of the voltage utilization percentage. It validates also the positive impact of high SM voltage utilization rate on the measurement accuracy. Moreover, higher ADC resolution can slightly improve the estimation accuracy. However, the commonly used 12 bits ADC is good enough compared with the available voltage sensors, whose accuracy is actually a bottleneck of the whole measurement system.

Table 5.5: Combination of capacitors to emulate capacitance drop. Source: [J4]

[uF]	C_{sm}	C_2	C_3	C_4	C_{m}	Capacitance drop
C_{rated}	1640	22	22	10		
C_{cap1}	*	*	*	*	1694	0%
C_{cap2}	*	*		*	1672	1.30%
C_{cap3}	*	*			1662	1.90%
C_{cap4}	*				1640	3.20%

5.3.4 Experimental Validation

A 15-kVA three-phase MMC platform is shown in Fig. 5.6. There are four SMs in each arm. Phase-shifted carrier modulation is used to control the MMC with the carrier frequency being 3.0 kHz. The DC bus voltage is 600 V, and the average voltage is 150 V for each SM. To demonstrate the effectiveness of the proposed RSB method, the upper arm of phase C is chosen with two lower SMs (SM_3 and SM_4) being the reference and the monitored SMs, respectively. The other two SMs (SM_1 and SM_2) function to support the DC bus voltage and to track the arm voltage reference. Moreover, several capacitors having small values (e.g., C_2, C_3, and C_4 listed in Table 5.5) are connected

in parallel with the original SM capacitor C_{sm}. When disconnecting one or several of them from a large SM capacitor, the capacitance drop due to the degradation can be emulated. The SM voltage measurement accuracy is 0.1% with the 100 V rated SM voltage defined for the CM purpose.

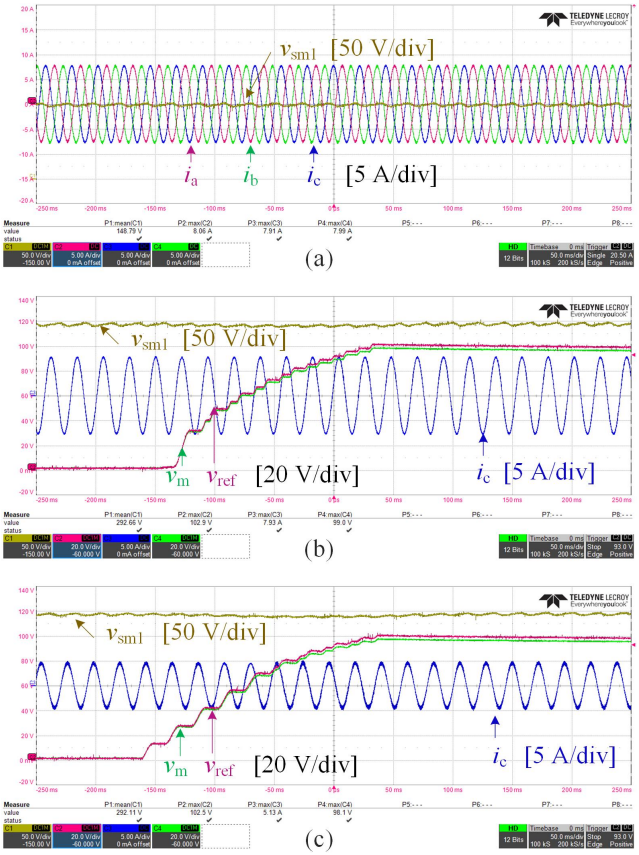

Fig. 5.20: Waveforms of SM_1's voltage, output current of phase C and voltages of reference and monitored SMs under different loading conditions: (a) 3 kW, (b) 3 kW, and (c) 1 kW. (See Fig. 5.12, where i_a, i_b and i_c are the three phase output currents; v_{sm1} is the voltage of SM_1; v_m and v_{ref} are the voltages of the monitored SM and the reference SM.) Source: [J4]

Fig. 5.20(a) shows the experimental waveforms of the three phase output current and the voltage of SM_1 prior to CM process. The three phase currents are 50 Hz sinusoidal waveforms, and the average voltage of SM_1 is about 150 V, which is the result of 4 SMs supporting the DC bus voltage. During the CM process, SM_3 and SM_4 are bypassed first then inserted with increasing voltage as shown in Fig. 5.20(b) and (c). In this case, SM_1 and SM_2 are working to support the DC bus voltage with the average of roughly 300 V.

A voltage difference can be observed from the voltage of SM_3 and SM_4 due to their capacitance difference. Moreover, two different loading conditions (i.e., 3 kW and 1 kW in Fig. 5.20(b) and (c)) are applied to verify that the proposed RSB method is independent of the power loading condition of the MMC since both SMs can be charged to the rated voltage.

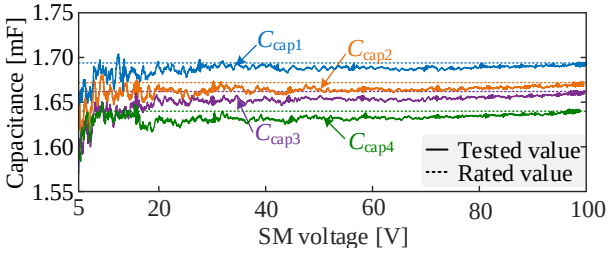

Fig. 5.21: Measured SM capacitances (see Table 5.5) under different SM voltages. Source: [J4]

In addition, a series of experiments with different capacitances listed in Table 5.5 are conducted to show the accuracy of the proposed RSB method. The experimental results are shown in Fig. 5.21. In the low SM voltage range (e.g., 5-20 V), the estimated capacitance fluctuates significantly around its rated value. However, the estimation results tend to become stable and more accurate as the voltage increases.

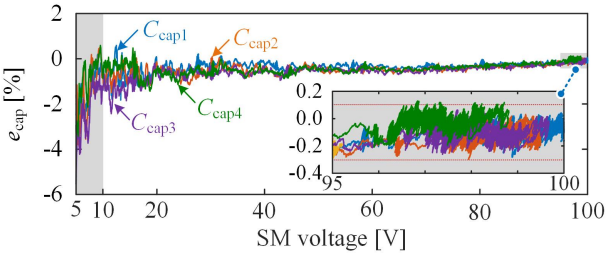

Fig. 5.22: SM capacitances estimation error under different SM voltages. Source: [J4]

The measurement error of the four testings are shown in Fig. 5.22. By dividing the SM voltage into 20 intervals (5 V per interval), the maximum error combining the four testings in each interval is shown in Fig. 5.23. It can be seen that when the voltage is lower than 15 V (equivalent to 15% SM voltage utilization rate), the capacitance detection error is higher than 2.4%, which agrees well with the result in Fig. 5.19(c). The lower the voltage is, the larger the error will be. Therefore, for the original RSB CM method utilizing SM voltage ripple below 10% of the rated voltage, the error larger than 2.43% will make it pretty difficult or even fail to detect the 5% capacitance drop of film capacitors at the end-of-lifetime. By contrast, the proposed method

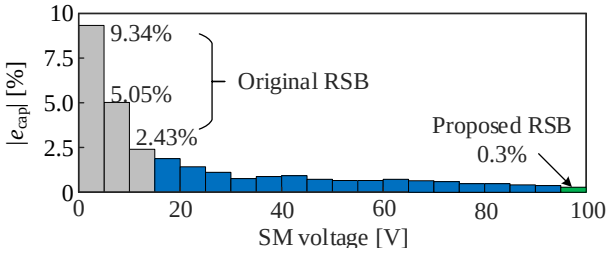

Fig. 5.23: SM capacitances estimation error under different SM voltages (RSB: reference SM based method). Source: [J4]

can achieve a monitoring error as low as 0.3% by utilizing the full SM voltage sensor range (100 V in this case study). It is in well agreement with the analytical result of 0.26% (10 bits) in Fig. 5.19(b). Additionally, since the proposed method is independent of the power loading condition of the MMC, ten or even higher times accuracy can be expected compared to the original RSB method when a lighter power loading is applied.

5.4 Summary

In this chapter, two SM capacitor condition monitoring approaches are proposed in order to schedule preventive maintenances with reduced repair time and operational cost of the MMC system. The first one is based on the DC-side start-up of the MMC. The principle of the method and several practical considerations regarding its implementation are discussed. The merits are summarized as below:

- No additional hardwares are required with no extra reliability issues being introduced into the MMC system.
- Condition monitoring can be done to all SM capacitances at one time and the measurement error can be reduced by averaging several testings at different time points $n\tau_{\text{equ}}$.
- No impact is posed on the normal operation of the MMC since the whole CM process is done during the start-up.
- Complicated controls and calculations are not involved.

The second one is based on reference SMs with a known capacitance. Besides its basic working principle, two reference SM topologies are proposed with reduced number of capacitors and its measurement circuit. Its advantages over the original RSB method have been discussed based on an accuracy analysis as listed below:

- The monitoring accuracy can be ten or more times that of the original RSB method.
- Be independent of the power loading condition of the MMC.
- Capacitances can be estimated directly from the measured instantaneous voltages without a detection of peak-to-peak voltages.
- Insignificant computational burden is introduced.

Chapter 6

Conclusion and Outlook

This chapter summarizes the research outcomes and contributions of this Ph.D. project- ***Mission Profile Based Control and Reliability Improvement Strategies of Modular Multilevel Converters***. The main contributions are highlighted and the research perspectives for future work are discussed.

6.1 Summary

The main research focus of this project is on the reliability improvement strategies for modular multilevel converters targeting especially two kinds of components prone to failure, namely the power semiconductors and the SM capacitors. This project investigates reliability improvement strategies by answering the overall research question: ***How to improve the reliability performance of modular multilevel converters by control and condition monitoring?*** In the following, a brief summary of this Ph.D. thesis is presented in terms of the three subquestions mentioned in Chapter 1.

- ***How to emulate the operation conditions of MMCs with a minimum viable down-scaled laboratory prototype used for model validation and reliability-related testing?***

In Chapter 2, an experimental platform, namely the MMC mission profile emulator, for both Ph.D. project research activities have been discussed. The full-bridge converter based current source in the setup is able to emulate real and practical current profiles of the MMC. The coupling inductor allows reactive power flow inside the emulator, which can significantly reduce the power requirement of the power supply in the current source. With the aid of an auxiliary SM, the current profiles and switching profiles of the SM under test are decoupled. Switching profiles with a wide range of practical switching frequencies of the MMC can be applied without deteriorating the

arm current harmonic performance. Moreover, since the voltage of the power supply in the current source is also decoupled with the high voltage of the capacitor C_2, the voltage of the power supply can be, theoretically as low as possible. Implementation considerations regarding the capacitor voltage control strategies, control parameters selection and hardware components sizing have been discussed. The impact of additional current ripples and the absence of capacitor voltage ripple on the power losses of the power modules are investigated. By demonstrating the capabilities, such as AC power cycling testing and electro-thermal model validation, the effectiveness of the proposed mission profile emulator is validated experimentally. Therefore, it can be seen that the proposed mission profile emulator can address the above research subquestion.

- ***How to improve the reliability performance of the modular multilevel converters from a control point of view?***

When it comes to the reliability improvement of power modules from a control point of view, it is always about re-distributing the power losses to actively influence the junction temperature of the targeted components with reduced thermal stresses, such as reduced junction temperature swing, reduced average junction temperature, less thermal cycles and so on. For MMCs, one specific problem is that the power losses are unevenly distributed among SMs. In order to mitigate its impact on the junction temperature discrepancy, the balanced conduction loss distribution benefiting from the capacitor voltage balancing control have been investigated in Chapter 3. The reasons for switching loss spread among SMs are discussed as well. Based on the above two analysis, SM-level power loss balancing control for the MMC has been proposed to reduce the power loss imbalance level among SMs. Besides, the overall thermal stress of all components in the MMC can be actively relieved to mitigate the impact from loading variations. In Chapter 4, in order to further improve the efficiency and the reliability performance of the MMC, dynamic carrier frequency is employed according to varied loading conditions. The carrier frequency boundary is investigated with respect to particular operation requirements including the output current THD and SM voltage ripple. In order to ensure the effectiveness of the proposed method, reliability evaluation is carried out. The performance comparison regarding power loss, junction temperature, and other electro-thermal stresses are conducted based on practical mission profiles. A case study based on a down-scaled three-phase MMC is demonstrated with sufficient experimental results comparison.

- ***How to improve the reliability performance of the modular multilevel converters from a condition monitoring point of view?***

Apart from the above reliability-oriented control strategies, condition monitoring can also contribute to enhancing the availability of the MMC system.

Instead of the power modules, monitoring another major component prone to failure in the MMC, namely the SM capacitors as mentioned in Section 1.1, is the main research focus in Chapter 5. One potential challenge regarding monitoring the health status of film capacitors in the MMC is its small capacitance value drop (e.g., 5%) at the end-of-life. The monitoring accuracy has to be high enough to capture the degradation trend of the capacitor. In this project, two condition monitoring strategies are proposed based on the DC-side start-up process of the MMC and reference SM with a known capacitance. Both methods contribute to improving the monitoring accuracy by taking full advantages of the SM voltage sensor measurement range. Experiments with different SM capacitances have been carrier out and the accuracy results illustrate the effectiveness of the proposed methods. The proposed condition monitoring methods can help schedule preventive maintenance and conduct the lifetime prediction of the MMC system as a whole. Therefore, less repair time and lower system operation cost can be achieved in general.

6.2 Main Contributions

Based on the research outcomes, the main contributions of this Ph.D. project are summarized as below:

- Voltage-decoupled mission profile emulator for power modules in MMCs

  In order to facilitate the reliability-related testing of the MMC in the two Ph.D. research activities, a mission profile emulator is proposed in this Ph.D. project. By taking advantage of a coupling inductor, the emulator can greatly reduce the power requirement of the power supply used in the current source by allowing reactive power flow. The voltage stabilizer implemented by an auxiliary SM is able to decouple the voltage of the power supply and that of the SM under test as well as the current profiles and switching profiles. Therefore, the voltage of power supply is independent of that of the SM, and a wide range of practical current profiles and switching profiles can be applied in this setup.

- Sub-module level power loss balancing control of MMCs

  The balanced sub-module level conduction losses due to the internal thermal balancing mechanism contributed by the capacitor voltage balancing are revealed in this project. The switching losses imbalance among SMs have been discussed as well, which is caused by the low switching frequency operation and parameter mismatch. In this regard, a sub-module level power loss balancing control is proposed. The imbalance of switching loss among SMs can be greatly improved to be

less than 25%, especially under pure reactive power loading conditions. The reduced thermal mismatch among SMs can enhance the reliability of the MMC system.

- Adaptive carrier frequency control for reliability improvement of MMCs

  By exploring the carrier frequency boundary with respect to particular output current THD and SM voltage ripple requirements, a changeable carrier frequency has been employed in this project according to different power loading conditions of the MMC. By doing so, the equivalent switching frequency is reduced with the drop of corresponding power loss and thermal stresses of the power devices. Simulation and experimental results show the effectiveness of the proposed method.

- Accuracy-enhanced SM capacitor condition monitoring for MMCs

  In order to improve the availability of the MMC system and to schedule preventive maintenance, two condition monitoring strategies for the sub-module capacitors are proposed in this Ph.D. project. One is based on the DC-side start-up of the MMC and the other is based on reference SMs with known capacitances. Both methods are able to achieve high monitoring accuracy due to the fully utilized SM voltage sensor measurement range. Meanwhile, no additional hardwares and no heavy computational burden extend the application scope of the two methods. Their effectiveness are validated experimentally.

6.3 Research Perspectives

Even though multiple aspects of the modular multilevel converters have been investigated in this project, new challenges still exist and need to be addressed in the future. Several possible research directions regarding MMCs are pointed out in the following.

- Mission profile emulator for both power modules and capacitors

  In order to facilitate the reliability testing of the power modules in the MMC, the project proposes the mission profile emulator with reduced power and voltage requirement of testing setup. However, as one of the major components, the reliability of SM capacitors are supposed to be paid attention to. Thus, it would be interesting to be able to conduct the reliability testing of the two kinds of components based on one common setup. Meanwhile, the advantages of esisting emulator should be better reserved.

- Full-scale testing of the MMC

Even through a mission profile emulator is proposed and validated to facilitate the SM-based testing of the MMC in this Ph.D. project, no testing based on practical SMs from full-scale MMCs is conducted. The electro-thermal behavior for high voltage power devices (i.e., used in the full-scale MMC) and for low voltage power devices (i.e., used in the laboratory emulator setup) can be different in terms of losses, thermal stresses and so on. Thus, full-scale testings should be further carried out and explored in the future.

- Component-level thermal imbalance

  This project focuses more on the sub-module level power loss balancing control to enhance the reliability performance of the MMC. However, the component-level thermal stress imbalance inside one SM has not been addressed. The inherent thermal imbalance among devices is caused by the existence of the DC arm current component and the difference between the thermal resistance of IGBT and diode chips. It could be interesting to investigate possible methods to sort this problem out under different loading conditions. Moreover, the thermal control in abnormal operation of the system, such as unbalanced grid, low voltage ride through and short circuit, can be investigated as well since the stresses in this case is more severe. Besides, experimental validations regarding the thermal loading and reliability performance of power modules have not been carried out.

- Condition monitoring methods without special operation mode

  The proposed methods are simple and easy to be implemented without heavy computational burden. However, the limitation lies in that none of them can achieve an accurate monitoring without special operating mode of the MMC. Thus, in order to make the CM method applicable and attractive to the industry, CM methods achieving high accuracy and requiring no special operation mode still need to be explored and investigated.

- System level reliability calculation

  Several reliability improvement strategies are proposed in this project. However, only the reliability of the power modules has been discussed in terms of the adaptive carrier frequency control. Thus, a system-level reliability analysis covering major components like power modules and capacitors as well as proposed reliability improvement strategies is required to ensure the reliability performance of the entire MMC system.

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