Grid Fault Responses of Voltage-Source Converters in Wind Turbine Applications

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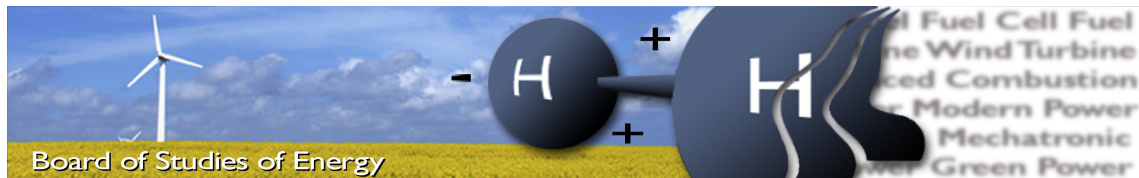STUDENT REPORT
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ABSTRACT:

With an increasing integration of converter-based power generation into the power system, concern regarding the stability and availability of future power systems has emerged. In order to address this, fault ride-through capability is required by installed generation to avoid a network collapse due to large disconnection of distributed generators. In addition, the interest in controlling grid-connected converters as synchronous generators is increasing, but little research has been done to uncover how such a control structure will perform during grid faults. Therefore, this project develops a state-of-the-art current-mode controller for a grid-connected converter and compares it to a described voltage-mode controller during both symmetrical and asymmetrical grid faults. It is shown that a voltage-mode grid-forming control structure, which emulates the principal parts of a conventional synchronous machine, can provide inherent grid-supporting functionalities, making it advantageous compared to a conventionally used current-controlled grid-following strategy. However, during grid faults, the fundamental principle of the grid-forming control makes a mandatory current limitation cumbersome. This project describes the advantages and disadvantages of the voltage-mode controller compared to the current-mode controller and proposes an enhanced grid-forming controller enabling the voltage-mode structure to be fully applicable for future control of grid-connected converters.

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Resumé

Med et globalt stigende elektrisk energiforbrug samt et ønske om en markant reduktion i nutidens CO_2 aftryk, kræves der nye løsninger i forhold til produktion og transmission af elektrisk energi i det nuværende og fremtidige elnet. For at erstatte fossile brændsler med vedvarende energikilder er der sket en stærkt forøgelse i antallet af nettilkoblede effektelektronikbaseret forsyninger. Dette inkluderer bl.a. integration af store land- og havvindmølleparker samt store solcelleanlæg. Især integration af vindenergi ses over hele verden, hvilket gør den til den mest modne teknologi indenfor de fluktuerende vedvarende energikilder. Den hastige kapacitetsforøgelse af vedvarende energikilder resulterer i de kommende årtier, i en stor andel af små distribuerede elforsyninger i forhold til konventionelt centraliseret elproduktion. Med et fremtidigt energisystem, baseret på effektelektronske løsninger, vil operationen af disse have en afgørende rolle i forhold til hvordan sådan et system skal opereres og kontrolleres således at systemet bevarer en høj pålidelighed samt en høj sikkerhed for forsyning til forbrugeren og industrielle belastninger. I dag er hovedparten af de installerede nettilsluttede konvertere opereret som en kontrollerbar strømkilde, som leverer aktiv effekt til el-nettet ved at synkronisere sit kontrolsystem til netspændingen. Disse konverterstrukturer kræver en veletableret og stabil netspænding for at operere korrekt. I fremtiden hvor store kulfyrede kraftværker ikke vil bidrage til denne stabile spænding må de installerede konvertere kontrolleres anderledes. Dette gælder ligeledes for nuværende systemer, hvor elnettet har en betydelig stor impedans, hvilket har en risiko for at mindske den stabile spænding. En metode som er ofte brugt i små alenestående systemer, er at operere den vedvarende energikilde som en kontrollerbar spændingsforsyning i stedet for en kontrollerbar strømforsyning. På den måde kan en eller flere enheder etablere en stabil spænding som andre strømregulerede forsyninger kan synkronisere sig til.

Med en udskiftning af antallet af store synkrongeneratorer vil den store kinetiske energi lagret i deres roterende masser forsvinde, hvilket vil medføre et elnet, som er mere sårbart overfor forstyrrelser såsom ændringer i forbrug eller store transiente forstyrrelser såsom kortslutningsfejl. Derfor er der nu et øget fokus på hvordan nettilkoblede effektelektroniske konvertere kan bidrage til at opretholde et stabilt system samt hvordan disse enheder skal kontrolleres under kortslutninger. For at højne elnettets stabilitet er der en øget interesse for hvordan spændingskontrollerede konvertere kan emulere en synkrongenerator hvormed et lignende respons, som i det kendte elnet kan etableres. En stor del forskning har undersøgt dette område og hvordan netværksstøttende regulering kan mindske systemets sårbarhed over for frekvens- og spændingsændringer. Dog er disse studier baseret på stationære tilstande og ikke på store transiente forstyrrelser. For at imødekomme et øget fokus for spændingskontrollede konvertere som kan emulere en synkrongenerator samt en øget frygt for udfald af elnettet efterfulgt af en kortslutningsfejl undersøger dette projekt hvordan spændingsregulerede kontra strømregulerede konvertere opfører sig under både symmetriske såvel som asymmetriske kortslutningsfejl inklusiv hvilke fordele og ulemper hver reguleringsstrategi indebærer. Efter en beskrivelse af den tilgængelige laboratorieopstilling, er hver reguleringsstrategi nøje gennemgået og de inkluderede

reguleringsløkker er beskrevet og designet.

De to reguleringsstrategier er verificeret under stationære tilstande hvor de er udsat for små forstyrrelser såsom en pludselig ændring i belastning, netfrekvens, netspænding, samt hvordan hver strategi opererer under en svag nettilslutning. Her er det vist at en spændingsreguleret strategi er stærkt overlegen den strømregulerede strategi med henblik på at støtte elnettet under diverse forstyrrelser. Desuden er det vist at den spændingsregulerede strategi kan operere under en særdeles svag nettilslutning, hvor den strømregulerede strategi er ustabil.

Angående store forstyrrelser er begge strategier udsat for en symmetrisk trefaset kortslutningsfejl samt to typer af asymmetriske kortslutningsfejl. Grundet at effektelektroniske konvertere har en beskeden margin i forhold til øget strømkapacitet, så har en spændingsreguleret konverter en fundamental ulempe når der sammenlignes med en strømreguleret strategi under fejlsituationer. Da en spændingsreguleret konverter er kontrolleret som en spændingsforsyning vil den strøm som reguleringssystemet behøver for at opretholde netspænding være mange gange større end den nominelle strøm, hvilket ikke er muligt for effektelektroniske konvertere. Derfor skal en spændingsreguleret konverter begrænse sin leverede strøm samtidig med at ydre reguleringssløjfer, som forbinder netspænding og netfrekvens med aktiv og reaktiv effekt, skal holdes under kontrol. Når dette er gjort, er det vist at en spændingsreguleret konverter kan gennemføre levering af aktiv og reaktiv effekt under symmetriske og asymmetriske fejl i overensstemmelse med godkendte netregulativer. Derudover har den et stort potentiale til at øge robustheden af fremtidens elnet sammenlignet med den nuværende strømreguleret strategi. I dette projekt er det vist hvordan den spændingskontrollede konverter kan give en øget robusthed under symmetriske netfejl. Dog har den foreslået løsning for den spændingsregulerede strategi stadig udfordringer i forhold til store transiente asymmetriske forstyrrelser. Det er derfor nødvendigt med yderligere undersøgelser omhandlende hvordan den foreslåede reguleringsstrategi kan generaliseres til at øge robustheden for spændingsregulerede konvertere under alle types af kortslutningsfejl.
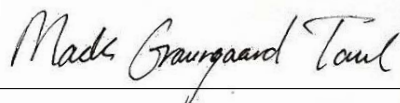
Preface

The following project is the work of a 3rd-4th semester student on the master program of Power Electronics and Drives at the Department of Energy Technology, Aalborg University. This project aims to describe present and new control strategies for grid-connected converter operation during grid faults as well as to investigate and discuss how such a fault control system can be realized for future control, which is expected to be based on voltage-mode grid-forming control.

The prerequisites for reading this project is a basic understanding of renewable energy sources including grid-connected converters, along with a developed understanding of engineering mathematics, electrical engineering including power electronics and classical control theory. As for the content, the author has made an effort to make it easy for the readers to familiarize themselves with the structure. This is done through leitmotifs in the form of short introductions and conclusions that will clarify what is examined in the forthcoming chapter and highlight the key points.

An acronym and nomenclature list are included in the beginning of the project. Throughout the project, citations are given with the IEEE Transactions style, i.e. a citation will appear in square brackets and a number will refer to the correct citation in the bibliography found as a last chapter in the project. Cross references to tables and figures are numbered after chapters, e.g. figure 1.1, for the first figure in chapter one. Equations are numbered after sections in a similar manner.

This project has been highly dependent on several software packages for different applications. MATLAB has been used for numerical calculations, coding, and figure development and MATLABs Simulink together with PLECS blockset have been used to make simulation models used to simulate normal operating conditions as well as fault responses of the described control strategies. For analytical derivations and calculations, the software Maple has been extensively used.

The appendices are found as an ending to the project report. They are included as a supplement to give the interested reader an insight into the laboratory setup as well as describing the basic theory for the analysis of asymmetrical systems.

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Acronyms

ADC	Analog to Digital Converter
BPSC	Balanced Positive Sequence Control
DFIG	Doubly-Fed Induction Generator
DG	Distributed Generator
DLG	Double Line-to-Ground
DSO	Distribution System Operator
DVC	Direct Voltage Controller
EMF	Electromotive Force
FFT	Fast Fourier Transform
FPNSC	Flexible Positive and Negative-Sequence Control
FPNSC+GCR	Flexible Positive and Negative-Sequence Control including Grid Code Requirements
FRT	Fault Ride Through
LCL	Inductor-Capacitor-Inductor
LVRT	Low-Voltage Ride-Through
PCC	Point of Common Coupling
PI	Proportional Integral
PLC	Power Loop Controller
PLL	Phase-Locked Loop
PMSG	Permanent Magnet Synchronous Generator
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Source
RPC	Reactive Power Controller
SCR	Short-Circuit Ratio
SLG	Single Line-to-Ground
SOGI	Second-Order Generalized Integrator

SPC	Synchronous Power Controller
SPWM	Sinusoidal Pulse Width Modulation
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
THIPWM	Third Harmonic Injection Pulse Width Modulation
TSO	Transmission System Operator
VCO	Voltage-Controlled Oscillator
VSC	Voltage-Source Converter
VSI	Voltage Source Inverter
VSM	Virtual Synchronous Machine
VUF	Voltage Unbalance Factor
WT	Wind Turbine
WTS	Wind Turbine System

Nomenclature

Symbol	Description	Unit
C_b	Base capacitance	$[F]$
C_{dc}	dc-link capacitance	$[F]$
C_f	ac-side filter capacitance	$[F]$
D_P	Droop coefficient for active power	$[kW/Hz]$
D_Q	Droop coefficient for reactive power	$[kVAr/V]$
D	Damping coefficient	$[N \cdot m \cdot s/rad^2]$
E_{dc}	Energy stored in the dc-link capacitor	$[J]$
E	Magnitude of virtual electromotive force	$[V]$
H	Inertia constant	$[s]$
I_{in}	dc-side input current	$[A]$
I_{lim}	Limit value of converter current	$[A]$
I_{nom}	Nominal converter current	$[A]$
J	Moment of inertia	$[kg \cdot m^2]$
K_i	Integral gain	$[-]$
K_p	Proportional gain	$[-]$
L_v	Virtual inductance	$[H]$
L_{cf}	Converter-side filter inductance	$[H]$
L_{gf}	Grid-side filter inductance	$[H]$
L_l	Transformer leakage inductance	$[H]$
P^*	Active power reference	$[W]$
P_G	Generator-side active power	$[W]$
P_e	Electrical power	$[W]$
P_m	Mechanical power	$[W]$
P_r	Remaining capacity for active power during fault	$[W]$
P_{WT}	Wind turbine active power	$[W]$
P_s	External setpoint of active power	$[W]$
P	Active power	$[W]$
Q^*	Reactive power reference	$[VAr]$
Q_G	Generator-side reactive power	$[VAr]$

Symbol	Description	Unit
Q_{max}	Maximum reactive power during fault	$[VAr]$
Q_s	External setpoint of reactive power	$[VAr]$
Q	Reactive power	$[VAr]$
R_v	Virtual resistance	$[\Omega]$
S_F	Fault signal	$[-]$
S_n	Rated Power	$[VA]$
S_{abc}	Converter switching signals	$[-]$
T_d	Time delay	$[s]$
T_s	Sampling period	$[s]$
V^+	Magnitude of positive-sequence voltage	$[V]$
V^-	Magnitude of negative-sequence voltage	$[V]$
V_b	Rated voltage (l-l rms)	$[V]$
V_{dc}^*	dc-link voltage reference	$[V]$
V_n	Rated peak voltage of phase-voltage	$[V]$
V_{pu}	Per unit value of point of common coupling voltage	$[-]$
V_{sag}	Sagged voltage during fault	$[V]$
Z_S	Source impedance	$[\Omega]$
Z_b	Base impedance	$[\Omega]$
Z_L	Line impedance	$[\Omega]$
Z_{fe}	Feeder impedance	$[\Omega]$
α_c	Bandwidth of current controller	$[rad/s]$
δ	Power angle	$[rad]$
γ	Rotation angle for elliptical current reference	$[rad]$
$\hat{I}$	Peak value of phase current	$[A]$
ω_0	Nominal electrical angular frequency	$[rad/s]$
ω_{LC}	Resonant angular frequency of grid-side LC filter	$[rad/s]$
ω_N	Undamped natural angular frequency	$[rad/s]$
ω_c	Critical angular frequency	$[rad/s]$
ω_r	Resonance angular frequency of LCL filter	$[rad/s]$
ω	Electrical angular frequency	$[rad/s]$
ϕ^+	Phase angle of positive-sequence voltage	$[rad]$
ϕ^-	Phase angle of negative-sequence voltage	$[rad]$
ϕ_h	Lead phase angle	$[rad]$

Symbol	Description	Unit
ϕ_m	Phase margin	$[rad/s]$
θ_{PCC}	Phase angle of PCC voltage	$[rad]$
θ_{PLL}	Phase angle of Phase-Locked Loop	$[rad]$
ζ	Damping ratio	$[-]$
d_{abc}	Three-phase duty cycles	$[-]$
e	Virtual electromotive force	$[V]$
f_0	Nominal electrical frequency	$[Hz]$
f_{bw}	Bandwidth frequency	$[Hz]$
f_r	Resonance frequency of LCL filter	$[Hz]$
f_{sw}	Switching frequency	$[Hz]$
f_s	Sampling frequency	$[Hz]$
f	Electrical frequency	$[Hz]$
h	Harmonic order	$[-]$
i_{PCC}	Current at point of common coupling	$[A]$
i_{dc}	dc-link current	$[A]$
i_f	Converter current	$[A]$
i_g	Grid current	$[A]$
i_{sd}	Stator-side direct axis current	$[A]$
i_{sq}	Stator-side quadrature axis current	$[A]$
k_1	Control ratio between sequence component voltages and active power	$[-]$
k_2	Control ratio between sequence component voltages and reactive power	$[-]$
s	Laplace variable	$[-]$
t_r	Rise time	$[s]$
u_{sd}	Stator-side direct axis voltage	$[V]$
$v_{\alpha\beta}$	Stationary-reference frame voltage components	$[V]$
v_{dc}	dc-link voltage	$[V]$
v_g	Grid voltage	$[V]$
v_{inv}	Inverter Switching Voltage	$[V]$
v_{pcc}	Voltage at point of common coupling	$[V]$
z	Discrete variable	$[-]$

Contents

Appendix

1 Introduction to Power Electronics-based Power System

A globally increasing electrical energy consumption imposes higher requirements for power system transmission capacity together with an increased demand for electricity production. This, together with the negative environmentally effects associated with high CO_2 emissions, have introduced a cooperative goal of achieving a 100% renewable and sustainable energy system [1]. To accommodate such an agenda, a high penetration of Renewable Energy Sources (RESs) such as Wind Turbine Systems (WTSs) and Photovoltaic (PV) solar farms have emerged into modern power grids. Especially, the integration of wind power is seen all over the world making it the most mature RES harvested today besides hydroelectric power plants [2]. The total installed capacity of wind power world wide is today around 650 GW with an expected increase to 840 GW by 2022 [3]. To that end, as an example, the wind power share of the total electricity generation in Denmark in 2017 and 2018 was more than 40% [4].

The rapid increase in capacity of RES, will cause a high share of distributed power generation compared to centralized power generation in the next few decades [5]. Future power electronic-based power systems interfaced with large- and small-scale wind farms, PV plants and micro-grids completely alter the way of operation compared to a power system based on large centralized power plants. Additionally, with remote generation and high converter-based transmission, issues of connection points with a varying and low Short-Circuit Ratio (SCR) may be encountered. Since power electronic converters act as an interface between RES-based Distributed Generators (DGs) (e.g. Wind Turbines (WTs)) and the grid (as shown in Figure 1.1), the control strategy employed by the converters dominates the behavior, performance, and power quality of the grid. In other words, it is the control strategy and not the converter topology and physical properties, which determine the dynamic performance of such systems. This is in direct contrast to the well-known behavior of synchronous machines where the dynamic response is dictated by
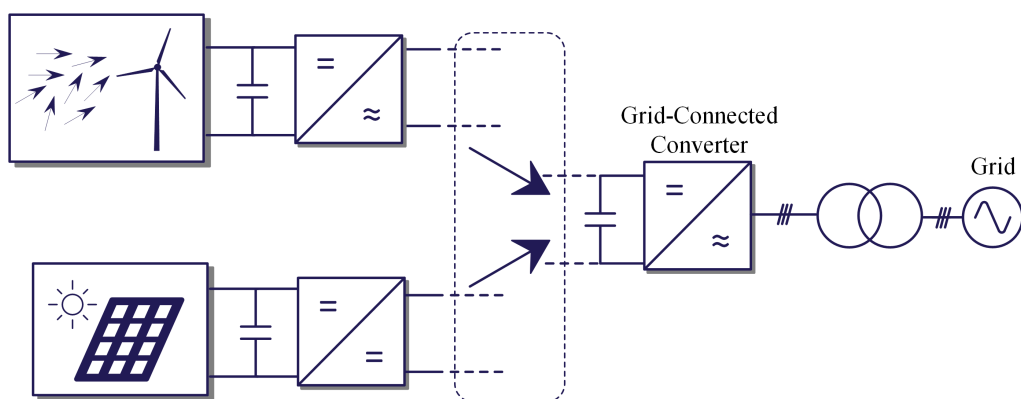

Figure 1.1: RES interfaced with power electronic converters.

the physical properties of the system, such as electrical damping and mechanical inertia [2]. This fact has drawn a large interest in research of converter control objectives, since one can control the converter to comply with certain grid requirements and higher levels of intelligent grid functionalities [6]. Besides increased controllability introduced by converter-interfaced RES, several challenges occur as well. In high penetration levels of RES, the enormous buffer of energy stored as rotational energy in the large synchronous generators of the conventional power plants will be significantly decreased or almost lost [7, 8]. This implies that the large support of energy delivered by synchronous machines during transients such as fault events will no longer be present in the same quantity as previously encountered. Hence, the capability for a system to ride through disturbances while maintaining a stable voltage and frequency is reduced and a high share of DGs has resulted in Transmission System Operators (TSOs) and Distribution System Operators (DSOs) issuing further requirements in the grid codes, where a certain behavior and performance during grid abnormalities and fault situations are required for grid-connected converters. The remainder of this chapter describes the fundamental prerequisites necessary to be familiarized with the state-of-the-art WTSs and their control. To that end, a large effort is devoted in describing the different controller possibilities for the grid-connected converter alongside the definition of grid-following and grid-forming converters. At last, power system faults and their respective voltage sag profiles are reviewed in addition to grid code requirements and standards for grid-tied converters. These will lay the foundation for the problem formulation and the subsequent parts of this project report.

1.1   Wind Power Fundamentals

During the last decades renewable energy has increased significantly in installed capacity. PVs and WTSs are the fastest growing resources where offshore wind farms are installed globally in a greater number than ever [9]. Besides the increased attention in wind power, bleeding edge technology has allowed for WTs with a power capacity of 12 MW [10]. This together with improvement in conversion efficiency and lower production costs, have paved the way for WTs being common property for most countries today. In addition to an increasing installation of onshore WTs, large-scale offshore wind farms have become a viable solution especially in the nordic european countries due to higher wind speeds and therefore higher energy production, no limit for available installation area, and no public concern regarding its audible and visual impact on the environment [11]. However, this comes with the cost of a high installation and maintenance cost together with the inconvenience of installing high-voltage substations and offshore switchgear alongside to finally transport the harvested energy via a submarine cable to land.

In order to transform the mechanical power in the turbine rotor to electrical power, an electrical machine is used. For large-scale WTs with an output power of several MW, the rotational speed of the rotor is low and a physically large and bulky generator is necessary to harvest the energy. Instead, a gearbox is often used to increase the rotational speed and decrease the mechanical torque on the generator rotor, which in turns reduces the size of the generator [1]. The most frequently adopted WTS includes a Doubly-Fed Induction Generator (DFIG) using a partial-scale power electronic converter. The stator windings of the DFIG are directly connected to the grid and the power electronic interface is only used on the rotor-side windings. This configuration has the advantage of a cost-effective

solution since the needed power rating for the back-to-back rotor-side converter only needs to be around 30% of the WT power rating. Disadvantages of this solution is that it has less controllability of the system compared to a full-scale power electronic solution [12] and it is vulnerable to disturbances in the grid [13]. Furthermore, since the maintenance of offshore turbines is highly undesireable, a replacement of DFIGs with low-speed direct-drive Permanent Magnet Synchronous Generators (PMSGs) eliminates the need for gearboxes, which significantly reduces the maintenance cost of the wind farm turbines [14, 15]. In terms of the overall system reliability, it is hard to directly state whether a type-IV WTS will enhance the reliability compared to a DFIGs-based WTS seen from the converter point of view [16]. However, the WT failure is often related to issues with the mechanical drive train. Therefore, a type-IV WTS may in this context be considered as more reliable. From this, the studied WTS for this project will be equipped with PMSGs and a full-scale back-to-back power converter, i.e. a type-IV WTS.

1.1.1 Fundamental Operation of a Type-IV WTS

The WT considered is equipped with a PMSG and a full-scale power converter topology. The converter topology considered will be a two-level Voltage-Source Converter (VSC) installed in a back-to-back configuration. This subsection has the purpose of describing the main control objectives for a grid-following type-IV WTS and clearly stating assumptions used to simplify the considered task.

The back-to-back converter topology is divided into two control structures, namely the control of the machine-side converter and the control of the grid-side converter, see Figure 1.2. Both converters are equipped with vector current control in order to achieve decoupled control for the active and the reactive powers.

The machine-side converter is responsible for controlling the generator and the pitch system. Here, the generator is controlled by regulating the electromagnetic torque to ensure maximum power extraction from the turbine at a given wind speed [15]. A maximum power point tracker is used to control the rotor speed and the pitch angle of the turbine to ensure an optimal tip-speed ratio at all operating points. According to the theory of Betz, the
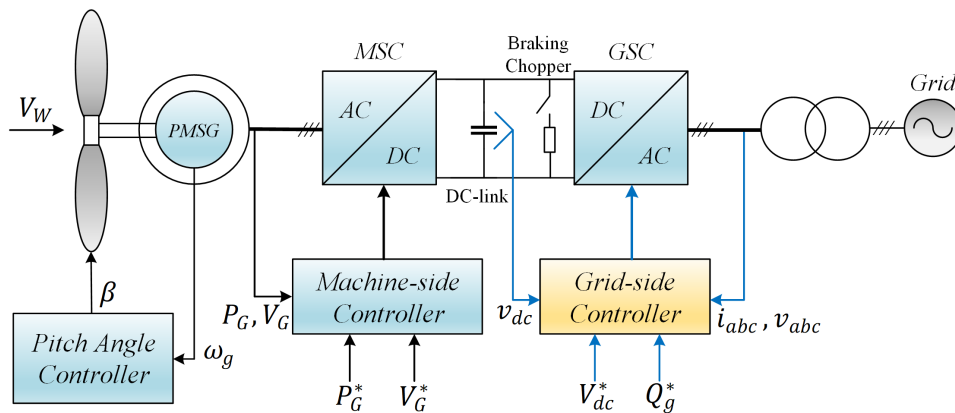

Figure 1.2: Control structure of type IV WT showed in a simplified electrical diagram. Only the grid-side controller will be considered in this project.

mechanical power harvested by a WT from the available wind is

$$P_{WT} = \frac{1}{2}\rho\pi R^2 V^3 C_p(\lambda, \theta) \tag{1.1.1}$$

where ρ is the air density, R is the radius of the circumference made by the WT blade rotation, V is the wind velocity and C_p is the non-linear power-coefficient dependent on the tip-speed ratio and the pitch angle of the blades [17]. According to the measured wind speed, the rotor speed of the turbine and the pitch angle of the blades can be adjusted to maximize the generated power from the WT. Furthermore, the pitch angle controller regulates the pitch of the rotor blades in order to limit the rotational speed of the WT in the case of strong winds and to protect the mechanical parts from overloading and excessive stress.

Control of Machine-Side Converter
Besides maximizing the active power production by controlling the wind turbine rotor speed, the machine-side converter is often controlled using *constant stator voltage control* or *unity power factor control.*

For the *constant stator voltage control*, the stator voltage is controlled to only include its *d*-axis component [14], which means that the stator voltage is not dependent on the angular speed of the machine. Using this, it is ensured that the generator always operate at its rated voltage and the active and reactive power can be controlled by the *dq*-axis currents as

$$P_G = \frac{3}{2}u_{sd}i_{sd} \quad Q_G = -\frac{3}{2}u_{sd}i_{sq}, \tag{1.1.2}$$

where u_{sd} is the stator voltage controlled in Figure 1.2. By using this control structure the generator requires reactive power, which increases the necessary converter rating [18]. In Figure 1.2, constant stator voltage control is shown for the machine-side converter where the nominal stator voltage is maintained by regulating the reactive power.

The unity power factor control aims to maximize the active power production while controlling the reactive power to zero. Using this method, the *d*-axis current regulates the reactive power while the active power is regulated by the *q*-axis current component. Besides these, other control methods for the machine-side controller include optimal- and direct-torque control [19] as well as maximum torque per ampere control [20]

The grid-side converter has the control objectives to regulate the dc-link voltage and the reactive power injected into the grid. Alternatively, the grid voltage can be controlled instead of the reactive power. By regulating the dc-link voltage, the active power will be balanced between the harvested power from WT and the injected power into the grid. Hence, in case of an increase in the dc-link voltage, an additional amount of active power will be injected to the grid for balancing. During normal operation, the reactive power is controlled to zero, whereas during fault conditions, Low-Voltage Ride-Through (LVRT) requirements determines the active and reactive power to be injected into the grid. For fault situations where the grid voltage suddenly drops, the active power is correspondingly decreased instantaneously. As a result of that, the dc-link voltage will increase due to the rotational energy stored in the WT rotor. To prevent the voltage from reaching dangerous

high values, a chopper circuit is controlled to dissipate the power accumulated in the dc-link during faults. The control structures of the machine-side converter and grid-side converter can be seen in Figure 1.2, where the grid-side controller is highlighted with yellow.

Due to the dc-link between the back-to-back converter configuration, the grid and generator sides can be considered decoupled and the two converters can be analyzed and controlled independently. Throughout this project, only the grid-side converter will be considered, whereas the WT, generator, and machine-side converter are considered as a constant current source.

1.2 Control of Grid-Side Converter

Fundamentally there are two types of converter control structures for the grid-side converter: grid-following and grid-forming converters [2, 21].

1.2.1 Grid-Following and Grid-Forming VSIs

Grid-following converters are by far the most utilized control structure for grid-connected RES due to its independent control of active and reactive power and its ability to limit the converter current [22]. Its control system comprises a Phase-Locked Loop (PLL) used to estimate the phase angle of the grid voltage. The phase angle is used together with outer power loops to construct a desired current reference, often regulated to be in phase with the grid voltage vector to inject active power to the grid. In this way, no matter if the desired current injection is active or reactive, it is developed according to the grid voltage at the converter terminals, hence this control structure is said to be grid-following. An example of a grid-following control structure without outer power controllers is depicted in Figure 1.3 a).

This type of converter control obviously requires "stiff" three-phase voltages at its terminal for proper operation. With the presence of large synchronous generators which control a stiff voltage with negligible voltage and frequency deviation, this requirement is satisfied and the converters will operate as grid-following current sources and can be represented as current sources with large parallel impedances [23]. However, as the share of converter-based generation increases, this assumption will no longer be valid and grid-following converters would need a grid-forming component to dictate the network voltage and frequency. Furthermore, the widely utilized control structure of a grid-following converter is somewhat restricted to the operation of strong grids as explained above, implying that stability of grid-following converters are at risk for weak-grid connections, which is the case for many offshore wind farms or fault events in general [24–26]. This destabilizing effect of grid-following converters operated in weak-grid conditions originates as a positive feedback path in the PLL and converter operation [25, 27]. Also as concluded in [28, 29], the PLL has a negative effect on the transient performance of the converter and will introduce negative resistance characteristics in the small-signal dynamics, which further threatens the stability. In summary this means that for a converter-based power system, grid-forming converters are necessary in order to regulate the grid voltages and frequency in a decentralized manner.

An example of a grid-forming control structure is shown in Figure 1.3 b). Here no PLL
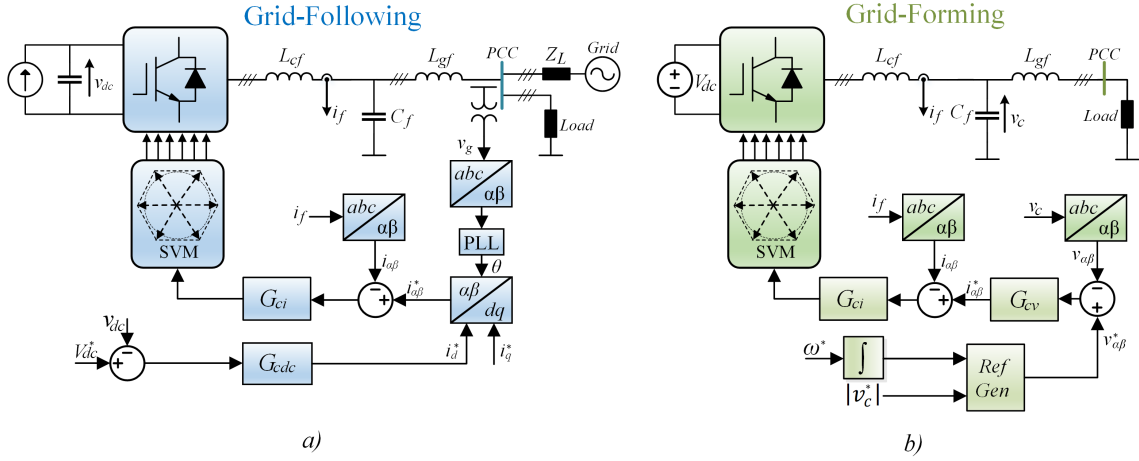
Figure 1.3: Fundamental structure of converter control operated in grid-following and grid-forming mode. The control block diagram of grid-following operation is shown in a) and the control block diagram of grid-forming operation is shown in b).

is needed since the converter will dictate the frequency and voltage magnitudes by itself. Hence, for this structure, the current is controlled indirectly using the voltage. A grid-forming converter can be represented as a controlled voltage source with a low series output impedance. In order to achieve a 100 % renewable energy system dominated by power electronic converters, grid-forming converters are desired to possess different features in order to successfully replace conventional synchronous generators and support the formed grid voltage and frequency [2]. Such features are categorized as grid-supporting features, which in general can be applied as an extension to either grid-following and grid-forming converters [6] in the form of e.g. droop control and virtual inertia emulation.

Utilizing grid-forming converters with grid-supporting functionalities enable parallel operation with equal power sharing without the need for an external communication protocol [6]. This kind of behavior is not possible with just paralleled voltage sources. Even though the control objective of the converters in general can be divided into grid-following and grid-forming converters, grid-connected converters are obliged to be grid-friendly. Thus, grid-supporting functionalities might be necessary in grids where synchronous machines are low in number, such as in ac microgrids or in weak-grid connections including low-voltage grids and fault events.

1.2.2 Grid-Supporting Converters

The following section has the purpose of describing the underlying structure of the grid-supporting converter either based on a grid-following or a grid-forming converter. Furthermore, a review of the different grid-supporting functionalities within the field of grid-following and grid-forming converters are given. This include droop control, the Synchronous Power Controller (SPC), and inertia emulation such as the Virtual Synchronous Machine (VSM).

Figure 1.4 depicts a conventional grid-following converter with its control structure. It is basically developed around one inner current loop used to regulate the injected grid current and two outer loops used to determine the current reference in order to obtain a

desired active and reactive power as well as maintaining a constant dc-link voltage.

To allow grid-following converters to support the grid frequency and voltage, the active and reactive power references are adjusted as for the case of synchronous machines. This is done using droop control where the steady-state operation set points of the converter are set according to the frequency and voltage deviation from the nominal values and the predefined droop settings (k_P and k_Q) [30]. The frequency and voltage regulations using droop control are depicted in Figure 1.5. As it can be seen, the active and reactive power references are adjusted proportional to the error in the frequency and amplitude of the grid voltage.

A grid-forming converter in the form as shown in Figure 1.3 b) is usually not applied to support the grid voltage and frequency. Such a structure often involves outer controllers specified by the grid code to enhance the supporting functionalities and enable the load sharing. Consequently, it is auspicious for grid-forming converters to acquire grid-supporting objectives, which contribute to improve the voltage quality. An example of this is droop regulation as described for grid-following converters where the injections of active and reactive power are modified with the purpose of maintaining the amplitude and frequency of the voltage close to nominal values. Such droop regulation is shown as an example in Figure 1.6.

As the conventional grid is dominated by synchronous generators, implementing power converters, which possess similar behavior is advantageous. This is due to the fact, that synchronous machines are seen to remain synchronized by means of a transient power transfer in circumstances where vector-controlled grid-following converters lose stability [31]. Even though the droop control is used to mimic the behavior of synchronous generators by adjusting the active and reactive power references proportional to the grid voltage and frequency, this control only emulates the static behavior of a synchronous generator. In order to attain dynamic and transient similarities as well, the electromechanical characteristics of a synchronous machine should be included in the converter control. Doing so, advantages like provision of inertia, robust weak-grid performance, unbalanced voltage
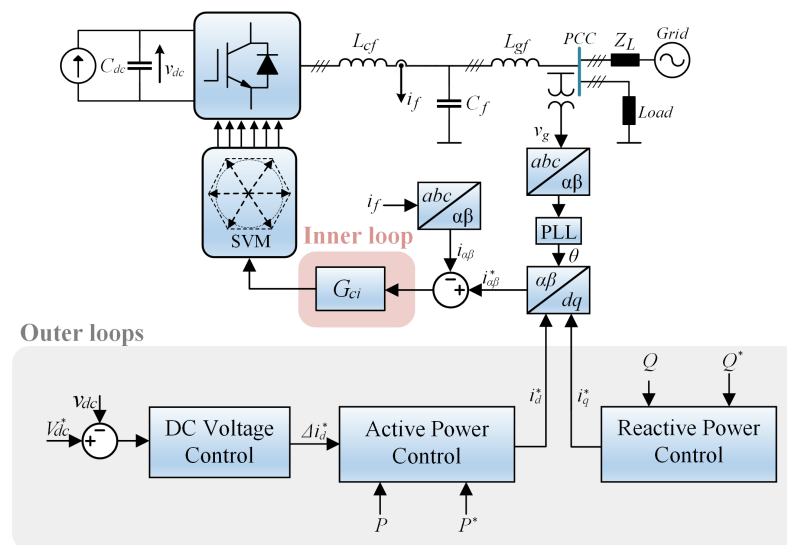

Figure 1.4: Fundamental control structure for a three-phase grid-following converter with outer power loops and an inner current loop.
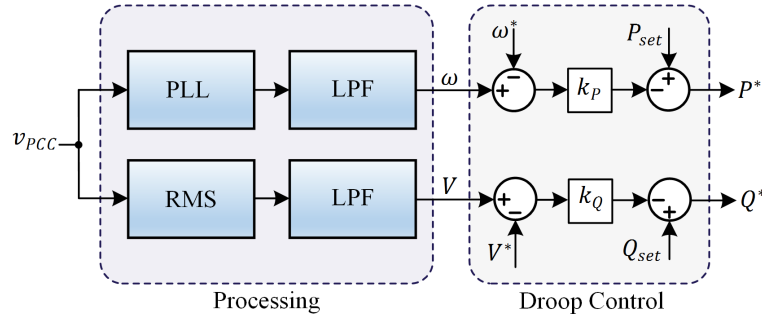
Figure 1.5: Active and reactive power reference regulation using voltage and frequency droop control, which provide the power references to the structure in Figure 1.4. LPF: Low-Pass Filter, RMS: Root-Mean-Square.
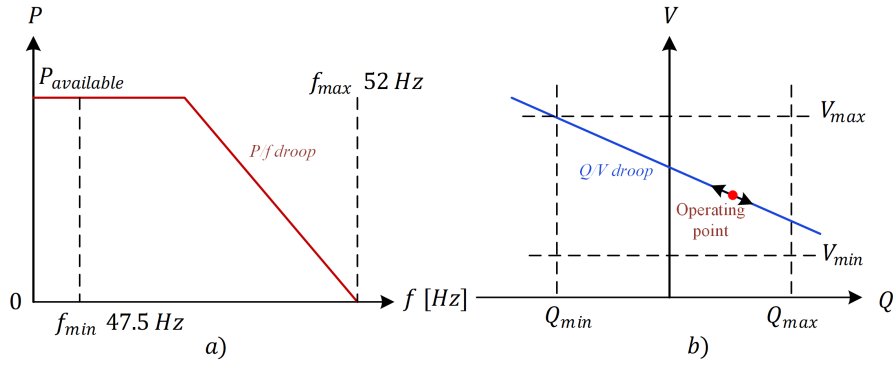

Figure 1.6: Example of grid code requirement for droop control. a) P/f droop control for frequency support. b) Q/V droop control for voltage support.

support and inherent load sharing associated with synchronous machines can be obtained using power converters [32]. To that end, recent grid codes require a synthetic inertia response of grid-connected converters [33], which has further motivated the development of inertia emulation through VSMs. The main idea of a VSM is to control the converter to attain the essential behavior of a synchronous machine by, to some extent explicitly involving the governing differential equations of a synchronous machine within the converter control [34]. Depending on the complexity needed, the machine model varies from a second-order model to a seventh-order model including damper windings together with transient and sub-transient reactances. Often the inertia emulation is implemented as a formulation of the well known swing equation. Three types of provision of synthetic inertia is discussed in this project based on [32], which includes a comprehensive literature review on this specific topic.

1) The first type which is directly applicable for a grid-following converter is to introduce an additional control loop linking the PLL frequency with the active power output of the converter in order to emulate the damping power and inertia response of a synchronous machine [35]. The change in active power reference is a function of the estimated PLL frequency expressed as

$$\Delta P = -k_{vi}\frac{df}{dt} + k_{vd}f(f_0 - f),\tag{1.2.1}$$

where f is the estimated PLL frequency, f_0 is the nominal frequency, k_{vi} is the virtual inertia constant, and k_{vd} is the virtual damping constant. For this control structure, the dc-link voltage controller can be omitted. Alternatively, the inertia emulation could be introduced in the dc-link voltage controller by modifying the dc-link voltage reference as

$$V_{dc}^* = \sqrt{\frac{4 S_n H}{C_{dc}} \left(\frac{f}{f_0} - 1 \right) + V_{dc0}^2}, \tag{1.2.2}$$

where S_n is the nominal power, C_{dc} is the dc-link capacitance, H is the synthetic inertia constant, V_{dc0} is the operating point of dc-link voltage and f is the estimated PLL frequency [36]. Hence, if the estimated frequency is higher than the nominal frequency, the dc-link voltage is increased causing the injected active power to be reduced in the grid side such that the frequency will decrease. The emulation of inertia in this way has the advantage of easy implementation in a conventional grid-following control structure. Unfortunately, both methods are still dependent on the stability of the PLL and the method shown in equation (1.2.1) needs an implementation of the derivative of the frequency, which is noise sensitive.

2) Instead of introducing an additional control loop, emulation of inertia can be introduced in the PLL structure itself [37]. This is shown in Figure 1.7, where E is the amplitude of the virtual electromotive force, X is the virtual machine reactance, ω_0 is the nominal grid angular frequency, and J is the virtual moment of inertia. This structure is similar to a PLL without any proportional gain and the synchronization of the converter is performed in a similar way as for a synchronous machine by regulating the active power accordingly. This type has similar advantages as for the additional loop, namely easy implementation for a grid-following control structure.

Nevertheless, this type of converter is still grid-following and needs a predefined grid voltage for proper operation, which is not the case for a synchronous machine (which is the aim to emulate). To accommodate this challenge, the output impedance defining the electrical characteristics (inherent power sharing and voltage droop) together with the mechanical characteristics resulting in desired dynamic behavior are introduced into a grid-forming control structure, which is the third class of structures included here.
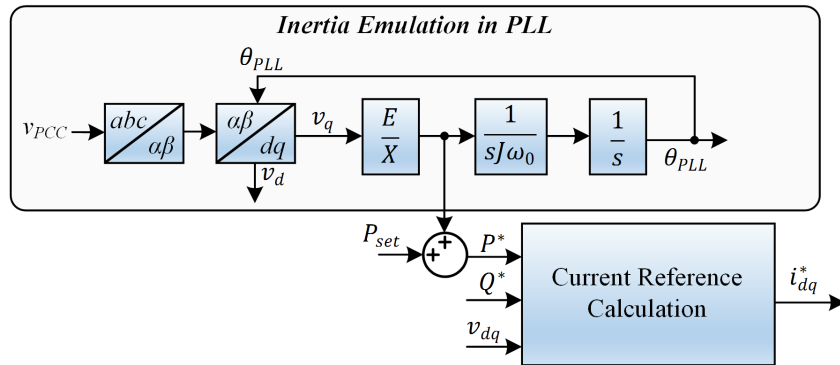

Figure 1.7: Inertia emulation by modifying the PLL structure of a grid-following control structure. E is the amplitude of the virtual electromotive force, X is the virtual machine reactance, ω_0 is the nominal grid angular frequency and J is the synthetic moment of inertia [32, 37].

Different control structures exist, which mainly differ in the way the inner control loops are developed. Here, two different control structures will be described, which only differs in the way the current reference is generated.

3) In the first structure (Figure 1.8), the internal control is realized by a cascaded voltage and current controller [34, 38]. The droop control is used to calculate the reference value for the voltage amplitude and frequency where a Voltage-Controlled Oscillator (VCO) integrates the angular frequency to get the phase angle, which together with the voltage amplitude is used to construct the electromotive force of the virtual synchronous machine expressed in either abc or $\alpha\beta$ domain. A Proportional Integral (PI) or Proportional Resonant (PR)-based voltage controller determines the current references, which are fed to the current controller. In order to protect the converter against over-currents, the output current reference of the voltage controller must include a limiter.

As shown in [34], the small-signal behavior of droop control is identical to the small-signal dynamics of the swing equation. Hence this structure is also included here as a method of inertia emulation. The P/f and Q/V dependency needed for the droop control to be accurate is derived based on the assumption that the grid network is highly inductive. This is true for medium-voltage and high-voltage grids but can in some cases including connections to low-voltage grids be violated. Typically, to circumvent this problem, a virtual impedance is including in the control loop (see Figure 1.8) to regulate the voltage reference in such a way that the output impedance seen from the converter is highly inductive. It should be noted in Figure 1.8, that the active and reactive power references are obtained based on the linear droop principle as shown in Figure 1.5. The second control structure is the Synchronous Power Controller (SPC), which is depicted in Figure 1.9 [39]. To overcome the negative effects associated with the PLL during weak-grid conditions, as for the structure shown in Figure 1.8, the SPC uses the internal synchronization mechanism in ac networks similar to synchronous machines and most VSMs. This inherent synchronization structure is obtained by using a regulator of the active power error (Power Loop Controller (PLC)) to generate the synchronization angle/frequency and a Reactive Power Controller (RPC) is used to regulate the amplitude of the voltage reference [24]. The disadvantage of this structure compared to a vector-controlled grid-following converter is that the converter ac current is not directly controlled, which needs to be limited in the case of a fault event. For the SPC shown in Figure 1.9, the mechanical characteristics of the VSM is defined in the PLC whereas the fast electrical
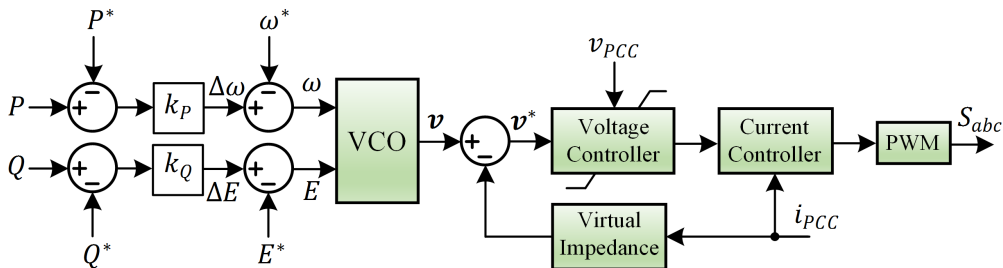

Figure 1.8: Control block diagram of cascaded control structure of a grid-forming voltage-controlled converter including droop control and virtual impedance to regulate the output impedance.
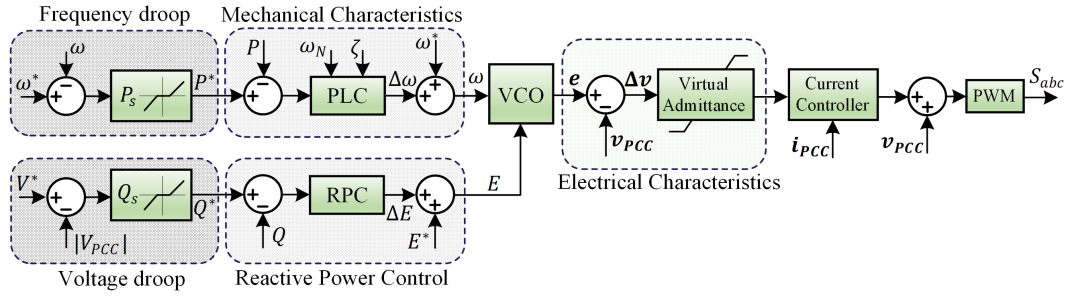
Figure 1.9: Control block diagram of synchronous power control. The PLC (Power Loop Controller) regulates the frequency dependent on the active power change from the droop controller with defined natural oscillating frequency and damping coefficient.

characteristics of the synchronous machine is emulated in the voltage controller which for this structure is the virtual admittance of the virtual machine. Thus, the SPC structure shown in Figure 1.9 has the advantage of being able to operate both in stand-alone and grid-connected mode while supporting the grid in a similar way as conventional synchronous machines. Due to this and some advantages described later, the SPC will be considered grid-forming voltage-controlled structure for this project.

Now that the control structures of the grid-following and the grid-forming converters have been described, it is needed to understand the conditions they may experience during grid faults and how they should respond to this. To do this, the following sections aim to describe why and how grid faults occur in the power system as well as reviewing the requirements that converters must comply with during such events.

1.3 Faults in Power Systems

Analysis of power system faults are very important regarding insulation coordination together with design and control of machines, circuit breakers and protection coordination. To that end, faults could jeopardize the overall system stability and may lead to total system collapse and blackout if not carefully considered. Therefore, this section aim to describe the fundamentals of why power system fault analysis is important seen from a system stability point of view. Also, the types of fault and resulting voltage sags which are to be experienced in a power system are reviewed. This will lay the foundation of understanding the voltage sags that converters may experience during their operation.

Power system faults are abnormal conditions, which may be caused by failure of an electrical component, extreme weather conditions, malfunctioning of relays, and human errors [40]. These include both symmetrical and asymmetrical faults where asymmetrical faults are the most common. Depending on the fault type, the location, and the grounding impedance, one fault may evolve into multiple faults. An example of this could be a non-grounded system where a Single Line-to-Ground (SLG) fault occurs. As a result of the high grounding impedance, a high over-voltage or voltage swell occur in the non-faulted phases which may cause a flash-over in these phases, introducing an additional fault. Most faults for overhead lines are weather-related. These include faults as a result of lightning strikes, strong wind causing conductors to either touch or get within distance where the
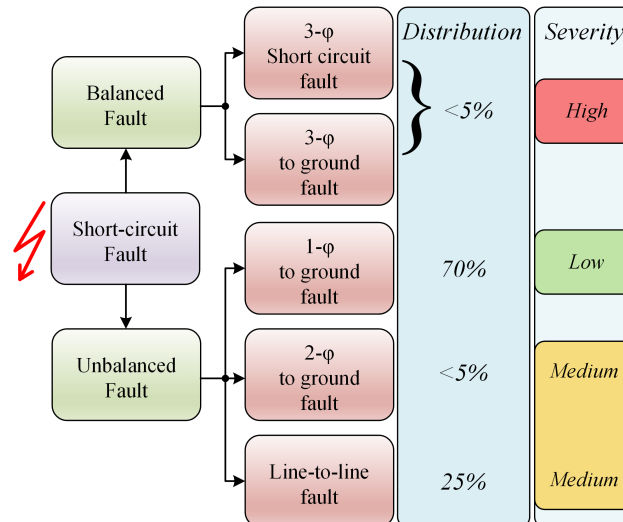
Figure 1.10: Different types of line faults including their distribution of occurrence and severity of impact on the power system network [40].

electrical field ionizes the air between them, salt pollution and rain, which changes the breakdown voltage level of the surrounding air, and natural disasters including flooding and wildfires where both the smoke and hot air reduce the breakdown field of the air. In the case of lightning strikes, a large surge of current is injected to an overhead line or the earth conductor. This high frequency, high amplitude impulse current causes a large over-voltage, which may cause an arc to ground or nearby phases and thereby creates a short-circuit fault. Failures of power system components may also cause short-circuit faults, including e.g. failure of machines, transformers, insulation etc.

As mentioned, unbalanced faults are by far the most common types of faults, where balanced three-phase faults only take up to 5% of the faults occurring. A single-phase to ground fault is the most common fault type and is mostly caused by lightning strikes during non-ideal weather conditions such as heavy rain or salt pollution [40–42]. Based on observations from the Nordic and Baltic countries, line faults and substation faults are responsible for more than 85% of all grid faults, where line faults takes up most of it [42]. The different types of short-circuit faults in its original form are visualized in Figure 1.10 including the distribution of occurrence and impact on the network for each fault type. Later, it will be shown how the voltage sag experienced will also depend on the load connection configuration and the transformer winding configuration. As it can be seen, even though symmetrical three-phase faults are rarely occurring, they pose the largest threat to the power system and should therefore always be considered. The faults considered in this project include symmetrical and asymmetrical short-circuit faults, i.e. no open-circuit faults, which can happen if e.g. a broken overhead line becomes an open-circuit.

1.3.1   Voltage Sag Caused by Faults

A voltage sag is defined as a short duration reduction in the rms or peak value of the voltage which is usually caused by short-circuits or high loads such as the starting of large induction motors [43]. If a voltage sag is very deep, the voltage profile seen from the consumer side might be referred to as an interruption. Theoretically, an interruption will be

a voltage sag of 100%. However, for many voltage-sensitive loads, also a non-zero voltage may result in tripping and disconnection due to the under-voltage lock-out. An example of a sensitive load is computer systems, which could lose memory, adjustable speed drives with an uncontrolled rectifier on the grid side, or induction motors which due to a reduced speed may cause a stop of production lines. Sensitive loads which do not accept tripping as a result of severe voltage sags or interruptions include e.g. data centers and hospitals, which usually install uninterruptible power supplies using batteries or flywheels to ensure the supply of power for interruptions up to several seconds [44]. Sensitive loads, which have a negative impact on the voltage stability both during the voltage sag and the voltage recovery include induction motors. When the voltage drops, an induction motor will slow down, which causes its impedance to drop significantly due to the increased slip frequency. This decreased impedance will draw a large current, which further decrease the voltage sag due to an increased loading of the system. In addition to this, as often seen in a network with large induction motors, is when the fault is cleared, the voltage does not return to the nominal voltage immediately but instead jumps to e.g. 80-90% where after it has a slow ramp back to the nominal value. This happens due to the reestablishment of the air-gap field in the motor which acts as a short-circuited transformer. This draws a large current, up to ten times the rated. After the development of the air-gap field, the motors must be accelerated back to nominal speed which also draws large amount of currents at a low power factor, effectively extending the voltage sag during the voltage recovery.
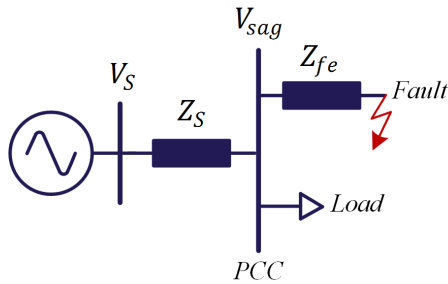

Figure 1.11: Voltage divider circuit used to calculate sagged voltage at Point of Common Coupling (PCC).
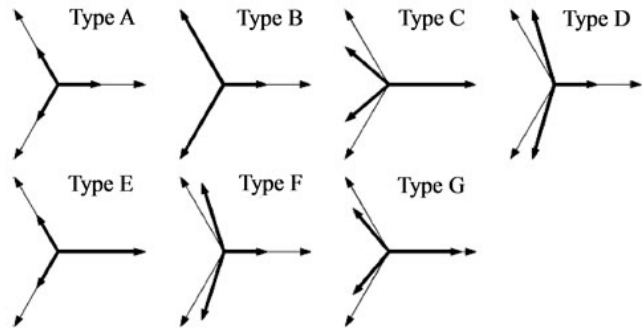

Figure 1.12: The fundamental seven distinct voltage sags profile to be experienced during a power system fault.

When a fault occurs, the voltage sag experienced at a given PCC is highly dependent on the impedance between the PCC and fault location. Hence, the voltage sag will be less severe with an increased distance to the fault and by propagation through different voltage levels where transformers possess a significant impedance, which decouples the local voltage sag with the voltage at the fault location. This is often explained using a simple voltage divider circuit to represent the power system as the one seen in Figure 1.11. Considering nominal voltage at the source, the magnitude of the sagged voltage considering a symmetrical fault is

$$V_{sag} = \frac{Z_{fe}}{Z_S + Z_{fe}} \tag{1.3.1}$$

where Z_{fe} is the feeder impedance and Z_S is the source impedance. Hence, if the feeder impedance is large, the voltage sag will be low and V_{sag} will be close to the nominal value. In additional to this it can be seen that if the external grid is strong (Z_S is low), then

the voltage sag will be independent on the feeder impedance. This is not true in general since an external grid cannot deliver any amount of short-circuit power into the fault as it is assumed here. For asymmetrical faults, the voltage divider circuit can be expressed for each sequence component and then connected at the fault location.

As it was shown in Figure 1.10, five distinct short-circuit faults can occur. However, seven voltage sag profiles may be experienced at the equipment terminals depending on the short-circuit fault type, the connection configuration of the load (star or delta), and the winding configuration of the step-up and step-down transformers. These seven voltage sag profiles are shown in Figure 1.12 where the characteristic voltage (voltage sag in affected line) is assumed to be 50%. In the figure, the pre-fault voltage phasors are shown together with the sagged voltage phasors, which is shown as bold. For the seven sag profiles it is assumed that there is no coupling between the three phases, i.e. the positive- and negative sequence impedances are equal, the zero-sequence voltage will not influence the phase-to-ground voltages, and load currents are neglected [43].

As it can be seen, Type A originates as a result of a three-phase symmetrical fault where all three phase voltages are decreased. The Type B fault can be seen to represent a SLG fault where one phase voltage is decreased. The phase-to-ground voltages during a Type B sag is

$$V_a = V, \quad V_b = -\frac{1}{2} - j\frac{\sqrt{3}}{2}, \quad V_c = -\frac{1}{2} + j\frac{\sqrt{3}}{2}, \tag{1.3.2}$$

where V is the characteristic voltage or sagged voltage level. If the load or generator which is connected to the network is delta-connected, it will only see the line-to-line voltages, which can be calculated as

$$V_a' = j\frac{V_b - V_c}{\sqrt{3}}, \quad V_b' = j\frac{V_c - V_a}{\sqrt{3}}, \quad V_c' = j\frac{V_a - V_b}{\sqrt{3}}. \tag{1.3.3}$$

Using this transformation and ignoring the prime used to designate line-to-line quantities, the line-to-line voltages seen from a delta-connected unit during a single line-to-ground fault is

$$V_a = 1, \quad V_b = -\frac{1}{2} - j\sqrt{3}\left(\frac{1}{6} + \frac{V}{3}\right), \quad V_c = -\frac{1}{2} + j\sqrt{3}\left(\frac{1}{6} + \frac{V}{3}\right), \tag{1.3.4}$$

which has a similar sag characteristic as Type C and is often denoted C^* in the literature. Type C occurs for a line-to-line fault where the two faulted phases move towards each other as seen in Figure 1.12. This type of voltage sag will give the following phase-to-ground voltages

$$V_a = 1, \quad V_b = -\frac{1}{2} - j\frac{V}{2}\sqrt{3}, \quad V_c = -\frac{1}{2} + j\frac{V}{2}\sqrt{3}. \tag{1.3.5}$$

For a delta-connected load, the line-to-line voltages become

$$V_a = V, \quad V_b = -\frac{V}{2} - j\frac{\sqrt{3}}{2}, \quad V_c = -\frac{1}{2} + j\frac{\sqrt{3}}{2}, \tag{1.3.6}$$

which is the Type D profile in Figure 1.12. The three remaining voltage sag types originates as a result of a double line-to-ground fault and its propagation through different types of transformers. All transformer types can be categorized into three groups [43]:

1. Transformers which do not change the voltages. Only a Yy transformer with both neutral points grounded gives this feature.

2. Transformers which remove the zero-sequence component where the voltage at the secondary side is the voltage at the primary side with the zero-sequence voltage removed. Yy with either one or both sides not grounded, Dd, and Dz (delta-zigzag) transformers belong to this group.

3. Transformers that interchange the line and phase voltages where the secondary-side voltage equals the difference between two primary-side voltages. Dy, Yd and Yz transformers belong to this type.

The voltage transformation of the three types of transformers can be expressed as

$$T_1 = I_3, \qquad T_2 = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}, \qquad T_3 = \frac{j}{\sqrt{3}} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}, \qquad (1.3.7)$$

where I_3 is the three-dimensional identity matrix.

The voltage sag shown as Type E results from the phase-voltages of a Double Line-to-Ground (DLG) fault which are

$$V_a = 1, \quad V_b = -\frac{V}{2} - j\frac{V}{2}\sqrt{3}, \quad V_c = -\frac{1}{2} + j\frac{V}{2}\sqrt{3}. \qquad (1.3.8)$$

The voltage sag of Type F results from a Type E after a type 3 transformer (e.g. Dy) which gives the voltages

$$V_a = V, \quad V_b = -j\frac{\sqrt{3}}{3} - \frac{V}{2} - j\frac{V}{6}\sqrt{3}, \quad V_c = +j\frac{\sqrt{3}}{3} - \frac{V}{2} + j\frac{V}{6}\sqrt{3}. \qquad (1.3.9)$$

Finally, Type G results after two type 3 transformers or one type 2 transformer of a DLG fault which gives the phase-to-ground voltages

$$V_a = \frac{2}{3} + \frac{V}{3}, \quad V_b = -\frac{1}{3} - \frac{V}{6} - j\frac{V}{2}\sqrt{3}, \quad V_c = -\frac{1}{3} - \frac{V}{6} + j\frac{V}{2}\sqrt{3}. \qquad (1.3.10)$$

The sag types F and G are derived under the assumption that the positive-, negative-, and zero-sequence impedance are all equal. In case this is not valid, the resulting voltage sag profile will be a mix of different types of sags. The voltage sag propagated through different transformer windings and its dependence on the load connection configuration, are summarized in Table 1.1 and Table 1.2.

During power system short-circuit faults not only the magnitude of the voltage is changed, usually so is the phase angle. Phase jumps occur as a result of a difference in the X/R ratio from the pre-fault to the fault conditions and due to transformations in different types of transformers. The seven types of voltage sags just described will change when

Fault Type	Star-connected load	Delta-connected load
Three-phase	Type A	Type A
Double line-to-ground	Type E	Type F
Line-to-line	Type C	Type D
Single-line-to-ground	Type B	Type C*

Table 1.1: Voltage sag types dependent on fault type and load connected.

	Sag type on Primary Side						
Transformer Type	Type A	Type B	Type C	Type D	Type E	Type F	Type G
Type 1 (YNyn)	A	B	C	D	E	F	G
Type 2 (Yy, Dd)	A	D*	C	D	G	F	G
Type 3 (Yd, Dy)	A	C*	D	C	F	G	F
	Secondary-Side Voltage Sag Type						

Table 1.2: Secondary-side voltage sag types dependent on primary-side fault type and transformer winding configuration.

phase-angle jumps are considered. Then, the characteristic voltage V will be a complex quantity instead of a constant real value. In the case that higher impedance faults are considered, the sag characteristics are further complicated. Due to this and since the aim of this section is only to introduce the voltage sag characteristics in power systems, phase-angle jumps are neglected throughout this study. To that end, the impact of transformers on the voltage sag profile is also neglected and only the performance and response of the power electronic converter to some specified voltage sags are considered. Therefore, this section is simply provided for understanding the voltage sags that can be encountered in power systems and then later in this project analyze different converter controllers during some of these sags.

Voltage Sags and Power System Stability

As mentioned, voltage sags can easily cause under-voltage lock-out and tripping of loads and connected generators such as synchronous machines in the network. Therefore, loads should be able to comply with voltage-tolerant requirements, which is similar to the fault ride-through requirements issued for installation of e.g. installation of WTS. It has been mentioned that voltage sags are dependent on the fault location, and obviously, the location where the voltage sag is of interest. If the fault occurs at the transmission level, the distribution sagged voltage or the consumer-end load voltage may be very different depending on the load connected configuration and the transformer winding configuration as seen in Table 1.1 and Table 1.2. To lower the risk that a short-circuit at the transmission level will cause loss of generation and eventually blackout of the system, which will trip all connected loads, generators installed at the transmission and/or distribution network should remain connected and aim to support the grid voltage as much as possible. Along these lines, all synchronous generation may lose synchronism and become unstable during a fault which further threatens the voltage and frequency stability of the overall system. Finally, this may cause a chain reaction where one generator is tripped, which makes the voltage sag more severe and then another generator trips etc. Therefore, LVRT capability is very important as will be discussed in the following section.

1.4   Grid Code Requirements and Standards

For a power electronic-based power system, grid requirements are becoming increasingly stringent in order to ensure a stable operation during all operating conditions. WTSs not simply need to be grid-following elements, but should to a higher extent behave as

grid-supporting elements and provide ancillary services to the power system [45, 46]. In order to install a WTS, the system must be able to comply with requirements stated by the TSOs or DSOs within the area of installation. This means that depending on the location of installation, the requirements might differ. Hence, to design and control the WT converter, these requirements must be understood and carefully addressed. In the following, only the most important grid code requirements necessary for Fault Ride Through (FRT) compliance will be discussed. The aim is to design and control a converter system for a WT application to comply with the requirements issued by the German association of energy and water industries BDEW [47]. Requirements regarding recurring faults, flicker, and protection will not be discussed. Furthermore, all higher level control and monitoring requirements including SCADA system and external communication will not be considered, since only one WT converter is addressed in this project.

Fault Ride-Through and Grid Support
The requirements to be met include demands for both normal and fault conditions. In case of frequency deviations on the PCC, the WTS must be able to perform frequency control and support the grid stability by changing its active power injection through droop regulation [48].

Previously, when the penetration of wind power was low, WTs were allowed to disconnect during grid faults since their impact on the power system were negligible. However, for a power electronic-based power system dominated by RES such as WTs, a disconnection of a large number of turbines will cause a large deficit in power generation when the fault has cleared, which together with a low-inertia grid will reduce the system frequency and increase the risk of a blackout [11]. Thus, to avoid frequency and/or voltage instability, a need for DGs to stay connected during grid faults has emerged. This has resulted in the requirement of FRT capability of DGs. During short-circuit faults, LVRT requirements are issued by TSOs in order for WTSs to stay connected and inject reactive power to support the grid voltage. In Figure 1.13(a), it can be seen which requirements exist for the WTS to stay connected during a short-circuit fault. As it can be seen, the LVRT profiles for Spain and Germany require the system to stay connected even when the PCC voltage drops to zero.

In Figure 1.13(b), the minimum requirement for the injection of reactive current during grid voltage sags can be seen. In Denmark, the converter is required to deliver 1 pu of reactive current when the voltage drops below 0.5 pu. In case of a short-circuit fault, the voltage support has a higher priority than maximum power extraction from the WT. Thus, the active current injection might be limited or decreased in order for the converter to inject the required reactive current [49]. As an example, the Danish grid-code requirements enforces the WTS to inject 1 p.u. of reactive current for 500 ms and the reactive current injection is required when the voltage is below 0.9 pu. When a fault is cleared, the production of active power must be restored at least 500 ms after the voltage is within normal operating conditions [33].

The grid-code requirements for the FRT capability and reactive current injection from the German BDEW grid code is shown in Figure 1.14(a) and 1.14(b), respectively. The injected reactive power support must be activated within 20 ms after the fault recognition. These are the requirements considered in this project for converter control fault conditions. It must be noted that the low-voltage profile shown in Figure 1.14(a) is normally referred to
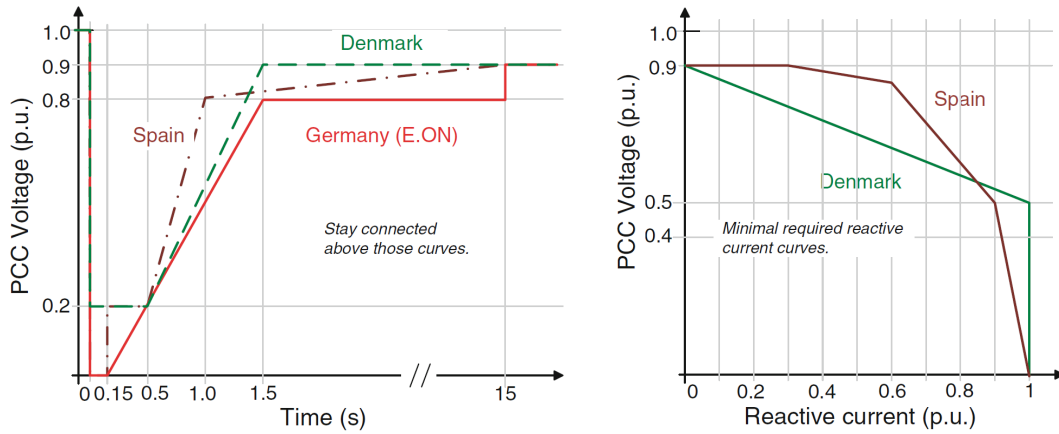
(a) Required LVRT profiles for Spain, Denmark and Germany.

(b) Requirements of injection of reactive current depending on the PCC voltage.

Figure 1.13: Requirements of stay-connected time and injected current for a low PCC voltage in a WTS above 1.5 MW [48, 49]. E.ON. has the same requirement of dynamic reactive power support as it is shown for Denmark in (b).

the connection point at the high-voltage side of the transformer behind eventual connection lines. This means that, in most cases, even though the high-voltage potential drops to zero, the voltage at the WT terminal is likely to be around 0.15 pu depending on the system impedance [50]. Several grid codes, e.g. the Danish grid code requires the WT to withstand
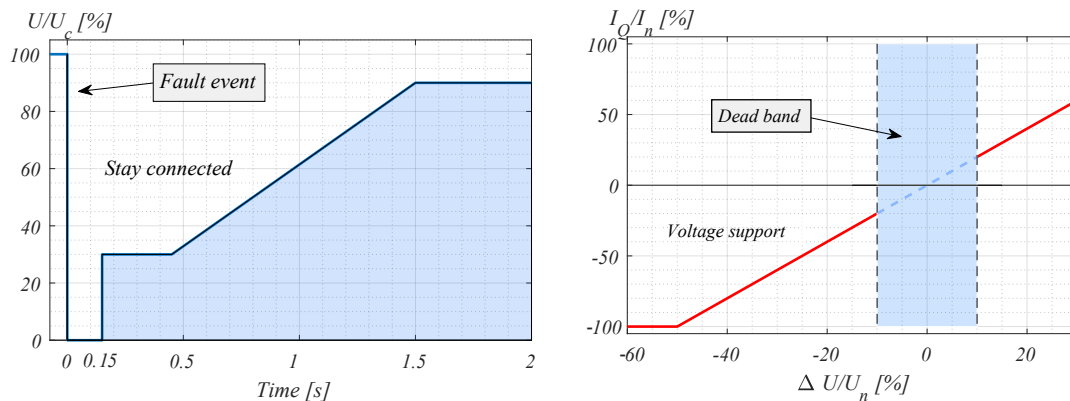
(a) Required LVRT profile from BDEW.

(b) Requirements of injection of reactive current dependent on PCC voltage during voltage disturbances.

Figure 1.14: (a): Requirement from BDEW for low-voltage ride-through capability during a fault event. (b): Voltage support by injection of reactive current in either overexcited or underexcited operation [51].

asymmetrical faults and should be tested against single-phase and two-phase faults for a duration up to 150 ms. Reactive current injection should be performed as shown in Figure 1.14(b) regardless whether the fault is symmetrical or asymmetrical.

Like for short-circuit faults, where the converter must inject reactive current to restore the grid voltage, the converter must absorb reactive current in the case where over-voltages

are to experienced on the PCC. Since voltage-sags are the most common consequence of grid faults [49], the High-Voltage Ride Through and reactive current absorption requirements will not be considered in this project.

Power Quality and Harmonic Injection

To ensure that the power delivered from the WTS to the grid does not cause adverse effects to loads and other equipment connected to the grid, distortion limits is provided of the injected grid current. The Total Harmonic Distortion (THD) should be less than 5% of the rated fundamental frequency output current. The distortion limits for the different harmonics are given in Table 1.3, where even order harmonics should be <25% of the limits given for the odd order harmonics. Normally the harmonic distortion is calculated for each individual frequency component of the current and then using the network impedance, the corresponding voltage distortion can be calculated and then its THD. However, no or limited information is available of the network impedance, which implies that only harmonic analysis of the current is performed [52].

Distortion Limits of Current

Odd harmonics	Distortion limit
$3^{rd} - 9^{th}$	$< 4.0\%$
$11^{th} - 15^{th}$	$< 2.0\%$
$17^{th} - 21^{st}$	$< 1.5\%$
$23^{rd} - 33^{rd}$	$< 0.6\%$
Above the 33rd	$< 0.3\%$
THD	$< 5\%$

Table 1.3: Distortion limits for output current of 2L-VSC as recommended in IEEE Std 1547-2003 and reaffirmed in 2008 [53]. All limits are given in procentage of the rated fundamental frequency current.
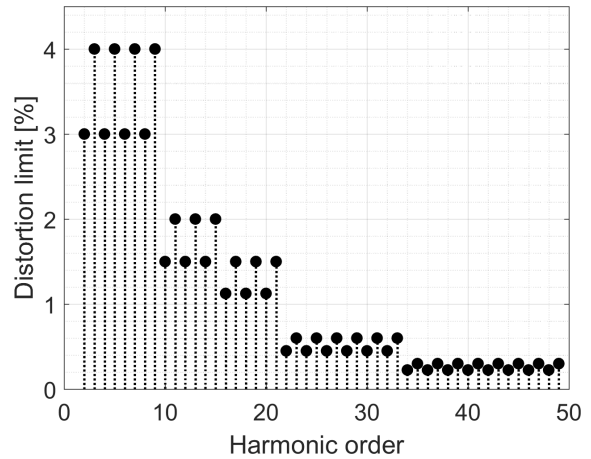

Figure 1.15: Visualization of the disortion limits from Table 1.3 in percent of rated fundamental current up to the 50th harmonic.

1.5   Formulation of the Problem

Grid-connected converters can be categorized into three types: grid-following, grid-forming, and grid-supporting where grid-following acts as a controlled-current source, grid-forming acts as a controlled-voltage source and the grid-supporting control can rely on either of them. As outlined previously, in a power electronic-based power system dominated by power converters, the control structure cannot solely rely on grid-following converters since they need one or more dominant grid-forming components to dictate the grid voltage. To that end, the synchronization loop (PLL) of grid-following converters is destabilized during weak-grid connections such as long connection lines, low-voltage grids or fault situations. Along these lines, it is required to introduce a certain share of grid-forming and especially voltage-controlled grid-supporting converters into the

grid to alleviate these negative effects associated with grid-following converters and the retirement of synchronous machines. An extensive volume of literature has described the performance of voltage-controlled grid-supporting converters operated in microgrids with the possibility of switching between stand-alone and grid-connected mode for numerous different applications. This is certainly an area of interest for voltage-controlled converters due to the fact that low-voltage microgrids often involves weak-grid connections and that in islanded conditions converters dictating the grid are required.

As specified, weak-grid conditions also appear during fault situations where the otherwise stable grid-following structure might not be able to comply with grid codes and remain connected. The investigation of using voltage-controlled grid-supporting converters to possibly enhance the fault ride-through performance of grid-connected converters in e.g. WTSs is not well documented and its advantages/disadvantages compared to a grid-following structure remains unclear.

In [54], an improved virtual inertia based voltage controller for a grid-connected converter is tested for its fault ride-through ability. Here, the control structure is changed to grid-following control in case of unbalanced faults in order to limit the converter current. A VSM is tested during a three-phase fault in [55] where the focus is put on current limiting without considering any grid support, which was the initial motivation for such control strategies. In [56], an additional method used to avoid converter over-current of a VSM during asymmetrical faults is proposed. Similarly as for the other papers, no investigations regarding how the performance of the grid-forming structure is lost due to the current limitation are conducted. To that end, since many publications aim to modify the desired synchronous machine behavior to a grid-following structure during fault situations, the robust weak-grid performance of the grid-forming converter will be lost during the fault. Therefore, questions arise whether it is possible to achieve fault ride-through of the grid-forming converter, which is kept as grid-forming during the fault, while considering mandatory current limitation, which could improve the stability and robustness compared to conventional current-mode control structure.

Extensive researches are carried out for the operation of grid-following converters during balanced and unbalanced faults [46]. Similar analysis is lacking for the grid-forming/grid-supporting control structure and especially a benchmark between the two structures during grid faults is a gap in the present research alongside how a grid-forming converter should be controlled during grid faults to overcome the previously mentioned drawbacks of the grid-following converter. Therefore, this project aims to fill out some of this gap by conducting a comparative study of current-controlled and voltage-controlled converters during symmetrical and asymmetrical grid faults to assess whether the fault ride-through of the converter can be enhanced using a voltage-controlled structure rather than a traditional current-controlled structure. This aim or problem can be formulated as follows:

Can the fault ride-through behavior of grid-connected converters be enhanced by utilizing a voltage-controlled converter structure rather than a conventional current-controlled structure?

To assist answering the stated problem, several detailed sub-questions are formulated in order to more clearly identify which topics need to be addressed to answer the main question.

- *How can the considered system of study be modeled?*

- *How should the converter be controlled in case of a current-controlled structure?*

- *How should the converter be controlled in case of a voltage-controlled structure?*

- *How is the voltage-controlled structure advantageous compared to the current-controlled structure during normal operating conditions and small-signal perturbations?*

- *How can each of these structures be controlled during symmetrical and asymmetrical faults?*

- *How is it possible to keep the voltage-controlled structure during grid faults when converter current limitation is considered in order to overcome the drawbacks of the current-controlled converter?*

A simulation model of a grid-connected converter operating in a WT application will be developed for both current-mode (grid-following) and voltage-mode (grid-forming) control. The parameters used for the simulation are presented in Table 1.4, where the values used for the simulation are selected to match the ones available in a laboratory setup in order to make an easy comparison between modeling/simulation and experimental work. For the current-mode control, conventional grid-following operation will be considered whereas for the voltage-mode control, the SPC as described in section 1.2.2 will be studied.

Symbol	Description	Simulation	Experimental
V_g	Grid voltage (rms line-to-line)	400 V	400 V
S_n	Nominal power	7.35 kVA	7.35 kVA
f_0	Fundamental grid frequency	50 Hz	50 Hz
f_{sw}	Converter switching frequency	10 kHz	10 kHz
f_s	Control sampling frequency	10 kHz	10 kHz
V_{dc}	DC-link voltage	730 V	730 V
L_{cf}	Converter-side inductor	6 mH	6 mH
C_f	Filter capacitor	10 μF	10 μF
L_{gf}	Grid-side inductor	0 mH	0 mH
L_l	Transformer leakage inductance	0.05 pu/ 3 mH	0.05 pu/ 3 mH
Z_L	Thevenin/Line impedance	0.04-0.5j pu	0.04-0.1j pu

Table 1.4: Main parameters for the grid-connected VSC used for the simulation studies and experimental setup.

Limitations of Project

The limitations, assumptions and simplifications made in this project are as follows:

- The generator-side converter, wind turbine model, mechanical drive train alongside wind fluctuations are all considered as a controllable current source at the dc-side for the simulation part and as a constant dc source for the experimental verification.

- The simulation results and experimental verification are both performed on a down-scaled system with a much smaller power level than a realistic wind turbine system.

- Only the leakage inductance of the wind turbine system step-up transformer is considered. The actual transformer operation is neglected.

- The grid/line impedance is considered purely inductive, i.e. any potential impact of grid/line resistance is neglected.

- The external grid is represented as a Thevenin equivalent.

- For the inverter modeling, it is assumed that the switches and anti-parallel diodes are ideal i.e. no deadtime, infinite slew rates as well as no parasitic capacitances and inductances of the power modules and gate drive circuits.

- The influence and operation of circuit-breakers, surge arrestors, fuses etc. will not be considered during fault conditions.

- The sequence components are considered decoupled during the a fault condition, i.e. the voltage at the fault location is directly controlled to emulate a given fault type, whereas the actual physical connection between different phases and ground is neglected.

1.6   Project Outline

This project describes how to develop and control two types of converter control for grid-connection: current-mode control and voltage-mode control. Based on these, their performance, advantages, and disadvantages during normal operating conditions and especially during grid faults are revealed.

At first, a description of the Voltage Source Inverter (VSI), how to model and modulate it, together with a design of the passive Inductor-Capacitor-Inductor (LCL) output filter are presented in Chapter 2. In Chapter 3, a thorough examination of the state-of-the-art current-mode and voltage-mode controllers are given. This includes a description and design of the inner current regulator, how to accurately discretize it, the PLL used for the grid synchronization including pre-filtering stages, and the dc-link voltage controller. In addition, a detailed analysis together with the design of the synchronous power controller is given, which include droop control, the inner current regulator, the virtual admittance together with the outer power loop controller and reactive power controller. Following this in Chapter 4, the developed controllers are implemented in a detailed simulation

model developed in MATLABs Simulink and PLECS blockset and experimentally verified using the laboratory setup. This includes step responses of current and power references, the ability to provide grid-supporting functionalities alongside operating in weak-grid conditions.

Chapter 5 discusses the fault behavior of the studied controllers where both controllers are exposed to symmetrical as well as asymmetrical grid faults. Here it is clearly seen from the tests presented in Chapter 4, that the advantages of the voltage-mode controller are highly diminished during grid faults. During a symmetrical fault, a proposed voltage-mode controller is shown to be able to successfully ride through the fault while complying with the considered grid code by introducing circular current limitation and modification of the references for the outer power loops. For the asymmetrical fault, the issue is further complicated due to the difficulty of limiting the asymmetrical currents. Thus, in order to make the voltage-mode controller ride through the asymmetrical fault, the proposed controller is basically switched to current-mode control during the fault while again constraining the outer power loops. For the asymmetrical fault, a current reference strategy which comply with recent grid codes for the negative-sequence currents is proposed. This proposed method is compared to pure positive-sequence current injection and no current injection, in order to show the benefits of the dual-sequence current injection seen from the grid point of view.

Finally the project is concluded in Chapter 6 where the findings of the project are listed and the future work to be done is described. It is disclosed that with the adoption of the proposed current reference strategy the fault performance can be enhanced seen from the grid stability point of view. Also, with the utilization of proposed fault-mode control of the voltage-mode structure fault ride-through can be accomplished in a way which keep the benefits of the grid-forming converter. Lastly, the laboratory setup, data acquisition, and the basic theory of symmetrical component analysis are included in the appendices.

The proposed current reference generation scheme for asymmetrical fault control and the proposed fault control for the voltage-controlled converter in Chapter 5 are both under review and considered for journal publication.

2 Modeling and Analysis of Grid-Tied VSIs

In order to develop the control for both the current-mode and the voltage-mode operation, it is necessary to describe and analyze the converter itself including how it should be modeled when the linear control system is to be constructed and designed. Therefore, this chapter has the purpose of describing the fundamental principle of the two-level VSC and its operation. This include its attainable switching configurations and how its discontinuous and non-linear operation can be approached when applying linear control. At first, a switching model of the converter, which is used to build a relationship between the dc and ac side is developed. Then, this model is transformed to a time-continuous model by means of averaging, which gives a relationship between ac-side voltages, dc-side voltage, and the control duty cycles. To that end, the chosen modulation strategy will be described and the ac output filter will be designed. The setup available in the laboratory is described in detail in Appendix A which includes the different components, how the control is performed, and data acquisition of its measured quantities. Also, the grid-side hardware of this setup will be described. This include the line-side converter and LCL filter.

2.1   Switching Model of Two-Level VSI

To convert the dc-link voltage into a sinusoidal ac voltage which is to inject a sinusoidal currents to the grid, a VSI is needed. The topology of the 2L-VSI is shown in Figure 2.1. It consists of three paralleled phase legs, each consisting of two IGBTs. Since a half-bridge topology is used for each phase, the phase voltage with respect to the negative DC rail only has two levels. Each IGBT has an anti-parallel diode used to commutate the current when switching off an inductive load. To avoid shoot-through in an inverter leg, the top and bottom transistors are not allowed to be conducting at the same time. This reduces the possible switching states of the inverter to eight states, where two of them short-circuits the load. If the IGBTs and their anti-parallel diodes are considered as ideal switches, neglecting dead-time and finite slew-rates, a phase-leg switching function can be defined.

The switching function is defined as $S_i \in \{1, -1\}$, $i \in \{a, b, c\}$, where if $S_a = 1$ the top transistor is on and the bottom transistor is off in phase-leg a and if $S_a = -1$ the top transistor is turned off and the bottom transistor is turned on. The important feature of the switching function is to establish the relationship between the voltage and current on the dc side with the three-phase voltages and currents on the ac side. Doing this, the eight possible switching states and the resulting dc-link current and ac-side line-to-line voltages can be seen in Table 2.1. This is represented in matrix form as
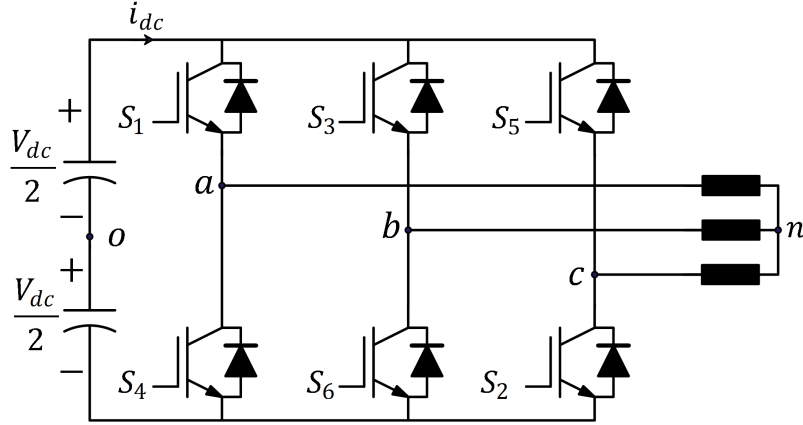
Figure 2.1: Schematic of VSI used to interface the dc-link voltage with the grid.

Switching states of the VSI

State No.	Switching State	i_{dc}	v_{ab}	v_{bc}	v_{ca}
0	000	0	0	0	0
1	100	$i_a - i_b - i_c$	V_{dc}	0	$-V_{dc}$
2	110	$i_a + i_b - i_c$	0	V_{dc}	$-V_{dc}$
3	010	$-i_a + i_b - i_c$	$-V_{dc}$	V_{dc}	0
4	011	$-i_a + i_b + i_c$	$-V_{dc}$	0	V_{dc}
5	001	$-i_a - i_b + i_c$	0	$-V_{dc}$	V_{dc}
6	101	$i_a - i_b + i_c$	V_{dc}	$-V_{dc}$	0
7	111	0	0	0	0

Table 2.1: The dc-link current and line-to-line voltages of the three phases for the eight possible switching states.

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}. \tag{2.1.1}$$

The three-phase voltages with respect to the dc-link midpoint is

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} S_a \\ S_b \\ S_{c.} \end{bmatrix} \tag{2.1.2}$$

The line-to-neutral voltages can be expressed as

$$v_{an} = v_{ao} - v_{no} \tag{2.1.3}$$

$$v_{bn} = v_{bo} - v_{no} \tag{2.1.4}$$

$$v_{cn} = v_{co} - v_{no} \tag{2.1.5}$$

and the voltage difference between point o and n (the zero-sequence voltage) is

$$v_{no} = \frac{V_{ao} + V_{bo} + V_{co}}{3}. \tag{2.1.6}$$

Using these and equation (2.1.2), the line-to-neutral voltages expressed by the switching function and the dc-link voltage can be written as

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{V_{dc}}{6} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{2.1.7}$$

The currents drawn from the dc-side to the ac-side can be expressed using column three as given in Table 2.1 as

$$i_{dc} = S_a i_a + S_b i_b + S_c i_c. \tag{2.1.8}$$

At this moment, both the expressions for the dc-link current and the phase-to-neutral voltages are developed with the use of switching functions. These two form the switching equations needed to develop a relationship between the dc and ac side and will later be used to develop the averaged model of the system. The switching model with inputs and outputs can be seen in Figure 2.2.
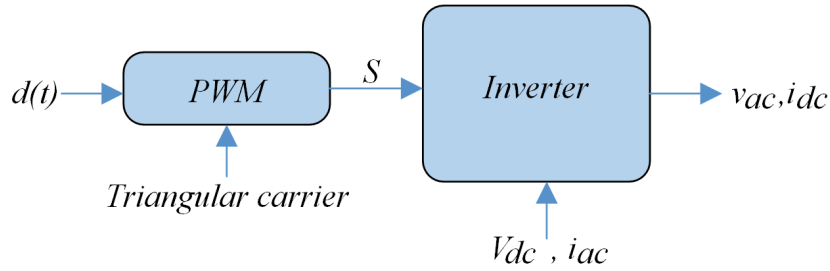

Figure 2.2: Block diagram of inverter switching model.

The switching model is developed to identify a relationship between the continuous dc-link voltage, ac-side current and the discontinuous dc-side current and ac-side voltage. The switching model can be used to identify the switching action of the system, Pulse Width Modulation (PWM) spectrum analysis using Fast Fourier Transform (FFT), identification of ac-side current ripple for inductor filter design and analysis of parasitic current paths to comply with Electromagnetic Compatibility requirements. These are some of the advantages of a switching model of a converter. The drawback include the fact that the output of the switching model is discontinuous and hence a small time step in the numerical solver is needed in order to describe and simulate the system. This implies larger computational times and memory requirements.

2.2 Averaged Model of Two-Level VSI

The switching model is now transformed from a time-discontinuous model to a time-continuous model. The averaged model of the converter eliminates the drawback of a discontinuous output which is the case for the switching function, which can be used to simulate the system in a much larger time frame in order to identify e.g. the converter

control behavior including low frequency components. Furthermore, it enables to model the converter operation when designing linear regulators. This is done by averaging the system over a time window equal to the switching period. Therefore, it is effectively a moving average model. Using this, the switching dynamics are ignored but the dynamics of the system are still preserved. The averaging operator of any signal is expressed as

$$\langle x(t) \rangle = \frac{1}{T_s} \int_{t-T_s}^{t} x(\tau) d\tau. \tag{2.2.1}$$

To develop the full averaged model, only the terms including the switching function need to be averaged. These are the line-to-neutral voltages and input current drawn by the converter. Then the remaining variables will automatically be its averaged value due to the averaged switching. The averaged value of the switching function is simply the duty cycle as

$$d_a = \langle S_a \rangle = \frac{1}{T_s} \int_{t-T_s}^{t} S_a(\tau) d\tau, \tag{2.2.2}$$

shown for phase-a. Performing the identical operation for the switching functions for phases b and c, the line-to-neutral phase-a voltage described in equation (2.1.7), can be written in its averaged form as

$$v_{an} = \frac{\langle V_{dc} \rangle}{6} \left(2d_a - d_b - d_c \right) = \frac{\langle V_{dc} \rangle}{6} \left(3d_a - \underbrace{(d_a + d_b + d_c)}_{=0} \right) = \frac{\langle V_{dc} \rangle}{2} d_a \tag{2.2.3}$$

Doing the same for phases b and c, the line-to-neutral averaged voltages can be expressed as

$$\begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix} = \frac{\langle V_{dc} \rangle}{2} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}. \tag{2.2.4}$$

This is under the assumption that the dc-link voltage can be considered constant, which
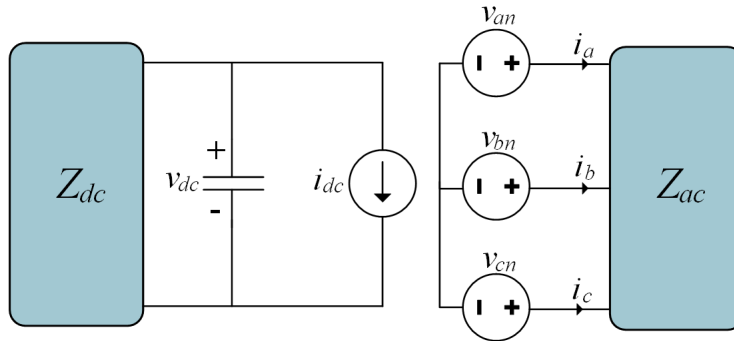

Figure 2.3: Equivalent circuit diagram of averaged model of three-phase VSI. All quantities are average values described by equation (2.2.4) and (2.2.5).

is its average value and without high-frequency variations. Using this and assuming the dc-link voltage to be stiff, it can be seen that the ac-side voltage of the converter can be modeled as an ideal linear amplifier. By this, the only input in this case for the ac-side voltages is the duty cycles, which are obtained from the closed-loop digital controller. Again

by assuming that the ac-side currents do not change significantly during the switching period, the averaged dc-side current can be expressed as

$$\langle i_{dc} \rangle = d_a \langle i_a \rangle + d_b \langle i_b \rangle + d_c \langle i_c \rangle. \tag{2.2.5}$$

Since both the ac-side currents and the duty cycles vary sinusoidally, the dc-side current cannot simply be approximated as a linear gain. From this, the averaged model of the 2L-VSI can generally be represented as shown in Figure 2.3, where Z_{dc} and Z_{ac} represent whatever network is connected to the dc and ac side of the converter. As it was seen, the averaged converter voltage can be approximated as a linear gain within the range of the dc-link voltage. To get as high voltage controllability as possible, the dc-link voltage used for this project is 730 V (as seen in Table 1.4), which is the highest voltage achievable in the laboratory setup for the used active rectifier. To that end, as will be described, Space Vector Modulation (SVM) will be adopted as the maximum line-to-line rms voltage can be increased to $0.707 V_{dc}$ compared to $0.612 V_{dc}$ for the case of Sinusoidal Pulse Width Modulation (SPWM) without introducing over-modulation. To further analyze the utilization of the dc-link voltage, the PWM modulation strategy is to be investigated.

2.3 Pulse Width Modulation Strategy

The final objective of most closed-loop control strategies of VSIs is to follow a desired output voltage reference at the converter ac terminals with a specified magnitude, frequency, and phase. Hence, a modulator is needed to synthesize the constant input voltage into the desired reference voltage.

The basic aim of any modulation scheme is to produce a train of pulses, which have the same fundamental volt-second balance as a desired given input. Besides the objective of modulating the desired low-frequency reference by adjusting on-time of the converter switches, the secondary objective of a selected modulation scheme is to limit the unwanted inevitable switching harmonics as much as possible [57]. In general, different PWM strategies are obtained by adjusting three parameters: the turn-on pulse width of the switching, the position of the pulse within the carrier interval, and the pulse sequence within and across carrier intervals.

Basically there are two methods to determine the harmonic content of the output voltage of the converter. The first is to represent the signal as a Fourier series expressed as an infinite summation of sinusoidal components. The second and probably the most used technique is to evaluate the harmonic content of a signal by calculating the FFT of a given waveform, using e.g. a simulation software. To avoid errors in the harmonic magnitudes using this approach, exact integer carrier ratios should be used [57].

In its basic form, PWM is achieved by comparing a reference with a carrier signal. When selecting the carrier waveform, the triangular carrier improves the harmonic characteristics of the pulse train compared to a sawtooth carrier. A conventional sine-triangular modulation scheme is called a double-edged naturally sampled modulation.

A disadvantage of the naturally sampled PWM is the difficulty of implementation in a digital controller. This is due to the transcendental equation used for the reference signal. Instead, the reference is sampled and held constant for each carrier interval. For a

triangular carrier, the sampling can either be symmetrical where the reference is sampled at either the positive or negative peak of the carrier, or it can be asymmetrical where the reference is sampled at both the positive and negative peaks of the carrier. This means that the sampling frequency is doubled but the switching frequency remains the same. The nature of the sampling process introduces a phase delay, which is one-half of the carrier period for symmetrical sampling and one-fourth of the carrier period for asymmetrical sampling. The asymmetrical sampling results in a voltage harmonic spectrum with less unwanted harmonics compared to the case of symmetrical sampling [57]. This advantage often leads to the use of asymmetrical sampling rather than symmetrical sampling when using a triangular carrier.

Compared to a single-phase inverter, a drawback of the three-phase inverter is the limitation of the peak output line-to-line voltage of $\sqrt{3}/2V_{dc}$ using a conventional sine-triangular PWM strategy. To accommodate this limitation, different common-mode third-harmonic components can be injected into the reference to increase the peak output voltage. Since this component is added to all the phase voltages it does not change the line voltages. Basically, PWM strategies like SVM, Third Harmonic Injection Pulse Width Modulation (THIPWM), and Discontinous Pulse Width Modulation are just modifications to SPWM in the way how the placement of the switching pulses is performed. This is done by changing the inactive zero space vector intervals within each half carrier period. Each of them have advantages and disadvantages dependent on the application of interest.
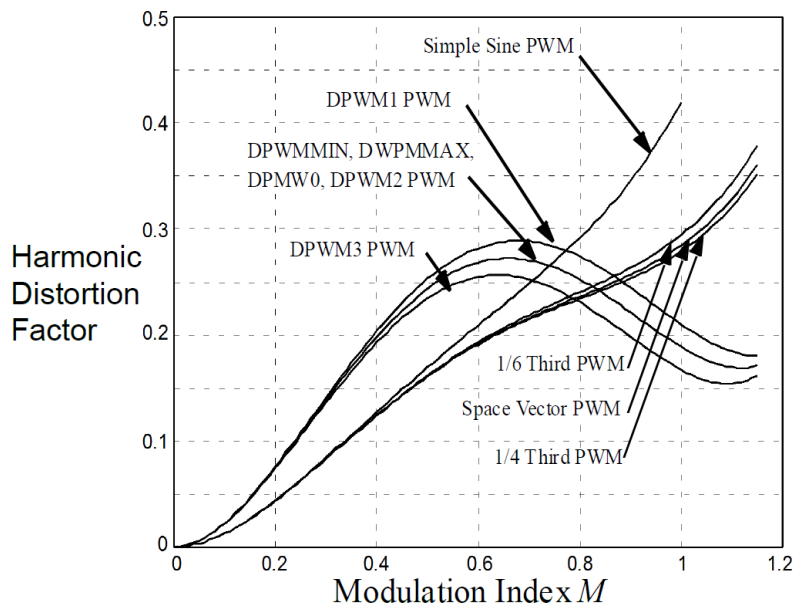

Figure 2.4: Comparison of harmonic distortion factors as function of modulation index for different modulation strategies [57].

The discontinuous switching strategies do not lead to an optimal condition regarding harmonic performance. The advantages of these strategies are the reduced switch transitions during the modulation, which effectively reduces the switching losses. As it can be seen in Figure 2.4, little difference exists between the harmonic distortion factors for the different modulation strategies injecting a third-order harmonic into the SPWM reference. Due to the ease of implementation, a high utilization of dc-link voltage, and

equal distribution of stress among the different transistors [58, 59], the SVM strategy will be the used modulation strategy in this project. Furthermore, the closed-loop control performed in the next chapter will be done in the $\alpha\beta$-frame, which makes the SVM an obvious choice since the transformation of coordinates is already performed.

2.3.1 Space Vector Modulation

Instead of using the three-phase variables as in the case of SPWM, SVM uses a reference voltage space vector to modulate the output voltage. Here, it can be utilized that a three-phase system can be reduced to a vector in a two-axis system. To ensure that the developed equations describe the same signals before and after the transformation, a common variable is defined for the system. This is the zero or common-mode component

$$x_0(t) = \frac{x_a(t) + x_b(t) + x_c(t)}{3}, \tag{2.3.1}$$

which is used to introduce the following three vectors

$$x_{a0}(t) = x_a(t) - x_0(t) \tag{2.3.2}$$

$$x_{b0}(t) = x_b(t) - x_0(t) \tag{2.3.3}$$

$$x_{c0}(t) = x_c(t) - x_0(t) \tag{2.3.4}$$

Assuming a symmetrical system where $x_0(t) = 0$, the space vector can be represented by projecting each phase variable to the real-axis of the two-coordinate system. Replacing the generic variable $x(t)$ with the phase voltages, the space vector is

$$\boldsymbol{v_{\alpha\beta}(t)} = \frac{2}{3}\left(v_a(t)e^{j0°} + v_b(t)e^{j120°} + v_c(t)e^{-j120°}\right) \tag{2.3.5}$$

$$= \frac{2}{3}\left(v_a(t) - \frac{1}{2}v_b(t) - \frac{1}{2}v_c(t)\right) + j\left(\frac{\sqrt{3}}{2}v_b(t) - \frac{\sqrt{3}}{2}v_c(t)\right) \tag{2.3.6}$$

This space vector is also said to be in the $\alpha\beta$ stationary-reference frame where the α-component accounts for the real part of the space vector and the β-component accounts for the imaginary part of the space vector. When put to the matrix form this is more widely known as the Clarke transformation

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{2.3.7}$$

In Figure 2.5, the eight switching states can be identified in the two-coordinate system. As previously described, these include six active vectors and two zero vectors. The reference space vector voltage can be achieved by averaging the two neighboring active states and the two zero vectors during the switching period. SVM is symmetrical around half the carrier frequency just as for SPWM using a triangular carrier. If it is not chosen to be symmetrical then it will behave as in the case of sawtooth carrier, which has some harmonic disadvantages.

The main idea is to calculate the time needed in the two active states and then the remaining time is equally divided between the two zero states. The active states are
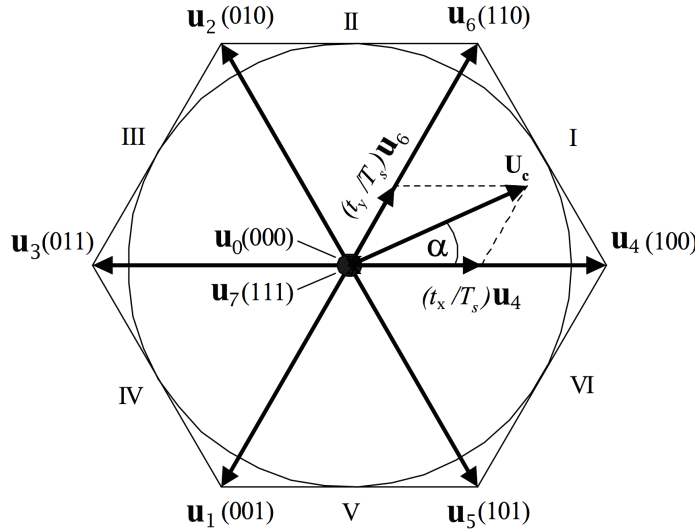
Figure 2.5: A view of the possible switching states ($\boldsymbol{U_0}$-$\boldsymbol{U_7}$) and the desired reference space vector $\boldsymbol{U_c}$ [60].

centered in each half of the switching period, which means that the zero vectors are located in the beginning, the middle, and the end of each switching period. Normally to implement SVM, the reference three-phase voltages are transformed into its equivalent $\alpha\beta$-components. These are then used to calculate the fractional time of the switching period that each active vector in the given sector has to be turned on. Based on this calculation, the switching times are used to formulate the needed duty cycle for each phase leg. All this can be implemented in a look-up table in the digital controller using six if statements, one for each sector.

A more effective way of implementing SVM is to recognize that the difference between SVM and SPWM is the injection of a third harmonic component in the reference phase voltages. This third harmonic components can simply be calculated as

$$v_{z,3rd} = -\frac{max(v_a, v_b, v_c) + min(v_a, v_b, v_c)}{2} \tag{2.3.8}$$

When this is calculated based on the three reference signals, the switching pulses can be created using an asymmetrical regular sampled reference compared to a triangular carrier. Using this method, the added third-harmonic component enables the duty cycle to be increased to 1.154 without entering over-modulation. This effectively implies that the maximum line-to-line rms output voltage will be increased to $0.707V_{dc}$.

2.4   Design of Output Filter

To comply with IEEE Std. 1547, IEC 61000-3-2, 61000-3-12 among others on distortion limits of the injected grid current, an output filter is needed to suppress harmonics introduced by the modulation [61]. To that end, a filter is also needed to ensure that high-frequency grid harmonics do not interfere with the converter as well as the high-frequency harmonics generated by the converter does not cause adverse affects on other grid-connected equipment.

The most simple way to filter the output current is to place a large bulky inductor on the ac side of the converter. This, however, implies that the inductor needed will be large in size and also expensive [62]. To that end, the system dynamics will be poor as the voltage drop in the inductor is large. Therefore, a trend has been to explore a more cost-efficient solution, which has resulted in the LCL filter being widely used in grid-connected converter applications [63, 64]. Besides the reduction in price, the transition from a first-order filter to a third-order filter also gives a much higher attenuation capability. However, increased controller complexity arises using an LCL filter due to resonance that may occur between the filter elements [65, 66]. This can lead to controller instability and it often requires that either passive or active damping is needed. Other filter topologies include trap-filters designed to attenuate the major carrier harmonics and its sidebands by introducing a parallel LC path to the original filter capacitor. An LCL filter including a trap branch (LCL-LC) can also be used dependent on the attenuation needed and constraint on filter price, volume, weight etc [67]. With an LCL-LC filter, the overall filter size can be reduced including the voltage drop in the filter, which in turn give the opportunity for operating with a lower dc-link voltage. However, the order of the filter will obviously also increase, which introduce additional resonance frequencies which may be needed to be damped either passively or actively in order to achieve a stable control system. Since the aim of this project is not on advanced filter analysis or current controller design, an often used LCL filter will be considered and designed.
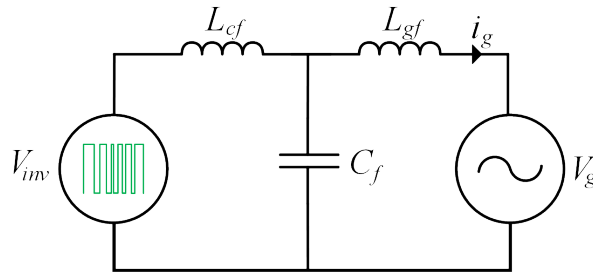

Figure 2.6: LCL Filter used to interface the converter with the grid.

Considering a balanced system, the filter design can be done on a per phase basis. The core loss of the two inductors and the winding resistance are neglected in the analysis, resulting in an worst case undamped situation [68]. Assuming the system in Figure 2.6 to be linear, then the grid current in the multiple input system can be represented as a linear combination of the independent input signals acting alone on the grid current. Since the task when designing the LCL filter is to comply with the harmonic distortion limits defined for i_g, the relationship between the output grid current and the inverter voltage is of interest and can be expressed as

$$G_{LCL} = \left.\frac{i_g(s)}{v_{inv}(s)}\right|_{V_g=0} = \frac{1}{s(L_{cf} + L_{gf}) + s^3 L_{gf} C_f L_{cf}} = \frac{1}{s(L_{cf} + L_{gf})} \cdot \frac{\omega_r^2}{s^2 + \omega_r^2}, \quad (2.4.1)$$

where the resonant frequency can be found to be

$$\omega_r = \frac{\sqrt{L_{cf} L_{gf} C_f (L_{cf} + L_{gf})}}{L_{cf} L_{gf} C_f} = \sqrt{\frac{L_{cf} + L_{gf}}{L_{cf} L_{gf} C_f}}. \quad (2.4.2)$$

The design of the converter-side inductor is a trade-off between the voltage drop across it and the ac current ripple. To limit the voltage drop during operation, the total filter inductance should be kept below 0.05-0.1 p.u. [64, 69]. The filter capacitance should be selected such that the decrease in power factor is less than 5% and that the resonant frequency should be kept within ten times the line-frequency and on half of the switching frequency in order to limit the resonance excitation by the harmonic spectrum from the converter [63]. Considering experimental tests, the grid-side inductor can be represented as an inductor together with the leakage inductance associated with the step-up transformer of the wind turbine $L_g = L_{gf} + L_{lT}$ [64]. The minimum converter-side inductance which results in a defined maximum current ripple is

$$L_{cf,min} = \frac{\sqrt{3}M_i V_{dc} T_s}{12\lambda_r I_1},\tag{2.4.3}$$

where M_i is the modulation index and λ_r is the allowed percentage ripple relative to the fundamental rms current, I_1. In [70], a ripple value around 25% is considered acceptable whereas in [52, 69] where offshore WTs are considered, the acceptable ripple considered is 10%. Equation (2.4.3) is derived for a converter modulated by THIPWM, but is reported to be equally applicable for SVM [70]. The maximum filter capacitance can be calculated according to the limitation of decrease in power factor. The capacitance is then limited to 5% of the base impedance, which is $Z_b = V_n^2/S_n$, where V_n is the rms line-to-line voltage and S_n is the nominal three-phase power. The base capacitance then becomes

$$C_b = \frac{1}{\omega_0 Z_b}\tag{2.4.4}$$

and the maximum filter capacitance is calculated as

$$C_f \leq \lambda_c \frac{S_n}{\omega_0 V_n^2}.\tag{2.4.5}$$

where $\lambda_c = 0.05$. The capacitance value can also be obtained by using the per-phase power and the line-to-neutral rms voltage instead in equation (2.4.5). The derivation of the capacitance is based on the assumption that the power factor is close to unity.

When the converter-side inductance and the filter capacitance is calculated, the grid-side inductance is calculated such that the injected grid current comply with the standards such as IEEE Std. 929-2000 and IEEE Std. 1547-2003. From [63, 70], if the filter is attenuating the first lower side-band harmonic of the switching frequency $(f_{sw} - 2f_0)$ to an acceptable value, the remaining distortion limits will be met. From this, the minimum grid-side inductance can be calculated as

$$L_{gf} = \frac{1}{L_{cf}C_f\omega_h^2 - 1} \cdot \left(L_{cf} + \frac{|v_{inv}(j\omega_h)|}{\omega_h \lambda_h I_1} \right),\tag{2.4.6}$$

where $\omega_h = 2\pi(f_{sw} - 2f_0)$, $|v_{inv}(j\omega_h)|$ is the magnitude of the converter voltage harmonic at that frequency before the grid-side inductance is added, and λ_h is the percentage distortion limit for that given harmonic. To give some margin this can be set to half of the maximum distortion limit [70]. According to [71], the amplitude of the voltage harmonic can in the case of SVM be calculated as

$$
A_{mn} = \frac{4V_{dc}}{m\pi^2}
\begin{bmatrix}
\frac{\pi}{6}\sin\left(\frac{(m+n)\pi}{2}\right)\left(J_n\left(\frac{3mM_i\pi}{4}\right) + 2\cos\left(\frac{n\pi}{6}\right)J_n\left(\frac{\sqrt{3}mM_i\pi}{4}\right)\right) \\
\left. +\frac{1}{n}\sin\left(\frac{m\pi}{2}\right)\cos\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{6}\right)\left(J_0\left(\frac{3mM_i\pi}{4}\right) - J_0\left(\frac{\sqrt{3}mM_i\pi}{4}\right)\right)\right|_{n\neq 0} \\
+\sum_{\substack{k=1 \\ k\neq -n}}^{\infty}
\left\{
\begin{array}{l}
\frac{1}{n+k}\sin\left(\frac{(m+k)\pi}{2}\right)\cos\left(\frac{(n+k)\pi}{2}\right)\sin\left(\frac{(n+k)\pi}{6}\right)\cdot \\
\left(J_k\left(\frac{3mM_i\pi}{4}\right) + 2\cos\left(\frac{(2n+3k)\pi}{6}\right)J_k\left(\frac{\sqrt{3}mM_i\pi}{4}\right)\right)
\end{array}
\right\} \\
+\sum_{\substack{k=1 \\ k\neq n}}^{\infty}
\left\{
\begin{array}{l}
\frac{1}{n-k}\sin\left(\frac{(m+k)\pi}{2}\right)\cos\left(\frac{(n-k)\pi}{2}\right)\sin\left(\frac{(n-k)\pi}{6}\right)\cdot \\
\left(J_k\left(\frac{3mM_i\pi}{4}\right) + 2\cos\left(\frac{(2n-3k)\pi}{6}\right)J_k\left(\frac{\sqrt{3}mM_i\pi}{4}\right)\right)
\end{array}
\right\}
\end{bmatrix},
\tag{2.4.7}
$$

where m is the multiple of the switching frequency and n is the order of the fundamental frequency. $J_p(x)$ is the pth order of the Bessel function of the first kind expressed as

$$
J_p(x) = \sum_{k=0}^{\infty} \frac{(-1)^k}{k!(k+p)!}\left(\frac{x}{2}\right)^{2k+p}.
\tag{2.4.8}
$$

Equation (2.4.7) is derived from the naturally sampled SVM. To evaluate the harmonic amplitudes for double-edge asymmetrical sampled SVM simply substitute m with $q = m + n(\omega_0/\omega_{ca})$ in all the Bessel's functions only, where ω_{ca} is the carrier frequency. Based on the design guidelines just described, a maximum converter current ripple of 15%, and the simulation system parameters shown in Table 1.4, the values for the LCL filter is calculated to be

$$
L_{cf} = 5.92 \ mH
\tag{2.4.9}
$$

$$
C_f = 7.31 \ \mu F
\tag{2.4.10}
$$

$$
L_{gf} = 517 \ \mu H
\tag{2.4.11}
$$

The grid-side inductance is calculated using equation (2.4.7) considering naturally sampled SVM and with $\lambda_h = 0.0012$, which is 40% of the distortion limit at the 48th harmonic. This filter gives a resonance frequency of $f_r = 2.7\,kHz$ which satisfies

$$
10f_0 < f_r < 0.5f_{sw}.
\tag{2.4.12}
$$

The leakage inductance of the WT transformer connected to a medium-voltage network is normally in the range of 0.04-0.06 pu [67]. Considering this to be valid here as well with a voltage base of $400\,V$ (l-l rms) and a power base of $7.35\,kVA$, this is equivalent to a leakage inductance of $3\,mH$, which means that no additional grid-side inductance needs to be used in this case in conformity with the conducted filter design. Since the actual transformer is not considered in this project and the voltage levels in the entire system will be the same (low-voltage), only its leakage inductance will be included. Therefore, a $3\,mH$ inductor is used as the grid-side filter to emulate the presence of the transformer by including its impedance. To that end, any additional line and grid impedance will simply add to the equivalent grid-side impedance, which results in an even more smooth output current.

Now that the considered hardware have been described, modeled, and designed, the remainder of the report will address the converter control and its operation under normal as well as fault conditions.

3 Control of Grid-Connected Converters

This chapter has the purpose of identifying the state-of-the-art control solutions for grid-connected converters in both current-mode and voltage-mode control. Firstly, the current-mode control structure will be described, which includes analysis of converter-current control, the influence of delays caused by the digital control, and a description of design guidelines. To that end, grid-voltage feed-forward control, the design of the Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) and associated sequence filters, and the design of the dc-link voltage control will be given.

Subsequently, a thorough description of the voltage-mode control structure, namely the SPC, will be given. This comprises a detailed description and design of droop controllers, the PLC, the RPC, together with the virtual admittance and the inner current control. These two fundamentally different control structures will then be tested and compared in later chapters of this project.

3.1 Current-Mode Control

This section is developed to design the current-mode controller for the grid-connected VSC equipped with an output LCL filter. This includes an understanding the effects of time delay has on the system stability. Besides this, controller designs of the current loop, the PLL and the Direct Voltage Controller (DVC) are made and described. The converter including the different control loops can be seen in Figure 3.1. This is a repeated figure without local load of the grid-following converter presented in Figure 1.3 where the current controller (G_{ci}), the PLL and the DVC (G_{cdc}) are to be designed in the following subsections.
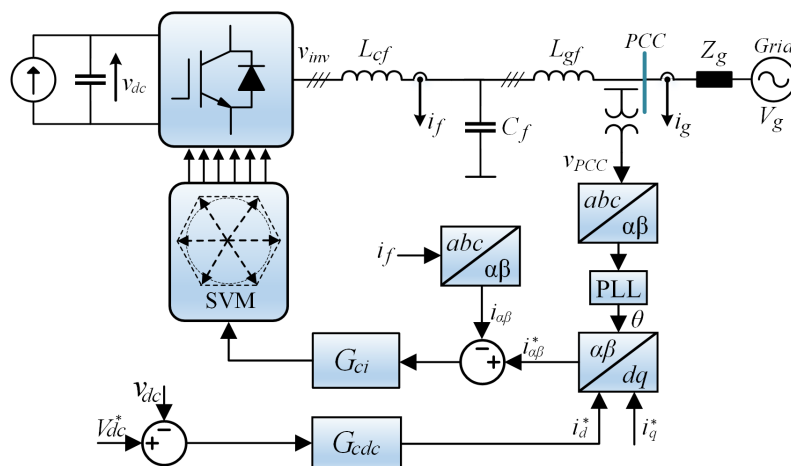

Figure 3.1: VSC control block diagram including current controller, PLL and dc-link voltage controller.

3.1.1   Design of Converter-Current Controller

In order for grid-connected converters to regulate the current injected into the grid, the converter currents need to be controlled in a negative feedback loop. The controller is usually implemented either as a PI controller in the synchronous-reference frame or as a PR-controller in the stationary-reference frame. Basically, the PR controller is equivalent to the double dq-reference frame current control. However, the controller gains in either case are the same and the controllers are equivalent in a balanced system [72]. Normally, the converter current is used as the feedback signal for the controller, since this is already measured for protection against over-current and therefore provides a more cost-efficient solution. The relationship between converter voltage and the converter current and the grid current are

$$G_{if}(s) = \frac{i_f(s)}{v_{inv}(s)}\bigg|_{V_g=0} = \frac{s^2 + \omega_{LC}^2}{L_{cf}s(s^2 + \omega_r^2)}, \tag{3.1.1}$$

and

$$G_{ig}(s) = \frac{i_g(s)}{v_{inv}(s)}\bigg|_{V_g=0} = \frac{1}{s(L_{cf} + L_{gf}) + s^3 L_{gf} C_f L_{cf}} = \frac{1}{s(L_{cf} + L_{gf})} \cdot \frac{\omega_r^2}{s^2 + \omega_r^2}, \tag{3.1.2}$$

respectively, where

$$\omega_{LC} = \frac{1}{\sqrt{L_{gf} C_f}} \tag{3.1.3}$$

and

$$\omega_r = \sqrt{\frac{L_{cf} + L_{gf}}{L_{cf} L_{gf} C_f}}. \tag{3.1.4}$$

At this point, the grid impedance Z_g is considered to be zero, i.e. $V_g = V_{PCC}$. Since a third-order plant complicates the controller design, only the dominant pole can be considered with a negligible error in the low-frequency range. For frequencies below half
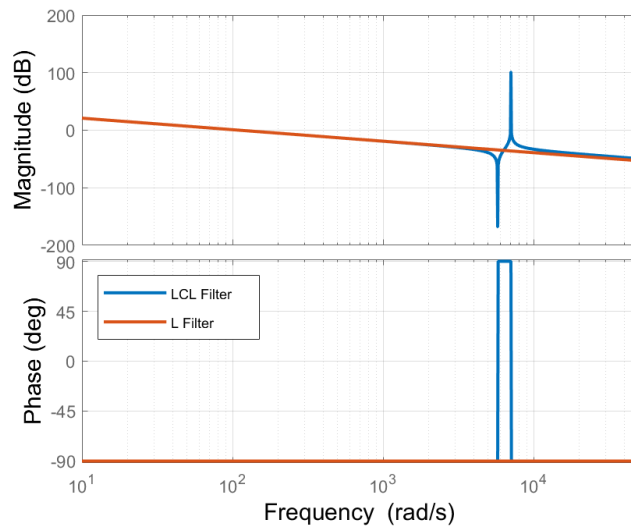

Figure 3.2: Frequency response of $G_{if}(s)$ considering an L filter and an LCL filter impedance with filter values from Table 1.4. For the L-filter $L = L_{cf} + L_{gf}$. Any equivalent series resistance is neglected.

of the filter resonance, assuming the LCL filter to be an aggregated inductor gives no practical differences from the full-order representation, no matter whether the converter current or the grid current is to be controlled. This point can be seen in Figure 3.2 where the frequency response of the two filters are seen to be matching in the low-frequency range. From this, the open-loop transfer function of the current control loop is shown in Figure 3.3 and can be expressed as

$$G_{ol,c}(s) = \frac{K_p s + K_i}{s} \cdot \frac{e^{-T_d s}}{(L_{cf} + L_{gf})s}, \tag{3.1.5}$$

where the time delay is $T_d = 1.5T_s$ due to the digital implementation (T_s) and the digital modulator ($0.5T_s$) with T_s being the sampling period. As it can be seen, the 2L-VSC is not included in the diagram. This is because when considering the linear averaged model of the inverter, it simply cancels in the control block diagram. This is, the voltage reference obtained from the output of the current regulator should be divided by $V_{dc}/2$ to get the duty cycles. Then using the average model of the inverter, the linear gain between the duty cycles and the phase voltages are $V_{dc}/2$, hence, these cancel out in the block diagram and are not included in the analysis. Only the delay associated with the PWM operation and the digital control is included. The delay is the root cause of system instability due to a decreasing phase as the frequency increases, which at some point will result in an unstable system. The phase lag introduced by the delay, plant, and current regulator at the crossover frequency is

$$\angle \left(\left(K_p + \frac{K_i}{j\omega_c} \right) \frac{e^{-j\omega_c T_d}}{j\omega_c (L_{cf} + L_{gf})} \right) = -\tan^{-1}\left(\frac{1}{\omega_c \tau_i} \right) - \frac{\pi}{2} - \omega_c T_d = -\pi + \phi_m \tag{3.1.6}$$

where $\tau_i = K_p/K_i$, and the phase of the plant is approximated as $-\pi/2$ provided that the inductor resistance is small or that $\omega_c(L_{cf} + L_{gf})/R \gg 1$. Limiting the phase lag from the controller by selecting $\omega_c \tau_i \gg 1$ then $\tan^{-1}(1/(\omega_c \tau_i)) \approx 0$. Using this approximation, the instability of the system occurs when the phase is $-\pi$ (i.e. a zero phase margin), which is at the critical crossover frequency fulfilling

$$-\pi = -\frac{\pi}{2} - \omega_c 1.5T_s \tag{3.1.7}$$

$$\rightarrow \quad \omega_c = \frac{\pi}{3T_s} = \frac{2\pi}{6T_s} = \frac{\omega_s}{6}, \tag{3.1.8}$$

which means that the critical crossover frequency is one sixth of the sampling frequency. The critical proportional gain can be found by solving the open-loop gain equal to unity at the critical frequency, ω_c [73]. This gives a critical value for the proportional gain of 94.25. When designing the controller, the proportional gain should be selected to get a desired non-zero phase margin. Here, it should be kept in mind that the integral gain is selected to minimize the controller phase delay ($\omega_c \tau_i \gg 1$). This is often done by placing the controller zero at least one decade below the crossover frequency. From the phase lag introduced by the plant, delay, and controller while considering a desired phase margin, the desired crossover frequency (where the open-loop gain crosses 0 dB) is

$$-\pi + \phi_m = -\frac{\pi}{2} - 1.5T_s \omega_c \rightarrow \omega_c = \frac{\pi/2 - \phi_m}{1.5T_s}. \tag{3.1.9}$$
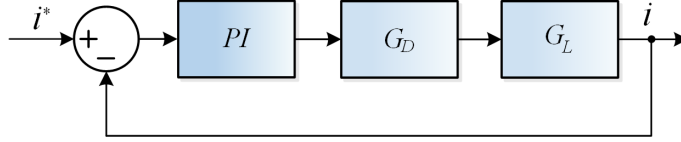
Figure 3.3: General control block diagram of current loop including controller
delay and simplified plant.

This means at this frequency, the magnitude of the open-loop transfer function should be
1 or 0 dB, expressed as

$$1 = \left| \left(K_p + \frac{K_i}{j\omega_c} \right) \frac{e^{-jT_d\omega_c}}{j\omega_c(L_{cf} + L_{gf})} \right| = \frac{K_p\sqrt{(\tau_i\omega_c)^2 + 1}}{\omega_c^2\tau_i(L_{cf} + L_{gf})}, \tag{3.1.10}$$

which gives

$$K_p = \omega_c(L_{cf} + L_{gf}), \tag{3.1.11}$$

considering that $(\tau_i\omega_c)^2 \gg 1$ which is ensured by selecting the controller zero to be placed
one decade below the desired crossover frequency. Using the inductance values shown in
Table 1.4 and a phase margin of $\pi/4$, the proportional gain can be calculated to be

$$K_p = 47.12. \tag{3.1.12}$$

From this, the integral gain is calculated to place the controller zero one decade below ω_c
($\tau_i = 10/\omega_c$) as

$$K_i = K_p \cdot \frac{\omega_c}{10} = 24674. \tag{3.1.13}$$

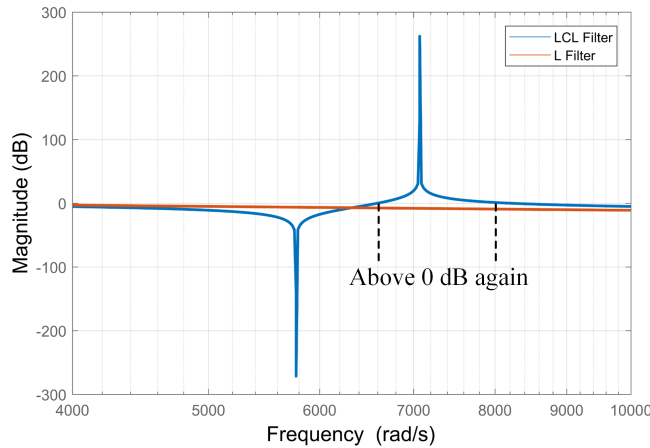Using this controller, the phase margin was found to be 39°, which is a bit below

Figure 3.4: Open-loop bode diagram of PI controller, exact delay and LCL
filter for both L and LCL filter, where the instability effects caused by LCL
filter around resonant frequency are highlighted. $K_p = 25$, $K_i = 24000$, and
the parameters for the LCL filter is given in Table 1.4.

the desired. Also, this phase margin was calculated when the plant is considered as
an aggregated inductor. When the transfer function of the full LCL filter is included
together with the PR controller, the system was actually unstable due to the resonant

frequency of the LCL filter causing the magnitude response to once again increase above 0 dB in the frequency range highlighted in Figure 3.4 with a negative phase margin. Therefore, in order to achieve an acceptable response considering the high-frequency instability caused by the LCL filter, the proportional gain was lowered to 25 and the integral changed to 24000, which resulted in the desired phase margin with a gain margin of 11 dB and a closed loop bandwidth of 1 kHz for the plant considered as an aggregated inductor. Using these parameters and considering the high-frequency effects of the LCL filter, the gain margin, phase margin, and closed loop bandwidth are 4.7 dB, 12.8°, and 665 Hz, respectively. This phase-margin will generally be considered as low and can be increased to around 25° by reducing the proportional gain to 10 and the integral gain to 2000. However, this will also result in a decreased closed-loop bandwidth to around 250 Hz, which is desired to be fast when included several slower outer control loops. Accordingly, this design ($K_p = 25$, $K_i = 24000$) is kept for now and may be retuned at a later stage if necessary. Implementing the current controller in the stationary-reference frame has certain advantages compared to the synchronous-reference frame, since this controller implementation inherently compensates both positive and negative sequence components as will be necessary in later sections. Furthermore, when operating in the stationary-reference frame, there are no need for trigonometric calculations involving the Park transform and decoupling networks, which reduces the computational burden of the digital controller [23]. Shifting the PI controller from the synchronous-reference frame with $-\omega_0$, the equivalent controller is achieved in the stationary-reference frame for the positive-sequence component. This is done by substituting $s \to s - j\omega_0$ which gives

$$G_{PI}^+ = G_{PI}(s - j\omega_0) = K_p + \frac{K_i}{s - j\omega_0}. \tag{3.1.14}$$

If the shift instead is performed with $+\omega_0$, the equivalent controller in the stationary-reference frame is obtained for the negative sequence as

$$G_{PI}^- = G_{PI}(s + j\omega_0) = K_p + \frac{K_i}{s + j\omega_0}. \tag{3.1.15}$$

By adding the transfer function for the positive and negative sequence controller expressed in the stationary-reference frame, the often used PR controller emerges as

$$G_{PR} = G_{PI}^+ + G_{PI}^- = 2K_p + \frac{2K_i s}{s^2 + \omega_0^2}, \tag{3.1.16}$$

Therefore, the gains just calculated will be used on the resonant controller as ($2K_p = 25$, $2K_i = 24000$) where the controller is able to track the sinusoidal reference at ω_0. Using this, the open-loop bode diagram is as shown in Figure 3.5. Here both the resonance from the controller and the parallel and series resonance of the LCL filter can be seen. The PR controller then provides an infinite open-loop gain at the positive and negative sequence fundamental frequencies which enables unity gain and zero phase shift at that frequency in the closed-loop system [74]. Using this structure, several paralleled resonant terms can be included in the control for accurate closed-loop control of harmonic components as well as the fundamental component.

3.1.2 Improving Resonant Controllers for Digital Implementation

When implementing the PR controller digitally, a widely used technique is to use two interconnected integrators, where the direct integrator is discretized used the forward
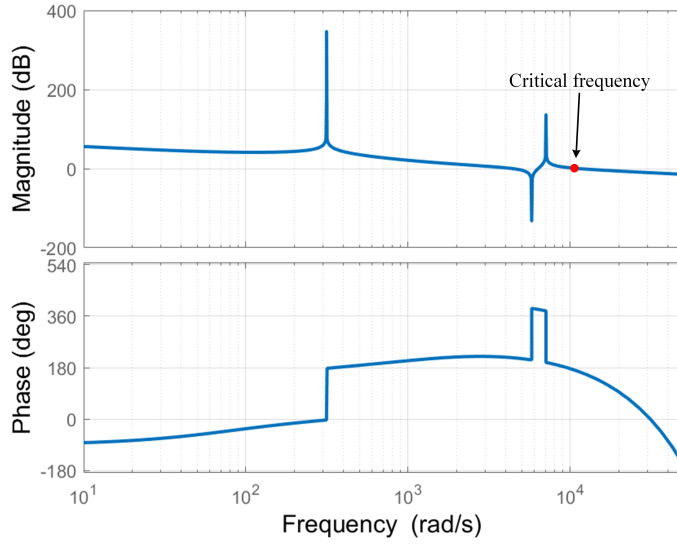
Figure 3.5: Open-loop bode diagram of PR controller, exact delay and LCL filter. $2K_p = 25$, $2K_i = 24000$, and the parameters for the LCL filter is given in Table 1.4.

Euler method and the feedback integrator is discretized using the backward Euler method. Proposals using the Tustin transformation have also been given, but this highly used choice of digital implementation results in the most significant deviation in the resonant frequency considering the discretized resonators [74]. Unfortunately, the discretization of the resonant controller is introducing an error in the location of the desired resonant frequency [75]. The implementation with the forward and backward Euler method unfortunately also implies that accurate tracking is not possible. In [75], it is concluded that the interconnection of the two discrete integrators has a high computational efficiency (low burden) and acceptable frequency adaption, but at the expense of a displacement of the resonant poles, which means that the open-loop gain at the designed frequency is reduced, effectively introducing steady-state errors in the controlled current. Furthermore, the digital implementation of the controller results in a time-delay, introducing a phase-lag to the regulator. Hence, to improve the stability and frequency response of the regulator this phase-lag should be compensated by introducing a phase-lead term into the controller and the displacement of the resonant poles should be corrected [76, 77].

To compensate the system delay, a phase lead term ϕ_h is introduced around the targeted harmonic frequency $h\omega_0$. The continuous representation of the PR controller including delay compensation is [78]

$$G_{PR}^d(s) = 2K_p + 2K_i \frac{s\cos(\phi_h) - h\omega_0\sin(\phi_h)}{s^2 + (h\omega_0)^2}, \qquad (3.1.17)$$

which when discretized becomes [75]

$$G_{PR}^d(z) = 2K_p + 2K_iT_s \frac{z^{-1}(\cos(\phi_h) - h\omega_0 T_s \sin(\phi_h)) - z^{-2}\cos(\phi_h)}{1 - 2z^{-1}(1 - (h\omega_0 T_s)^2/2) + z^{-2}}, \qquad (3.1.18)$$

where superscript d denotes that delay compensation is included. It should be noted that during the discretization, the phase-lead introduced in the continuous transfer function will

not be equal to the resulting phase-lead seen when implementing its discrete equivalent. Thus, the discrete transfer functions will not provide infinite gain at the selected frequency. Problems regarding inaccurate resonance frequency and phase-lead compensation will now be addressed.

Correction of Resonant Frequency

In order to achieve accurate resonant frequency placement it is shown in [79], that the discrete transfer function should have a denominator on the following form

$$Den(z) = 1 - 2z^{-1}\cos(h\omega_0 T_s) + z^{-2}. \tag{3.1.19}$$

As can be seen from equation (3.1.18), the desired $\cos(h\omega_0 T_s)$ term is represented as a second-order Taylor-series approximation. Since the online calculation of trigonometric functions is infeasible, one could include a better approximation for the cosine term, i.e. using a higher-order approximation in equation (3.1.18). The trigonometric cosine function can be represented as the infinite series

$$\cos(h\omega_0 T_s) = \sum_{n=0}^{\infty} (-1)^n \frac{(h\omega_0 T_s)^{2n}}{(2n)!} \tag{3.1.20}$$

The term $(h\omega_0)^2$ is provided by the PLL from outside the resonant controller, hence the following form of the controller can be written as

$$G_{PR}^d(z) = 2K_p + 2K_i T_s \frac{z^{-1}(\cos(\phi_h) - h\omega_0 T_s \sin(\phi_h)) - z^{-2}\cos(\phi_h)}{1 - 2z^{-1}(1 - C_h T_s^2/2) + z^{-2}} \tag{3.1.21}$$

where equating $(1 - C_h T_s^2/2)$ to equation (3.1.20) gives

$$C_h = 2\sum_{n=1}^{\infty} (-1)^{n+1} \frac{(h\omega_0)^{2n} T_s^{2(n-1)}}{(2n)!}. \tag{3.1.22}$$

Thus by letting C_h include a higher-order approximation of the cosine function, the resonance frequency displacement will be reduced. In [75], it is shown that by including 2-3 terms in the approximation of C_h, the steady-state error up to the 20th harmonic is negligible. The first three terms of C_h is

$$C_h = h^2 \omega_0^2 - h^4 \frac{\omega_0^4 T_s^2}{12} + h^2 \frac{\omega_0^6 T_s^4}{360}. \tag{3.1.23}$$

Correction of Phase-Lead Angle

As derived in [75], in order to achieve an accurate delay compensation, the numerator in equation (3.1.21) should be altered to match the zeros of the PR controller discretized with the impulse invariant method. Doing so, the PR controller should be implemented in the following form

$$G_{PR}^d(z) = 2K_p + 2K_i T_s \frac{z^{-1}\cos(h\omega_0 T_s + \phi_h) - z^{-2}\cos(\phi_h)}{1 - 2z^{-1}(1 - C_h T_s^2/2) + z^{-2}}, \tag{3.1.24}$$

where

$$\phi_h = \frac{3}{2} h\omega_0 T_s \tag{3.1.25}$$
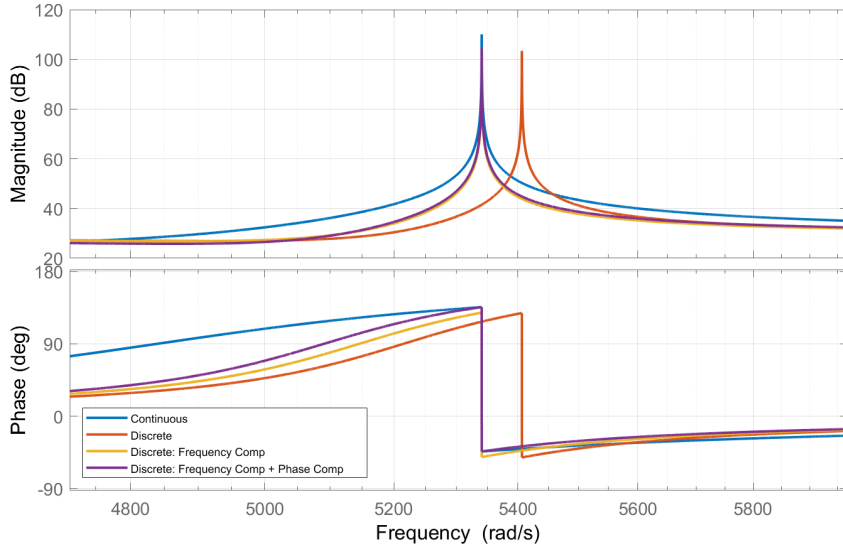
Figure 3.6: Bode diagram of PR controller improvement. Continuous is equation (3.1.17), Discrete is equation (3.1.18), Discrete: Frequency Comp is equation (3.1.21) and Discrete: Frequency Comp + Phase Comp is equation (3.1.24). Case shown for tracking of the 17th harmonic with same system parameters as in Figure 3.5.
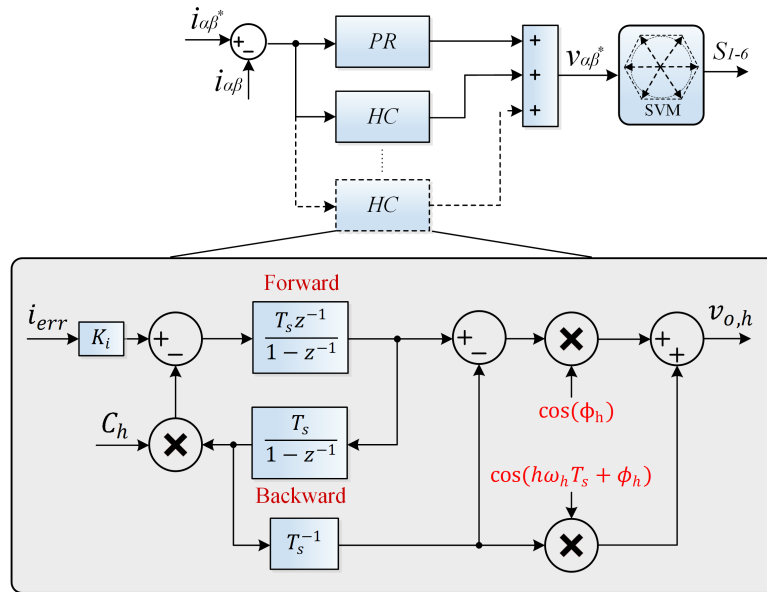

Figure 3.7: G_{ci} block diagram of the discretized PR controller including correction of resonant frequency and phase-lead angle. The implementation of one harmonic compensator (HC) is shown here.

in order to compensate the time delay associated with the computational delay and the delay of the PWM modulator [80]. The incremental improvements performed to the discretized PR controller is shown in Figure 3.6 where the regulator is controlled for the 17th harmonic. This is done since it is easier to visualize the improvements for higher frequencies. However, for near fundamental frequencies, discrepancies will also exist in the location of the resonant frequency. Thus, if the high open-loop gain occurs at a

narrow bandwidth, a small frequency error may introduce a significant steady-state error in the current tracking capability. It can be seen, that without correction of the resonant frequency, the controller resonates at the wrong frequency. Also, with the phase-lead angle compensation introduced in equation (3.1.24), the phase does not match the desired continuous counterpart.

This discrete transfer function in equation (3.1.24) can be represented by the block diagram depicted in Figure 3.7, where both the correction of the resonance frequency and phase-lead angle are included.

3.1.3 Grid-Voltage Feed-Forward

To improve the disturbance rejection capability of the control system and enhance the dynamic response of the current controller, voltage feed-forward can be added to the reference voltage generated from the current regulator. By using the measured PCC voltage directly as a feed-forward term in the control, improved steady-state performance, low current distortion, and fast response to grid transients such as voltage sags are possible [81–83]. Therefore, this section has the aim to analyze the influence that voltage feed-forward has on the system performance and decide whether this should be used to enhance the converter performance during fault situations. Using the circuit diagram shown in Figure 2.6 and also considering a nonzero grid impedance Z_g, the transfer function from the inverter voltage and grid voltage to converter current are

$$G_1(s) = \frac{i_f(s)}{v_{inv}(s)} = \frac{Z_2 + Z_g + Z_c}{Z_c(Z_1 + Z_2 + Z_g) + Z_1(Z_2 + Z_g)} \tag{3.1.26}$$

and

$$G_2(s) = \frac{i_f(s)}{v_g(s)} = \frac{Z_1(Z_2 + Z_g + Z_L) - (Z_2 + Z_g)(Z_2 + Z_g)}{Z_1(Z_c(Z_2 + Z_g) + Z_1(Z_2 + Z_g + Z_c))} \tag{3.1.27}$$

respectively, where $Z_1 = R_{cf} + sL_{cf}$, $Z_2 = R_{gf} + sL_{cf}$, and $Z_c = 1/(sC_f)$. This can be represented as the block diagram shown in Figure 3.8 where $G_{PR}(s)$ is the PR current controller and $G_d(s)$ is the delay. Here, the open-loop transfer function is

$$L(s) = G_{PR}(s)G_d(s)G_1(s) \tag{3.1.28}$$

with the following closed-loop expression

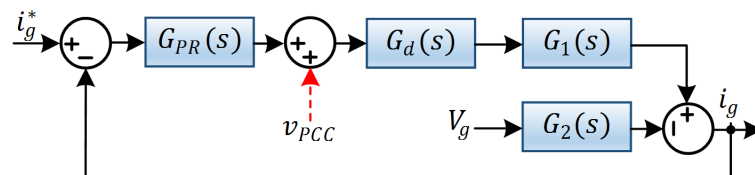$$G_{cl}(s) = \frac{i_f(s)}{i_f^*(s)} = \frac{L(s)}{1 + L(s)} \tag{3.1.29}$$

Figure 3.8: Block diagram of grid current including control and grid. The red line denotes the voltage feed-forward control. Here, it is assumed that i_g and i_f are identical at the fundamental frequency since the capacitor current has mostly high-frequency content.

and the sensitivity function to the grid voltage is

$$d(s) = \frac{i_f(s)}{v_g(s)} = -\frac{G_2(s)}{1 + L(s)}. \tag{3.1.30}$$

The block diagram of the control loop including the disturbance from the grid voltage was depicted in Figure 3.8, which were derived without considering the voltage feed-forward. Next, the voltage feed-forward seen in the dashed red line will be included in the analysis. Since the grid voltage is not directly known, the PCC voltage is used as an approximation of the grid voltage to try to cancel the disturbance from the actual grid voltage. By knowing that the PCC voltage is

$$V_{PCC}(s) = V_g(s) + i_g(s)Z_g(s), \tag{3.1.31}$$

the control block diagram as shown in Figure 3.9a) can be constructed. This can be further simplified to the control block diagram shown in Figure 3.9 b) where the sum block in the middle can be eliminated and moved to the input and output, respectively. To achieve this, the part with $V_g(s)$ can be added to the output as $V_g(s)G_d(s)G_1(s)$ and the part with $Z_g(s)$ can be added to the input as $Z_g(s)/G_{PR}(s)$. From this, the loop gain can be calculated by first ignoring the independent disturbance V_g and then calculate the closed-loop transfer function of the positive feedback, which then will be the loop gain since the negative feedback term is a unit gain. This is

$$L_{FF}(s) = \frac{G_{PR}(s)G_d(s)G_1(s)}{1 - Z_g(s)G_d(s)G_1(s)}. \tag{3.1.32}$$

From this, it can be noticed that by introducing the feed-forward voltage control, a positive feedback loop emerges in the control, which can cause a destabilizing effect, which is seen to be dependent on $Z_g(s)$. The closed-loop transfer function, and the sensitivity function to grid disturbances of the feed-forward control can be written as

$$G_{cl,FF}(s) = \frac{G_1(s)G_d(s)G_{PR}(s)}{1 + G_d(s)G_1(s)(G_{PR}(s) - Z_g(s))} \tag{3.1.33}$$

and

$$d_{FF}(s) = \frac{i_g(s)}{V_g(s)} = \frac{-G_2(s) + G_d(s)G_1(s)}{1 + G_d(s)G_1(s)(G_{PR}(s) - Z_g(s))}, \tag{3.1.34}$$

respectively. Thus, by using the feed-forward control two resultant effects follow: improved disturbance rejection since the term $G_d(s)G_1(s)$ is introduced in the numerator and an
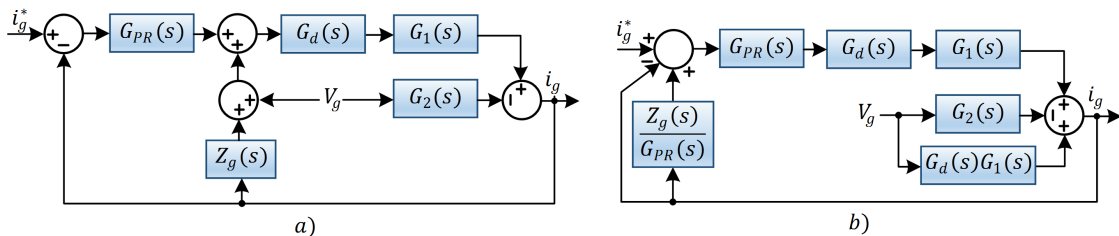

Figure 3.9: Block diagram of control loop including voltage feed-forward.
a): replacing the PCC voltage with the grid voltage, grid current and grid impedance. b): Simplification of the block diagram shown in a)

added positive feedback path, which degrades the stability as a function of the impedance $Z_g(s)$. If the grid voltage could be used as the feed-forward term, exact disturbance rejection is obtained. However, as mentioned, the grid voltage is unknown, which means that the disturbance rejection will not be optimal. As it can be seen from the positive feedback path, $G_{PR}(s)$ will be canceled but the stability of the feed-forward control scheme is highly dependent on the impedance, $Z_g(s)$, which could be a problem for weak grids or in a case of multiple paralleled converters [81].

In Figures 3.10, 3.11, and 3.12, the bode plots of the closed-loop, open-loop and sensitivity function of the control system with and without feed-forward control can be seen, respectively. As it can be seen in Figure 3.10 and Figure 3.11, voltage feed-forward actually damps the resonant frequency of the LCL filter. In Figure 3.12, it can be seen that the rejection of disturbances is significantly improved using voltage feed-forward. However, the resonance occurring at around 1 kHz is shifted to lower frequencies for higher Z_g, which causes decreased robustness in the higher frequency range.
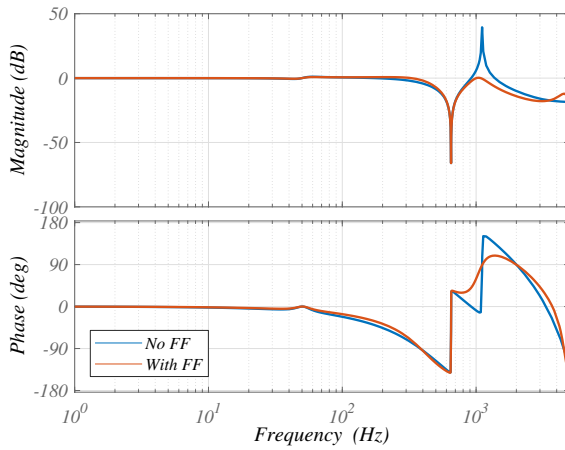

Figure 3.10: Bode plot of closed-loop transfer function of control system with and without voltage feed-forward. Z_g is 3 mH and LCL parameters are in Table 1.4.
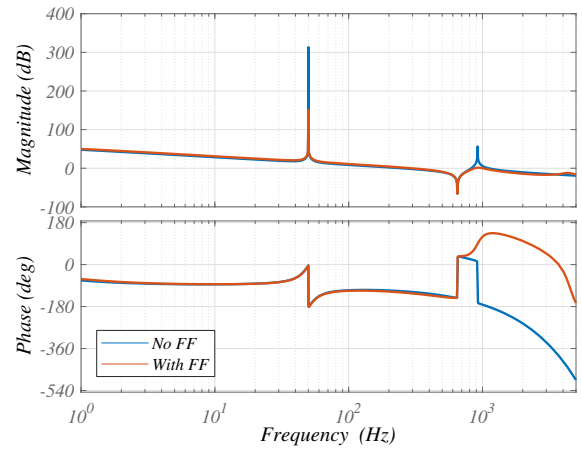
Figure 3.11: Bode plot of open-loop transfer function of control system with and without voltage feed-forward. Z_g is 3 mH and LCL parameters are in Table 1.4.

Hence as it has been presented, the use of feed-forward control of the PCC voltage is a trade-off between a high dynamic performance against e.g. voltage sags and the current loop stability and robustness. Besides the positive feedback loop, a delay associated with the sampling of the PCC voltage is also present, which further reduces the robustness of the controller. In [82], an improved voltage feed-forward control is proposed where a phase lead is added to the control in order to decrease its sensitivity to the grid impedance. In [83], it is discussed that a feed-forward control can be used to suppress grid current harmonics to achieve a good steady-state performance with low distortion since the harmonics from the grid is ideally canceled out. However it is explained that for high grid impedances, these harmonics from the grid will introduce a destabilized behavior. Therefore, it is proposed to use a Second-Order Generalized Integrator (SOGI) filter to extract only the fundamental component of the PCC voltage in the feed-forward term and then use PR controller to reduce the distortion of the injected grid current. By using the SOGI, the phase margin
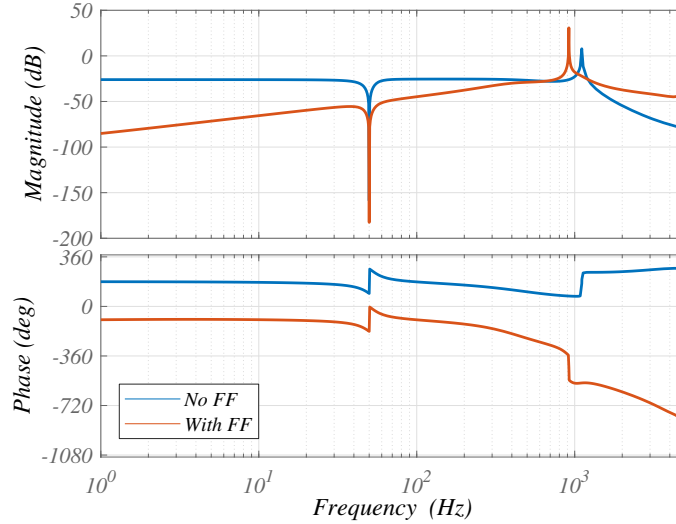
Figure 3.12: Bode plot of sensitivity of grid voltage disturbances to the injected current with and without voltage feed-forward (FF). Z_g is 3 mH and LCL parameters are in Table 1.4.

and gain margin of the control system can be significantly improved on the cost of a slower transient performance due to the SOGI and the need to use PR controllers to compensate grid harmonics. None of these proposals will be implemented in the control as it is, but may be considered for controller improvement if instabilities occur due to high grid impedances or multiple converter operation.

3.1.4 Design of SRF-PLL for Grid Synchronization

In order to inject a desired current, often expressed as desired active and reactive power, the instantaneous location of the PCC voltage vector has to be known. This implies that in order to construct the desired current references, the current amplitude needs to be known together with the angle of the grid voltage. The current amplitude and angle relative to the PCC voltage are obtained from outer power loops, dc-link control or just as predefined references. The most commonly used synchronization technique is the PLL, which is a closed-loop controller where an internal oscillator or clock is controlled to maintain or lock the phase of some external periodic signals, in this case the grid voltages or voltages at the point of connection [84, 85]. Commonly used is a SRF-PLL where a rotation transformation is used for phase detection [86]. The basic operation of the SRF-PLL is to ensure that the PCC voltage vector is aligned with the d-axis in the synchronous-reference frame. To do this, the phase error between the defined synchronous-reference frame and the PCC voltage vector is

$$\Delta\theta = \theta_{PCC} - \theta_{PLL}. \tag{3.1.35}$$

In closed-loop control, θ_{PLL} is regulated to ensure that $\Delta\theta = 0$, which gives that $v_{gq} = 0$ and the value of θ_{PLL} will be the desired angle. The PCC voltage space vector as depicted in Figure 3.13 can be written as

$$\boldsymbol{v_{gdq}} = Ue^{j(\theta_{PCC}-\theta_{PLL})}, \tag{3.1.36}$$

where U is the magnitude of the grid voltage. This principle however, has two options to regulate the q-axis component to zero. Either by aligning the d-axis with the grid

vector or the negative d-axis with the grid vector. In case of a normal control action where the measured signal is subtracted from the reference, then in the situation where the grid angle is larger than the estimated angle (θ_{PLL}), the q-axis component will increase, which means that the error will decrease, which eventually makes the PI controller to decrease the estimated angle. All this makes the synchronous frame to rotate away from the grid voltage vector. To solve this, the q-axis component is multiplied with minus one, such that the error signal will increase when the grid angle is larger, eventually causing the synchronous frame to increase its angle to synchronize with the positive d-axis.
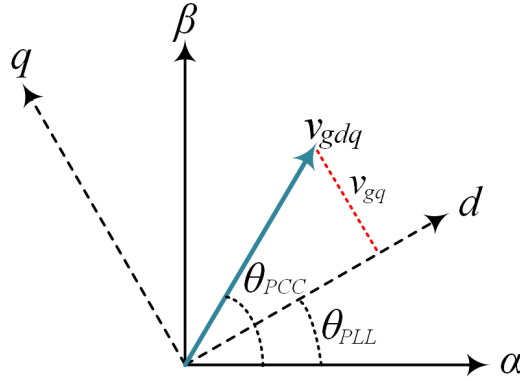

Figure 3.13: Representation of stationary and synchronous frame for the phase-locked loop operation.

To design the PI controller for the PLL, a small-signal model of the PLL is needed. The grid voltage vector is

$$\boldsymbol{v_{gdq}} = v_{gd} + jv_{gq} = Ue^{j(\theta_{PCC} - \theta_{PLL})}. \tag{3.1.37}$$

Assuming the phase error to be small, the exponential function can be approximated as $1 + j\Delta\theta$. Inserting this while only considering the q-axis component gives

$$v_{gq} = U(\theta_{PCC} - \theta_{PLL}). \tag{3.1.38}$$

The time-varying angle of the PCC voltage is

$$\theta_{PCC}(t) = \omega_0 t + \theta_0 \tag{3.1.39}$$

which when expressed in the Laplace variable includes a second-order pole at the origin. I.e. by using the final value theorem, a PI regulator will contain a steady-state error when trying to regulate such a system. To eliminate this steady-state error, a pure integrator is introduced after the PI controller. Since the small-signal model of the PLL is only valid when the error is small, an initial value for the controller is required during start-up. The start-up guess should be set to the angular velocity of the grid voltage, ω_0. The block diagram of the PLL can then be constructed and it is shown in Figure 3.14. The closed-loop transfer function of the PLL loop can be expressed as

$$\frac{\theta_{PCC}(s)}{\theta_{PLL}(s)} = \frac{T(s)}{1 + T(s)} = \frac{UK_p s + UK_i}{s^2 + UK_p s + UK_i}, \tag{3.1.40}$$
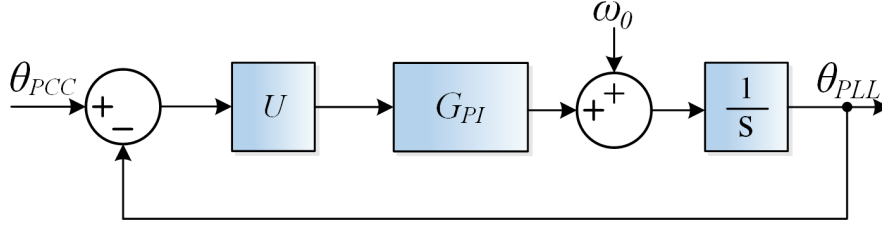
Figure 3.14: Block diagram of the used PLL.

where $T(s)$ is the open-loop gain. Since this is a second-order system on normalized form, the controller gains can be selected to achieve an approximate desired damping and natural frequency as

$$G_{2nd}(s) = \frac{2\zeta\omega_N s + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2},$$

(3.1.41)

where the relationship between the rise time and the natural oscillation frequency for the second order system can be approximated as

$$\omega_N \approx \frac{1.8}{t_r}$$

(3.1.42)

and the proportional and integral gain can be found to be

$$K_p = \frac{2\zeta\omega_N}{U} \qquad K_i = \frac{\omega_N^2}{U}$$

(3.1.43)

Selecting a desired damping of 0.707, a rise time of 50 ms and using $U = 1$ since the implementation will be performed using normalization of the PCC voltages, the proportional and integral gains are calculated to be $K_p = 50.9$ and $K_i = 1296$. For digital implementation, the integrators in the PLL are discretized using the backward Euler method.

3.1.5 Design of Complex Filter for SRF-PLL

In the case of ideal conditions as assumed until now, the grid voltage only consists of its fundamental positive-sequence component, which in many cases is the desired quantity to synchronize to. During an unbalanced situation or considering that the grid voltage contains harmonics, the grid voltage will consists of both positive and negative sequence components for the fundamental as well as its harmonic components. Hence, in order to inject e.g. balanced high-quality sinusoidal currents to the grid, the positive-sequence component of the grid voltage is needed. One way to do this, is to use symmetrical component theory to extract the positive-sequence component of the voltage signal and then synchronize to that. This is however rather slow, since it needs a delayed version of the stationary voltage vector. Furthermore, for a distorted grid, the harmonic components present in the signal will not be attenuated and will hence propagate into the control. Therefore, a more promising method is by using a filter to identify the positive sequence of the fundamental frequency. These filters can be divided into real-coefficient and complex-coefficient filters, where the complex coefficient filters will be considered since the real coefficient filters cannot distinguish in polarity of the frequency, i.e. it cannot just attenuate the negative sequence while freely passing the positive one [87].

To attenuate the fundamental negative sequence while providing unity gain at the fundamental positive sequence frequency, one can shift the location of unity gain by the fundamental frequency (ω_0) to the right to obtain unity gain at the positive sequence while providing attenuation at the fundamental negative sequence. A first-order low-pass filter employing this can be written as

$$CCF(s) = \frac{\omega_{cf}}{s - j\omega_0 + \omega_{cf}} = \frac{\frac{\omega_{cf}}{s - j\omega_0}}{1 + \frac{\omega_{cf}}{s - j\omega_0}}, \tag{3.1.44}$$

which has no phase change at the fundamental of the positive sequence. ω_{cf} is the cut-off frequency of the filter. Since this is a low-pass filter it will also participate in the attenuation of the grid harmonics. It should be noted that such a filter might not give acceptable results if the grid frequency deviates from the shifted one. Alternatively the filter could be adaptively changed dependent on the measured grid frequency from the PLL. Grid frequency variations are however not considered here. Equation (3.1.44) can be represented as a feedback loop in $\alpha\beta$ coordinates as it is seen in Figure 3.15 a).
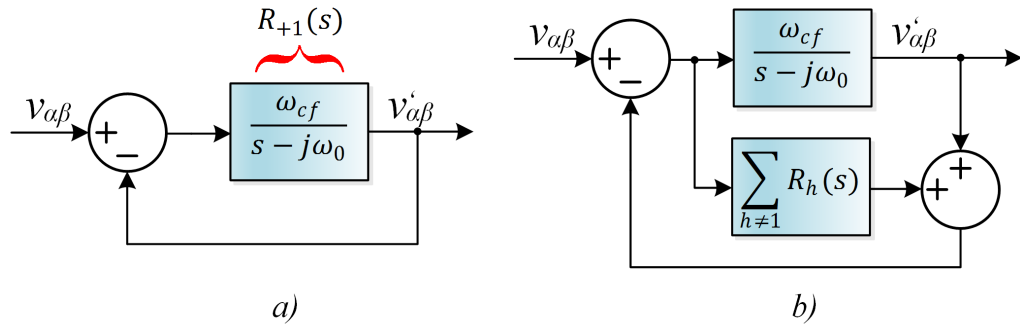

Figure 3.15: Block diagram of complex filter to be put between $\alpha\beta$ measurement of v_{PCC} and the PLL in Figure 3.1. a) shows the complex filter in the case of no attenuation for positive sequence component. b) shows the complex filter, which can remove any arbitrary positive/negative sequence component at a desired frequency.

The transfer function between the grid voltage and the filtered one is

$$CCF(s) = \frac{R_{+1}(s)}{1 + R_{+1}(s)} \quad \text{where} \quad R_{+1}(s) = \frac{\omega_{cf}}{s - j\omega_0}. \tag{3.1.45}$$

Hence for $s \to j\omega_0$, the open-loop gain tends to infinity, which gives that the closed-loop system tends to one, which is the desired response since the filter will not attenuate the positive sequence fundamental component. Besides this, it is desired to have an infinite attenuation at the negative sequence fundamental frequency, which is not achieved using this approach since letting $s \to -j\omega_0$ makes the open-loop system tend to $-\omega_{cf}/(j2\omega_0)$, eventually creating a closed-loop gain higher than zero. To achieve an infinite attenuation or zero gain of the negative-sequence component, one must let the open-loop transfer function tend to infinity when $s \to -j\omega_0$. This can be done by introducing the term $R_{-1} = \omega_{cf}/(s + j\omega_0)$ in the denominator of equation (3.1.45) as

$$CCF(s) = \frac{R_{+1}(s)}{1 + R_{+1}(s) + R_{-1}(s)} \to 0 \quad \text{as} \quad s \to -j\omega_0. \tag{3.1.46}$$

This procedure can be extended to any arbitrary positive/negative sequence harmonic to attenuate any unwanted frequencies from the measured grid voltage. Doing so, the filter transfer function can be written as

$$CCF(s) = \frac{R_{+1}(s)}{1 + R_{+1}(s) + \sum_{h \neq 1} R_h(s)}, \tag{3.1.47}$$

which is represented in its block diagram form in Figure 3.15 b). In Figure 3.16, the PCC voltages before and after filtering are presented. As it can be seen, the complex filter is capable of extracting only the fundamental positive sequence component of the distorted unbalanced voltage. The digital implementation of the complex filter is done as proposed in [87] and for the complex filter it is designed with a bandwidth of 35 Hz.
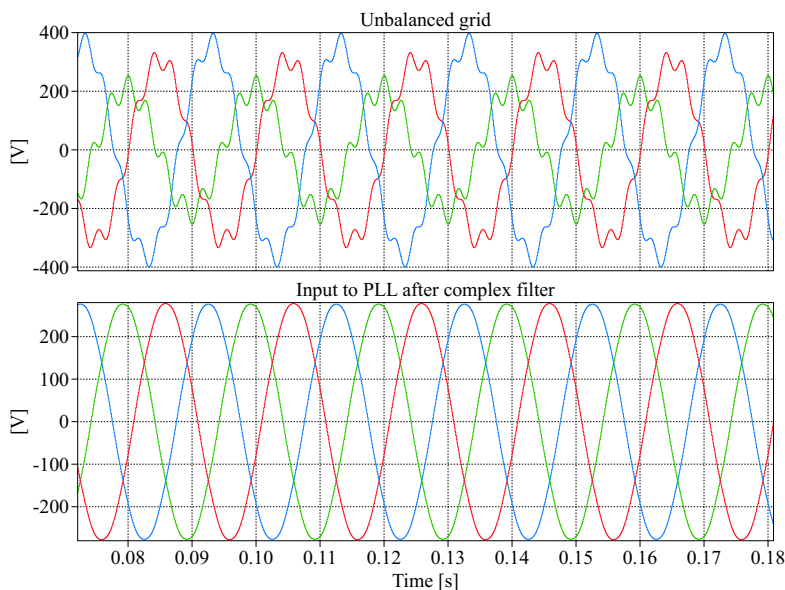

Figure 3.16: Performance of complex filter used to identify the fundamental positive sequence component from the distorted unbalanced grid voltage.

3.1.6   Design of DC-link Voltage Controller, G_{cdc}

When designing the inner current controller, a constant dc-link voltage is assumed. However, in most practical applications, the dc-side is connected to another converter extracting power from e.g. a WT or a PV system. In this case, the dc-link voltage is not constant but is determined from the power balance between the two converters. To improve the ac-side current quality and control the power flow, the dc-link voltage must be regulated. Furthermore, the ac-side voltage magnitude is desired to remain fixed, which means that the dc-link voltage must be kept at a value of around minimum two times the phase peak ac voltage to avoid over-modulation. This is the lower limit of the dc-link voltage whereas the upper limit is determined by the semiconductor and capacitor blocking voltage capability.

When the dc-link voltage is not considered constant, both the duty cycle and dc-link voltage are time-varying, which makes the modeling and control nonlinear. To deal with this, the outer dc-link voltage controller or DVC and the inner current controller can be decoupled by designing the dc-link control to be at least ten times slower than the inner

current loop. Doing this, the dc-link voltage can be assumed constant seen from the inner current controller and the current loop can be seen as a first-order low-pass filter or a simple unity gain seen from the DVC.

To establish a linear relationship between the dc- and the ac-side, the instantaneous power is considered, which is invariant between the two sides neglecting converter losses. Using this method, it is possible to select an ac-current reference, such that the dc-link voltage remains constant based on the average power exchange on the dc-link. The dc-link capacitance of the experimental converter setup is $C_{dc} = 500\mu F$ for a nominal power of $7.35\,\text{kVA}$, which will be the value considered for the dc-link controller in this part.

The active power balance of the system is

$$P_{WT} = P_{dc} + P_f + P_g, \tag{3.1.48}$$

where P_{WT} is the power received from the WT, P_{dc} is the power in the dc-link capacitor, P_f is the power loss in the inductive elements of the filter and P_g is the power delivered to the grid, where the large-signal equations can be expressed as

$$P_{dc} = \frac{dW_{dc}}{dt} = \frac{1}{2}C_{dc}\frac{d(v_{dc})^2}{dt}, \tag{3.1.49}$$

$$P_f = (i_d^2 + i_q^2)R_L + \frac{1}{2}L\frac{d(i_d^2 + i_q^2)}{dt}, \tag{3.1.50}$$

$$P_g = v_d i_d + v_q i_q. \tag{3.1.51}$$

Here, L is the sum of all the inductances and R_L is the sum of all the Equivalent Series Resistance of the output LCL filter. Using this, it is included that the instantaneous power in the filter is not zero. To be able to design the controller, the large-signal equations need to be perturbed and linearized. Doing so reveals the small-signal equations

$$\hat{P}_{WT} = \hat{P}_{dc} + \hat{P}_f + \hat{P}_g \quad \text{where} \tag{3.1.52}$$

$$\hat{P}_{dc} = C_{dc}V_{dc}\frac{d\hat{v}_{dc}}{dt} \tag{3.1.53}$$

$$\hat{P}_f = 2I_d R_L \hat{i}_d + LI_d\frac{d\hat{i}_d}{dt} \tag{3.1.54}$$

$$\hat{P}_g = V_d \hat{i}_d \tag{3.1.55}$$

$$\hat{P}_{WT} = I_{in}\hat{v}_{dc}, \tag{3.1.56}$$

where I_{in} is the constant input current and V_d is the peak value of the grid voltage. Using this, the expression for $\hat{P}_{WT}$ can be written as

$$I_{in}\hat{v}_{dc} = V_{dc}C_{dc}s\hat{v}_{dc} + V_d\hat{i}_d + 2I_d R_L\hat{i}_d + LI_d s\hat{i}_d \tag{3.1.57}$$

where the relationship between the dc-link voltage and the active current can be written as

$$G_{pdc}(s) = \frac{\hat{v}_{dc}}{\hat{i}_d} = \frac{V_d + sLI_d + 2I_d R_L}{I_{in} - sC_{dc}V_{dc}}, \tag{3.1.58}$$

which can be seen to be dependent on the operating point of the converter. This implies that during a change in operating point, the controller needs to be redesigned or adaptively corrected. To remedy this, the operating point can be fed forward after the controller,

which is to be discussed later in this section. Considering the inner current loop as a unity gain, the open-loop transfer function with a PI controller becomes

$$G_{c,dc}(s)G_{pdc}(s) = \frac{K_p s + K_i}{s} \cdot \frac{sLI_d + 2I_d R_L + V_d}{I_{in} - sC_{dc}V_{dc}}. \tag{3.1.59}$$

By letting the zero of the PI controller cancel the pole of the plant G_{pdc}, the following ratio should be chosen

$$\frac{K_i}{K_p} = \frac{-I_{in}}{C_{dc}V_{dc}}. \tag{3.1.60}$$

By selecting the proportional and integral gain as

$$K_p = \frac{2\pi f_{bwdc} C_{dc} V_{dc}}{V_d} \tag{3.1.61}$$

$$K_i = \frac{2\pi f_{bwdc} I_{in}}{V_d} \tag{3.1.62}$$

the ratio is kept unchanged and the parameters can be directly calculated based on the desired bandwidth of the closed-loop response. Using this, the closed-loop transfer function becomes

$$G_{cl}(s) = \frac{2\pi f_{bwdc}\left(s\frac{LI_d}{V_d} + \frac{2I_d R_L}{V_d} + 1\right)}{s\left(1 + 2\pi f_{bwdc}\frac{LI_d}{V_d}\right) + 2\pi f_{bwdc}\left(\frac{2I_d R_L}{V_d} + 1\right)}. \tag{3.1.63}$$

Here it can be seen from the first term in the denominator, that if the converter is operated in rectification mode (i.e. I_d is negative), a right half plane pole may exist. Hence, if the converter should be able to operate with bidirectional power flow, the stability has to be assessed in rectification mode as well as inversion mode.

One disadvantage of the DVC just discussed is that it is dependent on the operating point of the converter. To avoid this problem, one can regulate the power error instead of the dc-link voltage error. Using this method, feed-forward of the wind turbine generator power (P_{WT}) is included which is filtered through a low-pass filter. Neglecting the power loss in the output filter, the reference power obtained from the controller output is

$$P_{ref} = \left(K_{p,dc} + \frac{K_{i,dc}}{s}\right)\frac{(v_{dc}^{ref})^2 - v_{dc}^2}{2} + H_{dc}(s)P_{WT} \tag{3.1.64}$$

where $P_{WT} = I_{in}v_{dc}$ and

$$H_{dc}(s) = \frac{\alpha_d}{s + \alpha_d} \tag{3.1.65}$$

with $\alpha_d < 0.1\alpha_c$ with α_c being the bandwidth of the inner current controller [88]. To reduce the influence from the PCC voltage on the dc-link voltage, a filtered PCC voltage modulus is divided by the active power reference to achieve the d-axis current reference. The d-axis current reference is then

$$i_d^{ref} = \frac{P_{ref}}{E_f} \quad \text{where} \quad E_f = H_{dc}(s)\|V_{PCC}\|. \tag{3.1.66}$$

Since feed-forward is used, the integral gain can be selected just as a trimming function to obtain a desired response. Assuming the integral gain to be small, the proportional gain should be selected as

$$K_{p,dc} = \alpha_d C_{dc} \tag{3.1.67}$$

where α_d is the bandwidth of the DVC.

In the implementation of both types of DVCs, the controller output is multiplied with -1 since the plant is inherently incrementally negative. This is also seen from equation (3.1.60) where the ratio between the controller parameters should be negative. The control block diagram of the dc-link voltage controller independent on the operating point is shown in Figure 3.17.
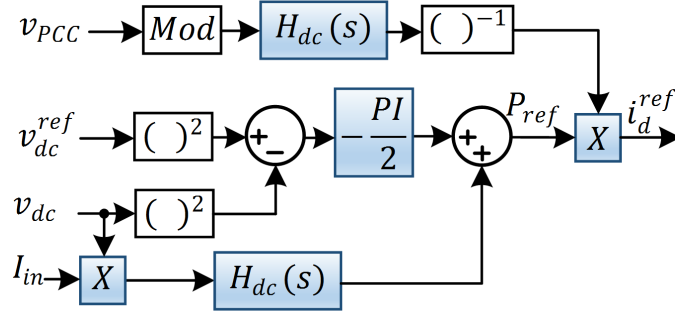

Figure 3.17: Block diagram of dc-link voltage controller with input power feed-forward. Besides the dc-link controller in Figure 1.3, the presented controller include a measurement of the dc-isde current and the voltage at the PCC.

3.2 Voltage-Mode Control

As mentioned in the introduction, the considered grid-forming and grid-supporting control structure is the one repeated in Figure 3.18. This section has the purpose of describing each control loop and block within the overall control system and design the controllers as it was done for the current-mode converter control presented in the previous section. By employing SPC as shown in Figure 3.18, the grid-connected converter is controlled
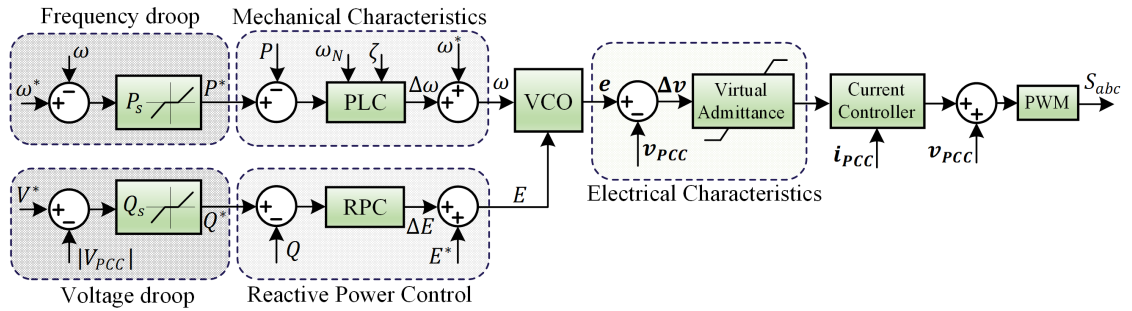
Figure 3.18: Considered control block diagram of the grid-forming synchronous power controller.

to emulate a conventional synchronous generator with virtual mechanical and electrical characteristics. The mechanical part of the synchronous generator is emulated by virtual inertia and damping, which aims to support the network frequency, and the electrical part is emulated by a virtual stator impedance, which can be used to define the power sharing and power exchange with the grid [32]. The PLC provides the converter with the mechanical property of a synchronous machine and calculates the virtual angular frequency of the emulated machine. The RPC provides the control with the voltage amplitude of

the virtual machine by controlling the reactive power. The virtual angular frequency is integrated to obtain the phase angle, which together with the voltage magnitude forms the inner virtual electromotive force of the emulated machine. As it can be seen in Figure 3.18, the SPC regulates the active power based on the frequency and regulates the reactive power based on the magnitude of the voltage. In this way, the converter exactly mimics the behavior of a synchronous machine.

Considering the two-bus diagram shown in Figure 3.19, the power exchange between the virtual machine and the grid can be calculated. The per-phase complex power injected
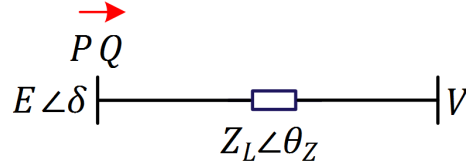

Figure 3.19: Two bus diagram used to calculate the power exchange between a virtual machine and the grid.

by the converter at the sending end bus is

$$\vec{S} = P + jQ = \vec{E}\vec{I}^* = \vec{E}\frac{\vec{E}^* - \vec{V}^*}{\vec{Z}^*} = Ee^{j\delta}\frac{Ee^{-j\delta} - V}{Ze^{-j\theta_Z}}, \tag{3.2.1}$$

where E and V represent the rms value of the sending-end and receiving-end bus voltage, respectively. Substituting the vectors with its complex variables and identifying the real and imaginary parts, the active and reactive powers are

$$P = \frac{E^2 R_L}{|Z_L|^2} + \frac{EV X_L \sin(\delta)}{|Z_L|^2} - \frac{EV R_L \cos(\delta)}{|Z_L|^2}, \tag{3.2.2}$$

$$Q = \frac{E^2 X_L}{|Z_L|^2} - \frac{EV X_L \cos(\delta)}{|Z_L|^2} - \frac{EV R_L \sin(\delta)}{|Z_L|^2}. \tag{3.2.3}$$

Considering that the electrical characteristics of the virtual machine are selectable, one can ensure that the stator output impedance is highly inductive. This simplifies the power transfer between the two buses to be

$$P = \frac{EV \sin(\delta)}{X} \approx \frac{EV\delta}{X} = \frac{P_{max}\delta}{3}, \tag{3.2.4}$$

$$Q = \frac{E^2}{X} - \frac{EV \cos(\delta)}{X} \approx \frac{E(E - V)}{X} \tag{3.2.5}$$

where δ is the phase angle difference between the two sources, X is the output reactance, and P_{max} is the three-phase nominal active power. Here it can be noticed, that the synchronous machine regulates its injected active and reactive power by modifying δ and the voltage magnitude of the inner electromotive force E, respectively. For this analysis, it is assumed that the two sources are synchronized in that sense, that the phase angle between them is small. In the following, a description and design of each control loop is given.

3.2.1 Droop Control

Even though the PLC and the virtual admittance defines the inherent droop characteristics for the P/f dependency and Q/V dependency respectively, outer direct droop controllers

can be included to define the overall droop gains, which can be set by the system operator. In this way, primary droop control is used to state the overall references for the active and reactive powers, whereas the PLC and the RPC are allowed to modify these references in order to further support the grid voltage and frequency dynamically. Since this structure aims to support the frequency and amplitude of the grid voltage, reverse droop control is applied [89] as

$$P^* = P_s + (\omega^* - \omega)D_P \tag{3.2.6}$$

$$Q^* = Q_s + (V^* - V)D_Q \tag{3.2.7}$$

where P_s and Q_s is the set point of the active and reactive power respectively, ω is the virtual oscillating frequency calculated from the PLC, and D_P, D_Q are the droop gains for the active and reactive powers, respectively. In this way, the droop coefficients regulates the power references dependent on the error in frequency and amplitude of the voltage. This is a simple approach extensively used in micro-grid applications to make a grid-connected converter to emulate the basic characteristics of a synchronous machine [90, 91]. However, compared to droop-controlled converters, the SPC uses the PLC after the droop controller, which results in a more accurately emulation of the synchronous machine behavior. Dead-bands can be included in the droop control to disable the proportional gain around the nominal values. The dead-band included for the frequency is 50 mHz whereas no dead-band is included for the voltage droop. The droop coefficients can be selected by e.g. the DSO or TSO and should be selected dependent on the power rating of the generating unit which facilitates power sharing between parallel generators in proportion to their power rating. Normally the droop gain between active power and frequency is set to 4% and the droop gain between voltage and reactive power is set to 4% as well [92].

The 4% of the voltage regulation is often related to a given reactive power, which ensures that a certain power factor is kept during normal operating conditions. From [50], a power factor above 0.95 in either underexcited or overexcited operation should be kept in relation to variations in the voltage. This means that for a voltage deviation of 4% the change in reactive power should be limited to $\cos^{-1}(0.95) \approx 0.3$ pu. Hence, the actual droop gains are selected to be

$$D_P = \frac{S_n}{4\% \cdot 50Hz} = 3.675 \ [kW/Hz] \tag{3.2.8}$$

$$D_Q = \frac{\cos^{-1}(0.95)S_n}{4\% \cdot V_b\sqrt{2/3}} = 0.169 \ [kVAr/V] \tag{3.2.9}$$

It should be noted that as explained in [92], the set-point for the reactive power is slowly modified (<1 Hz) based on an overall voltage controller at the on-shore connection point, which sends respective reference values to each wind turbine in a large wind power plant. Therefore, this value can also be considered just to take into account any needed global droop effects. Since this project just focus on one single wind turbine, droop controllers can be explicitly used to emulate this.

3.2.2 Virtual Admittance and Inner Current Control

The inner loops of the SPC consist of a virtual admittance structure and an inner current regulator. The virtual admittance emulates the output impedance of the stator windings

of a synchronous machine and can easily be used to dictate the grid impedance without the need to estimate the impedance in low X/R ratio grids. In this way, decoupled control of active and reactive power can be achieved. When implemented, it is beneficial to implement the electrical characteristics as a virtual admittance since one can avoid numerical differentiation as is needed for the case of virtual impedance. The virtual admittance can be designed to allow for accurate load sharing and easy start-up procedure [39]. Thus, when a load is increased, the current drawn from the machine is increased which due to the stator impedance, will lower the available terminal voltages, which effectively decreases the injected power. Normally, the load sharing will be defined in the speed droop or P/f droop controller. When the reference voltage has been calculated based on the PLC and RPC, the current reference is calculated based on the virtual admittance as

$$\mathbf{i}_{\alpha\beta}^* = \frac{\mathbf{e}_{\alpha\beta} - \mathbf{v}_{\alpha\beta}}{R_v + sL_v} \tag{3.2.10}$$

where R_v and L_v is the virtual resistance and inductance of the output stator impedance respectively, $\mathbf{e}$ is the virtual Electromotive Force (EMF) calculated from the two outer power loops, and $\mathbf{v}$ is the PCC voltage. Since the reactive power in a highly inductive grid is $Q = \frac{V^2 - VE}{X}$, it can be seen that the virtual admittance structure inherently acts as a proportional droop control between reactive power and voltage magnitude. The inner control is a cascaded loop with an inner current controller, which uses the same structure and design technique as discussed for the current-mode controller together with an outer voltage loop. The selection of the virtual admittance should be set such that the bandwidth of the voltage loop is significantly slower than the inner current loop. As discussed in [93], the virtual reactance should be fixed to 0.3 pu of the rated impedance of the converter. This is also a typical reactance value for a grid-connected synchronous machine. Then, the virtual resistance can be selected to get a desired cut-off frequency of the virtual admittance low-pass filter. Selecting a cut-off frequency that is at least ten times slower than the inner current controller gives a virtual resistance of around 0.1 pu.

3.2.3 Power Loop Controller

The main task of the PLC is to emulate the inherent active power to frequency relationship of a synchronous machine. This is achieved by calculating a desired virtual angular frequency of the emulated inner electromotive force based on a mathematical model of a synchronous machine and a given active power error. To closely resemble the properties of a synchronous machine and with a desire for a non-complex implementation, the selected model is widely known as the swing equation

$$J\omega_0 \frac{d^2\delta}{dt} = P_m - P_e - D\omega_0 \frac{d\delta}{dt} \tag{3.2.11}$$

where P_m is the mechanical power, P_e is the electrical power, J is the moment of inertia, D is total damping coefficient including mechanical friction, damper windings, etc., ω_0 is the rated angular frequency, and δ is the load angle of the machine relative to the grid. Note that the accelerating torque and damping torque are multiplied with ω_0 since the equation is expressed in terms of power rather than torque. It is known that $J\omega_0$ is the angular momentum of the rotor at synchronous speed, which is also called the inertia constant, M. Normalizing this with respect to the rated power at synchronous speed enables the more

familiar notation of the inertia constant

$$H = \frac{J\omega_0^2}{2S_n} \quad [s] \tag{3.2.12}$$

where S_n is the rated power of the machine. Putting this into the swing equation gives

$$\frac{2HS_n}{\omega_0}\frac{d^2\delta}{dt} = P_m - P_e - D\omega_0\frac{d\delta}{dt}. \tag{3.2.13}$$

Knowing that $\delta = \int(\omega - \omega_g)dt$, the small-signal transfer function between the angular frequency and the active power is

$$G_{PLC}(s) = \frac{\Delta\omega}{\Delta P} = \frac{\omega - \omega_g}{P_m - P_e} = \frac{1}{\frac{2HS_n}{\omega_0}s + D\omega_0}. \tag{3.2.14}$$

Using the mechanical power as the power reference and the electrical power as the power injected to the grid, the virtual angular frequency of the converter, ω, can be calculated dependent on a desired mechanical response [32]. From this, the control block diagram shown in Figure 3.20 can be constructed, which has the closed-loop transfer function

$$\frac{P(s)}{P^*(s)} = \frac{\frac{P_{max}\omega_0}{2HS_n}}{s^2 + \frac{D\omega_0^2}{2HS_n}s + \frac{P_{max}\omega_0}{2HS_n}} = \frac{\omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \tag{3.2.15}$$

with

$$\omega_N = \sqrt{\frac{P_{max}\omega_0}{2HS_n}}, \tag{3.2.16}$$

$$\zeta = \frac{\sqrt{2}D\omega_0^2}{4HS_n\sqrt{\frac{P_{max}\omega_0}{HS_n}}}. \tag{3.2.17}$$

Then, based on a desired damping factor and undamped natural oscillating frequency, the inertia constant and damping coefficient of the virtual machine can be calculated. Besides the benefits of power system frequency support, this structure is able to synchronize with the grid without any need for a dedicated synchronization unit, e.g. a PLL. In this way, the converter synchronizes with the grid based on the active power balance instead of estimating the grid voltage phase angle, also when the grid voltage angle is unknown. The implementation of the PLC can be seen in Figure 3.21. Here, the calculated virtual angular frequency ω is used together with the voltage magnitude to calculate the reference voltage in the VCO. The sensitivity function, i.e. the power change as a result of grid frequency variations can be found to be

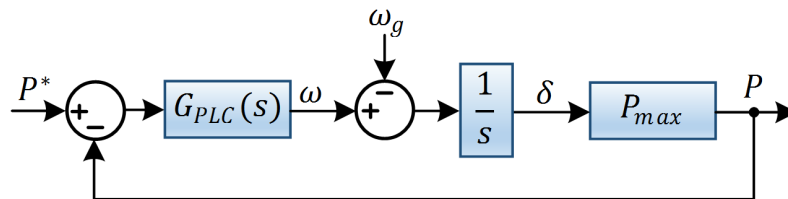$$\frac{P(s)}{\omega_g(s)} = -\frac{P_{max}}{P_{max}G_{PLC}(s) + s}, \tag{3.2.18}$$

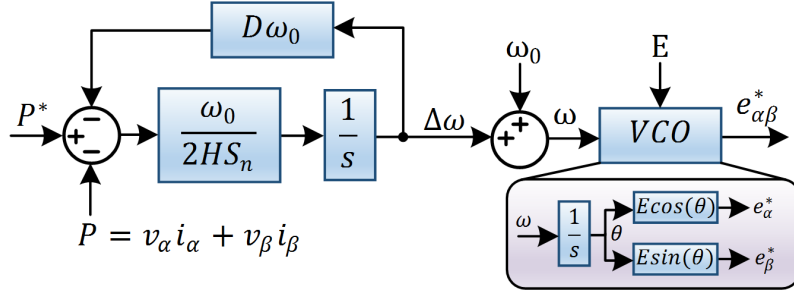Figure 3.20: Control block diagram of active power controller using PLC.

Figure 3.21: Implementation of PLC and mechanical characteristics with selected virtual inertia constant and damping. The virtual angular frequency is used together with E obtained from the reactive power controller to construct the voltage reference.

which is a negative low-pass filter and shows the inherent droop characteristic of the control. As it can be seen, if the grid frequency increases, the controller will lower its active power and if the grid frequency decreases the controller will increase its active power output just like a synchronous generator. It can be seen that the inherent features of the emulated synchronous machine means that this structure can be utilized without the need to introduce an additional outer loop for the frequency droop control [94]. Furthermore, it can be seen that the inherent droop gain will cause a steady-state error in the injected active power. The steady-state inherent droop gain can be evaluated by letting $s \to 0$ in equation (3.2.18) which gives

$$D_{p,ss}(s) = -\frac{1}{G_{PLC}(0)} = D\omega_0. \qquad (3.2.19)$$

From this, it can be seen, that if it is desired to limit the steady-state active power error, the damping coefficient should be selected small.

An alternative to this is to realize the PLC as a PI controller which introduces a zero at the origin when evaluating the transfer function between active power and grid frequency variations [95]. Therefore to closer compare with the current-mode controller and only support the frequency during transients, a PLC based on a PI controller is developed to ensure that the injected active power has no steady-state error. Then the outer frequency droop control aims to change the reference to further support the frequency in steady-state conditions. Using a PI controller instead of $G_{PLC}(s)$ in Figure 3.20, the active power response becomes

$$\frac{P(s)}{P^*(s)} = \frac{P_{max}K_p s + K_i P_{max}}{s^2 + K_p P_{max}s + K_i P_{max}} = \frac{2\zeta\omega_N s + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \qquad (3.2.20)$$

which can be approximated as a general second-order response. This gives that

$$\omega_N = \sqrt{K_i P_{max}}, \qquad (3.2.21)$$

$$\zeta = \frac{P_{max}K_p}{2\sqrt{K_i P_{max}}}. \qquad (3.2.22)$$

Comparing this to equation (3.2.16), the integral gain should be

$$K_i = \frac{\omega_0}{2HS_n} \qquad (3.2.23)$$

and the proportional gain can then be calculated using equation (3.2.21) and (3.2.23) to be

$$K_p = \zeta \sqrt{\frac{2\omega_0}{HS_nP_{max}}}. \tag{3.2.24}$$

Now, the active power response to change in the grid frequency becomes

$$\frac{P(s)}{\omega_g(s)} = -\frac{P_{max}s}{s^2 + P_{max}K_p s + P_{max}K_i} \tag{3.2.25}$$

which at steady-state is zero, i.e. no steady-state error in the injected active power. To tune the controller, it is only left to select a desired damping ratio and inertia constant of the emulated machine. An optimal and often used choice for the damping ratio is $\zeta = 1/\sqrt{2}$. Thus, the inertia constant can either be selected to emulate a given size of a machine of be selected dependent on stability considerations and power response characteristics. Since the machine emulation is done in software, the inertia constant and damping characteristics of the machine is not constrained by any physical design associated with real synchronous machines, i.e. the parameters can be set without limitations. It is, however, required that the converter can facilitate the resulting characteristics.

In Figure 3.22, the poles of the characteristic equation of (3.2.20) are shown as a function of the damping ratio and inertia constant. It can be seen that by increasing the inertia constant, the poles move closer to the origin. Any damping larger than zero will, as anticipated, keep the poles in the stable left-half plane. As the inertia constant increases, the natural oscillating frequency decreases, which means that a slower response is achieved. This matches with what is expected from a machine: that a large machine with a high inertia constant will take longer time to respond to disturbances. From this, selecting a damping ratio of 0.707, any inertia constant within a reasonable range will result in a stable system ignoring the effects of the inner control loops. A typical range of inertia constants for synchronous machines is 1-10 s. As discussed in [96], double-line frequency oscillations occur in the instantaneous output power of the VSC during
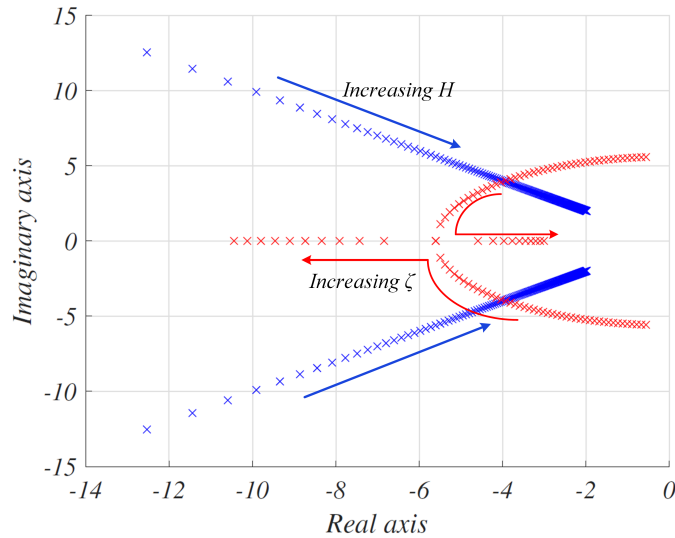

Figure 3.22: Poles of the characteristic equation of equation (3.2.20). Blue denotes $\zeta = 1/\sqrt{2}$ with varying inertia constant from 0.5 to 20. Red denotes constant inertia constant, H, of 10 and varying damping ratio from 0.1 to 1.2.

unbalanced conditions. Therefore the bandwidth of the PLC should be tuned to be lower than the fundamental frequency to achieve decoupled control of the active and reactive power.

It must be mentioned, that to fully emulate the behavior of a synchronous machine, the natural power reserve stored in the rotating mass must be physically available in order to actually support the grid and provide inertia to the system. This can either be done using energy storage or power curtailment. In this project, this is not addressed and it is simply assumed that the needed power is available or that the system is not operated at maximum capacity.

DC-Link Voltage Regulation for SPC

It was attempted to implement a DVC to support the dc-link voltage by regulating the active power reference send to the PLC. However, since the PLC is already slow, tuning a DVC capable of regulating the dc-link voltage in a stable and accurate manner, has so far not been successful. To that end, a control structure which regulates the dc-link voltage and the reactive current can be altered to include inertial characteristics by modifying the DVC to utilize the dynamics of the dc-link capacitor. However, this structure still need a PLL to achieve the grid synchronization as it was discussed in the introduction [31, 38]. Also, performing synchronization based on the power balance and at the same time controlling the power balance on the dc-side to control the dc-link voltage may counteract as they do opposing actions. E.g. if the grid frequency drops, the SPC injects more active power to support the grid. However, this additional energy is being momentarily taken from the dc-link voltage which the outer DVC now try to restore, effectively acting against the grid frequency support just performed. In this way, oscillations may be likely and the two methods may not work in a cooperative state as experienced in this project. Accordingly, for this project, in case of the voltage-mode controller, the dc-link voltage is considered constant and is left for future work.

3.2.4 Reactive Power Controller

This subsection has the purpose of describing the RPC, which regulates the reactive power with the purpose of supporting the voltage at the PCC. The three-phase reactive power can be described as

$$Q = \frac{3}{2}\frac{E_p^2 - E_p V_p}{sL_{eq}} \tag{3.2.26}$$

where p denotes peak values, and the reactance is approximated with the equivalent reactance, which is the sum of all inductances between the converter terminal voltage and grid voltage including the virtual reactance. Perturbing and linearizing around $Q = 0$, which means that $E_p = V_p$, reveals that

$$\hat{Q} = \frac{3}{2}\frac{2E_p - V_p}{L_{eq}s}\hat{E}_p = \frac{3E_p}{2L_{eq}s}\hat{E}_p. \tag{3.2.27}$$

The small-signal model of the RPC based on a PI controller is as shown in Figure 3.23, which gives the following closed-loop transfer function

$$\frac{Q(s)}{Q^*(s)} = \frac{\frac{3E_P K_{pq}}{2L_{eq}}s + \frac{3K_{iq}E_p}{2L_{eq}}}{s^2 + \frac{3E_P K_{pq}}{2L_{eq}}s + \frac{3K_{iq}E_p}{2L_{eq}}}. \tag{3.2.28}$$
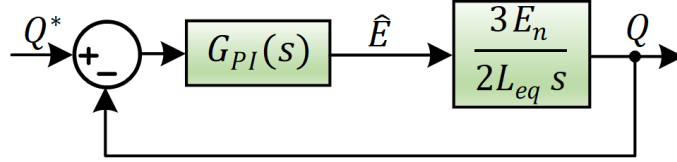
Figure 3.23: Control block diagram of reactive power controller with PI controller and plant.

This is the approximation of the general second-order system as shown multiple times previously. Here the inner loops are approximated as a unity gain since they are much faster than the outer power loops. Using this, the proportional and integral gains of the RPC can be selected as

$$K_{pq} = \frac{4\zeta\omega_N L_{eq}}{3E_p}, \tag{3.2.29}$$

$$K_{iq} = \frac{2\omega_N^2 L_{eq}}{3E_p} \tag{3.2.30}$$

where

$$L_{eq} = L_v + L_{cf} + L_{gf} + L_g + L_L \quad \text{and} \quad L_v = \frac{X_v V_b^2}{\omega_0 S_n}. \tag{3.2.31}$$

Likewise, as explained for the PLC, the RPC should also be tuned with a bandwidth significantly lower than the fundamental frequency in order to achieve decoupled control between the active and reactive power. As what was seen for the PLC, the utilization of the PI controller enables zero steady-state errors due to a disturbance in the grid voltage magnitude. As it can be seen in Figure 3.23, considering $Q^* = 0$, then for a grid voltage dip, the RPC will dynamically support the voltage by injecting reactive power. Thus, even though the steady-state point of e.g. $Q = 0$ will not change as the grid voltage changes, a transient response will occur which aims to support the PCC voltages. However, when the outer droop controllers are considered, these will modify the reactive power reference in an attempt to support the voltage, also during steady-state operations.

With this, both the grid-following and grid-forming control structure has been carefully described and tuned. The following chapter aims to compare and test the performance of each of the controllers during different steady-state conditions.

4   Validation of Current-Mode and Voltage-Mode Control

Now that the two control structures have been presented and designed, these are to be tested and compared. Firstly, different tests during normal operating conditions are performed to investigate the performance of each controller. Then the performance of the controllers are verified under both symmetrical and asymmetrical grid faults in the following chapter.

4.1   Verification of Current-Mode and Voltage-Mode Control

A simulation model of each of the two controllers are developed in MATLABs Simulink using PLECS blockset. Each controller is integrated with the same converter operated at identical grid circumstances. The grid impedance is simulated as a pure reactance with an inductance of 3 mH, which is around 0.04 pu and represent a strong grid connection with a SCR of 25. Each controller is tuned as described in the previous chapter and the controller parameters of the current-mode control and voltage-mode control are presented in Table 4.1 and Table 4.2, respectively. In order for the simulation model to emulate the physical experimental setup as accurately as possible, the simulation is performed with two different time constants as shown in Figure 4.1. The discrete controller which will be implemented in a Microcontroller or Digital Signal Processor in the laboratory setup is emulated by triggering the discrete controller subsystem every T_s. The continuous electrical part is solved much faster such that the electrical part can be approximated by the continuous system in the laboratory. Due to this triggering and by including a sample delay and a transport delay associated with the PWM, the electrical plant sees a total delay of $1.5T_s$ as desired.
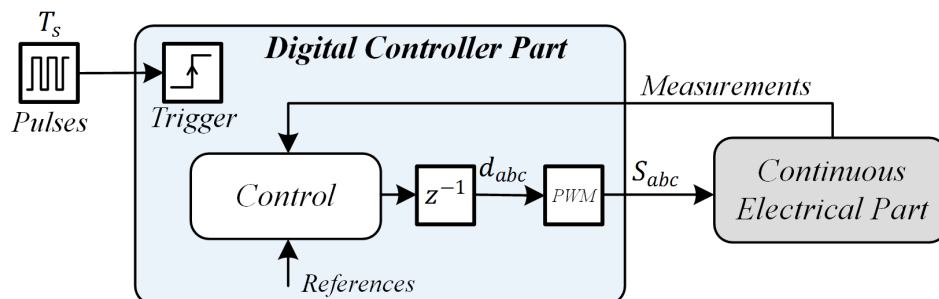

Figure 4.1: Simulation model structure including a discrete controller part triggered with the sampling frequency and a continuous electrical part used to emulate the experimental system.

Controller	Parameters
Current Controller	$K_p = 25$, $K_i = 24e3$, $f_{bw} = 665$ Hz
Voltage Feed-forward	1 (Enabled)
PLL	$t_r = 50$ ms, $\zeta = 0.707$, $U = 1$, $K_p = 50.9$, $K_i = 1296$, $f_{bw} = 12$ Hz
DVC	$\alpha_{dc} = 10$ Hz, $K_{p,dc} = 31.4e\text{-}3$, $K_i = 1$, $f_{bw} = 10$ Hz

Table 4.1: Controller parameters for the current-mode control structure. The controller block where the parameters are integrated are shown in Figure 3.1.

Controller	Parameters
Droop Control	$D_P = 0$ kW/Hz, $D_Q = 0.169$ kVAr/V
Virtual Admittance	$R_v = 0.1$ pu, $L_v = 0.3$ pu
Current Controller	$K_p = 25$, $K_i = 24e3$, $f_{bw} = 665$ Hz
Voltage Feed-forward	1 (Enabled)
PLC	$H = 2$ s, $\zeta = 0.707$, $K_p = 1.7e\text{-}3$, $K_i = 10.7e\text{-}3$, $f_{bw} = 3$ Hz
RPC	$\zeta = 0.707$, $\omega_N = 5$ rad/s, $f_{bw} = 1.6$ Hz, $L_{eq} = 29.7$ mH

Table 4.2: Controller parameters for the synchronous power controller, i.e. voltage-mode control structure. The controller block diagram where the parameters are integrated is shown in Figure 3.18.

At first, the injected grid currents of the two structures are recorded and they are presented in Figure 4.2. As it can be seen, smooth sinusoidal currents are injected and both controllers have a low distortion in the injected currents of 0.22%, which complies with all distortion limits presented in Table 1.3. The utilized LCL filter strongly attenuates the harmonics seen in the converter currents.

Secondly, a step in the active power from 0.5-1 pu is performed and the dq-axis currents are monitored as it can be seen in Figure 4.3(a). Here, the SPC shows a slow response due to the inertial characteristics of the PLC. A fast response is evident considering the current controller and an overshoot above 40% is present. The simplified control block diagram of Figure 3.3 was used to test whether this high overshoot was also seen from the current controller design and here it was verified that an overshoot of 46% was present considering this analysis. The experimental test of this is visualized in Figure 4.3(b), which is shown to be in close agreement with the simulation study. For the response in Figure 4.3(b), the current regulator is retuned as it will be described later (in Figure 4.10) to decrease its overshoot. This obviously infer that for the laboratory results, the settling time for both the active and reactive current for the current-mode controller is a bit slower than what is seen from the simulation results in Figure 4.3(a).

To validate the DVC of the current-mode control, a constant current source, which steps from 5 A to 10 A is implemented on the dc-link. The dc-link voltage reference is set to 730 V during the test. This response is shown in Figure 4.4, where an active power
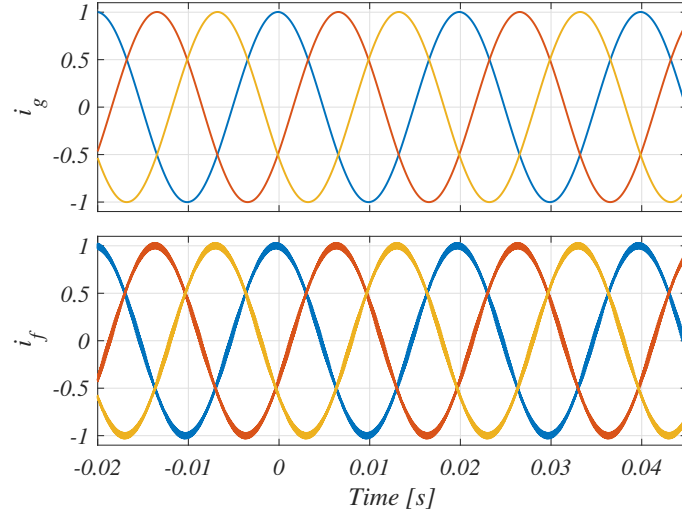
Figure 4.2: Simulated steady-state grid currents and converter currents using current-mode and voltage-mode control. Only the results from one of the controller are presented as the steady-state current waveforms are identical for the two. Both have a $THD_I = 0.22\%$ in the grid current and a $THD_I = 2.32\%$ in the converter currents.

(a) Simulation results.

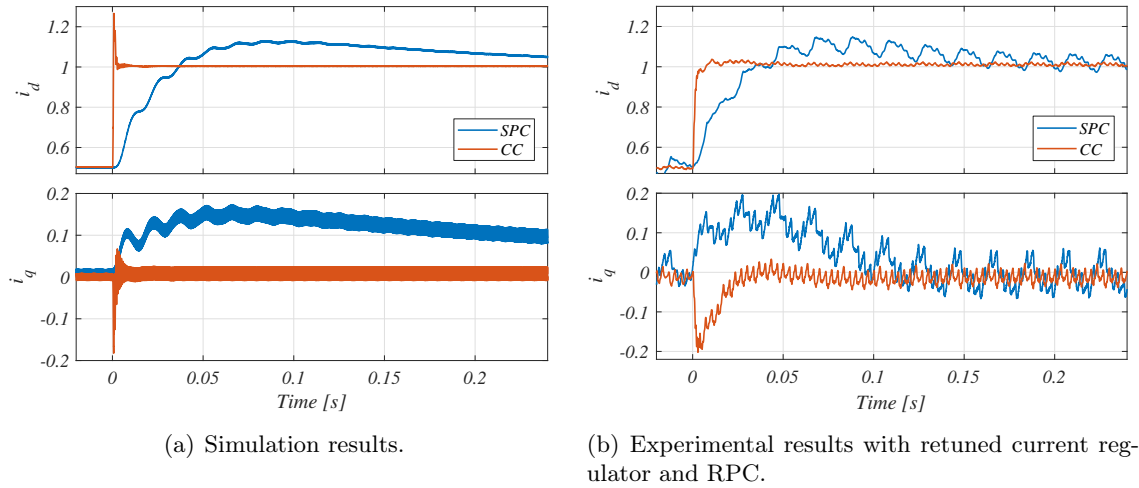(b) Experimental results with retuned current regulator and RPC.

Figure 4.3: Simulated and experimental responses to a step in the injected active power from 0.5-1 pu for the SPC and the current-mode control.

response similar to that seen from the SPC can be seen. Furthermore, the DVC is able to track the dc-link voltage reference and balance the power between the dc and ac side.

To visualize the supporting functionalities of the SPC compared to the current-mode controller, a drop in the grid frequency and grid voltage magnitude is performed separately. The response of each controller are shown in Figure 4.5(a) and Figure 4.6(a). When the frequency drops, the SPC initiates a transient response where it increases its active power in order to support the frequency. Since a PI controller is implemented in the PLC, the active power (shown in Figure 4.5) is seen to return to its reference value since no droop control was used for the active power loop. Also, the synchronization of the two controllers can be seen where they both synchronize to the decreased grid frequency. It can also be
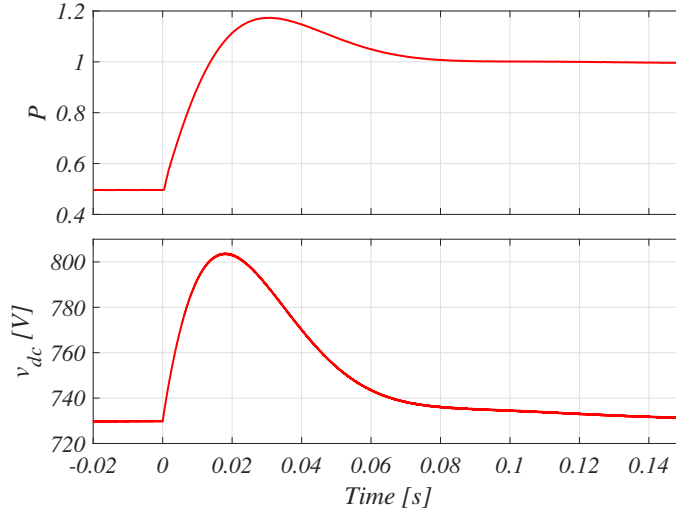
Figure 4.4: Simulated response of DVC where a step from 5 A to 10 A is performed in the dc-side current.

noticed that the rise time of the PLL is faster than the 50 ms, which it was designed for. This is due to the fact that the expression for the rise time is only an approximation for the second-order system and that for the expression to be valid, the second-order system must not contain any zeros, which in this case is strictly violated. The experimental counterpart to this test is shown in Figure 4.5(b). Again, the same trend is seen but a faster response both for the current-mode controller and the SPC is seen both in terms of frequency and active power injection. In addition to this, it can be observed that a significant amount of noise is present in the measurements obtained from the laboratory setup, which may be due to limitation in measurement precision, electrical noise which is conducted and radiated from the high-frequency switching actions to the measurement circuit, and unwanted pick-up of the ac supply voltage. As the active power for the SPC contains a 50 Hz component, this may indicate ac supply pick-up and a not fully balanced experimental network.

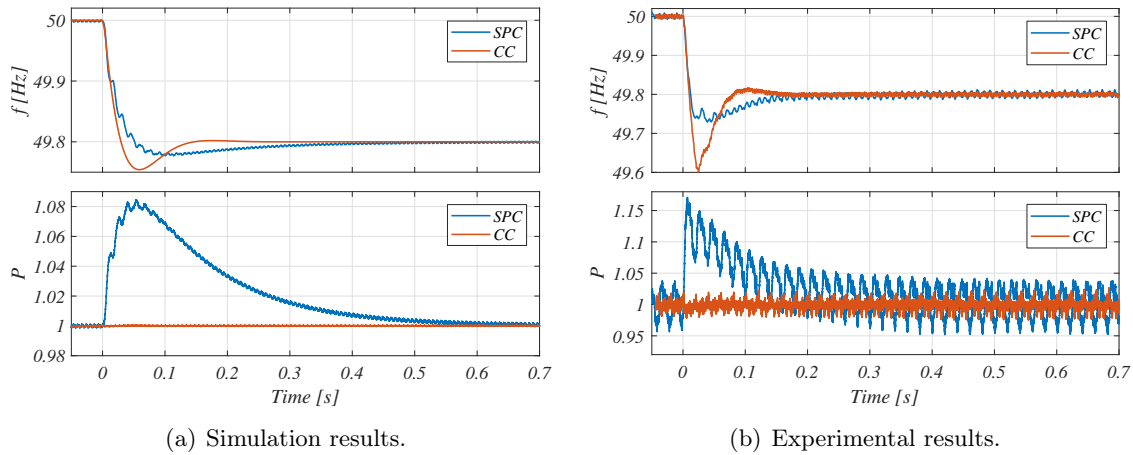

(a) Simulation results.

(b) Experimental results.

Figure 4.5: Simulated and experimental responses to a drop in the grid frequency where the SPC changes its injected active power in order to support the network frequency. CC is used to denote the current-mode controller.

In Figure 4.6(a), it is seen that the SPC aims to support the network voltage by increasing its reactive power injection whereas the current-mode controller in both cases is ignorant to the disturbance. For the reactive power loop, the Q/V droop controller changes the reactive power reference in order to support the voltage. As it can be seen in Figure 4.6(a), oscillations in the injected reactive power are present due to improper controller gains. This test is also performed in the laboratory as it can be seen in Figure 4.6(b). Here the same oscillations were observed and a retuned set of controller gains were used to improve the experimental result. It should be noticed that the actual grid voltage is not measured in the lab, only the PCC voltage, therefore the voltage shown in Figure 4.6(b) does not exactly drop to 0.98 pu but is supported by the reactive power injection.

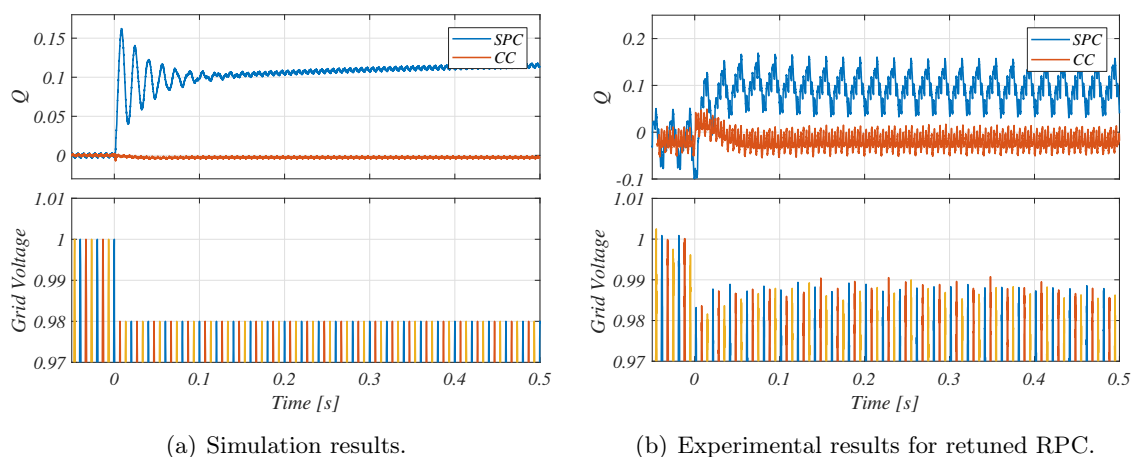(a) Simulation results.   (b) Experimental results for retuned RPC.

Figure 4.6: Simulated and experimental reactive power responses as a result of a small grid voltage dip from 1 pu to 0.98 pu.

Due to the large oscillations seen in the reactive power in Figure 4.6(a) and the rather slow response in the i_q for the SPC in Figure 4.3(a), the RPC is retuned with a proportional gain of 1.6e-3 and an integral gain of 0.4. This gives an effective bandwidth of the RPC of 20 Hz, much faster than in the initial design with a bandwidth of 1.6 Hz. The reactive power injection as a result of a small dip in the grid voltage is performed again with the retuned RPC. This is shown in Figure 4.7, where it is evident that the reactive power has much lower amplitudes in the oscillations and the coupling to the active power is also small.

4.1.1 Performance Analysis under Weak-Grid Conditions

The performance of the two controllers has so far only been validated during very strong grid conditions. Accordingly, it is investigated how each of the controllers behave during weaker grid conditions. At first, the grid impedance is increased to 0.4 pu giving a SCR of 2.5. This condition is tested for the current-mode controller, which is shown in Figure 4.8(a). Here, a highly distorted response is evident, which results in an unacceptable performance of the converter. For the graph of the *dq*-axes currents both the reference values (blue) and the actual values (red) are shown. As discussed in the analysis of the voltage feed-forward control, a high grid impedance can seriously deteriorate the performance during weak-grid conditions. Furthermore, the robustness of the PLL is also highly decreased when the grid impedance increases. Therefore, the same test condition is performed but
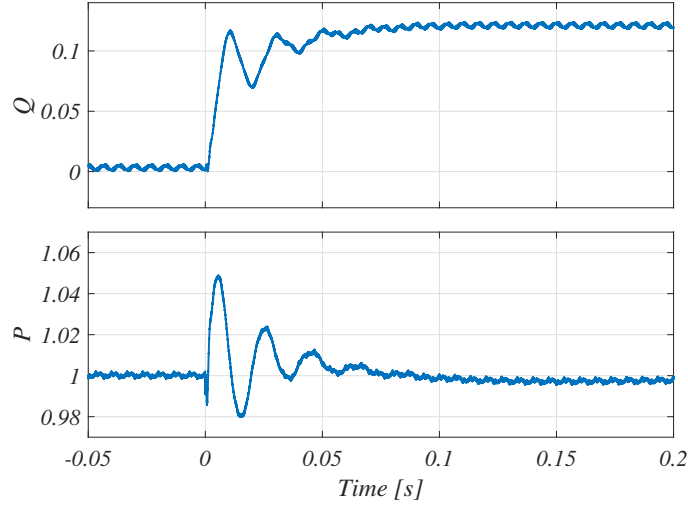
Figure 4.7: Simulated response of retuned RPC exposed to the voltage dip as shown in Figure 4.6(a)

with the voltage feed-forward disabled, which can be seen in Figure 4.8(b). As anticipated, the robustness of the controller is highly increased where both dq-axes currents, estimated PLL frequency, and dc-link voltage can be tracked. To further stress the controller, the

(a) Voltage feed-forward is enabled.
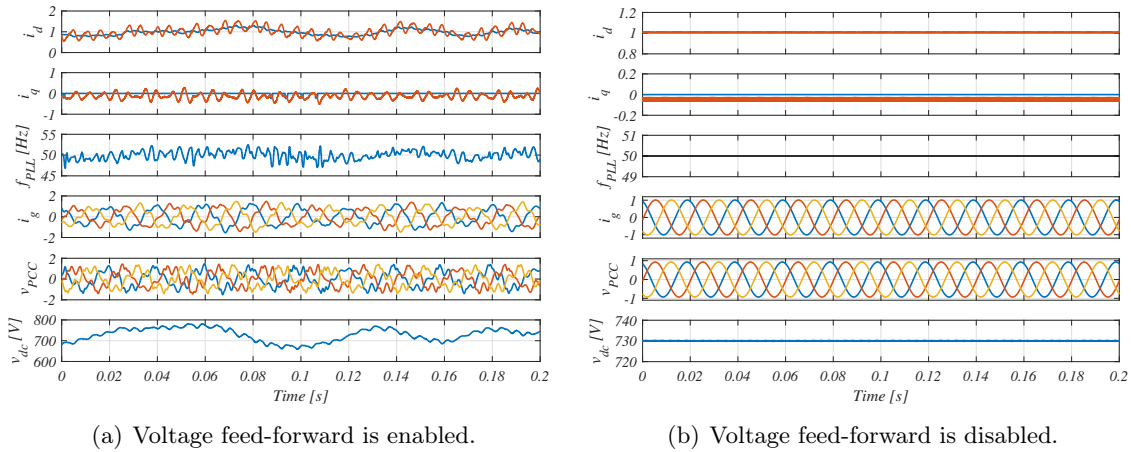
(b) Voltage feed-forward is disabled.

Figure 4.8: Current-mode control where grid impedance is increased to 0.4 pu which results in an SCR of 2.5.

grid impedance is increased to 0.5 pu resulting in a SCR of 2. The performance of this is shown in Figure 4.9(a). Here, both the DVC and the voltage feed-forward is disabled in an attempt to stabilize the system. As it can be seen, a poor steady-state response is achieved in the PLL, which highly distorts the generation of the $\alpha\beta$-reference currents and therefore the voltage at the PCC. The test performed in Figure 4.9(a) is also done for the SPC. The performance of this is shown in Figure 4.9(b), where it can be seen that the voltage-mode control structure is much more robust against weak-grid conditions and it is capable of injecting its reference currents with low distortion in the injected currents and PCC voltage. From this, besides grid-supporting services such as frequency and voltage support, the SPC is seen to be a better candidate for converters operated in weak grids. It can also be seen that the inherent synchronization in the PLC, which
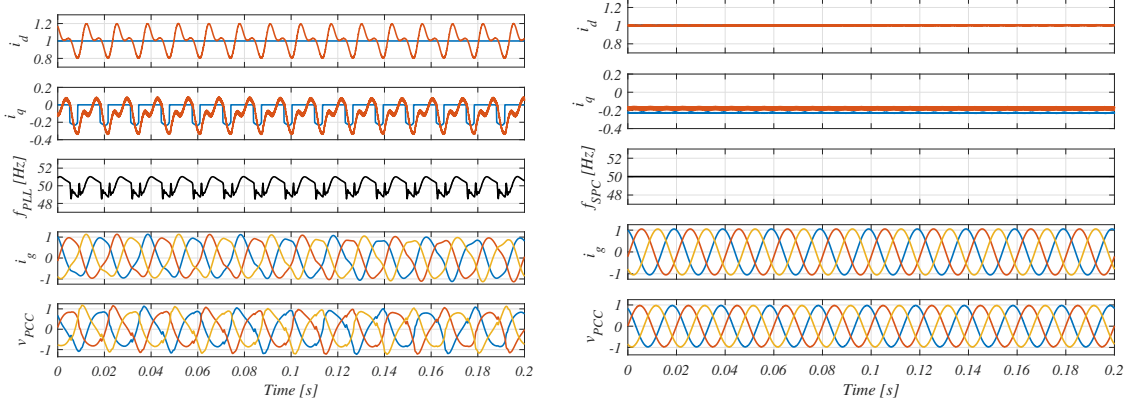
(a) Current-mode controller where voltage feed-forward and DVC is disabled. The *d*-axis current reference is set to 1 pu.

(b) Voltage-mode controller.

Figure 4.9: Response where the grid impedance is increased to 0.5 pu which results in an SCR of 2.

avoids the need of a PLL, results in a stable low ripple frequency estimation. No weak-grid conditions were conducted in the laboratory since the needed inductance was not available.

Current Controller Retuning

As it was seen in Figure 4.3(a), a quite large overshoot in the *d*-axis current was observed when exposed to a step change in its reference. This issue was also highlighted in subsection 3.1.1 where an alternative tuning for the controller gains were given, which resulted in the phase margin to be increased to 25°. To that end, a retuning of the PR current controller is done at this point to increase the phase margin and hence decrease the current overshoot. The newly selected parameters are 12 and 2000 for the proportional gain and the integral gain, respectively. It should be noted that these gains are the full proportional and integral gains used in PR controller, i.e. the formulation for the PR controller in equation (3.1.16) where a factor of two is included in both gains are equal to these values. I.e. $2K_p = 12$ and $2K_i = 2000$.

A step response in the *d*-axis current with the retuned current regulator with and without the use of voltage feed-forward can be seen in Figure 4.10(a) for the simulated case. Here, a fast response with a rise time around 1 ms and negligible overshoot can be seen. Furthermore, the dynamic improvement by using voltage feed-forward can be seen with regards to the *dq*-axes currents and the PLL frequency. Besides improved transient performance, the use of voltage feed-forward also improves the converters response during initial connection. The results are experimentally verified as it is shown in Figure 4.10(b). Even though an improved transient response with regards to current overshoot is obtained by the current regulator retuning, its performance during weak-grid conditions is further reduced compared to what was seen in Figure 4.9(a). From this, a trade-off between the controller robustness and transient performance must be made when selecting the current regulator gains.
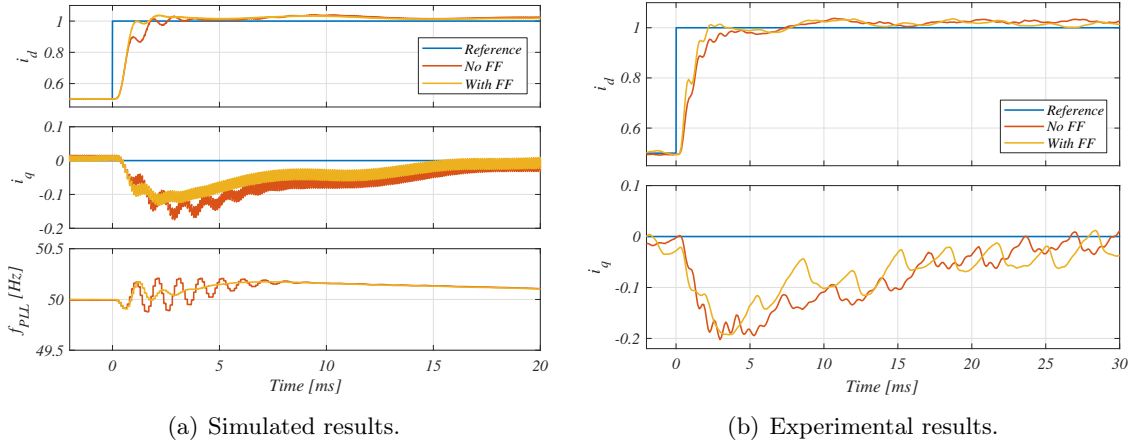
(a) Simulated results.

(b) Experimental results.

Figure 4.10: Step response in i_d reference current for retuned current-mode control with and without voltage feed-forward.

Practical Start-up Procedure using SPC

When initiating the operation of the current-mode controller in the laboratory, the PLL is simply locked to the PCC voltage before the converter PWM generation is enabled and the current reference is increased. However, for the voltage-mode controller the synchronization is performed through the PLC, which means that the controller cannot synchronize to the PCC voltage without enabling converter operation. If this is attempted, the converter is instantly tripped due to over-currents resulting from high initial injection of current during the synchronization. To circumvent this problem, the virtual inductance in the virtual admittance structure is during startup ramped down from $1000L_v$ to L_v in a few seconds. This ensures that the current reference is strongly limited during startup such that grid synchronization can be achieved without tripping the converter. For both controller structures the integrator of the current regulator should be reset just before converter operation is enabled. This is done since when the converter is disabled, the integrators might wind up. Then if the integrator reset is not performed, one might trip the converter when the PWM is enabled since a large reference value is stored in the previously blocked integrator.

With this, the two controllers have been tested and compared in simulation as well as in the laboratory. It has been seen, that both controllers are able to operate and a great match between the simulation and the experimental results are evident. To that end, the potential advantages of employing the grid-forming controller are highlighted. With this, the final part of this project report puts focus on the fault responses of both controllers and proposes different methods on how to accomplish acceptable fault control. This will make it possible to answer the initial formulation of the project, whether the fault response of grid-tied converters can be enhanced by using a grid-forming control structure rather than a grid-following structure.

5 Fault Behavior Analysis and Enhancement of VSCs

The chapter aims to test and compare the voltage-mode control and the current-mode control during different fault conditions. At first, the current reference generator during symmetrical faults is developed and tested for the current-mode controller, which also includes dc-link chopper control for the simulation part. Power and current limiting of the voltage-mode control structure is proposed during the symmetrical fault, which allows for safe converter and controller behavior during the fault while keeping the characteristics and advantages of the grid-forming controller during the fault. Besides a symmetrical fault, two asymmetrical faults are considered for both the current-mode and voltage-mode controller. A current reference generation strategy based on modern grid codes requiring unbalanced current injection during asymmetrical faults is developed and proposed. This is then tested for the current-mode controller and expanded to be applicable for the voltage-mode structure as well. The developed method is compared to balanced current injection during two asymmetrical faults and it is seen how the Voltage Unbalance Factor (VUF) can be reduced through injection of unbalanced currents. All the analysis and simulations conducted are experimentally verified. For both symmetrical and asymmetrical faults, the test conditions used are severe, meaning that either solid short circuits or deep voltage sagged faults are considered. This is done to create a high stress during either symmetrical or asymmetrical faults for the control system, e.g. to identify potential instability of the synchronization unit of the current-mode controller and severe issues regarding current limitation and controller wind-up of the voltage-mode controller. For both symmetrical and asymmetrical faults, the step-up transformer between WT and the line impedance is neglected in order to achieve an easy comparison between simulations and the experimental results where a transformer is not utilized. The influence, which the transformer has on the voltage sag type and profile, was discussed in details in Section 1.3.

5.1 Symmetrical Faults

In this section, the current reference generator during symmetrical faults is developed. The current-mode controller including dc-link chopper control is tested during a severe symmetrical fault. For the voltage-mode controller, reference power adjustment and converter current limitation are proposed to allow for safe converter and controller behavior during the symmetrical fault. Experimental results are provided to test and verify the developed controllers.

5.1.1 Symmetrical Fault Control of Current-Mode Controller

As it is stated by the grid codes, reactive current injection should be prioritized during such events in order to support the grid voltage. Therefore, since the current-mode controller

inherently does not support the grid, the current reference generation has to be modified during the fault. To that end, the control strategy should consider the current rating of the converter semiconductor devices in case of a fault condition and limit the current between rated and two times rated current, dependent on design margins and application [97]. In this project a limit of 1.2 pu is considered. Limiting the converter current can be achieved in numerous ways dependent on whether balanced or unbalanced currents are to be injected during the fault [98, 99]. Assuming the converter to always inject balanced currents independent on the fault type, the converter current can be limited using

$$I_{lim} = \sqrt{i_d^2 + i_q^2}. \tag{5.1.1}$$

In the case of voltage support, the reactive current is prioritized and i_d can be set to fulfill equation (5.1.1).

In a fault situation, the ability of a converter to rapidly detect a fault is key regarding system protection, grid support, and accurate time-tracking to comply with LVRT requirements [100]. For the symmetrical cases in this project, a fault is detected by measuring the voltage at the PCC. If the PCC voltage magnitude drops below 0.9 pu of the nominal value, a fault signal activating the voltage support is generated. The active current reference is obtained from the dc-link voltage control loop whereas the reactive current reference is calculated according to Figure 1.13(b). For the experimental verification the active current is simply set based on the corresponding active power reference. Using the measured PCC voltage, the reactive power reference is calculated as

$$i_q^* = \begin{cases} 0 & \text{if } V_{pu} > 0.9, \\ -2I_{nom}(1 - V_{pu}) & \text{if } 0.5 < V_{pu} < 0.9, \\ -I_{nom} & \text{otherwise,} \end{cases} \tag{5.1.2}$$

where I_{nom} is the nominal converter current and V_{pu} can be calculated as a filtered response of

$$V_{pu} = \sqrt{\frac{3}{2}} \cdot \frac{\sqrt{V_\alpha^2 + V_\beta^2}}{V_b}, \tag{5.1.3}$$

where V_b is the base rms line-to-line voltage and $\sqrt{3/2}$ origins since the amplitude invariant Clark transformation is utilized. Considering the current-mode control such a strategy is easily formulated and implemented since the structure only need to know the current reference to operate. Therefore, limiting and selecting the current reference as a result of different grid scenarios is straight forward.

DC Chopper to Avoid Overvoltage during Fault

If a grid fault happens close to the voltage terminals of the WT, extremely low voltage levels might be present at the PCC. During such an event, the power transfer capability between the WT and the grid is highly affected. Actually, as was discussed regarding grid code requirements, the converter must stay connected and support the grid with reactive power injection for a solid short circuit connection for 150 ms. As described previously, then considering an inductive grid, the active power transfer is

$$P = \frac{V_{PCC}V_g}{X}\sin(\delta). \tag{5.1.4}$$

Thus, if $V_g \approx 0$, no active power can be transferred. This means, that if the WT is still operating at e.g. nominal wind speed, this power is not able to be transferred to the ac-side, which causes overvoltages on the dc-link which can destroy the converter semiconductor devices and dc-link capacitor. This is true even though DVC is used since the power received from the generator cannot be delivered to the grid. The energy stored in the dc-link capacitor is

$$E_{dc} = \frac{1}{2}C_{dc}v_{dc}^2 \implies v_{dc} = \sqrt{\frac{2E_{dc}}{C_{dc}}}. \tag{5.1.5}$$

By knowing that the energy stored in the capacitor is the integral of the power being accumulated at the dc-side, the dc-link voltage can be expressed as

$$v_{dc} = \sqrt{\frac{2}{C_{dc}} \int (P_{WT} - P_g)dt} \tag{5.1.6}$$

where P_{WT} and P_g is the power from the wind turbine and power delivered to the grid, respectively. Here it can be seen that if P_g is strongly limited due a low-voltage situation, the dc-link voltage will increase and the converter can nothing do since its currents are strongly limited as well [101].

To fix this problem, a chopper circuit is normally implemented on the dc-link in order to dissipate the excess energy for full-scale back-to-back converters [102] as it can also be seen in Figure 1.2. The chopper circuit consists of a parallel connected resistor which can be switched in and out using a power transistor. Therefore, by regulating the duty cycle of this transistor, a controlled resistance can be constructed. In case the grid voltage is absent, the chopper resistance should be designed such that it can dissipate the rated power. This is

$$R_{chop} = \frac{V_{dc,rated}^2}{P_{max}} = \frac{(730\,V)^2}{7.35\,kW} = 72.5\,\Omega. \tag{5.1.7}$$

A PI controller is used to regulate the chopper circuit during the fault. The control law for the duty cycle of the chopper circuit is

$$d_{chop} = (v_{dc} - v_{dc}^*)(K_{p,chop} + K_{i,chop})S_F \tag{5.1.8}$$

where S_F is the fault signal, which is set high when a fault is detected. Selecting $K_{p,chop} = 0.01$ and $K_{i,chop} = 0.125$ is found to give a good response during a considered low-voltage situation.

Control of the dc-link voltage and the described current limiting procedure are tested during a symmetrical three-phase fault where the fault magnitude drops to 0.3 pu for 150 ms before the fault is cleared. The simulated response is shown in Figure 5.1 where it can be seen that full reactive current is injected while the active current is reduced such that the current magnitude is limited to 1.2 pu. Furthermore, it can be seen that the chopper circuit, which is enabled quickly after the fault instant, is capable of dissipating the excess energy to avoid any dc over-voltage during the fault. When the fault is cleared, the chopper circuit is deactivated, which gives a transient in dc-link voltage when the active power is again raised to the nominal value. When performing the experimental tests, a constant dc-link is considered. It can be seen, that by using a chopper-circuit, this assumption can be made during the fault. The experimental verification of the current-mode controller during the symmetrical fault is shown in Figure 5.2. As it can be seen, the converter is able to ride through the fault while injecting the required reactive current. A close tracking

Figure 5.1: Simulated fault response of current-mode control during a symmetrical fault with a voltage magnitude of 0.3 pu including voltage feed-forward and retuned PR controller ($K_p = 12$, $K_i = 2000$). Control of the chopper circuit is included to regulate the dc-link voltage during the fault. The grid impedance is 0.04 pu.
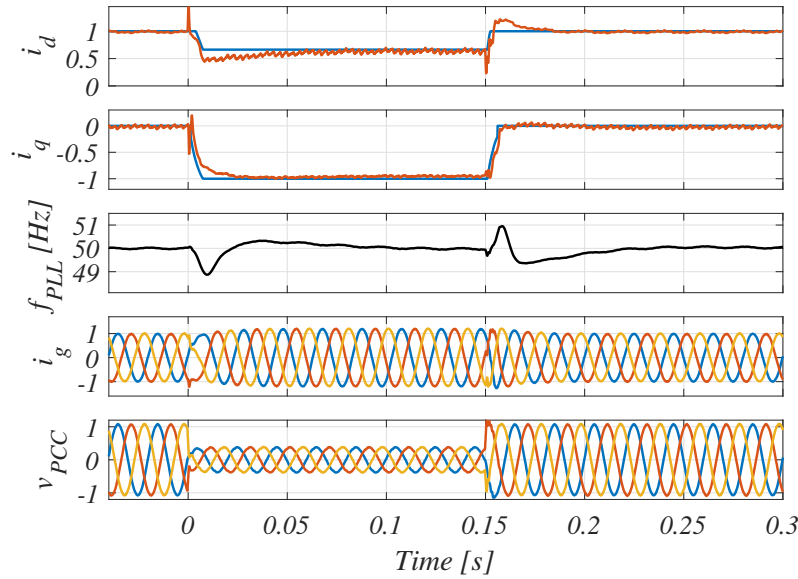
Figure 5.2: Experimental verification of Figure 5.1.

of the reactive current reference is evident from Figure 5.2 with an overshoot in the active current injection during the fault recovery. Additionally, an altered response is seen in the estimated frequency of the PLL as a slower PLL was utilized in experimental setup to decrease the ripples during steady-state conditions. Thus, the experimental results are in good agreement with the simulation study performed.

5.1.2   Symmetrical Fault Control of Voltage-Mode Controller

Due to the grid-supporting functionalities of the SPC, the symmetrical three-phase fault as considered in Figure 5.1 for the current-mode control is tested for the voltage-mode controller as well. The result of this can be seen in Figure 5.3. Here it can be noticed that the voltage at the PCC is highly supported by the voltage-mode structure without any control modification during the fault. However, this voltage support is realized through a large injection of reactive current, which results in an injected grid current with a magnitude of 6.7 pu.

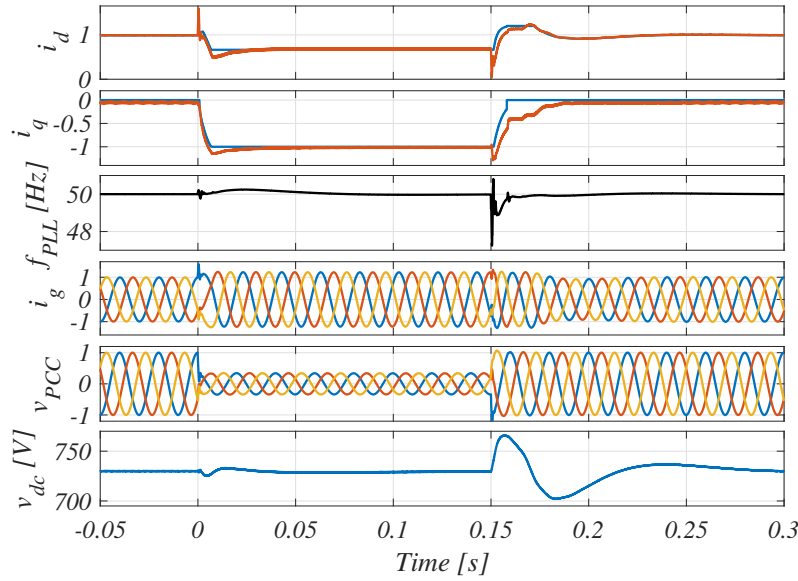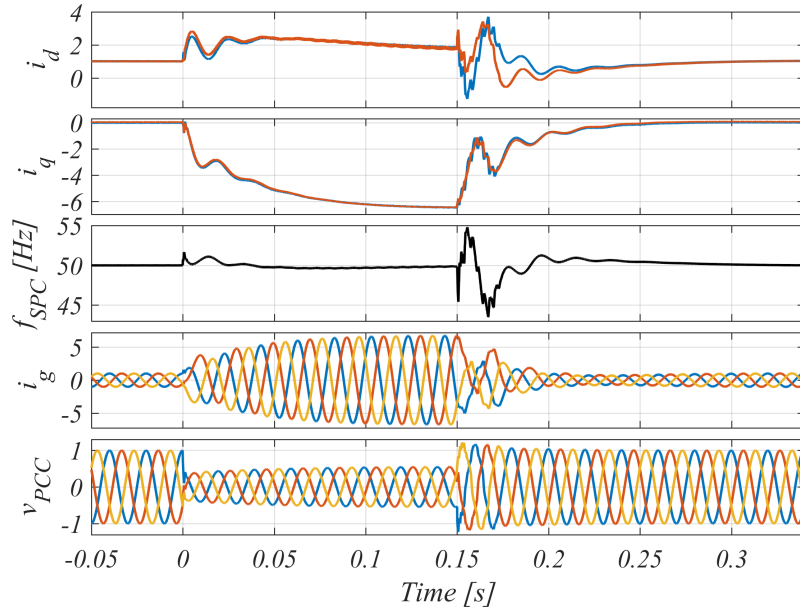

Figure 5.3: Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu including voltage feed-forward and retuned PR controller. The grid impedance is 0.04 pu. An unacceptable large reactive current injection is evident during the fault.

Since the SPC is a voltage-mode control structure, it simply asks for a given current reference in order to achieve the reference virtual EMF in order to satisfy the demands from the PLC and the RPC. This means that compared to the current-mode controller, the SPC behaves as a voltage source with controlled amplitude and frequency. In case of short-circuit situations, the controlled voltage source will simply respond by injecting very high current values. However, since VSCs must be protected from overcurrent situations, the current references must be limited in the case they are higher than allowed.

As explained in [103], the current limiting will greatly decrease the stability margin of the voltage-controlled converters during transients, since the active power may not be sufficient to remain synchronized with the grid. Furthermore, it is shown that when utilizing a PLC, which provides virtual inertia, the stability margin is further decreased compared to a cascaded voltage-current control structure with outer droop controllers. Even though the SPC can provide grid-supporting functionalities, provided that a power reserve is available, which enhances the transient stability of the network, the synchronization stability of the converter may be diminished in case of grid faults when including current limiters. From this, it is desired to test different limiting strategies to evaluate how a voltage-mode control structure can be employed during symmetrical grid

faults.

It is concluded that current limiting is needed but during transient events such as grid faults where the converter may be saturated, synchronization instability may be at risk. One solution is of course to oversize the converter such that it is able to handle larger currents. However, this comes with an increased converter cost, which is highly undesired. Another solution is to switch the control structure to grid-following mode during a fault, to provide current limiting that does not violate the objectives of the outer loops [104]. Even though this can be a solution, when to switch and how to achieve a seamless transition becomes a challenge. To that end, the advantages of the voltage-mode structure including its robustness towards weak-grid conditions will be lost during the fault. One test was conducted in this work where the current reference is limited to 1.2 pu. Since the control structure operates with sinusoidal signals, an instantaneous hard limiter clips the crest of the signal resulting in deteriorated current waveforms and square-wave resemblance. Therefore, a circular limiter is implemented where the stationary frame current reference is determined as

$$
\mathbf{i}^*_{\alpha\beta} = \begin{cases} \mathbf{i}_{\alpha\beta} \dfrac{I_{lim}}{\sqrt{i^2_\alpha + i^2_\beta}} & \text{if} \quad \sqrt{i^2_\alpha + i^2_\beta} > I_{lim}, \\ \mathbf{i}_{\alpha\beta} & \text{otherwise}, \end{cases} \tag{5.1.9}
$$

where I_{lim} is 1.2 pu of the nominal converter current. The response including the current limiter can be seen in Figure 5.4. Here it can be seen, that the current is limited to 1.2 pu during the fault and the outer control loops injects reactive power to boost the voltage and lowers its active power due to a jump in the virtual frequency. However, a few things should be noticed. Even though, capacitive reactive current is injected, the converter does not comply with the grid code since the voltage support is lowered during the fault period. Furthermore, due to the high power references during the fault, the slow outer loops, and the saturation of the current reference, a very long unsatisfactory response is seen after the fault is cleared caused by integrator windup in the outer loops. Here, the active power is increased slowly to 1.2 pu till it manages to fit its power references to the current limiter and return to 1 pu and the desired steady-state conditions.

Using this, it can be seen that the converter currents can be limited but the fault response and especially the post-fault response need to be improved. One problem of the method just discussed is that the outer power loops are not adjusted to take into account that the converter has very limited margins with respect to the injected currents.

One method which aims to limit the converter output by changing the active and reactive power references in case of a fault is presented in [105]. Here, the rated converter power during low-voltage conditions is updated when the fault occurs as

$$
S_{new} = \sqrt{\frac{3}{2}} \cdot \frac{V^+ - V^-}{V_b} S_n \tag{5.1.10}
$$

where S_n is the nominal converter power, V_b is the base rms line-to-line voltage at the PCC and $V^+ = \sqrt{v^{+2}_\alpha + v^{+2}_\beta}$ and $V^- = \sqrt{v^{-2}_\alpha + v^{-2}_\beta}$, is the amplitude of the positive and negative sequence voltages during the fault, see Appendix B for a detailed explanation of sequence components. Using this, it is considered that the converter should only inject positive-sequence currents during any type of fault. This consideration is to be further analyzed in later sections. Thus, in case of symmetrical faults $V^- = 0$ and using equation
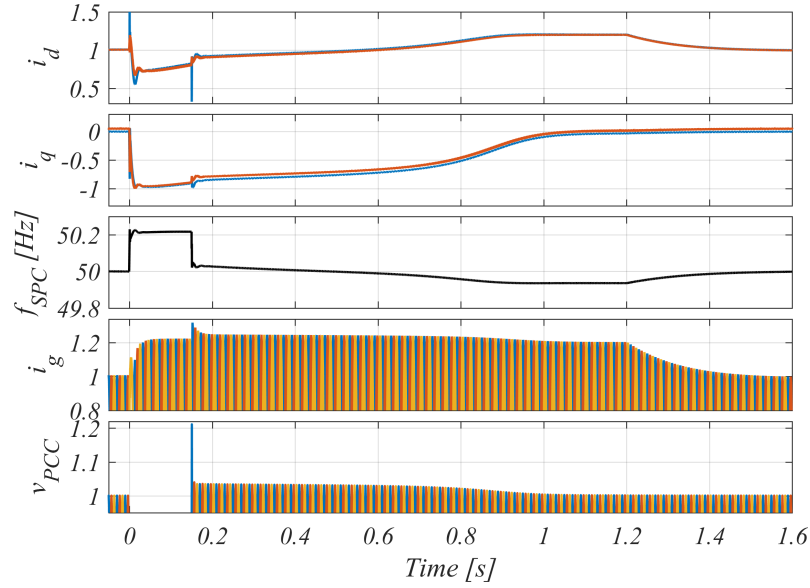
Figure 5.4: Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu including voltage feed-forward and retuned PR controller. The grid impedance is 0.04 pu and the current reference is limited to 1.2 pu.

(5.1.3), the expression reduces to

$$S_{new} = V_{pu}S_n. \tag{5.1.11}$$

The converter reactive power can then be calculated as

$$Q^* = \begin{cases} \text{Voltage Droop} & \text{if } V_{pu} > 0.9, \\ 2S_{new}(1 - V_{pu}) & \text{if } 0.5 < V_{pu} < 0.9, \\ S_{new} & \text{otherwise.} \end{cases} \tag{5.1.12}$$

Using the updated converter rated power and the reactive power reference, the active power reference preventing the converter overcurrent is calculated as

$$P^* = \sqrt{S_{new}^2 - Q^{*2}}. \tag{5.1.13}$$

In the case the reactive power reference is greater than the new rated converter power, the active power reference is set to zero and the reactive power reference is set equal to S_{new}. This is very similar to what was presented for the current-mode controller during fault events but in this case the reference power is used, which enables the use of the outer power controllers and the full SPC structure. The power limiting method presented in equation (5.1.12) are tested during a symmetrical fault as shown in Figure 5.5. Here it can be seen, that the current peaks is highly limited to around 3 pu and steadily decreases to 1 pu as the reference dictate. Despite that, it still takes more than 10 fundamental cycles till the current peaks are below 1.2 pu. This is because of the transient response of the outer PLC and RPC.

Current Limiting and Reference Power Adjustment

Since it is desired to limit just the current and not anything else during the fault, the
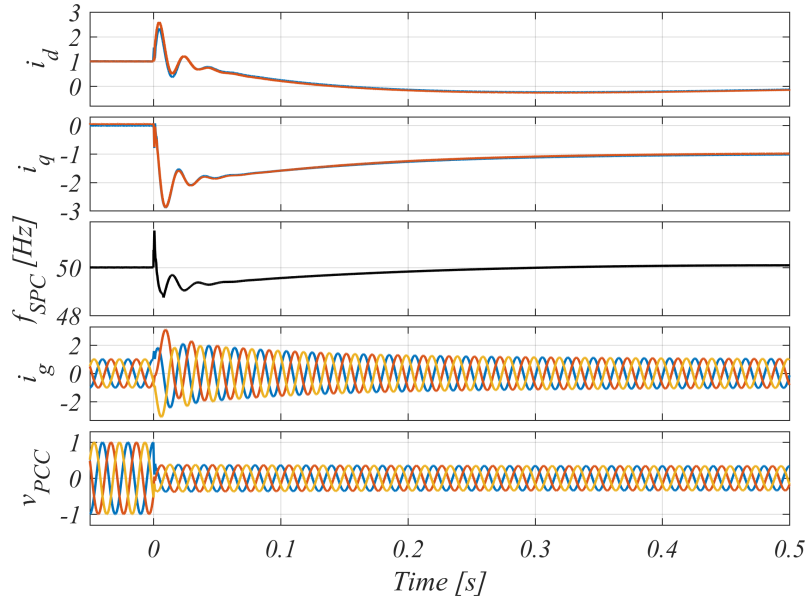
Figure 5.5: Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu including voltage feed-forward and retuned PR controller. The grid impedance is 0.04 pu and the power references are limited as shown in equation (5.1.12).

current reference is still the most logical place to do so. Therefore, the method where the reference power is adjusted based on the voltage dip during the fault (equation (5.1.12)) together with the circular current limitation is tested. Using this, the currents will be limited and the reference values set to the outer power controllers will be adjusted based on the grid code requirements. This structure can be seen in Figure 5.6 where S_F is used to select between the power references from the outer droop controllers and the power reference based on the requirements for the grid codes. S_F is an automatic signal which switches to fault-mode control when a fault is detected. The fault signal S_F is activated when the magnitude of the stationary-reference frame voltage vector drops below 0.9 pu. The fault-mode control is again switched back to the outer droop references when the fault is cleared but with a delay of 50 ms. This is done in order for the control to return around its nominal values before the droop controllers are again allowed to operate. The response of this method can be seen in Figure 5.7. Using this control approach, the current injection during the fault comply with the grid code and the post-fault response is significantly improved without exceeding the current limit and having to employ a pure current-mode control structure during the fault. As proposed in [31, 54], if a grid unbalance or grid fault is detected, the power-synchronization control is switched to current-mode control in order to limit the converter currents. This can effectively be done but has the need of a backup PLL, which is used in order for the converter to remain synchronized with the grid during the fault. As mentioned in the introduction and as explained in [106, 107], the PLL is a critical component for the controller stability of a converter, especially during low-voltage situations. Therefore, it is a great advantage that the proposed method shown in Figure 5.6 can be used to limit the converter currents, comply with grid code requirements while still employing the synchronous power controller structure, i.e. no need for a backup PLL. In this way, the SPC can provide grid-supporting functionalities during normal operating
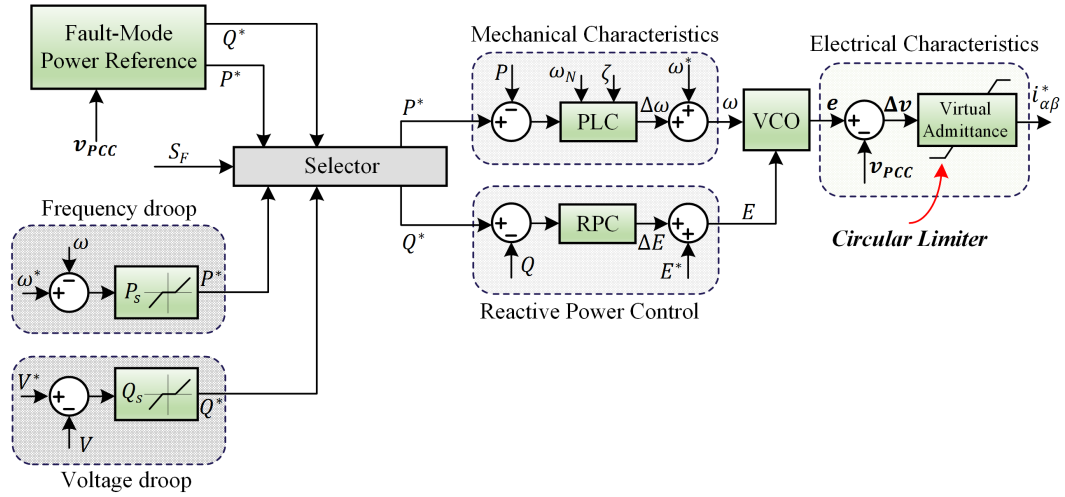
Figure 5.6: Control structure of SPC during fault-mode where the fault detection signal S_F selects between droop control and power reference control based on grid code requirements and a circular limiter is used to constrain the current reference.
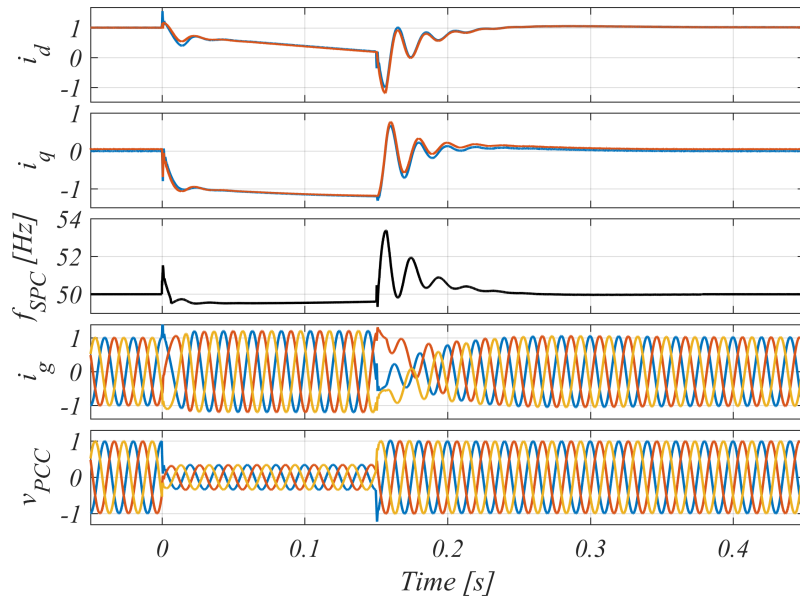
Figure 5.7: Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu including voltage feed-forward and retuned PR controller. The grid impedance is 0.04 pu and the control structure shown in Figure 5.6 is used for the reference power calculation. The fault mode signal S_F is high 200 ms after the fault occurs.

conditions and by only modifying the outer power reference generation instead of the inner structure, fault ride-through capability is achieved.

The experimental verification of Figure 5.7 is shown in Figure 5.8. In order for the converter to inject current during the fault without tripping the converter's over-current protection, the integral gain of the PLC is decreased to 1/10 of its original value. As it can be seen, the response during the fault is very similar to what is attained from the simulation. As the integral gain of the PLC is decreased, a more damped frequency

response is to be observed. Also, the fault recovery shows an excellent agreement between the experimental verification and the simulation results. Due to measurement noise and small phase unbalances, an oscillating component is present in the dq-axes current in the experimental results from Figure 5.8.

Figure 5.8: Experimental verification of Figure 5.7. The integral gain of the PLC is reduced with a factor ten. The converter outer power loops leave the fault mode control 200 ms after the fault instant.
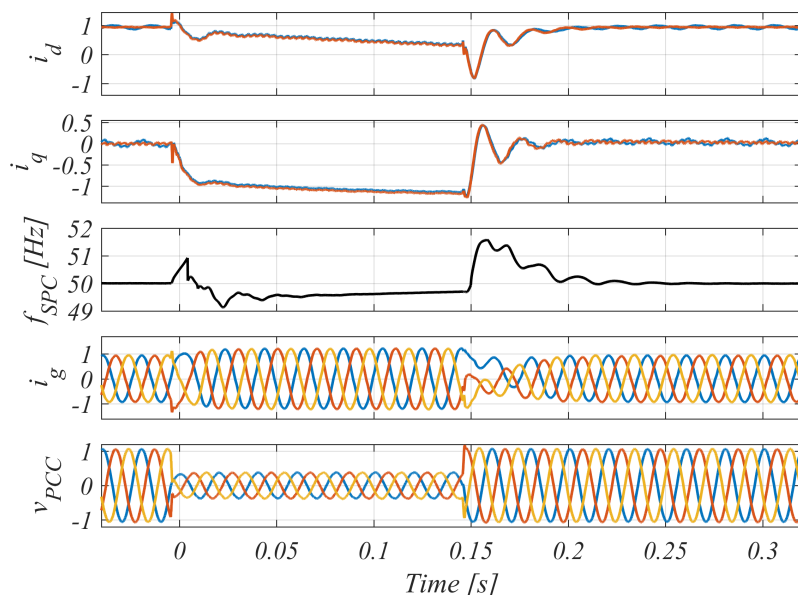
Remark: By applying a circular current limiting method and adjusting the outer power loops during the fault, the grid-forming structure can successfully ride through the fault as was achieved using the current-mode grid-following structure. To that end, no mode switching is performed for the voltage-mode controller, which implies that the benefits such as robust operation under weak-grid conditions can be utilized during a symmetrical fault as well.

5.2   Asymmetrical Faults

Despite that unbalanced grid faults takes up almost all fault occurring, requirements for negative-sequence current provision is rarely required by todays grid codes during asymmetrical faults. The majority of grid codes as the ones reviewed in subsection 1.4, only state requirements for the positive-sequence currents relative to the positive-sequence voltage during any fault type [108, 109].

Provision of dual-sequence currents during asymmetrical faults is often deliberated from the view of the power electronic converter. This means that many methods have been proposed to include negative-sequence currents during a fault in order to improve certain issues with respect to the converter. However, seen from the external network, inadequate work has studied the unbalanced control which benefits the power system and TSOs.

With regards to the power system during fault situations, the converter should support the grid voltage by injection of reactive currents. However, for asymmetrical faults this is likely not done by injection of positive-sequence currents only. As reported in [108], during injection of positive-sequence current during asymmetrical faults, the voltage in all phases are boosted, also in the healthy phases which might introduce undesired over-voltages. When this is the case, the converter possesses ideally an infinite impedance to the negative-sequence voltages which is far from the behavior provided by conventional synchronous machines. These possess significant impedance to negative-sequence voltages, which makes them effective in mitigating the negative effects of asymmetrical faults [40].

In the light of this and from the fact that power system operators prefer system operation as what is done with synchronous machines, it might be beneficial and logical that converters should inject negative-sequence currents as well during asymmetrical faults. In [108], it is shown that by injecting pure positive-sequence reactive currents, the negative-sequence voltage is actually boosted due to coupling between sequences at the fault location. As a result of this, over-voltages might occurs in the non-faulty phases. Therefore, it is shown to be beneficial to implement dual-sequence current injection where positive-sequence capacitive reactive current is injected to boost the positive-sequence voltages and negative-sequence inductive reactive current is injected to attenuate the negative-sequence voltages. As presented for the grid code for positive-sequence voltage support, a proportional term is included between the voltage drop and capacitive reactive current injection. The same thing can be done for the negative-sequence voltage attenuation during asymmetrical faults. The recently revised German grid code VDE-AR-N-4120 actually contains requirements for negative-sequence current provision during asymmetrical faults [110]. Here, it is recommended to proportionally alter the negative-sequence reactive current with a factor of 2-6 in relation to the negative-sequence voltage drop. Since the proportional gain used for the positive-sequence is 2, the same value will be used for the negative-sequence reactive current injection in this project.

5.2.1   Current Reference Generation during Asymmetrical Faults

To establish a controller for asymmetrical fault conditions, three tasks are of significant importance. These include separation of sequence components of the PCC voltage, current regulation of both positive and negative sequence components, and the approach at which the reference current is constructed as it is shown in Figure 5.9. Separation of the sequence components is usually done using a Dual Second-Order Generalized Integrator PLL (DSOGI-PLL) [111, 112], Double Synchronous Reference Frame PLL (DSRF-PLL) [113], or a SRF-PLL with complex coefficient notch and band-pass filters as discussed previously in this project. The asymmetrical current regulation can be directly performed using the developed PR controllers since they inherently can regulate both sequences.

Regarding the generation of the reference currents, which is the focus of this subsection, many methods are proposed with different aims including suppression of active power and dc-link voltage oscillations, suppression of oscillations in the reactive power, pure balanced current injection, or injecting positive-negative-sequence currents in order to support the positive-sequence voltage while suppressing the negative-sequence grid voltage, i.e. reducing the grid VUF [108]. One of the simplest methods, known as Instantaneous Active-Reactive Control (IARC) aims at all times to inject constant active and reactive
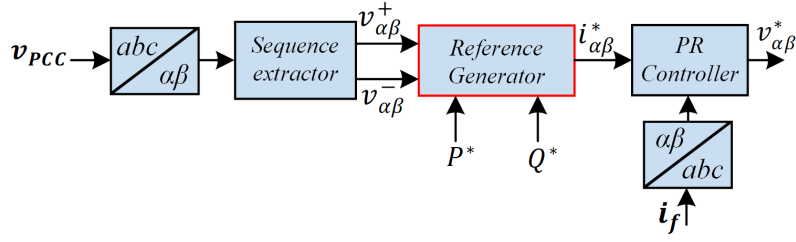
Figure 5.9: General fault control during asymmetrical faults. The reference generation of the currents are of interest in this subsection.

power. It utilizes that any current aligned with the voltage vector $\mathbf{v}$ will generate active power and any current vector aligned with $\mathbf{v}_\perp$ will generate reactive power. The big disadvantage of this approach is that during unbalanced grid conditions, the injected currents will be highly distorted with a second-order harmonic component, which is not acceptable in regards to the previously mentioned distortion limits. This second-order component originates naturally as it is not possible to inject pure fundamental frequency currents and achieve zero ripple in the active and reactive power during unbalanced voltage conditions simultaneously.

Another widely utilized method is called Balanced Positive Sequence Control (BPSC) which aims to inject a current vector synchronized with the positive-sequence grid voltage. This method has the advantage of injecting sinusoidal balanced currents but due to the interaction between the positive-sequence currents and the negative-sequence voltages, second-harmonic oscillations will be present in the active and reactive power as well as in the dc-link voltage.

One last method called Flexible Positive and Negative-Sequence Control (FPNSC) is used to develop a more general relationship between the current references and the positive and negative-sequence power references [109, 114, 115]. As described previously, since this project aims to provide grid-supporting functionalities, the last described method will be developed here, where both positive and negative-sequence currents can be injected and controlled in a flexible manner. In this work, it is desired to inject active power synchronized to the positive-sequence voltage, inject capacitive reactive power synchronized to the positive-sequence voltage (positive-sequence support) and inject inductive reactive power synchronized to the negative-sequence voltage (negative-sequence attenuation).

For a three-phase three-wire system, the voltages and currents can be fully described by the positive and negative-sequence components as [115]

$$\mathbf{v} = \mathbf{v}^+ + \mathbf{v}^- \quad \text{and} \quad \mathbf{i} = \mathbf{i}^+ + \mathbf{i}^-. \tag{5.2.1}$$

With the use of instantaneous power theory, the active and reactive power can be calculated as

$$p = \mathbf{v} \cdot \mathbf{i}, \quad q = \mathbf{v} \times \mathbf{i} = \mathbf{v}_\perp \cdot \mathbf{i} \tag{5.2.2}$$

where the orthogonal vector $\mathbf{v}_\perp$ expressed in the stationary-reference frame can be expressed as

$$\mathbf{v}_{\perp\alpha\beta} = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} \mathbf{v}_{\alpha\beta}. \tag{5.2.3}$$

In terms of the sequence components, the active and reactive powers in equation (5.2.2) can be written as

$$p = \underbrace{\mathbf{v}^+\mathbf{i}^+ + \mathbf{v}^-\mathbf{i}^-}_{P} + \underbrace{\mathbf{v}^+\mathbf{i}^- + \mathbf{v}^-\mathbf{i}^+}_{\tilde{P}} \tag{5.2.4}$$

and

$$q = \underbrace{\mathbf{v}_\perp^+\mathbf{i}^+ + \mathbf{v}_\perp^-\mathbf{i}^-}_{Q} + \underbrace{\mathbf{v}_\perp^+\mathbf{i}^- + \mathbf{v}_\perp^-\mathbf{i}^+}_{\tilde{Q}} \tag{5.2.5}$$

where each power consists of an oscillating and a constant term. The active and reactive power can also be expressed in the stationary-reference frame as

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \tag{5.2.6}$$

where each component consists of its sequence components. The currents can be confined by taking the inverse as

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{5.2.7}$$

Such an expression is normally augmented to identify the individual current components, which in the α or β frame provide active and reactive power [116]. This is

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ 0 \end{bmatrix} + \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ q \end{bmatrix} \triangleq \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix}, \tag{5.2.8}$$

where

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2}p, \qquad i_{\beta p} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2}p, \tag{5.2.9}$$

$$i_{\alpha q} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2}q, \qquad i_{\beta q} = -\frac{v_\alpha}{v_\alpha^2 + v_\beta^2}q, \tag{5.2.10}$$

which form the instantaneous active and reactive current terms on the $\alpha\beta$ axes. From this, FPNSC is developed where coefficients are introduced in order to be able to define a proportional ratio between the positive and negative sequence. In unbalanced cases, the $\alpha\beta$ components consists of both positive and negative-sequence components, e.g. $v_\alpha = v_\alpha^+ + v_\alpha^-$.

Thus, the current reference to be calculated can be written as

$$\mathbf{i}^* = \mathbf{i}_p^* + \mathbf{i}_q^* \tag{5.2.11}$$

where subscript p and q denote the current vector used to regulate the active and reactive power respectively, which both consists of its α and β axis components, each consisting of positive and negative-sequence components as just mentioned. This is

$$\mathbf{i}_p^* = \mathbf{i}_p^+ + \mathbf{i}_p^- \quad \text{and} \quad \mathbf{i}_q^* = \mathbf{i}_q^+ + \mathbf{i}_q^- \tag{5.2.12}$$

and e.g.

$$\mathbf{i}_p^+ = i_{p,\alpha}^+ + j i_{p,\beta}^+. \tag{5.2.13}$$

For the case of FPNSC, a parameter k_1 is used to regulate the ratio between positive and negative-sequence voltage on the active power current reference. This is expressed as

$$\mathbf{i}_p^* = k_1 \frac{P^*}{|\mathbf{v}^+|^2}\mathbf{v}^+ + (1-k_1)\frac{P^*}{|\mathbf{v}^-|^2}\mathbf{v}^- \tag{5.2.14}$$

where $0 \leq k_1 \leq 1$ and $|\mathbf{v}^+|^2 = (v_\alpha^+)^2 + (v_\beta^+)^2$. In the same way, the current reference used to regulate the reactive power is flexibly controlled by k_2 as

$$\mathbf{i}_q^* = k_2 \frac{Q^*}{|\mathbf{v}^+|^2}{\mathbf{v}_\perp}^+ + (1-k_2)\frac{Q^*}{|\mathbf{v}^-|^2}{\mathbf{v}_\perp}^- \tag{5.2.15}$$

where k_2 is used to determine the proportion at which the reactive power is controlled by the positive and negative-sequence voltage [86]. Here P^* and Q^* are the reference values for the active and reactive power, respectively. The full current reference can then be expressed as

$$\mathbf{i}^* = P^*\left(\frac{k_1}{|\mathbf{v}^+|^2}\mathbf{v}^+ + \frac{(1-k_1)}{|\mathbf{v}^-|^2}\mathbf{v}^-\right) + Q^*\left(\frac{k_2}{|\mathbf{v}^+|^2}\mathbf{v}_\perp^+ + \frac{(1-k_2)}{|\mathbf{v}^-|^2}\mathbf{v}_\perp^-\right). \tag{5.2.16}$$

If $k_1 = k_2 = 1$ in equation (5.2.16), then BPSC is achieved. Hence, this can be used to test the difference between the two and investigate how the injection of negative-sequence reactive power affects the VUF, which is expressed as

$$VUF = \frac{V^-}{V^+}. \tag{5.2.17}$$

For the implementation of the current reference generation during asymmetrical conditions, equation (5.2.16) is expressed in stationary coordinates including its positive and negative-sequence components. From this, the $\alpha\beta$-axis current references become

$$i_\alpha^* = P^*\frac{2}{3}\left(\frac{v_\alpha^+ k_1}{(v_\alpha^+)^2 + (v_\beta^+)^2} + \frac{v_\alpha^-(1-k_1)}{(v_\alpha^-)^2 + (v_\beta^-)^2}\right) + Q^*\frac{2}{3}\left(\frac{v_\beta^+ k_2}{(v_\alpha^+)^2 + (v_\beta^+)^2} + \frac{v_\beta^-(1-k_2)}{(v_\alpha^-)^2 + (v_\beta^-)^2}\right) \tag{5.2.18}$$

$$i_\beta^* = P^*\frac{2}{3}\left(\frac{v_\beta^+ k_1}{(v_\alpha^+)^2 + (v_\beta^+)^2} + \frac{v_\beta^-(1-k_1)}{(v_\alpha^-)^2 + (v_\beta^-)^2}\right) - Q^*\frac{2}{3}\left(\frac{v_\alpha^+ k_2}{(v_\alpha^+)^2 + (v_\beta^+)^2} + \frac{v_\alpha^-(1-k_2)}{(v_\alpha^-)^2 + (v_\beta^-)^2}\right) \tag{5.2.19}$$

where $2/3$ is included since a peak invariant Clarke transformation is used whereas for the instantaneous power theory discussed earlier a power invariant method was utilized to simplify the analysis. Notably, as this current reference strategy both consist of its positive and negative sequences, an expression for the three-phase converter currents is needed in order to avoid destructive over-currents during the fault.

Estimation of Maximum Converter Current
A relationship between the active and reactive power references, FPNSC coefficients and the corresponding converter current must be found in order to limit the converter currents. When this is found, one can solve for either active or reactive power references in order for the converter to inject currents not exceeding a predefined maximum value. Two approaches to estimate the converter currents, such that these can be limited, have been found. The first one, as described in [117], limit the converter currents based on the

magnitude of the space vector expressed in the stationary $\alpha\beta$ reference frame. This method has the advantage of not needing the information of the phase angle of the instantaneous positive and negative-sequence voltage but comes with the drawback that during unbalanced conditions, the limited space vector only utilizes the full converter current capacity if the maximum current is aligned with either the α or β axis. This means, that this method is precise during a SLG fault whereas the full current potential is not utilized for e.g. DLG faults.

The second method directly calculate the peak value of each converter phase current and then limits the converter output such that the highest of them does not exceed the maximum allowed current. The advantage of this approach is that the full converter current capability can be utilized during any unbalanced condition. However, the current estimation is dependent on an accurate determination of the phase angle of the positive and negative-sequence voltages, which also further complicates the analysis.

The phase current estimation method presented in [114, 118–120] uses the $\alpha\beta$ coordinates of the generated current reference and by using inverse Clarke transformation determines each phase current amplitude. The sequence components can be used to represent the $\alpha\beta$-axis components as

$$v_\alpha^+ = V^+ \cos(\omega t + \phi^+), \quad v_\alpha^- = V^+ \cos(-\omega t + \phi^-), \tag{5.2.20}$$
$$v_\beta^+ = V^+ \sin(\omega t + \phi^+), \quad v_\beta^- = V^+ \sin(-\omega t + \phi^-), \tag{5.2.21}$$

where

$$V^+ = \sqrt{(v_\alpha^+)^2 + (v_\beta^+)^2}, \quad \phi^+ = \tan^{-1}\left(\frac{v_\beta^+}{v_\alpha^+}\right), \tag{5.2.22}$$

$$V^- = \sqrt{(v_\alpha^-)^2 + (v_\beta^-)^2}, \quad \phi^- = \tan^{-1}\left(\frac{v_\beta^-}{v_\alpha^-}\right), \tag{5.2.23}$$

and by defining

$$I_p^+ = \frac{2k_1 P^*}{3V^+}, \qquad I_p^- = \frac{2(1-k_1)P^*}{3V^-}, \tag{5.2.24}$$

$$I_q^+ = \frac{2k_2 Q^*}{3V^+}, \qquad I_q^- = \frac{2(1-k_2)Q^*}{3V^-}, \tag{5.2.25}$$

the current references presented in equations (5.2.18) and (5.2.19) can be written as

$$i_\alpha^* = (I_p^+ + I_p^-)\cos(\omega t) + (I_q^+ - I_q^-)\sin(\omega t) = I_\alpha \cos(\omega t + \theta_\alpha), \tag{5.2.26}$$
$$i_\beta^* = (I_p^+ - I_p^-)\sin(\omega t) - (I_q^+ + I_q^-)\cos(\omega t) = I_\beta \cos(\omega t + \theta_\beta), \tag{5.2.27}$$

where

$$I_\alpha = \sqrt{(I_p^+ + I_p^-)^2 + (I_q^+ - I_q^-)^2}, \qquad \theta_\alpha = \tan^{-1}\left(\frac{I_q^+ - I_q^-}{I_p^+ + I_p^-}\right), \tag{5.2.28}$$

$$I_\beta = \sqrt{(I_p^+ - I_p^-)^2 + (-I_q^+ - I_q^-)^2}, \qquad \theta_\beta = \tan^{-1}\left(\frac{-I_q^+ - I_q^-}{I_p^+ - I_p^-}\right), \tag{5.2.29}$$

where it is assumed that $\phi^+ = \phi^- = 0$ and that ϕ^+ is synchronized with the PLL. From this, the peak value of phase-a will be I_α. Instead of using the inverse Clarke transformation

to calculate the expression for phase-b and phase-c, the ellipse which is being formed by the trajectory of the asymmetrical $\alpha\beta$ current reference can be rotated such that the α-axis is aligned with phase-b ($+2\pi/3$ radians) and phase-c ($-2\pi/3$ radians). When this is done, the peak value can be calculated as the magnitude of the α-axis component after the rotation is being performed. This is mathematically identical to the Clarke transformation but only one expression is needed to be developed for all three phases. The current reference ellipse is rotated by γ as [120]

$$\mathbf{i}^{*\prime} = \begin{bmatrix} i_\alpha^{*\prime} \\ i_\beta^{*\prime} \end{bmatrix} = \begin{bmatrix} \cos(\gamma) & -\sin(\gamma) \\ \sin(\gamma) & \cos(\gamma) \end{bmatrix} \begin{bmatrix} I_\alpha \cos(\omega t + \theta_\alpha) \\ I_\beta \sin(\omega t + \theta_\beta) \end{bmatrix}. \tag{5.2.30}$$

Evaluating only the α component of the rotated ellipse gives

$$i_\alpha^{*\prime} = I_\alpha \cos(\gamma) \cos(\omega t + \theta_\alpha) - I_\beta \sin(\gamma) \sin(\omega t + \theta_\beta), \tag{5.2.31}$$

which is equivalent to performing the Clarke transformation on the stationary $\alpha\beta$ components. Expanding $\cos(\omega t + \theta_\alpha)$ and $\sin(\omega t + \theta_\beta)$ gives that

$$i_\alpha^{*\prime} = I_\alpha \cos(\gamma)(\cos(\omega t)\cos(\theta_\alpha) - \sin(\omega t)\sin(\theta_\alpha)) - I_\beta \sin(\gamma)(\sin(\omega t)\cos(\theta_\beta) + \cos(\omega t)\sin(\theta_\beta)), \tag{5.2.32}$$

which can be expressed as

$$i_\alpha^{*\prime} = A_1 \cos(\omega t) + B_1 \sin(\omega t) \tag{5.2.33}$$

where

$$A_1 = I_\alpha \cos(\gamma)\cos(\theta_\alpha) - I_\beta \sin(\gamma)\sin(\theta_\beta) \tag{5.2.34}$$

$$B_1 = -I_\alpha \cos(\gamma)\sin(\theta_\alpha) - I_\beta \sin(\gamma)\cos(\theta_\beta). \tag{5.2.35}$$

It can be noticed that $I_\alpha \cos(\theta_\alpha)$ is simply the projection of I_α to the α-axis, which is

$$I_\alpha \cos(\theta_\alpha) = I_p^+ + I_p^-. \tag{5.2.36}$$

Using the same simplification of axis projection then

$$I_\beta \sin(\theta_\beta) = I_q^+ + I_q^- \tag{5.2.37}$$

$$I_\alpha \sin(\theta_\alpha) = I_q^+ - I_q^- \tag{5.2.38}$$

$$I_\beta \cos(\theta_\beta) = I_p^+ - I_p^- \tag{5.2.39}$$

which gives that

$$A_1 = (I_p^+ + I_p^-)\cos(\gamma) - (I_q^+ + I_q^-)\sin(\gamma) \tag{5.2.40}$$

$$B_1 = -(I_q^+ - I_q^-)\cos(\gamma) - (I_p^+ - I_p^-)\sin(\gamma). \tag{5.2.41}$$

Finally, the magnitude of α-component of the rotated ellipse can be expressed as

$$\hat{I} = \sqrt{A_1^2 + B_1^2}. \tag{5.2.42}$$

Here γ is the angle of which the current reference ellipse is rotated. Considering that $\phi^+ \neq \phi^-$, the ellipse will be rotated by

$$\delta_s = \frac{|\phi^+| - |\phi^-|}{2}. \tag{5.2.43}$$

Using this, the rotation angle has three different values dependent on which phase current peak value is desired to calculate [120]. This is

$$\gamma = \begin{cases} \delta_s & \text{for phase-a,} \\ \delta_s + 2\pi/3 & \text{for phase-b,} \\ \delta_s - 2\pi/3 & \text{for phase-c.} \end{cases}$$

Enhanced Current Reference Generation based on Converter Current Limitation

Now that an expression for calculating the peak value of the three phase currents has been given, the power references can be calculated such that the converter current limitation is not violated.

Using sequence components, the reactive power reference can be described as

$$Q^* = Q^+ + Q^- \tag{5.2.44}$$

where

$$Q^+ = Q^* k_2 \quad Q^- = Q^*(1 - k_2), \tag{5.2.45}$$

just as before. However, previously, the relation was determined based on some fixed ratio of the desired division of reactive power between the positive and negative sequence. As mentioned previously, seen from the grid point of view, a fixed value for k_2 is not necessarily beneficial. Instead, one could flexibly modify it dependent on the voltage unbalance of the grid. After a fault has happened, the maximum reactive power is achieved when the full current capability is used for reactive power injection. Using this, the reactive power reference based on the grid code can be expressed as

$$Q^+ = \begin{cases} 0 & \text{if } V^+ > 0.9, \\ 2Q_{max}(1 - V^+) & \text{if } 0.5 < V^+ < 0.9, \\ Q_{max} & \text{otherwise.} \end{cases} \tag{5.2.46}$$

and

$$Q^- = \begin{cases} 0 & \text{if } V^- < 0.1, \\ 2Q_{max}V^- & \text{if } 0.1 < V^- < 0.5, \\ Q_{max} & \text{otherwise.} \end{cases} \tag{5.2.47}$$

Using this, the reactive power reference can be expressed as

$$Q^* = Q^+ + Q^- = 2Q_{max}(1 - V^+ + V^-) \tag{5.2.48}$$

and k_2 can be calculated as

$$k_2 = \frac{Q^+}{Q^*} = \frac{1 - V^+}{1 - V^+ + V^-}. \tag{5.2.49}$$

Using this, the reactive power is now split between the positive and negative sequence depending on the VUF, rather than a defined fixed value. This implies that during a symmetrical fault $k_2 = 1$ since no negative-sequence voltage exists, which ensures that only the positive-sequence voltage will be supported. To that end, with an increasing

negative-sequence component, k_2 will approach zero, which means that more work is devoted to decrease the negative-sequence component instead of supporting the positive-sequence component.

From equation (5.2.48), it is evident that Q_{max} needs to be calculated in order to set the reference for the reactive power. By expanding equation (5.2.42), the maximum phase current can be expressed as a function of active and reactive power together with control coefficients as [120]

$$
\begin{aligned}
\hat{I}^2 = {} & \frac{4}{9} P^{*2} \left(\frac{k_1^2 (V^-)^2 + (1-k_1)^2 (V^+)^2 + 2k_1(1-k_1)\cos(2\gamma)V^+V^-}{(V^+)^2(V^-)^2} \right) \\
& + \frac{4}{9} Q^{*2} \left(\frac{k_2^2 (V^-)^2 + (1-k_2)^2 (V^+)^2 - 2k_2(1-k_2)\cos(2\gamma)V^+V^-}{(V^+)^2(V^-)^2} \right) \\
& - \frac{4}{9} P^* Q^* \left(\frac{2V^+V^-\sin(2\gamma)(k_1 + k_2 - 2k_1 k_2)}{(V^+)^2(V^-)^2} \right) .
\end{aligned}
\tag{5.2.50}
$$

During a fault, the reactive power is prioritized over active power. Therefore, Q_{max} is calculated for a zero active power reference. By setting the active power to zero in the expression for the maximum phase current, the maximum obtainable reactive power for a given current limitation can be calculated as

$$
Q_{max} = \min \left(\frac{3}{2} \sqrt{ \frac{I_{lim}^2 (V^+)^2 (V^-)^2}{k_2^2 (V^-)^2 + (1-k_2)^2 (V^+)^2 - 2k_2(1-k_2)\cos(2\gamma)V^+V^-} } \right) .
\tag{5.2.51}
$$

After Q_{max} has been computed, Q^+ and Q^- are calculated from equation (5.2.46) and (5.2.47) and the reactive power reference is calculated as $Q^* = Q^+ + Q^-$.

It should be noted that if $Q^* > Q_{max}$ then $Q^* = Q_{max}$. Using the reactive power reference in equation (5.2.50), any unused power capacity can be allocated to the active power by solving

$$
0 = a P_r^{*2} + b P_r^* + c
\tag{5.2.52}
$$

where

$$
a = \frac{4}{9} \left(\frac{k_1^2 (V^-)^2 + (1-k_1)^2 (V^+)^2 + 2k_1(1-k_1)\cos(2\gamma)V^+V^-}{(V^+)^2(V^-)^2} \right) ,
\tag{5.2.53}
$$

$$
b = -\frac{4}{9} Q^* \left(\frac{2V^+V^-\sin(2\gamma)(k_1 + k_2 - 2k_1 k_2)}{(V^+)^2(V^-)^2} \right) ,
\tag{5.2.54}
$$

$$
c = \frac{4}{9} (Q^*)^2 \left(\frac{k_2^2 (V^-)^2 + (1-k_2)^2 (V^+)^2 - 2k_2(1-k_2)\cos(2\gamma)V^+V^-}{(V^+)^2(V^-)^2} \right) - I_{lim}^2,
\tag{5.2.55}
$$

which has the solution

$$
P_r^* = \frac{-b \pm \sqrt{-4ac + b^2}}{2a}
\tag{5.2.56}
$$

where only the positive solution is of interest. P_r^* should be compared to the commanded reference obtained from the DVC to either safely send through the active power reference of require active power curtailment by reducing the reference to P_r^* in order to avoid destructive converter over-currents. In that case, a chopper circuit might be necessary to dissipate the excess dc-link power. Using the proposed method presented above, one can based on a maximum value of the converter current and in compliance with the VDE-ARN-N 4120 grid code calculate the active and reactive power references which can be inserted in equation (5.2.18) and (5.2.19) in order to calculate the needed stationary-reference current reference during any asymmetrical fault.

5.2.2 Asymmetrical Fault Control of Current-Mode Controller

With the current reference generation method developed, this is to be implemented and tested both in simulation and experimentally. The control implementation is visualized in Figure 5.10, which shows the control structure which is being activated when a fault is detected. As it can be seen, the output of the DVC and any given external reactive power reference is together with the positive and negative-sequence voltages used to calculated the desired current reference during the unbalanced fault.
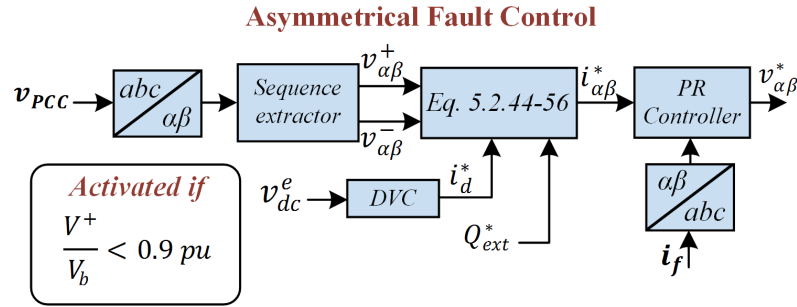

Figure 5.10: Asymmetrical fault control for current-mode controller activated when the positive-sequence voltage magnitude drops below 0.9 pu.

Two asymmetrical faults are considered for the verification: a solid SLG fault and a solid DLG.

As was mentioned previously, the WT step-up transformer is neglected in this work. However, referring to Table 1.2 in Section 1.3 for a transformer type 3, then a type B fault (SLG) observed on the converter terminals would result from a type C^* fault on the secondary side of the step-up transformer in a realistic scenario. Likewise, a type E fault (DLG) observed on the converter terminals would result from a type F fault on the secondary side of the step-up transformer.

In addition to the two fault types considered, three current reference generation methods are compared during each fault type. These are no support (current reference is zero during the fault), BPSC, and the proposed FPNSC taking into account the grid code requirements. The latter one is referred to as Flexible Positive and Negative-Sequence Control including Grid Code Requirements (FPNSC+GCR).

In Figure 5.11, the response with no support can be seen. The figure consists of five subplots: (a): three-phase grid currents, (b): positive- (blue) and negative- (red) sequence component of the converter current, (c) three-phase PCC voltage, (d) positive sequence (blue), negative sequence (red) and VUF (yellow) of the PCC voltage, and (e) instantaneous active power (blue) and reactive power (red). As expected, the currents and powers are reduced to zero and the sequence components of the PCC voltage can be extracted as a reference point of the system at a given fault type. From 0-0.15 s, the sequence components are shown for a SLG fault and from 0.15-0.3 s, the sequence components are shown for a DLG fault.

The performances of the BPSC and FPNSC+GCR exposed to a SLG fault are shown in Figure 5.12. Besides the five subplots described before, the dc-link voltage is included as well in the bottom subplot. It can be seen that the BPSC are activated from 0-0.15 s where the injected three-phase currents are balanced with a magnitude of 1.2 pu, i.e. the specified maximum fault current. At 0.15 s and until the clearance of the fault, the
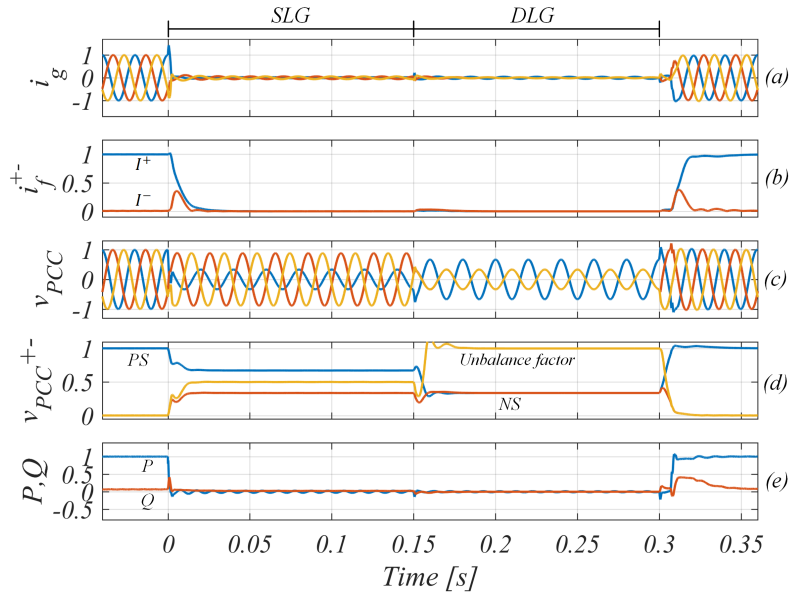
Figure 5.11: Simulation results of two consecutive asymmetrical faults without any support by the converter. At 0 s, a single line-to-ground fault occurs whereas at 0.15 s it develops into a double line-to-ground fault. The no support case can be used as a reference when evaluating different support functionalities. Line impedance is 0.1 pu, SCR is 10.

FPNSC+GCR is activated, which is easily seen by the injection of an asymmetrical set of currents. Similarly, the results for the BPSC and the FPNSC+GCR during a DLG fault can be seen in Figure 5.13. Interestingly, as it can be noticed from the DLG fault using the FPNSC+GCR, is that this set of unbalanced voltages together with the unbalanced injection of current results in constant active power as other current reference generation algorithms aim to achieve. This can also be seen in the dc-link where the voltage ripple is nearly zero. However, for the SLG shown in Figure 5.12, the dc-link voltage using the proposed FPNSC+GCR is a little bit larger compared to BPSC.

For comparison, the positive sequence, negative sequence, and VUF of the PCC voltage is read off for the three current reference methods during the two fault types, which can be seen in Table 5.1. Here it can be seen, that even though the positive-sequence voltage is decreased when switched from BPSC to FPNSC+GCR, the VUF is decreased for both cases. Also, the VUF is decreased with 30% with respect to the no support case for the FPNSC+GCR compared to 16% for the BPSC for the SLG fault. Besides a reduction in VUF by using the FPNSC+GCR, a larger headroom for voltage increase in the PCC voltage is achieved. That means that in case step-up transformers are included in the system, the risk of over-voltages at either sides is significantly reduced. It should be noted, that the grid impedance has a high influence on the improvement seen with the different methods. For example, if the grid impedance is very low, the PCC voltage will be nearly independent on the current injected by the converter. For a high impedance, a larger impact and difference between the BPSC and FPNSC+GCR will be seen.

The experimental results for the current-mode controller during an SLG fault are shown in Figure 5.14. Here, the experimental results are almost indistinguishably from the results

Figure 5.12: Simulated current-mode control during a solid single line-to-ground fault with retuned current regulator and enabled voltage feed-forward. The fault appears at 0 s and the control is switched to BPSC. At 0.15 s the asymmetrical fault control is switched to FPNSC+GCR before the fault is cleared at 0.3 s. Line impedance is 0.1 pu, SCR is 10.
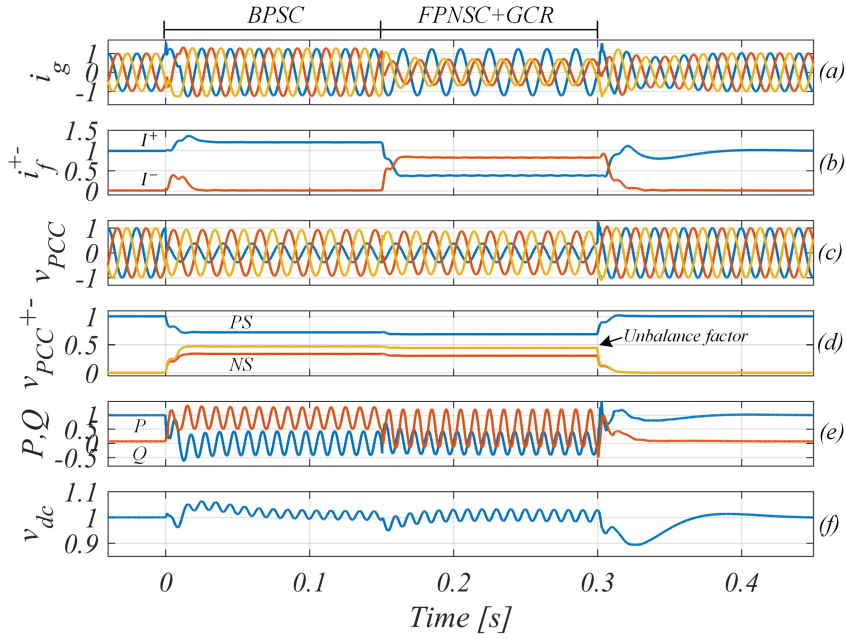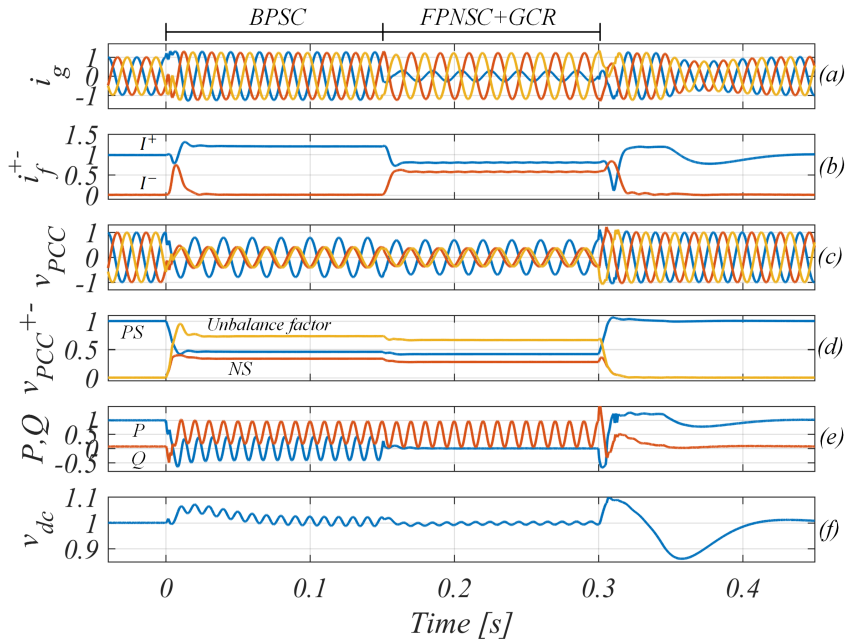

Figure 5.13: Simulated current-mode control during a solid double line-to-ground fault with retuned current regulator and enabled voltage feed-forward. The fault appears at 0 s and the control is switched to BPSC. At 0.15 s the asymmetrical fault control is switched to FPNSC+GCR before the fault is cleared at 0.3 s. Line impedance is 0.1 pu, SCR is 10.

Fault Type	Metric	BPSC		FPNSC+GCR		No Support	
SLG	V^+	0.79	0.77	0.71	0.71	0.68	0.68
	V^-	0.34	0.34	0.25	0.28	0.34	0.34
	VUF	0.42	0.46	0.35	0.41	0.50	0.50
DLG	V^+	0.46	0.42	0.42	0.39	0.34	0.34
	V^-	0.34	0.34	0.28	0.30	0.34	0.34
	VUF	0.73	0.85	0.67	0.79	1.00	1.00

Table 5.1: Voltage unbalanced factor (VUF) together with the positive and negative sequence component of the PCC voltage during two asymmetrical faults using three different reference generation methods. Blue numbers denote what are measured in the laboratory and black is the data obtained from the simulation.

obtained from the simulated case in Figure 5.12. Also, it can be noticed that the use of a constant dc-link voltage in the laboratory gives the same response as it was seen from the simulated case including a dc-link chopper.

Similarly, a DLG fault is performed in the laboratory where the results are shown in Figure 5.15. This is in great agreement with the simulated case where it can be observed that the active power is constant during FPNSC+GCR. The sequence components of the PCC voltage obtained from the experimental setup for the three injection methods are included in Table 5.1 marked with blue. Here, it can as well be noticed that the experimental verifications is in good agreement with the conducted simulations.
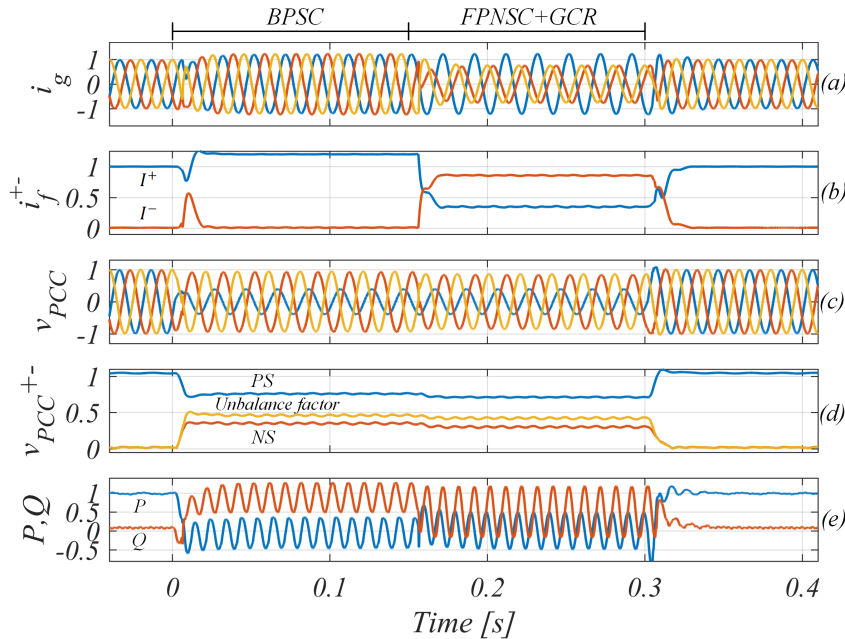

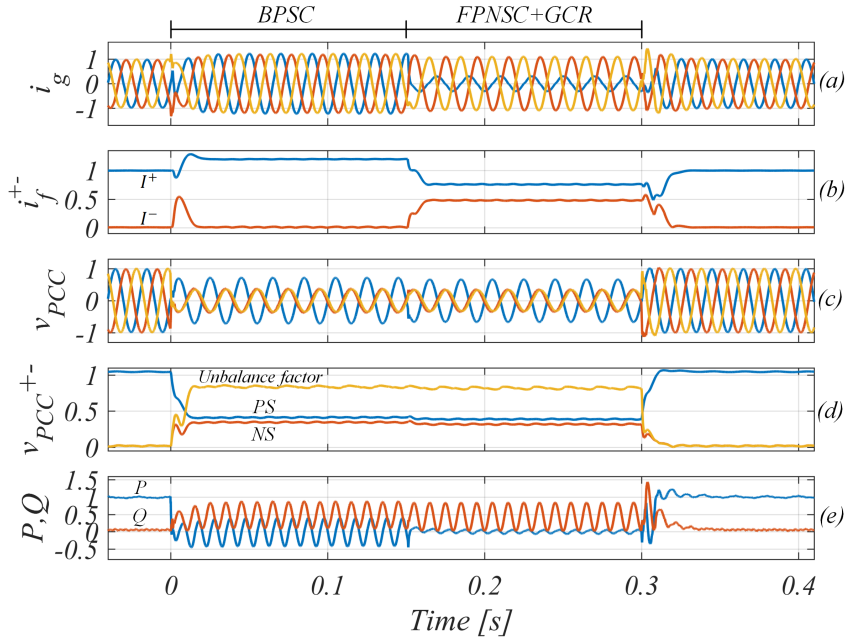Figure 5.14: Experimental validation of Figure 5.12 for a SLG fault.

Figure 5.15: Experimental validation of Figure 5.13 for a DLG fault.

5.2.3 Asymmetrical Fault Control of Voltage-Mode Controller

It was attempted to use the algorithm developed in subsection 5.2.1 to set the desired active and reactive powers during the asymmetrical fault for the outer PLC and RPC. In that case, two RPCs were implemented, one to control the positive sequence, and one to control the negative sequence of the reactive power by regulating the positive and negative sequence components of the virtual inner EMF. However, since the fault references are set in the outer loops, the response time for the fault current is way to slow to comply with any grid code requirements on fast fault-current provision. To that end, high converter currents are still injected at the initiation of the fault. Compared to the solution developed for the voltage-mode control during symmetrical faults where the references for the outer loops were modified and the inner current references were limited using a circular limiter, this approach cannot be used here due to the unbalanced nature of the converter currents, which do no longer form a circular trajectory, but an elliptical loci in the $\alpha\beta$ frame. This implies that if this approach is adopted using a circular limiter, the current reference will be highly distorted with a significant amount of 3rd, 5th, and 7th harmonics and the currents are not necessarily limited in the natural reference (abc) frame. Therefore, it is realized that the references must be provided directly in the inner loop in order to achieve an acceptable settling time of the fault current and to limit the elliptical current references. To that end, a more in depth look into state-of-the-art of asymmetrical fault control of voltage-mode control is performed to assess whether an already known solution can be employed.

In [121], an improved virtual synchronous power controller during unbalanced conditions is proposed. Here, the control structure developed does not include an inner current regulator and does only consider unbalanced conditions in steady-state, i.e. no consideration of fault events, grid code requirements, and fault current limitation. In [122], it is mentioned that multiple paralleled virtual admittances can be used to regulate both

the positive- and negative-sequence currents. Nevertheless, how to design the admittances is not described in much detail and the current limitation is not considered. To that end, how to set the outer power references during the fault is not addressed. In [123], the outer and inner loops are modified during the fault instant. That is the Q/V droop controller is shielded such that the outer loops will not attempt to raise the voltage back to nominal, which results in an unrealizable high reactive power reference. Also, the RPC is bypassed during the fault, such that no build up or wind-up will occur in the outer loops. This is basically similar to what was performed in this project during the symmetrical faults. A similar approach is proposed in [124], where both the references for the outer power loops and the inner current references are modified during the asymmetrical fault. The outer and inner reference modification are then calculated based on whether balanced currents, constant active power, or constant reactive power are desired during the fault. In this way, the basic grid-forming operation is kept during the fault, but results from the paper show that the full converter current capability is not being utilized during all conditions.

Based on this, a similar approach as was done for the voltage-mode controller during symmetrical faults are applied here, which is seen to be the most applicable developed method in state-of-the-art solutions. It should, however, be noted that since the circular current limitation cannot be employed during asymmetrical faults, the outer and inner loops must be completely decoupled during the fault, meaning that the inner loop is switched to current-mode control during the fault. Thus, the approach is to limit the outer power references such that wind-up will not occur in the outer loops, which significantly deteriorates the fault recovery response. In addition to this, the inner current references are calculated as it was done during the asymmetrical fault for the current-mode controller, such that the outer and inner loops are essentially separated during the fault. All of this is visualized in Figure 5.16, which is activated when the positive-sequence component of the PCC voltage drops below 0.9 pu. As it can be seen, when the fault occurs, the outer loops are effectively decoupled from the inner current regulator and the current reference is generated as what was done for the current-controlled converter during asymmetrical faults. In order to ensure that the outer loop will not wind up during the fault, the average power references are fed to the input of the outer loops. Figure 5.17 shows the plot of the active and reactive power references together with the measured active and reactive powers. Since the applied power references equal the average value of the measured active and reactive power, the error signal propagating through the PLC and RPC will not generate a virtual
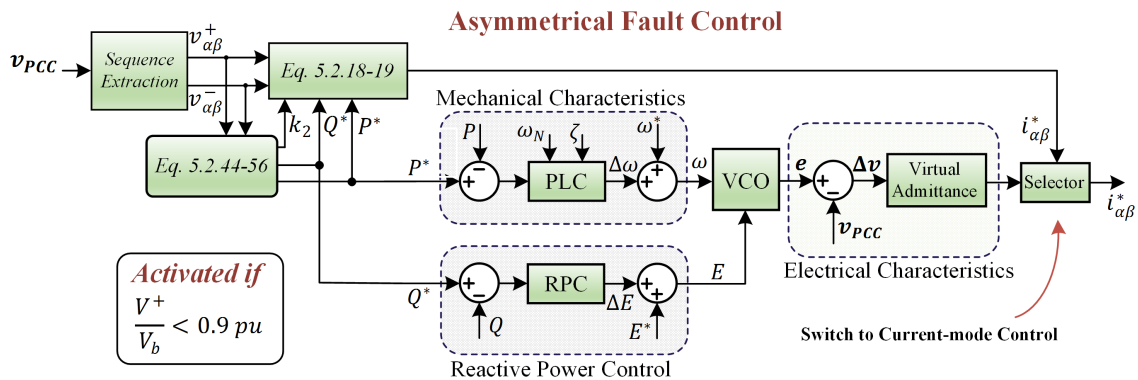
Figure 5.16: Asymmetrical fault control for voltage-mode controller activated when the positive-sequence voltage magnitude drops below 0.9 pu.

inner EMF, which will drift away during the fault. In this case, this should allow for a more seamless transition back to the voltage-mode control when the fault has been cleared.
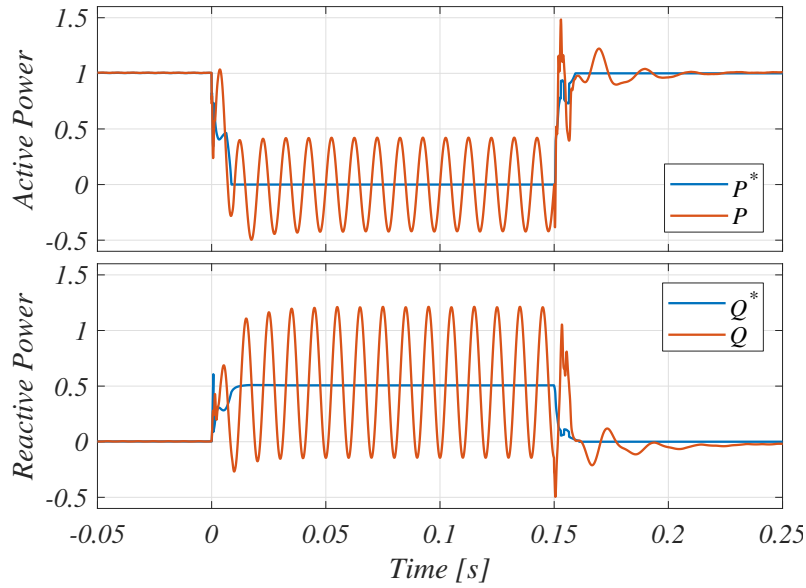
Figure 5.17: Simulated reference and measured power prior to PLC and RPC during an asymmetrical fault. The average value of the measured power is equal to the reference value.
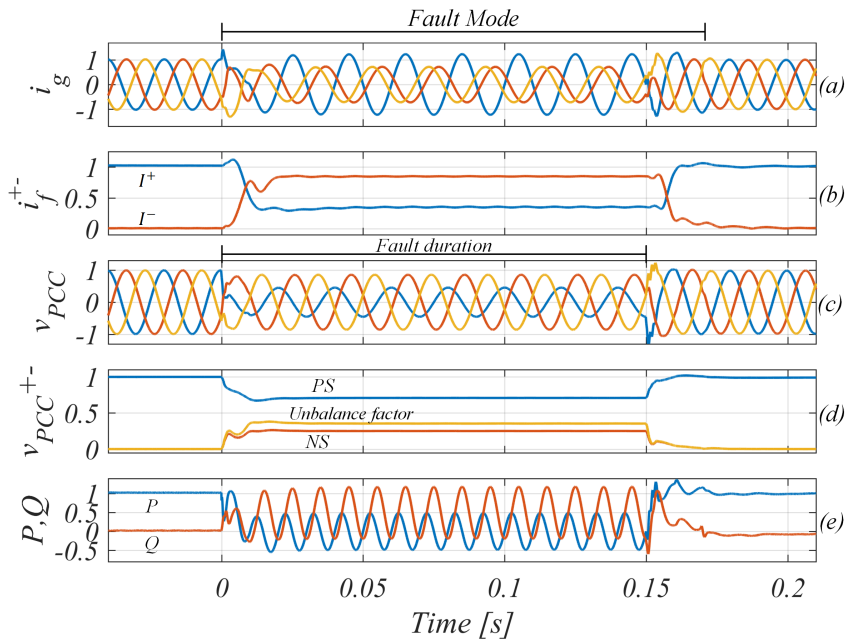
Figure 5.18: Voltage-mode control during solid single line-to-ground fault with retuned current regulator and enabled voltage feed-forward. Line impedance is 0.1 pu and the duration for the fault mode is indicated.

The SLG and DLG faults are as well tested for the SPC, which are shown in Figures 5.18 and 5.19, respectively. Since the current reference generation is identical to what was used for the current-mode control, the asymmetrical currents and PCC voltage sequence components are the same as shown for the current-mode verification and in Table 5.1.
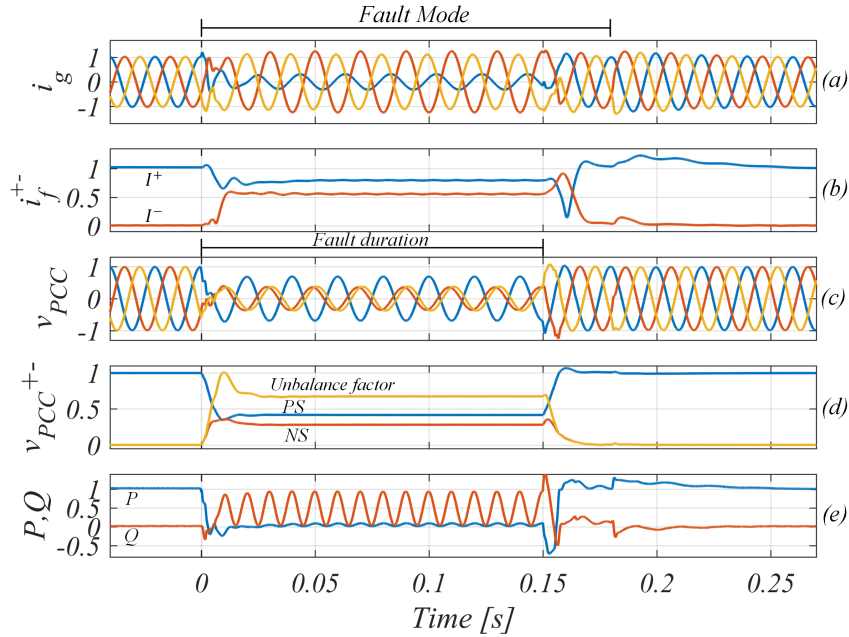
Figure 5.19: Voltage-mode control during solid double line-to-ground fault with retuned current regulator and enabled voltage feed-forward. Line impedance is 0.1 pu and the duration for the fault mode is indicated.

Here, the only difference lies in the transition to the current-regulated mode and back to voltage-regulated mode. As it can be seen, a rather smooth transition is achieved for the SLG fault as it is shown in Figure 5.18. However, sustained overshoots are seen in the active power and injected currents when the post-fault transition is made for the DLG fault as evident from Figure 5.19. This can be seen as a sudden jump in the power references after the fault clearance. This rather poor post-fault transition originates as a result of the inner EMF reference not being equal to the pre-fault reference when the system is switched back to voltage-mode control. This is suspected to be due to the reactive power difference between the average value from the fault controller and the measured one which is inherently different due to the reactive power consumption in the output LCL filter.

The asymmetrical fault control for the voltage-mode controller during a SLG and DLG fault is experimentally tested as shown in Figure 5.20 and Figure 5.21, respectively. Here the current reference is switched back to the voltage-mode 40-50 ms after the fault has been cleared and the outer power references leave the fault mode 200 ms after the fault has been cleared. As for the previous cases, the experimental verification of the asymmetrical faults of the SPC is closely matching the simulation results. Accordingly, the voltage-mode control structure can achieve fault ride-through behavior during asymmetrical faults in addition to the symmetrical faults considered previously.

It was mentioned in the problem formulation that it was unclear whether the voltage-mode controller could actually operate satisfactory during grid faults. It is seen that the advantages of the voltage-mode controller experienced during normal operating conditions including grid-supporting functionalities and its robustness against weak-grid conditions is reduced when exposed to grid faults. For such large disturbances, it is preferable to operate as a controlled current source and hence some inherent issues are present for the
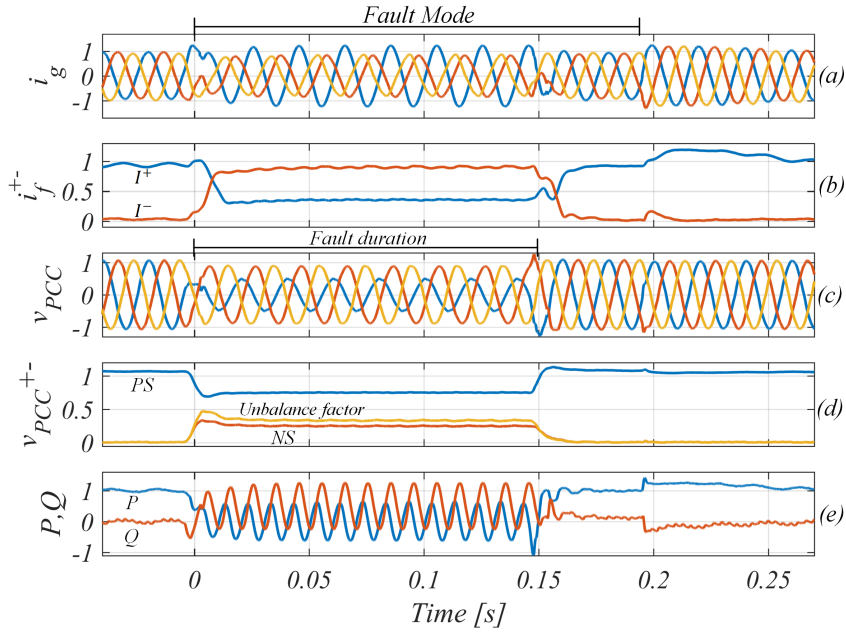
Figure 5.20: Experimental verification of Figure 5.18. The integral gain of the PLC is reduced with a factor ten. The converter current and outer loops leave the fault mode 190 ms after the fault instant.
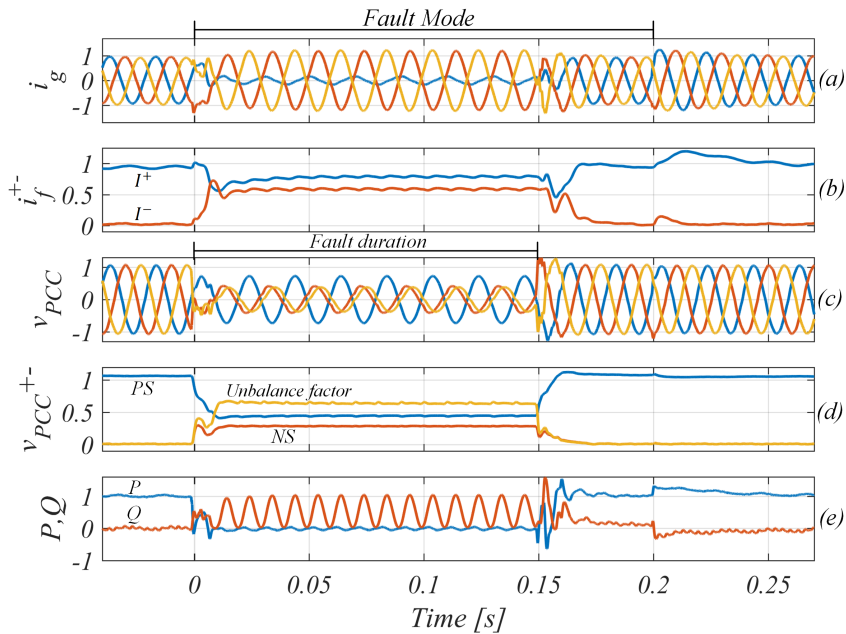
Figure 5.21: Experimental verification of Figure 5.19. The integral gain of the PLC is reduced with a factor ten. The converter current and outer loops leave the fault mode 200 ms after the fault instant.

voltage-mode controller, which must be handled carefully. For the symmetrical fault, the voltage-mode controller were successfully limited without compromising the grid-forming control structure during the fault. However, for the asymmetrical faults, the outer loops were basically just kept under control with the adjusted power references, whereas the actual converter behavior was switched to a current-controlled mode during the fault. In

addition to this, for asymmetrical faults, a PLL or frequency-locked loop is utilized for the extraction of sequence components used to generate the current reference. Hence, in this case, the voltage-mode controller is still dependent on a backup synchronization unit which is desired to be removed considering weak-grid conditions. Along these lines, more work is needed in the development of a general control structure for the voltage-mode control during grid faults to make the converter able to deal with both balanced and unbalanced grid faults where fault ride-through requirements are considered and the converter current is limited without compromising to much the outer loops and the fundamental grid-forming operation.

5.3   Summary of Developed Methods for Fault-Mode Control

A brief summary of the developed method is to be given for an easy comparison between the method and to highlight the main benefits and drawbacks of the current-mode controller and the developed voltage-mode controller. In this way, the reader can easily identify based on the controller of interest, how fault ride-through can be attained using each converter control structure alongside what fault response and performance are expected to be seen.

Symmetrical Faults

For the current-mode grid-following controller, the current references were directly set based on the considered grid-code requirements. In this way current limitation can easily by implemented and any available capacity for power transfer after reactive power support is allocated to active power injection. Using this approach, the dc-link voltage control can easily be implemented as well and a chopper circuit which can be used to dissipate any energy accumulation on the dc-link.

To achieve fault ride-through capability of the grid-forming structure, a circular current limiter was implemented while at the same time the outer power references were adjusted in order to avoid wind-up of the outer loops during the fault. Using this proposed method, the grid-forming structure can be sustained during the fault, while the injected currents comply with the grid codes and are safely limited. In this way, the robust performance towards weak-grid conditions is kept during the fault, which is a big advantage compared to the current-mode grid-following structure. Accordingly, in this case, enhanced performance can be attained using the grid-forming converter compared to the grid-following converter. On the other hand, as the dc-link voltage controller was seen to counteract the power synchronization mechanism, a constant dc-link voltage was considered for the grid-forming structure. Therefore, for WT applications, either the machine-side converter should control the dc-link voltage or more work should be devoted to combine the dc-link voltage control with the power-synchronization procedure of the grid-forming converter. A comparison of the developed fault-mode controller for the grid-forming structure is mentioned in relation to available literature in Table 5.2.

Asymmetrical Faults

During asymmetrical faults, the recent German grid code requiring dual-sequence current provision during asymmetrical faults was considered. To comply with this, a simple step-by-step tuning algorithm was developed based on the widely used FPNSC method

Symmetrical Faults

Ref	Solution	Pros	Cons
[31, 54, 104]	Grid-following mode during fault	Effective current limitation	Grid-forming structure is lost Needs a backup PLL Poor weak-grid performance
Proposed in subsection 5.1.2	Circular current limitation and outer power reference adjustment	Effective current limitation No need for backup PLL Keeps grid-forming structure	Does not cope with asymmetrical faults in its current form

Table 5.2: Overview and comparison between state-of-the-art solutions and solution from this project in terms of symmetrical fault control for grid-forming converters.

for current reference generation. Using this proposed strategy, the current references were once again directly set using the current-mode controller and a good fault ride-through capability was achieved including dc-link voltage control. Also, the proposed reference current generation strategy was shown to decrease the VUF and give an enhanced performance when compared to existing solutions.

For the voltage-mode grid-forming controller, the converter operation was switched to current-mode control during the fault and the outer loops were kept under control to avoid any wind-up causing issues during the later transition back to the grid-forming structure. With this, acceptable fault ride-through capability was attained but the grid-forming structure is lost during the fault alongside its robustness towards weak-grid conditions. Accordingly, more investigations need to be devoted for solving this issue. A comparison between the developed fault-mode controller for the grid-forming structure for asymmetrical faults and other available literature in provided in Table 5.3. From this is can be seen that the advantages from [124] and the proposed work for asymmetrical fault control may result in the desired grid-forming performance during the fault, since the basic grid-forming structure is kept and the converter currents are limited and fully utilized. Besides this, a general controller of the proposed symmetrical and asymmetrical fault control should be constructed such that it can easily handle both types or faults or at least distinguish the fault type and then select between the different solutions.

Asymmetrical Faults

Ref.	Solution	Pros	Cons
[104]	Grid-following mode during fault	Effective current limitation	Grid-forming structure is lost Needs a backup PLL Poor weak-grid performance
[121]	No fault-mode action	Keeps the grid-forming structure	Does not provide current limitation during fault
[122]	Multiple parallel positive and negative sequences virtual admittances	Current limitation can be achieved	The current limitation is depending on the voltage sag level and therefore the selected values for the admittances
[123]	Freezes droop controller, RPC and PLC during the fault	Provides current limitation Works for both symmetrical and asymmetrical faults	Outer loops are frozen and the mechanical and excitation emulation of the machine is not operating during the fault
[124]	Adjustment of power references and virtual admittance limitation	Grid-forming structure is kept for the positive-sequence control Effective current limitation	Full converter capacity is only utilized when $Q^* = P^*$ Does not consider grid-codes.
Proposed in subsection 5.2.3	Asymmetrical current reference tracking using grid-following mode during fault. Outer loops are controlled for seamless switching after fault recovery	Complies with recent grid codes Provides exact current limitation Seamless switching after fault recovery	Grid-forming structure is lost during the fault.

Table 5.3: Overview and comparison between state-of-the-art solutions and the solution from this project in terms of asymmetrical fault control for grid-forming converters.

6 Conclusion

As the power system becomes more and more dominated by power electronic converters, their control in present and future power systems are increasingly important in order to maintain a stable and reliable system with a high security of supply. Up till now grid-connected converters have been controlled as grid-following units, which simply inject maximum power following the available grid voltage. However, several issues of this type of control have been extensively discussed in the state-of-the-art literature. Firstly, for weak-grid conditions, the synchronization unit may become unstable. Secondly, with an increasing penetration of converter-based generation, additional grid-supporting functionalities are demanded, which can easily be achieved using a grid-forming control structure to support the grid. Finally, during islanding operation, a grid-following converter cannot operate alone. Therefore, a large interest has emerged to regulate the converter as a controlled voltage source to mitigate these drawbacks. However, during fault conditions, how to operate the voltage-mode grid-forming converter is lacking from state-of-the-art literature. To address this, the work of this project has developed and compared a conventional grid-following control structure to a grid-forming controller with special attention to their fault ride-through capability and performance.

The problem to be studied was specifically formulated after describing grid code requirements, general theory of power system faults together with the considered network parameters. After this, the modeling of the VSI was performed, its average model was derived, the utilized pulse width modulation strategy was selected, and the ac-side output LCL filter was designed. Subsequently, a thorough description of the current-mode controller was given. This includes a discussion and design of the inner current regulator including delays and digital implementation, voltage feed-forward, grid synchronization using a SRF-PLL, a prefiltering stage to the synchronization unit, and the dc-link voltage controller. Next, the same procedure was performed for the voltage-mode controller where the synchronous power controller was selected as reference. This includes development and design of outer voltage and frequency droop controllers, virtual emulation of mechanical and electrical parameters of a synchronous machine, together with an outer reactive power controller.

In Chapter 4, the developed current-mode and voltage-mode controllers were validated and compared during a few tests under normal operating conditions. Here it was seen that the robustness of the voltage-mode controller towards weak-grid conditions is superior to the response of the current-mode controller. Regarding grid-supporting functionalities in normal operating conditions, the synchronous power controller was shown to support the network frequency through short-term active power injection and the network voltages through a change in its reactive power injection set-point. This is highly beneficial for power system frequency and voltage stability whereas for the basic grid-following converter, no supporting reactions resulted.

The fault behavior of the current-mode and voltage-mode controllers were analyzed in Chapter 5 where both controllers were compared during symmetrical as well as asymmetrical grid faults. At first, the current references for the current-mode controller were developed based on grid code requirements. To consider any potential energy accumulation on the dc-link capacitor, dc-chopper control was implemented and tested in simulation. Here, it was seen that the current-mode controller without any issues follows its fault-mode current references while at the same time restores the dc-link voltage to its nominal value. During the test of the voltage-mode controller during a symmetrical fault, it was evident that a controlled voltage source for a device with a low margin for additional current is very challenging considering a grid fault. Hence, the fundamental operation of the voltage-mode controller cannot be used during fault conditions as current limitation is mandatory. To ride through the fault without overloading the converter, it was shown that saturation of the converter current in the inner loop was necessary. In addition to this, the references of the outer loops must be adjusted in order to avoid wind-up in the outer loops. Implementing these two modification allowed for an acceptable fault current response during the symmetrical fault for the voltage-mode grid-forming controller. This proposed method for fault-mode control of grid-forming converters during symmetrical faults is submitted and considered for journal publication.

Besides for the symmetrical faults, fault control for both control structures have been conducted during asymmetrical faults as well. Here, a proposed current reference strategy for asymmetrical faults based on new requirements of grid codes has been described in detail and implemented. This proposed reference current generation strategy is also submitted for journal publication. Using this method, both positive- and negative-sequence currents are to be injected dependent on the positive and negative sequence of the voltages measured at the PCC. At first, the current-mode controller was tested during a solid single line-to-ground and a solid double line-to-ground fault using three different current reference strategies: zero-current injection, balanced positive-sequence injection, and the proposed dual-sequence current injection. Here it was clearly demonstrated, that the voltage unbalance factor can be significantly reduced by injecting asymmetrical currents into the grid. Furthermore, lower peak voltages were achieved, which means that considering the effect transformers has on the voltage sag seen, the risk of exposing the system to phase over-voltages is reduced.

At last, the fault control during asymmetrical faults for the voltage-mode controller was discussed. Here, different strategies were investigated including a modification of the outer power references. However, due to the slow response of the outer loops, the fault current provision did not comply with grid code legislation and in addition to this, the converter current was not properly limited. In an attempt to implement an acceptable fault control algorithm for the voltage-mode controller, a more thorough look into the state-of-the-art literature was performed. Here it was enclosed that no direct applicable method is available and that the most developed methods aim to actually control the current references directly during the fault and then modify the outer power loops to avoid wind-up of the virtual electromotive force of the emulated machine. This approach, which is similar to what was performed during symmetrical faults, was done for the voltage-mode controller during asymmetrical faults. This basically means, that the structure was switched to a current-mode structure during the fault and at the same time, the references of the outer power loops were modified such that these will not change significantly from their pre-fault

state. Implementing this, it was seen as anticipated, that the sequence components of the PCC voltage were identical to the results obtained using the current-mode controller. However, even though the fault response is identical, the voltage-mode controller has the disadvantage that a non-seamless transition back to the voltage-mode controller will make the fault recovery response deteriorated. The performed simulations were validated using the experimental setup described in Appendix A which verified the accuracy of the developed simulation model and controller structures. The experimental verifications of both the current-mode and voltage-mode controller were in great agreements with the simulated cases.

It is concluded that the advantages and benefits associated with the voltage-mode controller during normal operating conditions including grid-supporting functionalities and a high robustness to weak-grid conditions is diminished when a large transient disturbance such as low-voltage conditions occur. Here, the current-controller is advantageous since the converter currents can be easily controlled. Along these lines, the voltage-mode controller is inherently in trouble during grid faults, since at such conditions, it is actually desired to have a converter, which behaves as a controlled current source in order to protect it. This means, seen from the author's point of view, that no matter how sophisticated a fault controller one develops for the voltage-mode control structure, it will be a workaround the fact that it is simply desired to inject carefully controlled currents considering the present small headroom for additional current. Therefore, as it was also stated in the introduction to this project, very limited work has been conducted about how to deal with a voltage-mode control structure during fault conditions. It has been shown in this project that fault ride-through capability can be attained by grid-forming converters during both symmetrical and asymmetrical faults by carefully designing the fault control and converter current limitation. However, for the asymmetrical faults, it was needed to switch to current-mode control during the fault, which has the disadvantage of losing the grid-forming structure and the enhanced weak-grid performance. Therefore, further research should be done in order to investigate how it is possible to achieve fault ride-through capability of the voltage-mode controller during asymmetrical faults without having to do transitions to and from current-mode during the fault. Finally the novelty and contributions of this project are as follows:

- Proposal of enhanced reference current generation strategy during asymmetrical grid faults which comply with the latest requirements for dual-sequence current injection. This proposed method is submitted for journal publication.

- Proposal of fault-mode controller for the grid-forming converter during symmetrical faults, which is able to keep the characteristics of the grid-forming structure while safely limiting the converter currents. This proposed control method is as well submitted for journal publication.

- Finally, in regards to answering the problem formulation, the fault ride-through behavior of grid-connected converters can be enhanced by utilizing a voltage-controlled converter rather than a conventional current-controlled converter. This is proven using the proposed method during symmetrical faults, but more work is needed in order for it to be generalized to any grid fault.

6.1 Future Work

This section is devoted to describe what actions and additional tasks that should be done to further verify the performed analysis as well as developing a robust, clearly understood, and trusted voltage-mode control structure able to cope with any power system condition.

Dc-link Voltage Controller
For the experimental results performed in this project, the dc-link voltage was controlled to be constant by an active rectifier. However, usually, it is the task of the grid-side converter to regulate the dc-link voltage as was performed in the simulation study. Therefore, it would be interesting to validate also the dc-link voltage controller during the considered fault conditions to see whether the developed control operates satisfactory in the laboratory as well. In addition to this, to perform a more realistic control structure for the voltage-mode controller, the dc-link voltage controller should be included in the control as well. In this way, during a fault, the system has to ensure that dc-link over-voltage will not occur in the case where the active power transfer capability is significantly reduced.

Include Industry Applied Parameters for Study
For this project, the system working conditions and parameters were selected to match the laboratory setup used in this project. This was done to allow for an easy comparison between the simulation and experimental results. However, for a real world application, wind turbines are operating at high power levels above several MW. In addition to this, the operating voltage is higher, which also implies that a higher dc-link voltage must be used, often above 1 kV. Usually, the generator voltage is 690 V (l-l rms), which implies that several kA must be injected to the output filter of the system. With such high currents, the filter inductances should be much smaller than what is considered in this project since in practice, the voltage drop across them cannot be too high. To that end, the filter capacitance is much larger in real world applications compared to what is considered here. Furthermore, due to the high power level, the switching frequency of the system will be reduced. As seen in [52], a switching frequency of 2 kHz for a 7 MVA wind turbine was used for a three-level neutral-point clamped converter. In [69], a 5 MVA wind turbine is controlled using a two-level converter at a switching frequency of 2.5 kHz, in [125], a switching frequency of 2.85 kHz is used for a 2.2 MVA system and in [67], a switching frequency of 2.55 kHz is used for a 2.2 MVA system. From this, when considering a high power level, a switching frequency in the range of 2-3 kHz is realistic. Besides these parameters, the step-up transformer was neglected in this project which means, that different voltage levels from the wind turbine to the external grid is not considered. All of these will have an impact on the system. Therefore, for future work, a simulation model should be established, which includes the parameters of a high power equivalent system.

Improve Fault-Mode Controller during Asymmetrical Faults and Develop General Controller for Any Fault Type for the Voltage-Mode Structure
Despite the advantages of the voltage-mode controller shown during normal operating conditions, it was shown that the current-mode controller is advantageous during grid faults as the injected currents are easily manipulated and safely tracked within allowed

limits. As discussed in Chapter 5 and in the conclusion, no good and robust approach to deal with voltage-mode control during any type of grid fault seem to be existing. In addition to this, a PLL/frequency-locked loop-less sequence extraction algorithm should be used to fully remove the need for a backup synchronization unit for the voltage-mode controller during any fault type. Additionally, in order to further analyze how the voltage-mode controller can be improved without having to switch between different controller modes, the fundamental issue of the problem should be fully understood and more work should be devoted to develop a general fault control method for the voltage-mode controller which eliminates the need to switch to current control during asymmetrical faults. One suggestion is to attempt to use the ideas presented in this work with the advantages of the proposed solution from the authors in [124].

Appendix

A Experimental Test Setup

This chapter describes the experimental test setup used to verify the current-mode and voltage-mode control structure developed in Chapter 4. The full experimental setup is depicted in Figure A.1. Here, a Yaskawa D1000 active rectifier is connected to the grid through a Dyn11 transformer and a circuit breaker. The Dyn11 transformer is an isolation transformer where the secondary-side is grounded and the line voltage of the star-windings lead the delta-windings line voltages by 30°, which is being used to remove circulating currents in the setup. The active rectifier is set to control the dc-link voltage to a desired value of 730 V. As it can be seen, only the inverter (Danfoss VLT FC-302 15 kW) is being controlled in this project. The converter currents, grid currents and PCC voltages are being measured using two types of LEM sensors. Between the PCC and the grid simulator (a Chroma Regenerative Grid Simulator Model 61845) is the line/grid impedance Z_L. At last, the grid simulator is connected to the grid which closes the entire circuit. The physical components of the machine-side converter (active rectifier), grid-side converter, LCL filter, Z_L, the dSPACE expansion box controller, and the grid simulator are visualized in Figure A.2.

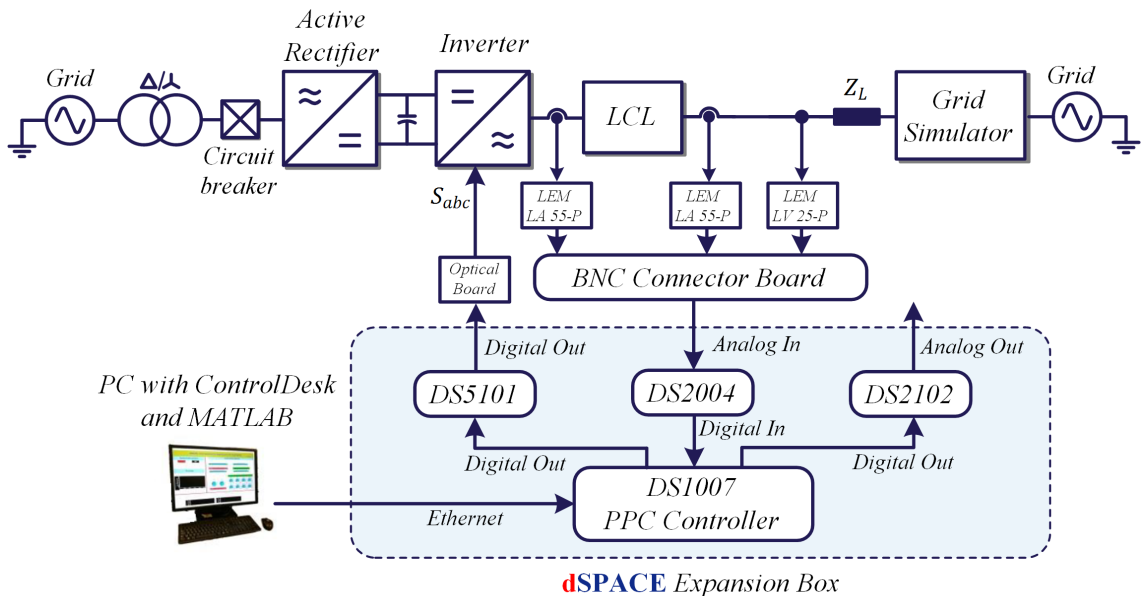Figure A.1: Diagram of the laboratory setup.

The gate signals calculated from the digital controller are converted into light pulses, which are being transferred through optical fibre. At the Danfoss converter, an add-on board is used to converter the light signals back to digital signals send to the gate driver circuit. This is done to achieve a high immunity to electromagnetic interference since the
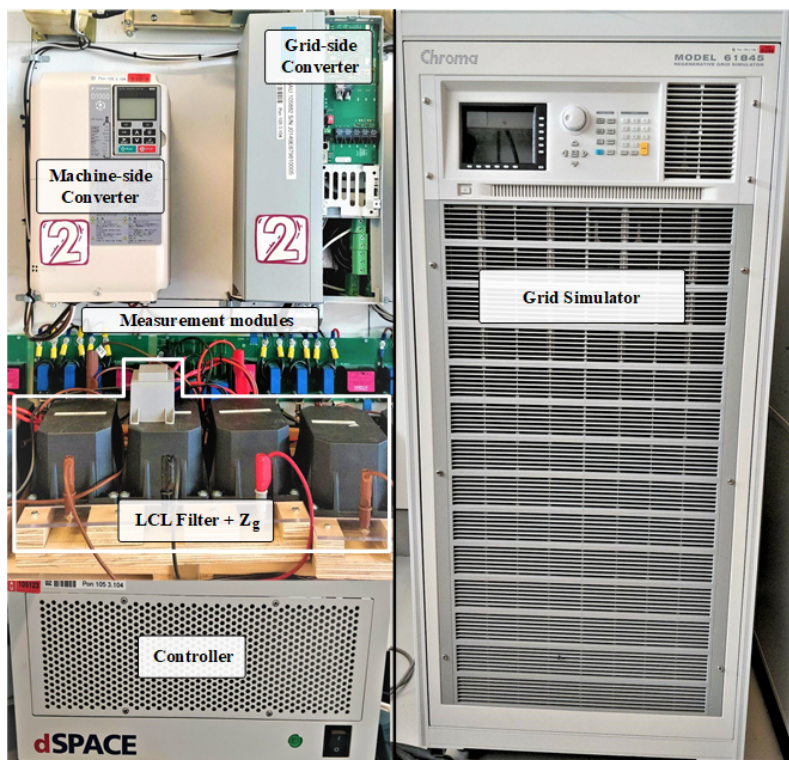
Figure A.2: Picture of the laboratory setup components including machine-side converter, grid-side converter, passives, measurements modules, dSPACE controller, and grid simulator.

distance from the PWM pulse generation is around 1-2 meters from the interface card to the inverter. The actual programming, control, and acqusition using dSPACE is to be described in the following paragraph.

dSPACE Control and Data Acquisition
Using a PC with *ControlDesk* and MATLAB installed together with the dSPACE expansion box with associated modules, it is possible to perform real-time control of the inverter using the environment of MATLABs Simulink. A Simulink model together with the real-time interface library from dSPACE, enables real-time control and monitoring of the voltages and currents together with online parameter change, which facilitates the emulation of e.g. load steps. As it can be seen from the dSPACE expansion box from Figure A.1, the interior of this box comprise a DS1007 PPC processor board, a DS5101 digital waveform output board, a DS2004 high-speed A/D board, and a DS2102 D/A board where the latter is not being used in the project.

Through an ethernet interface, the DS1007 2 GHz dual-core processor is being equipped with a compiled version of the built Simulink model and can also be used to have real-time model access during operation. This is transferred to machine code and is being stored in the flash of the PPC controller from where the actual program is run. To send and recieve digital signals, the DS1007 communicates with the DS5101, DS2004, and DS2102 via a fast PHS interface bus.

The DS5101 digital output board is specifically designed for generating pulse patterns such as PWM. It is equipped with 16 channels and has a time resolution of 25 ns where

pulse widths can be changed in real-time together with triggers and interrupts.

The DS2004 is an Analog to Digital Converter (ADC) with 16 independent input differential channels each with a resolution of 16 bits and a conversion time of 800 ns. This board is used to convert all analog current and voltage measurements to digital numbers to be used in the digital controller.

The DS2102 is a 6 channel, 16 bit Digital to Analog Converter output board facilitating to output signals from the controller to the continuous setup. This module will not be used in this project directly, but may be used to send a signal used to trigger measurements on the oscilloscope.

For accurate closed-loop control of the system, the PCC voltage and converter-side current need to be measured. Notably, the grid-side current is measured as well but not for a control purpose. These measurements are performed using two types of LEM sensors: LEM LA 55-P for the current and LEM LV 25-P for the voltage. Both transducers are connected to the BNC connector panel which is connected to the ADC module of the dSPACE expansion box. Since these transducers uses current to sense both current and voltage and thereby provide galvanic isolation, input resistors must be included for the voltage measurement to convert it to a desired range of current. This is shown as R_1 is Figure A.3. The rated input current of the voltage transducer is 10 mA rms and the used value for R_1 in the laboratory is 40 kΩ. This means that the nominal rms voltage that can be measured will be 400 V, which matches the line-to-line rms voltage which the transducer measures. The transducer can operate with a primary current up to ±14 mA so there is headroom for measuring voltages above the nominal value. The turns ratio from primary to secondary-side of the voltage transducer is $K_{nv} = 2.5$. This means that when the input voltage rms line-to-line is at its nominal value, the secondary-side current will be 25 mA. The input voltage range of the ADC of the DS2004 is ±10V. Thus, the secondary-side current needs to be converter back to a voltage utilizing as much range as possible of the ADC but with headroom. Here, a 220 Ω resistor (R_{Mv}) is connected across the BNC input directly at the BNC connector board. This gives a nominal ADC voltage at nominal line-to-line rms voltage of ±7.78 V. The actual resolution of the measured voltage is then

$$V_{PCC,res} = \frac{400V \cdot \sqrt{2}}{\frac{7.78V}{10V}(2^{16} - 1)} = 11mV. \tag{A.0.1}$$
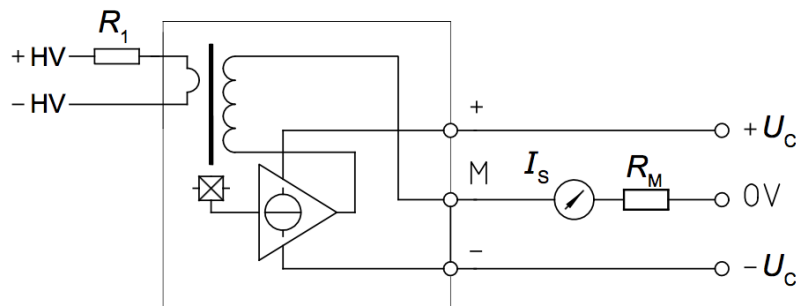

Figure A.3: Datasheet diagram of the LEM LV 25-P voltage transducer.

Similarly for the current transducer, nominal primary input current is 50 A where the conversion ratio from primary to secondary current is $K_{ni} = 1/1000$, i.e. 50 mA for

nominal current which is in rms. Since the converter used will deliver 7.35 kW, its nominal current is 15 A peak. To get a better utilization of the current transducer, the primary current is wound twice through the transducer primary coil, making the primary nominal current seem to be 30 A peak. As before, a secondary resistor with a value of $R_{Mi} = 220\,\Omega$ is used which gives a nominal ADC voltage reading of 6 V. Then the resolution for the measured currents become

$$i_{res} = \frac{2 \cdot 15A}{\frac{6V}{10V}(2^{16} - 1)} = 0.76\,mA. \tag{A.0.2}$$

The rated power of the employed grid-side converter is 15 kW, which means that there is headroom to operate above the considered power level for this project. From the ADC reading to the number achieved in the control system in dSPACE, the measured voltage is ten times lower than the expected due to an inherent voltage division in the dSPACE controller. Thus, the measured signals from the ADC must all be multiplies with 10 before any additional gain scheduling is performed. Effectively, the gain from ADC reading accessible in the software back to the original voltages and current are

$$K_{v,ADC} = \frac{10R_1}{K_{nv}R_{Mv}} = 727.27 \tag{A.0.3}$$

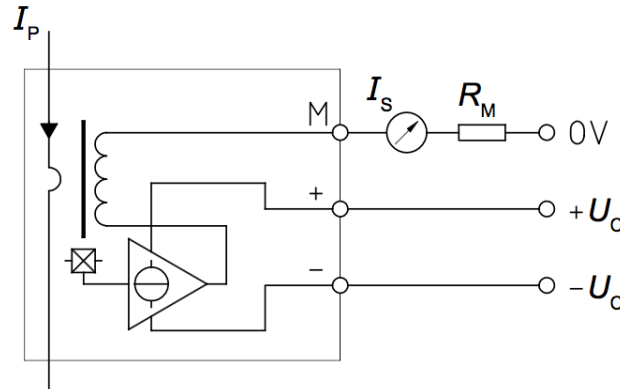$$K_{i,ADC} = \frac{10}{2 \cdot K_{ni} \cdot R_{Mi}} = 22.73 \tag{A.0.4}$$

Figure A.4: Datasheet diagram of the LEM LA 55-P current transducer.

B Sequence Components

Sequence components have for more than half a century been used to simplify the analysis of asymmetrical conditions including asymmetrical faults in power system. The principle is that for a three-phase system, an asymmetrical set of phasors can be represented as a linear combination of three sets of symmetrical phasors: positive sequence, negative sequence and zero sequence given that the network is balanced [40]. Thus, sequence components can be used to simplify the analysis of external unbalances such as voltages, currents, sources, or loads given that the system is internally balanced, i.e. a balanced impedance network. In this way, a coupled dependent asymmetrical set of phasors can be simplified since each phase sequence is linearly independent from each other and can thus be analyzed individually [126]. This means that a coupled complicated unbalanced system can be represented as three independent balanced networks. When each of these networks has been analyzed or solved in the sequence domain, these can be added up to find the phasor domain solution as well.

Besides the advantages of simplified analysis of unbalanced grid conditions, the easy calculation of the negative and zero sequence components can be used to detect fault events and control relays and circuit breakers effectively.

A three-phase balanced or symmetrical system is defined as three vectors with equal magnitude with an angular displacement of $120°$ and with a positive rotating direction, e.g. abc. By using a complex linear transformation using the phase rotation operator

$$\alpha = e^{j2\pi/3} \tag{B.0.1}$$

an unbalanced set of e.g. three-phase voltages can be represented as the sum of the positive sequence, negative sequence and zero sequence of that component as

$$v_a = v_a^+ + v_a^- + v_a^0 \tag{B.0.2}$$

$$v_b = v_b^+ + v_b^- + v_b^0 \tag{B.0.3}$$

$$v_c = v_c^+ + v_c^- + v_c^0 \tag{B.0.4}$$

where $+$ denotes the positive sequence, $-$ denotes the negative sequence, and 0 denotes the zero sequence. Expressing v_b and v_c in terms of the rotational operator and the phase-a voltage, one gets that

$$v_a^0 = v_0, \quad v_a^+ = v^+, \quad v_a^- = v^-, \tag{B.0.5}$$

$$v_b^0 = v_0, \quad v_b^+ = \alpha^2 v^+, \quad v_b^- = \alpha v^-, \tag{B.0.6}$$

$$v_c^0 = v_0, \quad v_c^+ = \alpha v^+, \quad v_c^- = \alpha^2 v^-, \tag{B.0.7}$$

which gives that the three phase quantities can be written as

$$v_a = v^0 + v^+ + v^- \tag{B.0.8}$$

$$v_b = v^0 + \alpha^2 v^+ + \alpha v^- \tag{B.0.9}$$

$$v_c = v^0 + \alpha v^+ + \alpha^2 v^-. \tag{B.0.10}$$

Putting this on matrix form and calculating the inverse reveals the expression for the three sequence components in terms of the abc-voltages as

$$\begin{bmatrix} v^+ \\ v^- \\ v^0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{B.0.11}$$

which is referenced to phase a. Here, all quantities are phasor quantities, i.e. complex numbers. As it can be seen, the zero sequence represents the average value of the three signals, i.e. the common-mode signal. The positive sequence is defined as the balanced part of the three voltages rotating in the positive defined direction and the negative sequence is defined as the balanced part of the three-phase voltages rotating on the negative defined rotating direction. It can be noticed that for a balanced three-phase signal, the zero sequence is zero and the complex operator will cancel out in the negative sequence also making that zero. Hence, the remaining part is the positive sequence. As wind turbines are connected to a step-up Δ-connected transformer, no return path is provided for the zero-sequence current and thus the phase current cannot contain any zero sequence component.

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