Demonstration of a 10 kV SiC MOSFET based Medium Voltage Power Stack

Dalal, Dipen Narendra; Zhao, Hongbo; Jørgensen, Jannick Kjær; Christensen, Nicklas; Jørgensen, Asger Bjørn; Beczkowski, Szymon Michal; Uhrenfeldt, Christian; Munk-Nielsen, Stig

Published in:
2020 IEEE Applied Power Electronics Conference and Exposition (APEC)

DOI (link to publication from Publisher):
10.1109/APEC39645.2020.9124441

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Demonstration of a 10 kV SiC MOSFET based Medium Voltage Power Stack

Dipen Narendra Dalal, Hongbo Zhao, Jannick Kjær Jørgensen,
Nicklas Christensen, Asger Bjørn Jørgensen, Szymon Bęczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen
Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark.
Email: dnd@et.aau.dk

***Abstract*—This paper presents a 10 kV SiC MOSFET based power stack, featuring medium voltage power conversion with a simple two-level voltage source converter topology. The design of the medium voltage (MV) power stack is realized in a commercial IGBT based three phase power stack frame. The power stack assembly comprises of the custom packaged single-chip half bridge 10 kV SiC MOSFET power modules, gate driver units with a very low isolation capacitance, DC-link capacitors, busbar and a liquid cooled heatsink. The designed power stacks are tested in a DC-fed three phase back-to-back setup with the total circulated power of 42 kVA, DC-link voltage of 6 kV, rms load current of 7 A and 5 kHz switching frequency. Under this operating conditions, an efficiency > 99% is deduced for the designed MV power stack.**

***Index Terms*—10 kV SiC MOSFETs, medium voltage (MV), two-level voltage source converter (2L-VSC), power stack**

I. Introduction

Silicon Carbide (SiC) semiconductor devices in 10 kV –15 kV voltage class offers unprecedented blocking voltage capability and superior switching characteristics compared to their Silicon (Si) counterparts [1]. These properties of the SiC power devices have resulted in an increased interest for their adoption in the medium voltage (MV) power electronics applications, since they enable simplification of the power converter topology, increased efficiency and operation at higher switching frequencies [2], [3]. In addition to this, the inherent benefits resulting from a superior material characteristics of SiC over Si opens up new possibilities for power densities and efficiency improvements in medium voltage high power conversion applications [4]. The lower switching losses due to the faster switching speeds of the MV SiC MOSFET enables the converter switching frequencies in the range of few tens of kHz to MHz for the DC-link voltages of 3 kV up to 10 kV in various hard switched or soft switched applications such as solid state transformers [5], [3], grid support [2], induction heating [6].

This paper demonstrates a 50 kVA MV power stack design based on the custom packaged single-chip half bridge 10 kV SiC MOSFET power modules, with a two-level voltage source converter (VSC) topology. The power stack is designed with the same frame of a commercial 500 kVA, 1.7 kV IGBT based 690 V three phase power stack. The rated power of up to 500 kVA is aimed to achieve in the same power stack footprint utilizing multi-chip 10 kV SiC MOSFET power modules as opposed to what is deployed here for the 50 kVA demonstration. The key specifications of the 50 kVA and proposed 500 kVA scalable MV power stack are presented in Table I.

TABLE I
Specifications of the medium voltage power stack.

Parameter	Value
Rated Power	50 kVA–500 kVA
DC-link voltage	6 kV–7.2 kV
Line-line AC voltage (rms)	4.16 kV
AC current (rms)	7 A–70 A
Switching frequency	5 kHz–10 kHz

The key components and sub-assembly of the power stack including the half bridge power module with reduced parasitic capacitance, low isolation capacitance gate driver, DC-link and busbar layout as well as thermal designs are presented in Section II. In Section III, the static characterisation related to the on-state resistance of the 10 kV SiC MOSFET and switching energy dissipation for the custom packaged half bridge SiC MOSFET power modules are presented to provide an insight into the semiconductor conduction and switching performance. The designed power stack are tested in a DC-fed three phase back-to-back test setup. The experimental results for the converter operation with the DC-link voltage of 6 kV, rms load current of 7 A at 5 kHz switching frequency are presented with a brief discussion on the designed power stack efficiency.

II. Medium voltage power stack

This section presents the key components and sub-assembly of the MV power stack.

A. Half bridge 10 kV SiC MOSFET power module

The power stack design is based on the custom packaged single-chip half bridge 10 kV SiC MOSFET power module [7], as shown in Fig. 1. This half bridge power module is populated with the 3rd generation 350 mΩ, 10 kV SiC MOSFET (CPM3-10000-0350) and JBS diode dies from Wolfspeed [4], which are soldered on a 0.63 mm Aluminium Nitiride (AlN) Direct Bonded Copper (DBC) with a 5 mm AlSiC baseplate. The power module is housed in a 3D printed plastic housing encapsulated in a Silicon gel. A plastic holder is placed inside the module which provides an access to the surface of the die.

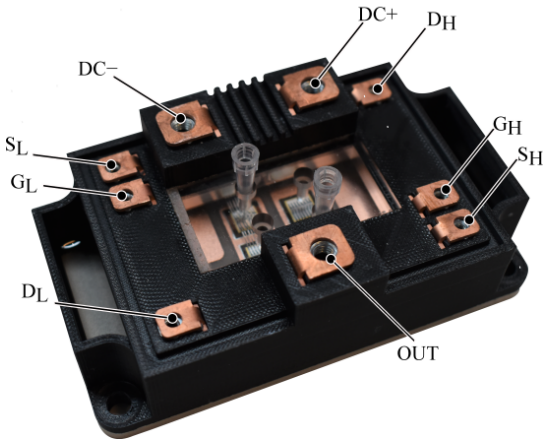

Fig. 1. Picture of the single-chip half bridge 10 kV SiC MOSFET power module.

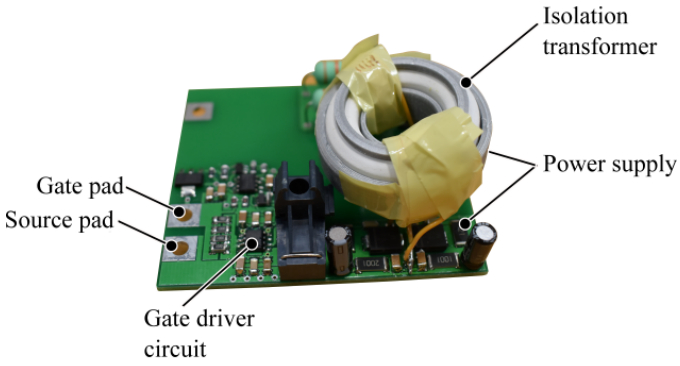

Fig. 2. Picture of an isolated DC-DC power supply and gate driver PCB.

With this arrangement the local surface temperature of the die can be monitored using a fiber optic temperature sensors.

With the SiC MOSFETs the dv/dt during the switching transitions can reach the magnitudes of extremely high values [2], therefore in case of the MV converter enabled by the SiC MOSFETs it is increasingly important to minimize the parasitic capacitances to limit the capacitive currents during the switching transitions. The power module is designed with a reduced capacitive couplings between the top copper layer of the DBC connected to the half bridge output as well as high side gate plane and baseplate [7]. This is required to limit the capacitive currents during the switching transitions, which results in an increased switching energy dissipation and conducted Electromagnetic Interference (EMI) [8], [9]. In contrast to the low voltage SiC or Gallium Nitrie (GaN) semiconductor devices, where the switching performance is sensitive to parasitic inductances in terms of over voltage and ringing, for MV power modules the lower parasitic capacitance design is necessary.

B. Isolated power supply and gate driver

To drive the high side SiC MOSFET in the half bridge SiC MOSFET power module, a gate driver power supply with an appropriate galvanic isolation is required. Furthermore, the high dv/dt switching transitions of the SiC MOSFET leads to the common mode current through the isolation capacitance of the high side gate driver power supply. From this point of view, an isolated DC-DC power supply with a low isolation capacitance and high dv/dt ruggedness is necessary for the reliable operation of the gate driver circuit [10]. A custom made DC-DC power supply with a very low isolation capacitance and isolation voltage rating of up to 10 kV was designed [11]. The picture of the PCB which includes both the the DC-DC isolated power supply and the gate driver circuit for the 10 kV half bridge SiC MOSFET power module is shown in Fig. 2.

A Flyback topology with a primary side sensing is chosen to avoid the additional coupling capacitance resulting from the feedback signals over the isolation barriers. For, the isolation transformer a high permeability 3F3 Ferrite core is used. For the windings, the triple insulated wire with insulation voltage of 15 kV is utilised to achieve the desired isolation level. The maximum isolation capacitance for the gate driver is measured to be 2.6 pF [12]. The power supply outputs +20 V and -5 V, which is the recommended turn-on and turn-off gate driver voltage respectively for the 10 kV SiC MOSFET.

The output stage of the gate driver is designed with a driver IC IXDN614 with peak sink/source current capability of 14 A. In order to prevent the Miller induced false turn-on, an Active Miller clamp functionality is incorporated in the gate driver stage. In order to provide the isolation and achieve increased dV/dt at the control interface, the gate signals to the driver from the DSP control card are transferred via an optic fiber link.

C. DC-link and busbar design

The DC-link capacitance for the power stack is designed considering the maximum converter power rating of 500 kVA. For a PWM (Pulse Width Modulated) converter, the worst case current stress on the DC-link capacitor appears for the converter operation with modulation range of approximately 0.6 and unity load power factor [13]. With the output line-line converter rms voltage of 4.16 kV and rated power of 500 kVA, the worst case DC-link current stress is calculated analytically ($i_{\mathrm{C_{DC},rms}}$ = 45 A) based on [13]. The minimum DC-link capacitance requirement established based on the maximum ripple voltage of 10% [14], is plotted in Fig. 3 for the converter switching frequency of 5 kHz and 10 kHz.

Taking into account the maximum ripple voltage criteria of 10 %, calculated worst case current stress and the available product range of the DC-link capacitors for MV applications, a 3.6 kV, 40 µF film capacitor (Electronicon E50.N14-403NTO [15]) is chosen for the designed DC-link, ensuring that it fulfills the maximum DC-link voltage ripple criteria of 10 % and the maximum rms current rating of the capacitor is well within the analytically obtained worst case DC-link current stress. Total DC-link capacitance of 100 µF with rated voltage

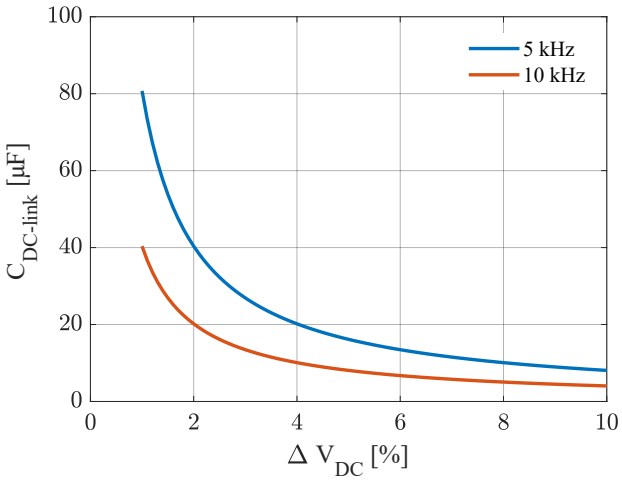

Fig. 3. DC-link capacitance requirement as a function of voltage ripple for switching frequency of 5 kHz and 10 kHz. (Obtained for the worst case capacitor ripple current)

of 7.2 kV is obtained using series/parallel combination of total ten 40 µF, 3.6 kV capacitors as shown in Fig. 4. The electrical connection from the DC-link capacitance to the SiC MOSFET power module is provided using, a three layer stacked busbar, which is cutout from the 1.2 mm steel sheet as shown in Fig. 4. (The choice of the steel for the busbar is to do with the required mechanical strength for the given bending radius at the power module connection terminals for the busbar.) Considering the low scale of economy in case of a laminated busbar for the designed prototype together with its intended operation in the laboratory environment, a simple approach is used to provide adequate isolation between each layer of the stacked busbar. Where, each layer of the sacked busbar is isolated with four layers of 50 µm Kapton tape providing isolation voltage withstand capability of approx. 48 kV [16]. The 3D CAD model of the designed busbar and the picture of the assembly is presented in Fig. 4. With

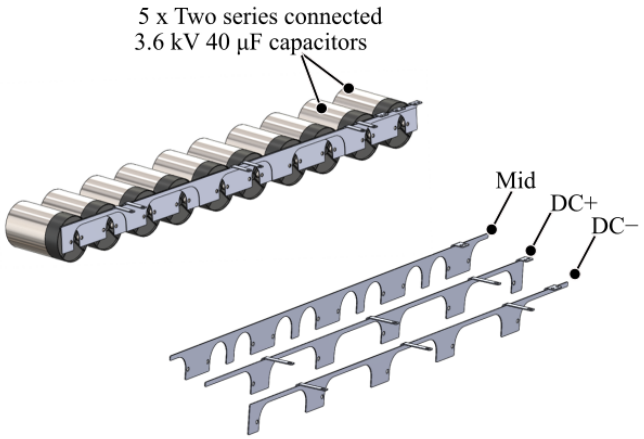

Fig. 4. 3D-CAD model of the DC-link capacitors and busbar assembly.

the rated blocking voltage capability of 10 kV for the SiC MOSFET and relatively low d*i*/d*t*, an extremely low inductive busbar design is of little to no importance since the inductance has minor influence on the switching performance in terms of the over voltages and ringing.

D. Thermal management

The significantly higher heat transfer coefficients for the liquid cooling in comparison to the air cooling provides a superior thermal performance, which enables a high power density and compact solution for a power electronics converter. Considering this fact, a direct liquid cooling solution (ShowerPower concept from Danfoss [17]) is opted for the designed power stack as shown in Fig. 5. In contrast to the indirect

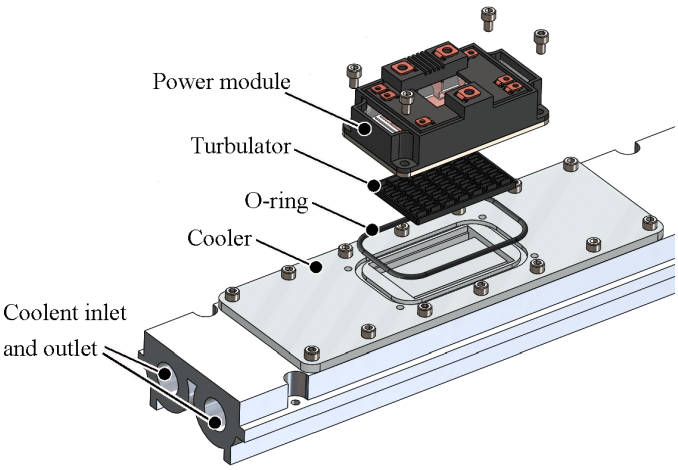

Fig. 5. 3D CAD model of the half bridge 10 kV SiC MOSFET power module and cooler assembly.

liquid cooling, the direct liquid cooling eliminates the thermal interface material (TIM) between the power module baseplate and cooler since in the case of direct liquid cooling the coolant is in direct contact with the baseplate. The TIM accounts for approximately 30%–50% of the total thermal resistance, so elimination of the TIM in the direct liquid cooling significantly improves the thermal performance [17].

The liquid cooling assembly shown in Fig.5 features a plastic turbulator, O-ring for sealing purpose and a custom-made adapter which is mounted on the cooler. The coolant reaches the turbulator through the grooves on the sides via the openings provided on the cooler. The turbulator which consists of multiple cells in X and Y directions, guides the coolant along the power module baseplate. The coolant flow rate and pressure for the shown liquid cooling systems are in the range of 20 litres/minute and 3 bars respectively.

E. Power stack assembly

The picture of the designed liquid cooled MV three phase power stack is shown in the Fig. 6. The power stack assembly consist of one single chip half bridge 10 kV SiC MOSFET power modules per phase, DC-link capacitors with busbars, gate drivers and a cooler.

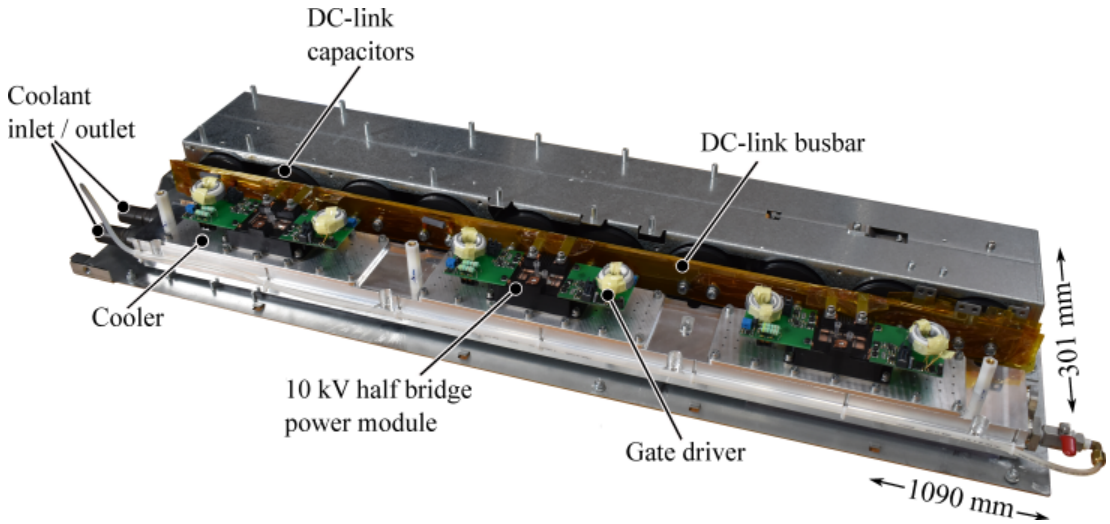

Fig. 6. Picture of the 10 kV SiC MOSFET based liquid cooled medium voltage power stack.

III. Experimental results

In this section, the static and dynamic characterisation results are presented to provide an insight into the MOSFET on-state resistance and switching energy dissipation for the 10 kV SiC MOSFET die and half bridge power modules respectively. In addition to this the key experimental results for the converter operation in a three phase back-to-back setup are presented with a brief discussion.

A. On-sate and switching characteristics of the half bridge 10 kV SiC MOSFET power module

Fig. 7a, shows the MOSFET on-state resistance $R_{\mathrm{DS(on)}}$ as a function of temperature for the two dies. These two dies represent the the upper and lower extreme of the on-state resistance from the sample of total 78 dies based on the spread in their VI characteristics at 25°C. The on-state resistance as function of temperature for these two dies is presented in Fig.7a, which is obtained by evaluating the slope of the MOSFET VI characteristics in ohmic region corresponding to the gate-source voltage of 20 V. The on-state resistance ranges within 340 mΩ - 380 mΩ at 25°C, which increases by approximately 120% to 795 mΩ - 840 mΩ at 125°C.

In the case when, the SiC MOSFET is operated in a third quadrant with a gate bias of 10 V–20 V, the intrinsic body diode conduction is predominantly through the MOSFET channel [18], since the channel resistance acts as a shunt in parallel with the body diode suppressing bipolar current injection through the diode [19], [20]. Therefore, the VI characteristics in the third quadrant follows the same slope as in the first quadrant for the gate bias of 10 V–20 V. In case, when the 10 kV anti-parallel JBS diode is used the current is predominantly shared between the MOSFET channel and the anti-parallel JBS diode. The forward VI characteristics of the 10 kV JBS diode is shown in Fig. 7b, where it can be seen that the forward voltage of the diode is in the range of 1 V–1.2 V for the temperature range of 25 °C–125 °C. In this temperature range, the slope of the JBS diode forward VI characteristics is found to be close to that of the on-state resistance of the 10 kV SiC MOSFET. During the third quadrant operation of the SiC MOSFET with a gate bias of 20 V and an anti-parallel 10 kV SiC JBS diode, the diode will start to share the current as soon the drain-source voltage of the MOSFET is above (-1 V)–(-1.2 V). Even in this case, the MOSFET channel shares the largest portion of the current.

The turn-on and turn-off switching energy dissipation (E_{on} and E_{off}) for the 10 kV half bridge SiC MOSFET power modules are obtained from its dynamic characterisation in a double pulse test setup with a baseplate temperature of 25°C. The E_{on} and E_{off} for the external gate resistance of 20 Ω is plotted in Fig. 7c and 7d respectively as a a function of load current and DC-link voltages of 1 kV–6 kV. For a given load current, the turn-on switching energy dissipation increases, whereas the turn-off switching energy dissipation remains almost constant or changes slightly with increase in the load current magnitude. The turn-on and turn-off switching energy dissipation for the load current of 14 A and DC-link voltage of 6 kV is measured to be 35.7 mJ and 1.6 mJ respectively. The turn-on dv/dt increases whereas the turn-off dv/dt decreases with increasing value of the load current magnitude [18]. The maximum turn-on and turn-off dv/dt is identified to be 28.1 kV/µs and 39.3 kV/µs for the load current magnitude of 0 A and 14 A respectively.

For the same DC-link voltage and the load current magnitude, the the turn-on switching speed of the SiC MOSFET increases resulting in a slightly lower turn-on switching energy dissipation at alleviated temperatures [18]. The increase in switching speed is due to the combined effect of the temperature dependent shift in the gate threshold and trans-conductance parameter, which lowers gate-source Miller plateau voltage with increasing temperature. Whereas, the temperature has almost no or negligible effect on the turn-off switching energy dissipation [18]. Considering that the

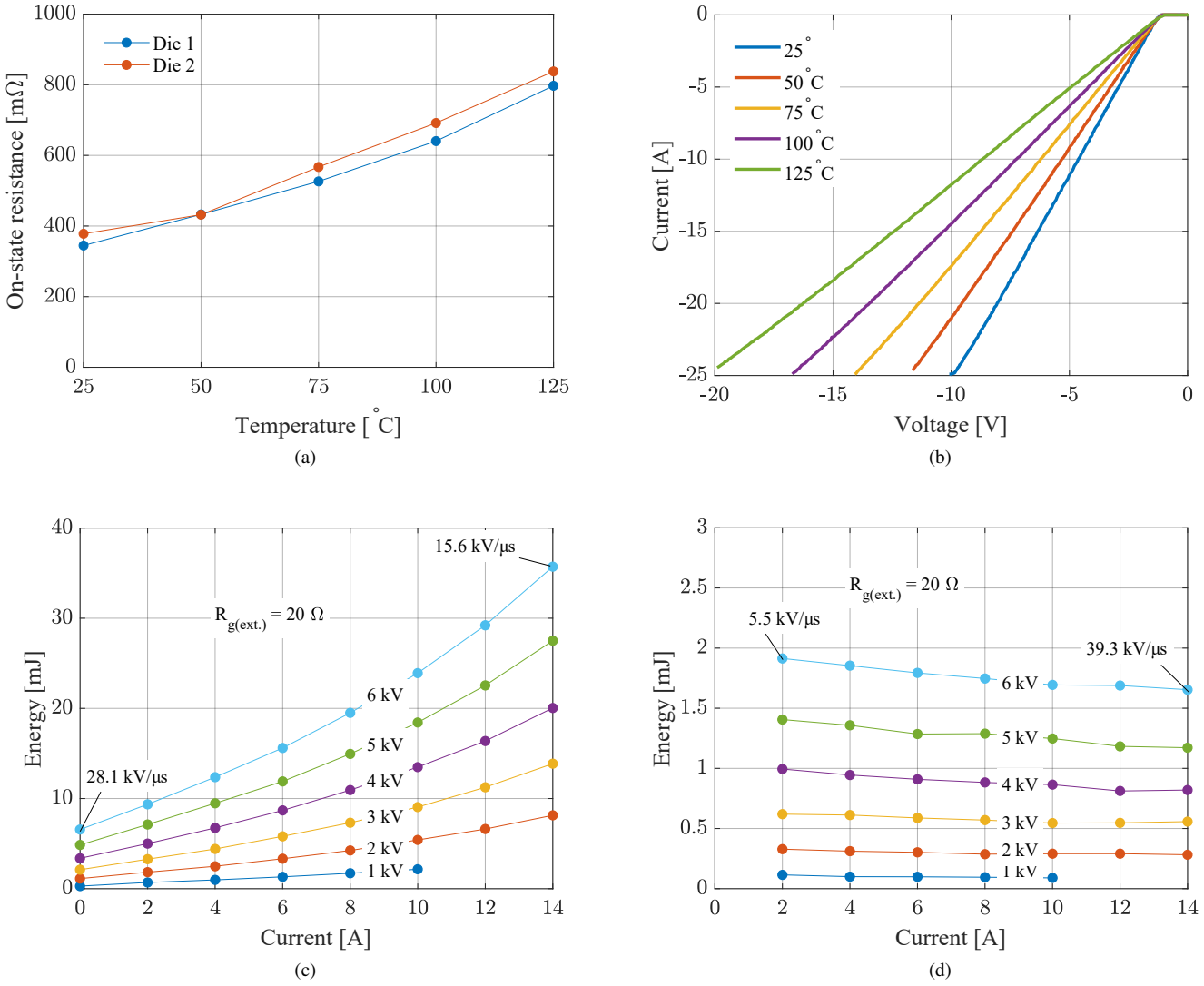

Fig. 7. (a) On-state resistance vs temperature of the 10 kV SiC MOSFET, (b) forward IV characteristics of 10 kV JBS diode, (c) turn-on and (d) turn-off switching energy dissipation for the 10 kV half bridge SiC MOSFET power module.

coolant temperature of the power stack is maintained at 23°C for the nominal operating conditions, the turn-on and turn-off switching energy dissipation shown in Fig. 7 measured at 25°C with gate resistance of R_{g} = 20 Ω can be regarded as the worst case scenario for the switching energy dissipation.

B. Experimental setup and test results

The designed power stack is tested in the DC fed three phase back-to-back setup with an inductive load of 60 mH per phase. The schematic and the picture of the laboratory test setup is shown in Fig. 8a and 8b respectively. In this test setup, the power cycles between the two converters where one of the converter can be regarded as a source and another as a load. The DC source supplies the losses contributed by semiconductors and magnetics. With such arrangement, the power modules can be exposed to the current and voltage stresses as experienced in a realistic three phase converter operation.

In the experimental test, the two back-to-back converters are controlled in the open loop, where the voltage magnitude or phase difference of the fundamental output voltage at the each phase of the two converters are adjusted appropriately to obtain the desired load current magnitude. The test results presented here on-wards are related to the converter operation at the DC-link voltage of 6 kV and switching frequency of 5 kHz. The modulation index (M) and the phase shift are set to 0.8 and 10 deg. respectively, which results in the rms load current $i_{\mathrm{ph,rms}}$ of approximately 7 A. Fig. 8c, shows the DC-link voltage and the zoomed view of the output voltages at phase-a for the two converters with respect to the mid-point of a DC-link. The phase output voltages v_{ao} and $v_{\mathrm{a'o}}$, show clean switching transitions without any significant overshoot

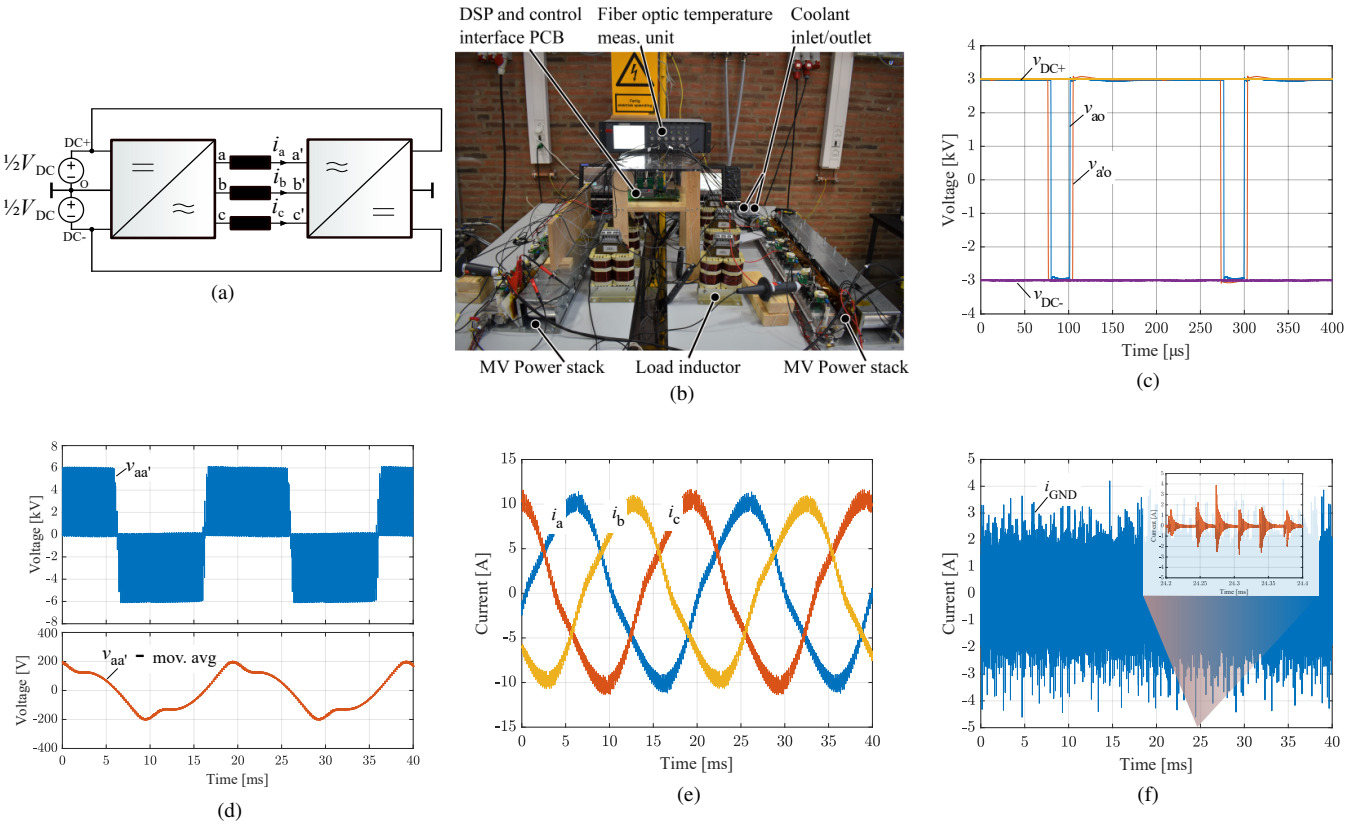

Fig. 8. (a) Schematic and (b) image of the thee phase back-to-back test setup, (c) measured phase-a half bridge output voltages, (d) Phase-a load inductor voltage and its moving average, (e) measured three phase load currents and (f) heatsink ground current.

or ringing. The voltage across the load inductor $v_{aa'}$ for the phase-a is obtained from the measured phase output voltages ($v_{aa'} = v_{ao} - v_{a'o}$) and its moving average is plotted in Fig. 8d. The measured three phase load currents are plotted in Fig 8e. Since, the converter is operated in an open loop without dead-time error compensation, the voltage error (due to the inverter non-linearities - i.e: deadtime, device parasitics..) resulting during the deadtime which is current polarity dependent, causes the distortion around the zero crossing of the load currents. To obtain the desired rms load current of 7 A with fundamental frequency of 50 Hz, the required average voltage across the 160 mH inductor is significantly low compared to the DC-link voltage of 6 kV. Due to this the voltage error during the deadtime is comparable to the average voltage across the inductor, resulting in a more pronounced distortion effect around the zero crossing of the three phase load currents.

The capacitive currents due to the charging and discharging of the power module parasitic capacitances conducts through the heatsink which needs to be grounded due to the safety requirements. The measured currents at the grounding connection point of the heatsink is presented in Fig. 8f, which shows the peak amplitude of 4 A with high frequency oscillations in the range of 1.1 MHz. Depending on the application and the heatsink grounding requirements, there is also a possibility of redirecting the heatsink ground current to the DC-link by providing a low impedance connection. In order to suppress the heatsink ground current the impedance can be inserted between the heatsink and ground, however this would result in the voltage potential on the heatsink during the converter operation. The magnitude and the voltage potential on the heatsink is determined by the nature of the inserted impedance network [21].

For the converter operation in the back-to-back test setup, the surface temperature of die is measured using a fiber optic temperature sensor (OTG F-10 from OpSense [22]) in order to monitor the expected junction temperature during the nominal operating conditions. With the coolant temperature of 20.5°C, the mean temperature of the MOSFET die under the converter steady state operating condition is measured to be 45° C. At this operating point, the total power losses for the back-to-back test setup is deduced to be 384 W from the DC power supply readout. Based on the on-state resistance measurement of the 10 kV SiC MOSFET die and switching energy dissipation for the half bridge power module presented in Section II as well as the DC-resistance of the inductor obtained from the impedance analyser measurement, it can be inferred that the major part of the total power losses is accounted due to the semiconductor switching and conduction and a small part of it is due to the copper losses in the inductor. It should be noted that in the presented test configuration the core losses

are almost negligible for the inductor due to significantly lower load current ripple. Considering that the power losses are distributed equally in the two power stacks under test, the power loss for the individual power stack (i.e conduction and switching losses in the three half bridge power modules) including the load inductor is deduced to be less than 1% of the total circulated power of 42 kVA, resulting in an efficiency > 99% for the designed power stack.

IV. Conclusion

This paper demonstrates the medium voltage liquid cooled power stack enabled by custom packaged single-chip half bridge 10 kV SiC MOSFET power modules. The power stack sub-assembly including the half bridge power modules, gate driver, DC-link busbar and heatsink is discussed briefly including the key design considerations imposed by the medium voltages and extremely fast switching speeds of SiC MOSFETs. The designed power stacks are tested in a DC fed three phase back-to-back setup with an inductive load at DC-link voltage of 6 kV and switching frequency of 5 kHz. Under this operating conditions with a total circulated power of 42 kVA, an efficiency > 99% is deduced for the designed MV power stack.

Acknowledgment

The work is carried out as a part of the MV-BASIC research project funded by Department of Energy Technology, Aalborg University together with industrial project partners KK Wind Solutions and Siemens Gamesa.

References

[1] E. Van Brunt, D. Grider, V. Pala, S. Ryu, J. Casady, and J. Palmour, "Development of medium voltage SiC power technology for next generation power electronics," in *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, May 2015, pp. 72–74.

[2] J. Thoma, B. Volzer, D. Kranzer, D. Derix, and A. Hensel, "Design and Commissioning of a 10 kV Three-Phase Transformerless Inverter with 15 kV Silicon Carbide MOSFETs," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Sep. 2018, pp. P.1–P.7.

[3] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, June 2019.

[4] J. B. Casady, V. Pala, D. J. Lichtenwalner, E. V. Brunt, B. Hull, G. Wang, J. Richmond, S. T. Allen, D. Grider, and J. W. Palmour, "New Generation 10kV SiC Power MOSFET and Diodes for Industrial Applications," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2015, pp. 1–8.

[5] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343–3360, July 2015.

[6] A. Jørgensen, T. Aunsborg, S. Beczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "High-frequency resonant operation of an integrated medium-voltage SiC MOSFET power module," *IET Power Electronics*, 6 2019.

[7] A. B. Jørgensen, N. Christensen, D. N. Dalal, S. D. Sønderskov, S. Bęczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sep. 2017, pp. P.1–P.8.

[8] D. N. Dalal, N. Christensen, A. B. Jørgensen, J. K. Jørgensen, S. Bęczkowski, S. Munk-Nielsen, and C. Uhrenfeldt, "Impact of Power Module Parasitic Capacitances on Medium Voltage SiC MOSFETs Switching Transients," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.

[9] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, and M. S. Mazzola, "Methodology for Characterization of Common-Mode Conducted Electromagnetic Emissions in Wide-Bandgap Converters for Ungrounded Shipboard Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 300–314, March 2018.

[10] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil, and S. Bhattacharya, "Design Considerations and Development of an Innovative Gate Driver for Medium-Voltage Power Devices With High dv/dt," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5256–5267, June 2019.

[11] D. N. Dalal, N. Christensen, A. B. Jørgensen, S. D. Sønderskov, S. Bęczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sep. 2017, pp. P.1–P.10.

[12] H. Zhao, D. Dalal, X. Wang, J. Jørgensen, C. Uhrenfeldt, S. Beczkowski, and S. Munk-Nielsen, ""Modeling and Design of a 1.2 pF Common-Mode Capacitance Transformer for Powering MV SiC MOSFETs Gate Drivers"," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*. IEEE Press, 2019.

[13] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535–543, July 2006.

[14] X. Lu and F. Z. Peng, "Minimizing DC capacitor current ripple and DC capacitance requirement of the HEV converter/inverter systems," in *2009 IEEE Energy Conversion Congress and Exposition*, Sep. 2009, pp. 1191–1198.

[15] Electronicon. PK 16, GA 85, E61 High Density DC Film Capacitors. [Online]. Available: https://www.electronicon.com/fileadmin/inhalte/pdfs/downloadbereich/Katalog/neue_Kataloge_2011/200.003-020030_PK16.pdf

[16] Dupont. Kapton Summary of properties. [Online]. Available: https://www.dupont.com/content/dam/dupont/products-and-services/membranes-and-films/polyimde-films/documents/DEC-Kapton-summary-of-properties.pdf

[17] A. Note:. Shower power cooling concept. [Online]. Available: http://files.danfoss.com/download/Drives/DKSPPM301A302_SP\%20Application\%20note_2016.pdf

[18] D. Johannesson, M. Nawaz, and K. Ilves, "Assessment of 10 kV, 100 A Silicon CarbidemosfetPower Modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5215–5225, June 2018.

[19] V. Pala, E. Van Brunt, S. H. Ryu, B. Hull, S. Allen, J. Palmour, and A. Hefner, "Physics of bipolar, unipolar and intermediate conduction modes in Silicon Carbide MOSFET body diodes," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, June 2016, pp. 227–230.

[20] K. Han and B. J. Baliga, "Comprehensive Physics of Third Quadrant Characteristics for Accumulation- and Inversion-Channel 1.2-kV 4H-SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3916–3921, Sep. 2019.

[21] N. Christensen and A. B. Jørgensen and D. Dalal and S. D. Sonderskov and S. Bęczkowski and C. Uhrenfeldt and S. Munk-Nielsen, "Common mode current mitigation for medium voltage half bridge sic modules," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sep. 2017, pp. P.1–P.8.

[22] OpSense. Fiber optic temperature sensors. [Online]. Available: https://opsens-solutions.com/products/fiber-optic-temperature-sensors/