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Published in:
IEEE Access

DOI (link to publication from Publisher):
10.1109/ACCESS.2020.3029153

Publication date:
2020

Document Version
Publisher's PDF, also known as Version of record

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

SPECIAL SECTION ON EVOLVING TECHNOLOGIES IN ENERGY STORAGE SYSTEMS FOR ENERGY SYSTEMS APPLICATIONS

Received September 8, 2020, accepted October 1, 2020, date of publication October 6, 2020, date of current version October 19, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3029153

Design and Implementation of Multilevel Inverters for Fuel Cell Energy Conversion System

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This work was supported by the Danida Mobility Grant, responsible for the Ministry of Foreign Affairs of Denmark (MFA), Act 7 on Denmark's International Development Cooperation under Project 19-MG06AAU.

ABSTRACT Power converter plays a significant role in Proton Exchange Membrane Fuel Cell (PEMFC) energy generation systems, which is an alternative of distributed energy generation systems. So there creates a demand for high-quality power conditioning used in PEMFC systems. This article proposes a converter topology as a power interface and also introduced a multilevel inverter topology for various levels of operation. The converter steps up the input voltage to the rated voltage and transforms to the DC bus, the multilevel inverter converts the voltage to AC and feeds to AC loads. In this article, we develop an entire unit stack, which can produce an output with positive and zero sequences. The addition of H-bridge to the fundamental unit known to be an advance cascaded H-bridge multilevel inverter resulting in the formation of all sequences like positive, zero and negative levels. The conventional multilevel inverters are compared with the proposed inverters in terms of switch count, DC sources, diodes, through which the lesser requirement of components in a multilevel inverter is possible to observe, which results in the reduction in cost, dv/dt stress, component space of the driver circuit. With this implementation, the better possibility of control, increase the quality of output, reliability of the inverter with a reduced THD, and stress. The converter output is tested and verified in MATLAB, and the respective results of the different levels like five, seven and fifteen of a single-phase cascaded inverter are tested experimentally and in MATLAB Simulink.

INDEX TERMS Multilevel inverter (MLI), proton exchange membrane fuel cell (PEMFC), converter, total harmonics distortion (THD).

I. INTRODUCTION

The basic configuration of inverters is of two-level, where the many drawbacks exist like input voltage is twice than that of the output voltage resulting in the severe harmonic distortions, high switching losses & frequency. It restricts these to only low-power applications as the power handling capacity is less [1]. Hence, the evolution of multilevel inverters (MLI) came into existence to wipe out the described disadvantages and to provide better reliability and higher in quality of output waveform. The multilevel inverter is an ideal choice to choose for high and medium power applications with its harmonic reduction difference with a conventional inverter with the same power in output and avoiding in increasing the switching frequency [2]–[4]. Multilevel inverters usually come in three forms [5], namely neutral clamping point (NPC), clamping diode (DCM) [6], flying capacitor (FLC) and cascaded H- (CHB) [7], [8]. The promising energy sources nowadays are the Renewable sources of energy such as solar panels and the fuel cell for the distributed

The associate editor coordinating the review of this manuscript and approving it for publication was Eklas Hossain.

generation systems [9]–[12]. From solar panel and fuel cell stacks, it uses the energy generation for energy transformation to feed the AC loads using power electronic devices with DC-AC, DC-DC conversion. It maintains the constant DC voltage at the DC bus by the step-up operation of the converter, and the inverter converts DC to AC and transforms the DC bus voltage to the AC loads. The way of electricity generation is from a fuel cell, which is an electrochemical device. The mixture of air and fuel are the standard inputs for the fuel cell, converts to water and the electric nature to the chemical reaction [13], [14]. Hydrogen plays a significant role in the fuel cell, which can operate parallel with internal combustion engines of the vehicles based on its availability. When the vehicles are on load, the battery characteristics are like a fuel cell. Sir William Robert Grove developed his first fuel cell in 1839.

Further, Sir Francis Bacon developed a usable fuel cell in 1950 with a capacity of 5 kW. Since then, these are popular and used for residential, industrial, and commercial purposes as primary power sources. In the current scenario, the attention towards fuel cells automobile industries for the development of eco-friendly vehicles. There are various types of multilevel inverters such as diode clamped (DC) [6], flying capacitor (FC), cascaded H-bridge (CHB), and a neutral point clamped (NPC). In both the flying capacitor multilevel inverters and neutral point clamped MLI, the balancing of capacitor voltage is the main problem because of which these are limited to only five-level not able to cascade, and output voltage reduces to half of the input voltage provides very high switching losses with high switching frequency. The diode clamping and capacitor voltage balancing are unnecessary for the cascaded multilevel inverters (conventional). Even in the CHB inverters, there is a clean possibility to get the higher output levels as these are series-connected: exempting the usage of DC sources is more. The proposed topology requires a smaller number of switches with which we can reduce the requirement of driver circuits compared with the conventional cascaded multilevel inverter [15]. There is a possibility of a reduction in the dv/dt stress on each switch with the usage of more DC sources, and it becomes reliable, straightforward with less circuit space, and the cost gets reduced [16]. There are many fundamental units and it imports various cascaded multilevel inverters [17], [19], [20], [36].

In this article, a fuel cell-based multilevel inverter is proposed. The basic units are in series to have a higher output level and reduced switch count. The addition of H-bridge achieves both positive and negative levels where the FC and DC are absent. The output constraints of the proposed multilevel inverter with five, seven, and fifteen levels are simulated in MATLAB, and it illustrates the results. The leftover part of this article is organized as: The modeling of the proposed system is analyzed in section-2. The 4-level boost converter with PEMFC with ANFIS MPPT technique is presented in section-3. Section-4 explains the simulation and experimental results of developed MLI topologies. Power loss calculations of the developed MLI are done in section-5, parameters comparison among the proposed MLI with various topologies are presented in section-6, and finally, conclusions are given in section-7.

II. PROTON EXCHANGE MEMBRANE FUEL CELL

The basic structure of the fuel cell is, as shown in Fig. 1 [21]. Electrochemical conversion is the principle involved in it. A fuel cell comprises two electrodes known as anode and cathode. When the anode is fed with hydrogen fuel, the catalyst activates with the separation of positive and negative ions. The generation of electricity happens with the mixture of hydrogen and oxygen in the cell in with the electrolyte. It produces only heat and water in this process, which is wastage, and the emission of gasses is absent [22]. It shows the principle involved in the fuel cell operation in Eq. (1).

It shows the operating principle of the fuel cell in Eq. (1).

$$2H_2\,(g) + O_2\,(g) \rightarrow 2H_2O + energy \tag{1}$$

It shows the chemical equation at cathode and anode in Equations. (2) and (3).

$$\text{At cathode:} \quad H_2 \rightarrow 2H^+ + 2e^- \tag{2}$$

$$\text{At anode:} \quad \frac{1}{2}O_2 + 2H^+ + 2e^- \rightarrow H_2O \tag{3}$$

Because of the reaction of O_2 and H_2, 1.23V is developed theoretically. Ohmic and activation losses reduce the voltage to be less than 1.23V [23].In general, there are various types of fuel cells based on electrolyte materials like Alkaline Fuel Cell (AFC), Molten Carbonate Fuel Cell (MCFC), Phosphoric Acid Fuel Cell (PAFC), Proton Exchange Membrane Fuel Cell (PEMFC), and Solid Oxide Fuel Cell (SOFC) [24], [25]. In these, PEMFC, DMFC, AFC, and PAFC having an operating temperature of less than 250oC. MCFC and SOFC having a high operating temperature of more than 500oC. The automobile field is the most starving of a fuel cell. In this scenario, the popular in automotive is PEMFC where the power density is high, nominal operating temperature, and very precise [26], [27].

The mathematical modeling of PEMFC is:

The PEMFC output voltage is [28]

$$V_{FC} = E_{nerst} - V_{ohm} - V_{act} - V_{Con} \tag{4}$$

where E_{nernst} is the open-circuited thermodynamic voltage; V_{ohm} is the ohmic voltage V_{act}, and V_{con} is the activation and concentrated voltages, respectively.

E_{nernst} is determined: [29], [30].

$$E_{Nerst} = 1.22 - 8.5e^{-4}\,(T_{FC} - 298.15) + 4.308e^{-5}[\ln\left(P_{H_2}\right) + 0.5\ln\left(P_{O_2}\right)] \tag{5}$$

where T_{FC} is PEMFC cell temperature, P_{H2} and P_{O2} are the partial pressures, respectively.

The expression of ohmic voltage is: [31], [32].

$$V_{ohm} = I_{cell}\,(R_M + R_C) \tag{6}$$

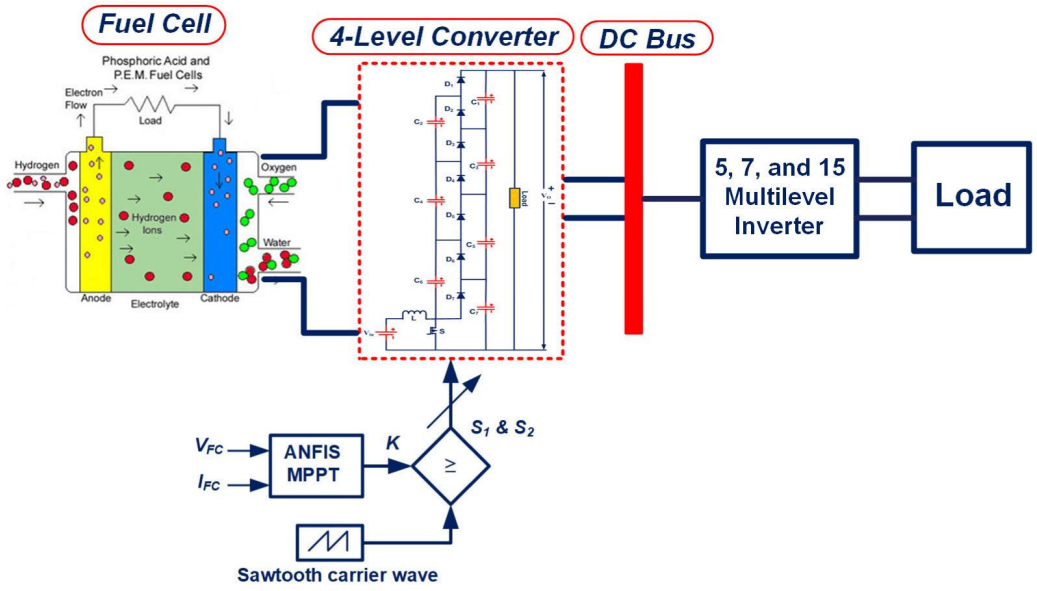

FIGURE 1. Proposed topology with fuel cell stack.

where R_C is the resistance of a proton and R_M is the equivalent of resistance. R_M is given by.

$$R_M = \frac{\rho_m L}{A} \tag{7}$$

$$\rho_m = \frac{181.6[1 + 0.03J + 0.062\left(\frac{T_{FC}}{303}\right)^2 J^{2.5}]}{[G - 0.634 - 3J]e^{\frac{4.18(T_{FC}-303)}{FC}}} \tag{8}$$

where ρ_m is the membrane specific resistivity, L is thickness, A is the area, G is water content, and J is the current density of the membrane. J is defined as

$$J = \frac{I_{cell}}{A} \tag{9}$$

It represents the activation voltage in the parametric form of:

$$V_{act} = \left(\zeta_1\zeta_2 T_{FC} + \zeta_3 T_{FC} \ln\left(C_{O_2}\right) + \zeta_4 T_{FC} \ln\left(I_{cell}\right)\right) \tag{10}$$

where ζ_1, ζ_2, ζ_3 and ζ_4 are each cell coefficients, it expresses the oxygen concentration CO2 as

$$C_{O_2} = \frac{P_{O_2}}{\left(5.08e^6\right) e^{\left(\frac{-498}{T_{FC}}\right)}} \tag{11}$$

The concentration overvoltage is given by

$$V_{Con} = -\frac{RT_{FC}}{nF} \ln\left(1 - \frac{J}{J_{max}}\right) \tag{12}$$

where F= Faraday's constant, R=gas constant, Jmax = Maximum current density.

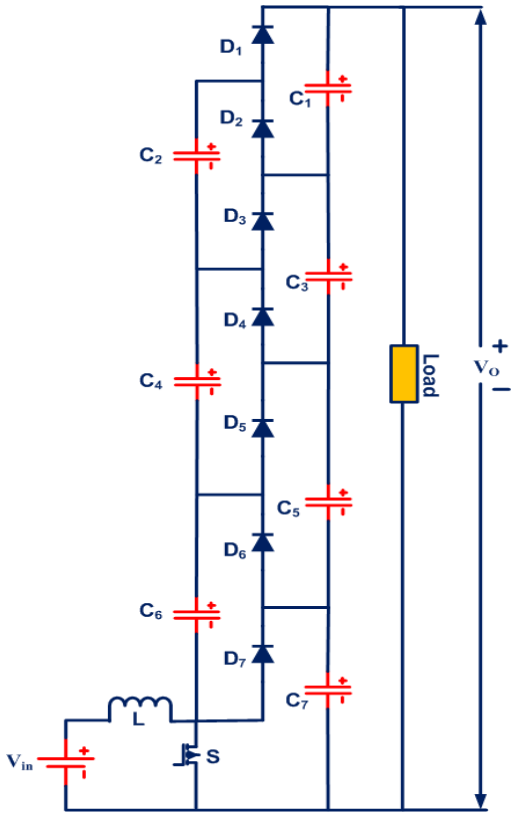

FIGURE 2. 4-level Boost Converter [33].

III. PEMFC BASED DC-DC CONVERTER

The 4-level boost converter [33] has seven capacitors, one switch and seven diodes, as shown in Fig. 2.

V_o is the output voltage of the converter which is the product of the number of levels N and the capacitor voltage

Vc is given by

$$V_o = N \times V_c = \frac{N \times V_{in}}{(1-D)} \tag{13}$$

where V_{in} is the input voltage, D is the duty cycle.

$$D = \frac{T_{on}}{T} \tag{14}$$

where T_{on} is on-state of the switch, T is the total time period.

At the instant of the closure of switch S, the voltage at the capacitance C_6 is less than C_7, at this point C_7 clamps C_6 voltage using diode D_6 along with the switch. Similarly, if the voltages at C_4 and C_6 are lesser than the capacitances C_5, and C_7, at this point C_5, and C_7 clamp the voltages at C_4, and C_6 using diode D_4 along with the switch. Correspondingly, C_3, C_5, and C7 clamp the voltages at C_2, C_4, and C_6. At the instant when the switch is open, the inductor current follows the diode D_7 and hence the capacitor C_7 gets charged. All inputs, inductor voltage, and C_6 clamp the voltages at C_5 and C_7 through the diode D_5 when D_7 conducts. Similarly, the inductor voltage and V_{IN}, C_4, and C_6 clamp the voltages at C_3, C_5, and C_7 through the diode D_3. At long last, inductor voltage and V_{IN} alongside C_2, C_4, and C_6 clips the voltages crosswise at C_1, C_3, C_5, and C_7. It is seen that the diodes D_1, D_3, D_5, and D_7 switches constantly. It is supplemented by the diodes D_2, D_4, and D6 along with the switch. Table I. shows the experimental parameters.

TABLE 1. Parameters of the proposed system.

$V_{FC}=V_{in}$	48V
V_o	400V
Switching frequency, f_{sw}	100kHz
Inductor L, with R_L	500µH with R_L=0.35Ω
Capacitor, C	10µF
Duty cycle, D	52.37%
dSPACE controller	RTI1104
Fuel cell	MT91S130-1000
IGBT	IGBT CM75DU-12, 600V, 75A
Resistive Load (Lamp)	100Ω
Inductive Load	175mH
Motor Load	Single-phase, 230V, 0.5HP

A. ANFIS MPPT CONTROLLER

A combination of neural networks and fuzzy systems produces an ANFIS system [34]. This system can learn neural networks, which is a significant advantage. There are five layers with dual inputs (x and y) and single-output (F). The if-then rules of the fuzzy system are given below:

Rule 1: if x is A_1 and y is B_1, then $F_1 = p_1X + q_1Y + r_1$ (15)

Rule 2: if x is A_2 and y is B_2, then $F_1 = p_2X + q_2Y + r_2$ (16)

It can vary the system temperature from 300K to 340K in a step of 20K by training ANFIS. By using these data sets, it generates a fuzzy interference system, where the parameters are tuned with a hybrid optimization method with the combination of least square and backpropagation algorithms.

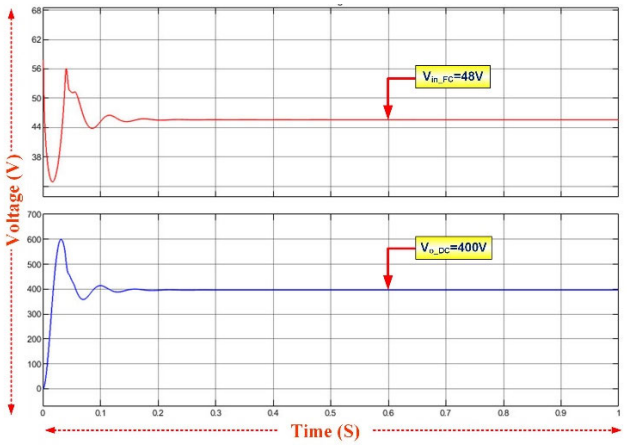

FIGURE 3. The 4-level converter & FC Simulation waveforms.

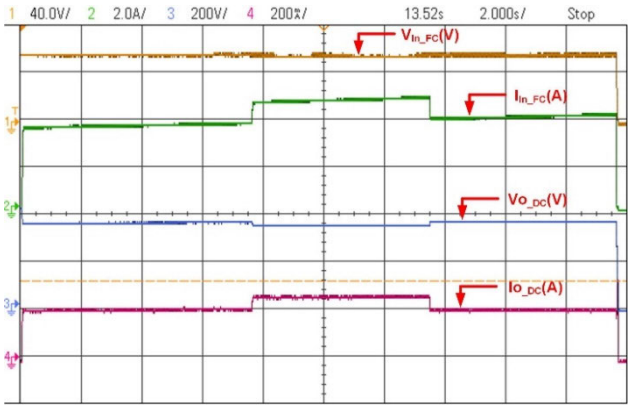

FIGURE 4. The 4-level converter & FC Simulation waveforms.

The proposed converter is simulated in MATLAB and validated experimentally with the dSPACE RTI1104 controller. The fuel cell stock input voltage $V_{In\ FC} = 48V$, switching frequency 100kHz, inductor 500H, resistance 0.35-ohm, capacitor 10F with duty cycle 53.37% for obtaining $V_{odc} = 400V$ are shown in Fig. 3 and Fig. 4 respectively. The rules and decisions follow: For the estimation of accuracy of the ANFIS MPPT controller. several simulations and experimentally are done in MATLAB/Simulink and dSPACE RTI1104 controller for the nominal operations of FC and the transient variations in the temperature of cells. It shows the DC link voltage of the FC along with the ANFIS MPPT controller in Fig. 1. The FC considered is having the output voltage is 48V and is boosted to 400V maintained at DC link using ANFIS [34].

IV. DEVELOPED STRUCTURE WITH PMFC

The proposed PEMFC inverter composed of a DC-DC converter supplied with fuel cell and it feeds the regulated DC output voltage from the converter to DC bus where the rated voltage can be maintained. It shows the fundamental unit

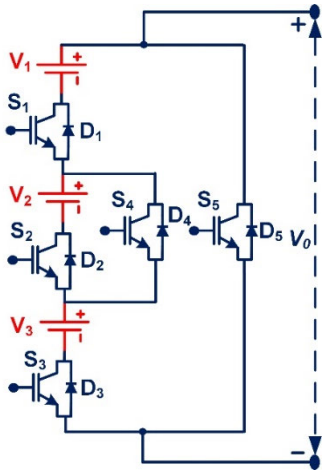

FIGURE 5. Developed fundamental unit.

in Fig. 5 comprises five switches from S_1 to S_5 and three DC sources V_1, V_2 and V_3 derived from DC bus voltage.

The switches (S2, S4), (S1, S2, S3, S5) and (S1, S3, S4, S5) are to take care that these should not turn on at an instant of time, to avoid short circuit. The various positive voltage levels only can be got. The basic units are to be connected in series to increase the voltage levels, along with this arrangement, the voltage of V_A is connected in series with a switch SA, and parallel to switch SB shown in Fig. 6, where the lowest amplitude of voltage level can be possible. A short circuit may occur with the simultaneous operation of the switches SA and SB, which is avoided.

The output voltage V_0 (t) is

$$V_0(t) = V_{0,1}(t) + V_{0,2}(t) + V_{0,3}(t) + - - - - - + V_{0,n}(t) + V_A(t) \quad (17)$$

There are only positive levels in the output voltage of a basic unit. To get the negative levels, an H-Bridge is added to the developed arrangement shown in Fig. 6. H-Bridge contains the switches S_{H1} to S_{H4}, where the operation of S_{H1} and S_{H4} produces the positive levels and the operation of S_{H2} and S_{H3} produces the negative levels of output voltage, resembles to be a multilevel inverter.

It cascades the developed fundamental units to get several levels of output like 5-level, 7-level. 15 levels shown below. The 5-level output can be got with the fundamental unit only, the several modes of operation, expected output waveform with the switching pulses could be represented below. Even though the switch count is high in the 5-level MLI, this is tested experimentally with a prototype, and we design further 7 and 15 level MLI with less device count and low THD.

A. PROPOSED 5-LEVEL MLI

The proposed 5-level MLI is designed with a developed fundamental unit without the addition of the circuit components. The circuit contains fewer number of switches compared with the existing topologies. This topology comprises nine switches with three DC sources without capacitors, diodes shown in Fig. 7. The power quality issues like THD, a smaller number of switches, dv/dt stress are minimized with this developed multilevel inverter. The circuit comprises three DC sources V_1, V_2, V_3, and nine switches S_1, S_2 S_3, S_4, S_5, S_{H1}, S_{H2}, S_{H3} and S_{H4} are the modules of H-Bridge. The arrangement reduces the additional DC source requirement and also simplifies the number of switches needed. The operating modes of the 5-Level MLI are shown in Fig. 8.

In this section, it illustrates the developed MLI operation with the steady-state voltage levels in several modes of operation. Here, all the DC source voltages are having equal magnitude, i.e., $V_1 = V_2 = V_3 = V_{dc} = 133.33$V. Mode-1: In this mode of operation, the switches S_1, S_2, S_3, S_{H1}, S_{H4} are in conduction state, hence the load current I_o path is through V_1-S_{H1}-S_{H4}-D_3-V_3-D_2-V_2- D_1. As all the DC sources are of the same magnitude, the addition of V_1, V_2, V_3 voltages can produce $3V_{dc}$. The operation of switches S_{H1} and S_{H4} in an H-Bridge produces a positive level of voltage. The output voltage level is $+3V_{dc}$ i.e., +400 volts.

Mode-2: In this mode, the switches S_1, S_3, S_4, S_{H1}, S_{H4} are in conduction state; hence the load current I_o path is through V_1-S_{H1}-S_{H4}-D_3-V_3-D_4- D_1. The voltages V_1, V_3 act in the circuits resulting in the formation of 2Vdc. The operation of switches S_{H1} and S_{H4} in an H-Bridge produces a positive level of voltage. The output voltage is $2V_{dc}$, i.e., +266.66 volts. Mode-3: In this mode, the switches S_5, S_{H1}, S_{H4} are in conduction state; hence the path follows: S_{H1}-S_{H4}-S_{H5}. No DC voltage source acts in the circuit produce $0V_{dc}$ output voltage. Mode-4: In this mode, the switches S_5, S_{H3}, S_{H2} are in conduction state; hence the path follows: S_{H1}-S_{H4}-D_5. As no DC voltage source acts in the circuit, produce $0V_{dc}$output voltage. Mode-5: In this mode, the switches S_1, S_4, S_3, S_{H2}, S_{H3} are in conduction state; hence the load current I_o path is through V_1-S_{H3}-S_{H2}-D_3-V_3-D_4- D_1. The voltages V_1, V_3 act in the circuits resulting in the formation of 2Vdc. The operation of switches S_{H3} and S_{H2} in an H-Bridge produces a negative level of voltage. The output voltage level is $2V_{dc}$, i.e., -266.66 volts. Mode-6: In this mode, the switches S_1, S_{H3}, S_{H2} are in conduction state; hence the load of current I_o passes through V_1-S_{H3}-S_{H2}-D_3-V_3-D_2-V_2- D_1. As the voltage sources V_1, V_2, V_3. Acts in the circuit produced an output voltage of $3V_{dc}$. The operation of switches S_{H3} and S_{H2} in an H-Bridge produces a negative level of voltage. The output voltage level is $-3V_{dc}$, i.e., −400V. It shows the standard output voltage waveform in Fig. 8(g). The respective switching table for the developed 7-level MLI is illustrated in Table II. It shows the simulation and experimental obtained results in Fig. 9(a) & (b). The hardware specifications used in the design of five levels of MLI are shown in Table I.

B. PROPOSED 7-LEVEL MLI

The proposed 7-level MLI is designed with a developed fundamental unit with the addition of one extra switch S_6 connected parallel to the series combination of the switch S_1 and

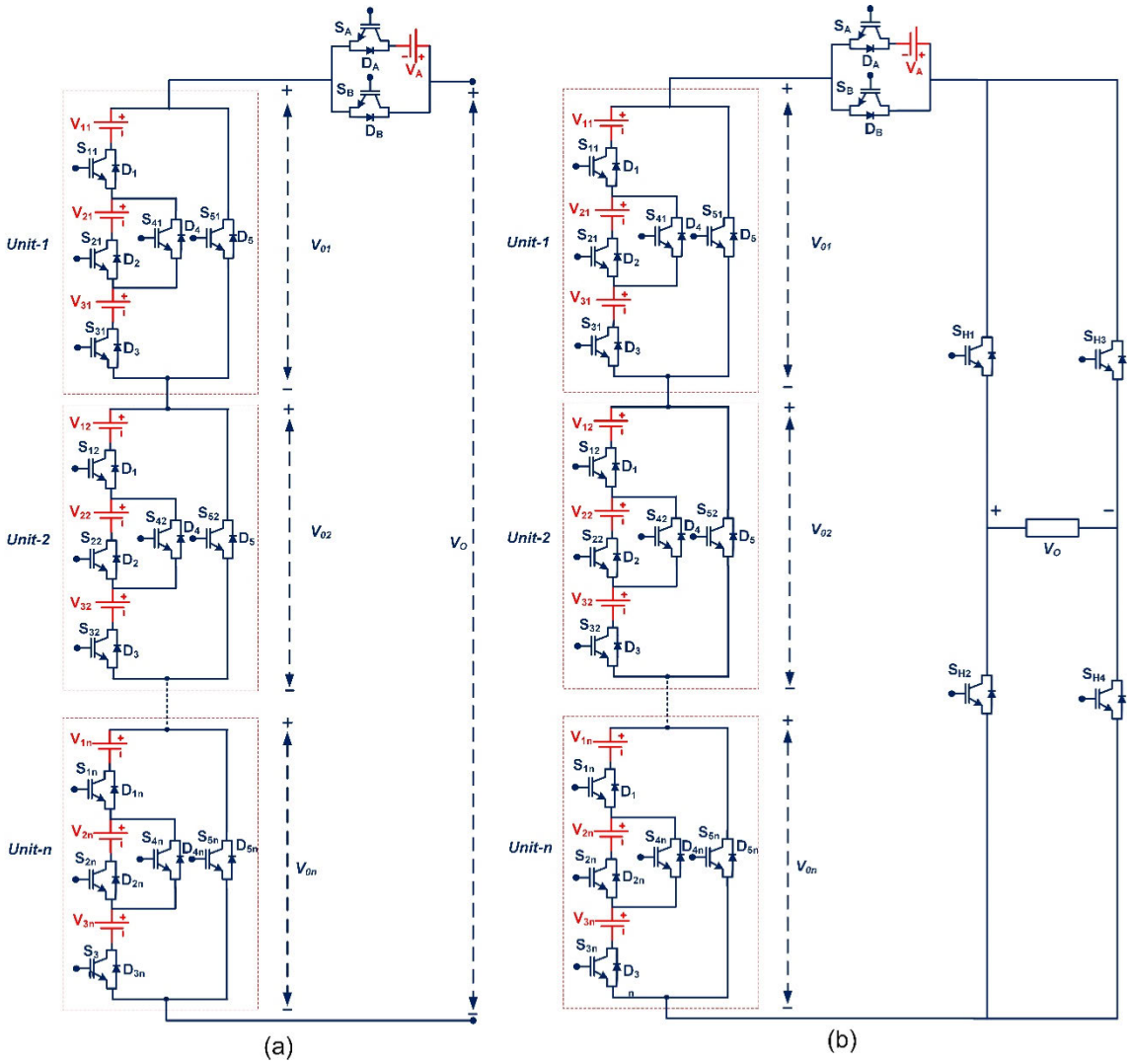

FIGURE 6. Developed cascaded multilevel inverter.

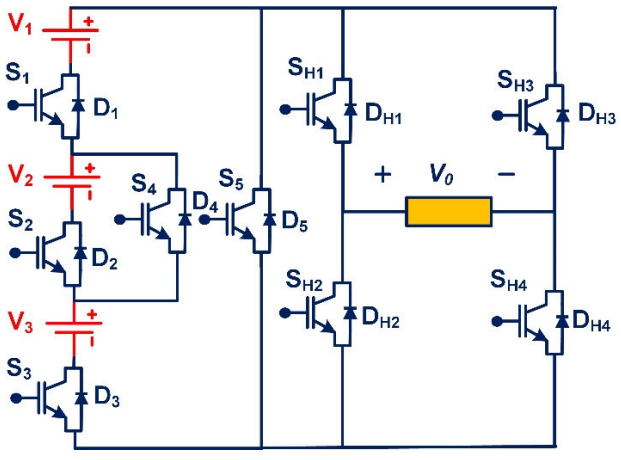

FIGURE 7. The basic structure of 5-level MLI.

voltage V_1. The circuit contains a fewer number of switches compared with the existing topologies. This topology has ten switches with three DC sources without capacitors, diodes shown in Fig. 10. The power quality issues like THD, a smaller number of switches, dv/dt stress are minimized with this developed multilevel inverter.

In this module, the developed MLI operation is illustrated in detail in Fig. 11 with the steady-state voltage levels in several modes of operation. Here, all the DC source voltages are having equal magnitude, i.e., $V_1 = V_2 = V_3 = V_{dc} = 133.33$V. Mode-1: In this mode, the switches, S_1, S_2, S_3, S_{H1}, S_{H4} are in conduction state; hence the load current I_o path is through V_1-S_{H1}-S_{H4}-D_3-V_3-D_2-V_2- D_1. As all the dc sources are of the same magnitude, the addition of V_1, V_2, V_3 voltages can produce $3V_{dc}$. The operation of switches S_{H1} and S_{H4} in an H-Bridge produces a positive level of voltage. The output voltage level is $+3V_{dc}$, i.e., +400 volts. Mode-2: In this mode, the switches S_2, S_3, S_6, S_{H1}, S_{H4} are in conduction state; hence the load current I_o path is through V_3-D_2-V2-S_6-S_{H1}-S_{H4}. The voltages V_2, V_3 act in the circuits resulting in the formation of $2V_{dc}$.The operation of switches S_{H1} and S_{H4} in an H-Bridge produces a positive level of voltage.

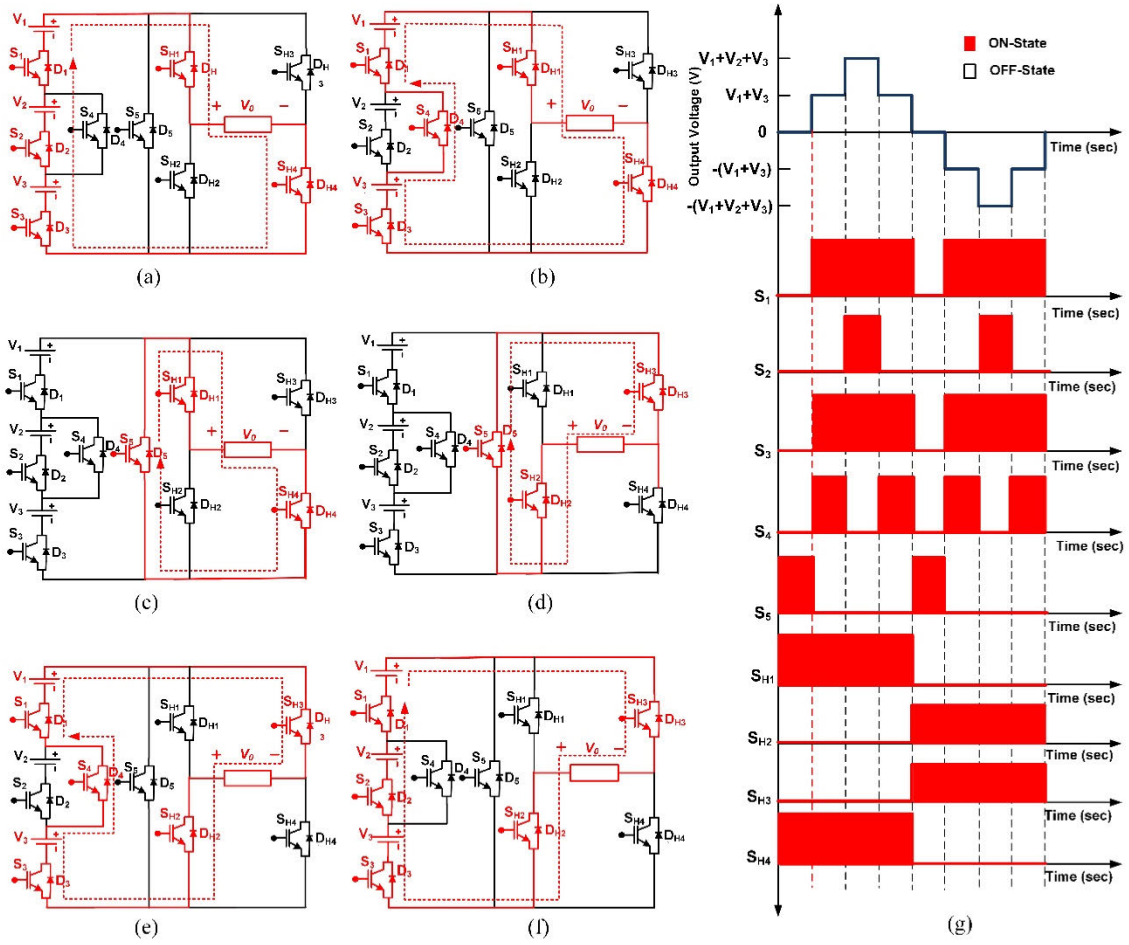

FIGURE 8. Modes of operation of the developed 5-Level MLI topology. (a): Mode-1, (b) Mode-2, (c) Mode-3, (d) Mode-4, (e) Mode-5, (f) Mode-6, (g) 5-Level expected output voltage waveform.

TABLE 2. Switching states for the developed 5-Level MLI.

Mode	Output Voltage (V_o) Volts	Switch State								
		S_1	S_2	S_3	S_4	S_5	S_{H1}	S_{H2}	S_{H3}	S_{H4}
1	$2V_{dc}$	1	1	1	0	0	1	0	0	1
2	V_{dc}	1	0	1	1	0	1	0	0	1
3	0	0	0	0	0	1	1	0	0	1
		0	0	0	0	1	0	1	1	0
4	$-V_{dc}$	1	0	1	1	0	0	1	1	0
5	$-2V_{dc}$	1	1	1	0	0	0	1	1	0

The output voltage level is $+2V_{dc}$, i.e., +266.66 volts. Mode-3: In this mode, the switches S_3, S_4, S_6, S_{H1}, S_{H4} are in conduction state; hence the load current I_o path is through V_3-S_4-S_6-S_{H1}-S_{H4}-D_3. The voltages V_3 acts in the circuit resulting in the formation of $V_O = V_{dc}$. The operation of switches $S_{H1}$and S_{H4} in an H-Bridge produces a positive level of voltage. The output voltage level is $+1V_{dc}$, i.e., $V_o = +133.33$ volts. Mode-4: In this mode, the switches S_5, S_{H1}, S_{H4} are in conduction state; hence the path follows S_{H1}-S_{H4}-S_5. No dc voltage source acts in the circuit produces $0V_{dc}$ output voltage. Hence $V_o = 0$ volts. Mode-5: In this mode, the switches S_5, S_{H3}, S_{H2} are in conduction state; hence the path follows S_{H3}-S_{H2}-S_5. As no dc voltage source acts in the circuit, produces $0V_{dc}$ output voltage. Hence $V_o = 0$ volts. Mode-6: In this mode, the switches S_3, S_4, S_6, S_{H3}, S_{H2} are in conduction state; hence the load current I_o path is through V_3- S_4-S_6-S_{H3}-S_{H2}-D_3. The voltages V_3 acts in the circuit resulting in the formation of 1Vdc. The operation of switches S_{H3} and S_{H2} in an H-Bridge produces a negative level of voltage. The output voltage level is $1V_{dc}$,

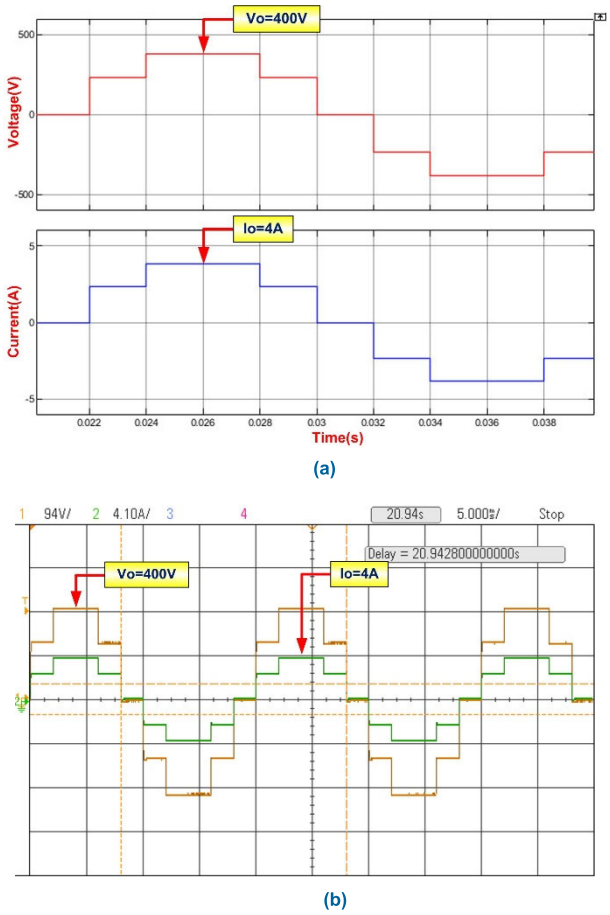

FIGURE 9. (a) Simulation output voltage and current waveforms of a five-level inverter. (b) Experimental output voltage and current waveforms of a five-level inverter.

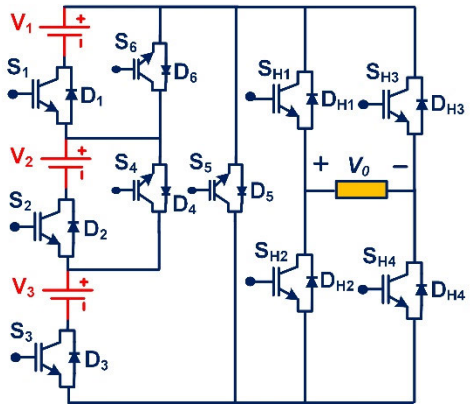

FIGURE 10. The basic structure of 7-level MLI.

i.e., $V_o = -133.33$ volts. Mode-7: In this mode, the switches S_2, S_6, S_{H3}, S_{H2}, S_3 are in conduction state; hence the load of current I_o passes through V_3-D_2-V_2-S_6-S_{H3}-S_{H2}-D_3. As two voltage sources V_2, V_3 acts in the circuit produce an output voltage of $2V_{dc}$. The operation of switches $S_{H3}$and S_{H2} in an H-Bridge produces a negative level of voltage. The output voltage level is $-2V_{dc}$, i.e., $V_o = -266.66$V. Mode-8: In this mode, the switches S_1, S_{H3}, S_{H2}, S_3, S_2, S_1 are in conduction state; hence the load of current I_o passes through V_1- S_{H3}-S_{H2}-D_3-V_3-D_2-V_2-D_1. As two voltage sources V_1, V_2, V_3 acts in the circuit produce an output voltage of $3V_{dc}$. The operation of switches S_{H3} and S_{H2} in an H-Bridge produces a negative level of voltage. The output voltage level is $-2V_{dc}$, i.e., $V_o = -400$V. It shows the typical output voltage waveform in Fig. 11(i). The developed MLI operation can be viewed from the switching pulses generated according to the operation of switches. It can power the state of switches with '1' or '0'. If the state of the switch is in '1', we turn it on. If the state is in '0', it resembles it turns the switch off. The respective switching table for the developed 7-level MLI is illustrated in Table III. We design the MLI with three equal magnitudes of voltages: V_1, V_2, V_3 having 133.33V each, therefore the 400V, 4A output voltage, and current with a load resistor of 100Ω. It shows the simulation and experimental obtained results in Fig. 12(a) & (b). With this arrangement, it is easy to get seven levels of output with which the power quality increases with a reduced THD. Table shows the hardware specifications used in the design of seven-level MLI I.

C. PROPOSED 15-LEVEL MLI

The proposed 15-level MLI is designed with two developed fundamental units in cascade without the addition of circuit components. This topology consists of sixteen switches with seven DC sources without capacitors, diodes shown in Fig. 13. The power quality issues like THD, less number of switches, dv/dt stress are minimized with this developed multilevel inverter. The switches S_{H1}, S_{H2}, S_{H3}, and SH4 are connected in an H-Bridge, where the negative voltage levels can be produced. The 15 levels developed circuit is shown in Fig. 13. The operation of switches is shown in Table III and a few modes of operation of the developed 15 levels MLI is represented in Fig. 14, the expected output voltage waveform is shown in Fig. 14.

The developed MLI operation can be simply viewed from the switching pulses generated according to the operation of switches. It can power the state of switches with '1' or '0'. If the state of the switch is in '1', we turn it on. If the state is in '0', it resembles it turns the switch off. The respective switching table for the developed 15-level MLI is illustrated in Table IV. We design the MLI with three equal magnitudes of voltages: V_1, V_2, V_3 having 58V each, therefore the 400V, 4A output parameters with a load resistor of 100Ω.

We simulate the developed cascaded MLI in MATLAB. The developed two units cascaded fifteen-level multilevel inverter simulation is shown in Fig. 14. It makes all the DC sources to be constant of 58V, concerning this voltage, the waveforms of the voltage and current are got and shown in Fig. 17. Initially, the switches S_{51} of unit-1, S_{52} of unit-2, and S_B are turned on. As it connects no DC voltage source in the circuit, the voltage becomes 0V. The switch S_{51} of unit-1, S_{52} of unit-2, and S_A are turned on, where the voltage source V_A acts alone in the circuit forms an output voltage of +57V with the H-Bridge operation of S_{H1} and S_{H4} gives positive

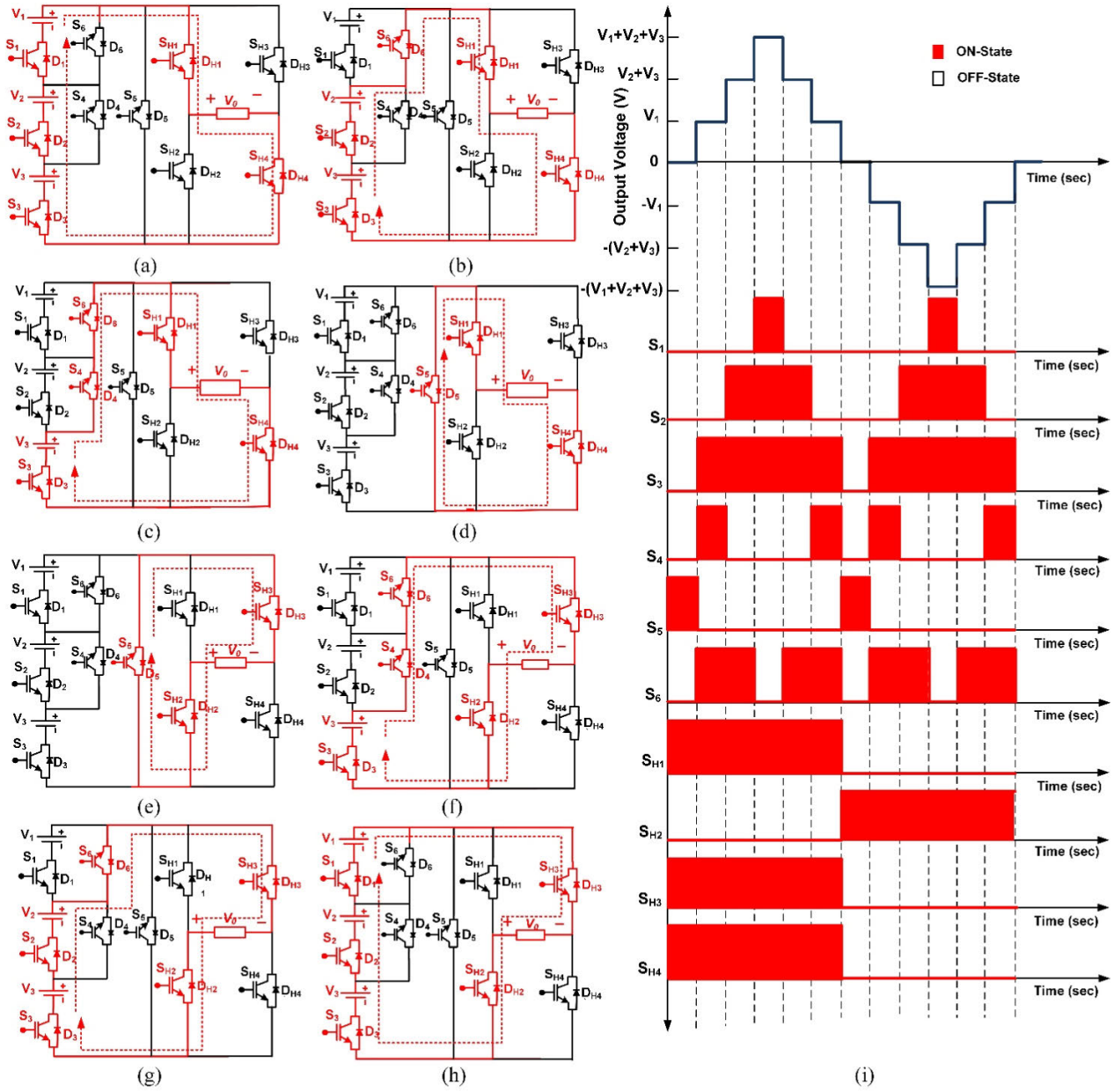

FIGURE 11. Modes of operation of the developed 7-Level MLI topology. (a): Mode-1, (b): Mode-2, (c): Mode-3, (d): Mode-4, (e): Mode-5, (f): Mode-6, (g): Mode-7, (h): Mode-8, (i): 7-Level expected output voltage waveform.

TABLE 3. Switching states for the developed 7-Level MLI.

Mode	Output Voltage (V_o) Volts	Switch State									
		S_1	S_2	S_3	S_4	S_5	S_6	S_{H1}	S_{H2}	S_{H3}	S_{H4}
1	$3V_{dc}$	1	1	1	0	0	0	1	0	0	1
2	$2V_{dc}$	0	1	1	0	0	1	1	0	0	1
3	V_{dc}	0	0	1	1	0	1	1	0	0	1
4	0	0	0	0	0	1	0	1	0	0	1
		0	0	0	0	1	0	0	1	1	0
5	$-V_{dc}$	0	0	1	1	0	1	0	1	1	0
6	$-2V_{dc}$	0	1	1	0	0	1	0	1	1	0
7	$-3V_{dc}$	1	1	1	0	0	0	0	1	1	0

voltage level. Then, the switches S_{51} of unit-1, S_{12}, S_{32}, S_{42} of unit-2, and S_B are turned on, where the voltage sources V_{12} and V_{32} acts alone in the circuit, getting the output voltage of +114V with the H-Bridge operation of S_{H1} and S_{H4}

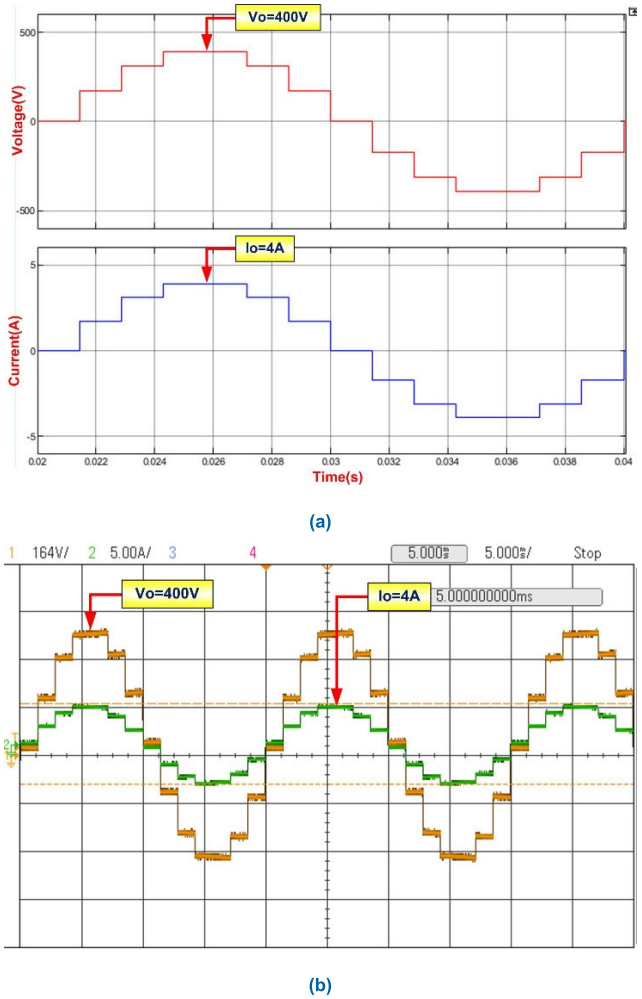

FIGURE 12. (a) Simulation output voltage and current waveform of Seven-level inverter. (b) Experimental output voltage and current waveforms of a seven-level inverter.

producing positive voltage levels. Then, the switches S_{51} of unit-1, S_{12}, S_{22}, S_{32}, of unit-2, and S_B are turned on, where the voltage sources V_{12}, V_{22}, and V_{32} acts in the circuit getting the maximum output voltage of +171V with the H-Bridge operation of S_{H1} and S_{H4} producing positive voltage levels. Then, the switches S_{51} of unit-1, S_{12}, S_{22}, S_{32}, of unit-2, and $S_A$are turned on, where the voltage sources V_{12}, V_{22}, V_{32}, and V_A acts in the circuit, getting the maximum output voltage of +228V with the H-Bridge operation of S_{H1} and S_{H4} producing positive voltage levels. Then, the switches S_{11}, S_{31}, S_{41} of unit-1, S_{12}, S_{32}, S_{42} of unit-2, and S_A are turned on, where the voltage sources V_{11}, V_{31}, V_{12}, V_{32}, and V_A acts in the circuit, getting the output voltage of +285V with the H-Bridge operation of S_{H1} and S_{H4} producing positive voltage levels. Then, the switches S_{11}, S_{31}, S_{41} of unit-1, S_{12}, S_{22}, S_{32} of unit-2, and S_A are turned on, where the voltage sources V_{11}, V_{31}, V_{12}, V_{22}, V_{32}, and V_A acts in the circuit, getting the output voltage of +342V with the H-Bridge operation of S_{H1} and S_{H4} producing positive voltage levels. Then, the switches S_{11}, S_{21}, S_{31} of unit-1, S_{12}, S_{22}, S_{32} of unit-2, and S_A are turned on, where the voltage sources V_{11},

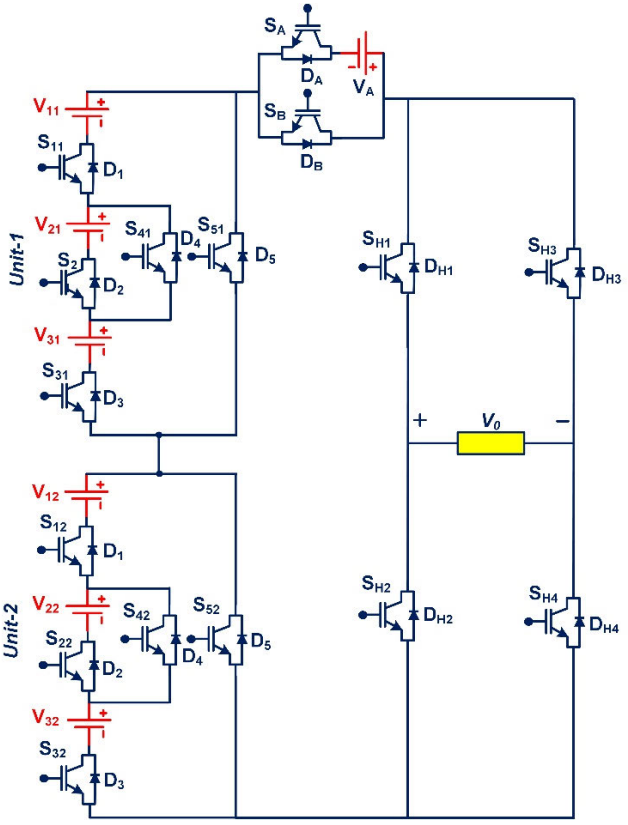

FIGURE 13. The basic structure of 15-level MLI.

V_{21}, V_{31}, V_{12}, V_{22}, V_{32}, and V_A acts in the circuit, getting the output voltage of +400V with the H-Bridge operation of S_{H1} and S_{H4} producing positive voltage levels. We get hence the positive cycle of output voltage waveform. For obtaining, the negative cycle, the H-Bridge is operated with the switches S_{H2} and S_{H3} in all modes of operation of the multilevel inverter. Hence the fifteen levels that can be achieved at the output of MLI with simulation THD are shown in Fig. 15 and Fig. 16 respectively. The simulation and experimental output waveforms and THD can be got shown in Fig. 17, Fig. 18, Fig. 19, and Fig. 20, respectively. With this arrangement, we can get the fifteen levels of output with a smaller number of switches with which the power quality increases with a reduced THD. The developed cascaded fifteen levels multi-level inverter is implemented experimentally and the results with R-Load shown in Fig. 20, with L-Load shown in Fig. 21, with R in parallel with L load shown in Fig. 21, Fig. 22 shows the output waveforms with L in parallel with R load. The load is with a resistance of 100Ω are verified with a simulation output waveform, and the respective THD from simulation and experimental are got shown in Fig. 23 and Fig. 24. It shows the experimental setup in Fig. 25. It shows the hardware specifications used in the design of fifteen levels of MLI Table I.

V. POWER LOSS CALCULATION

The crucial power loss of switches in MLIs are from conduction and switching losses [13] the switching losses and

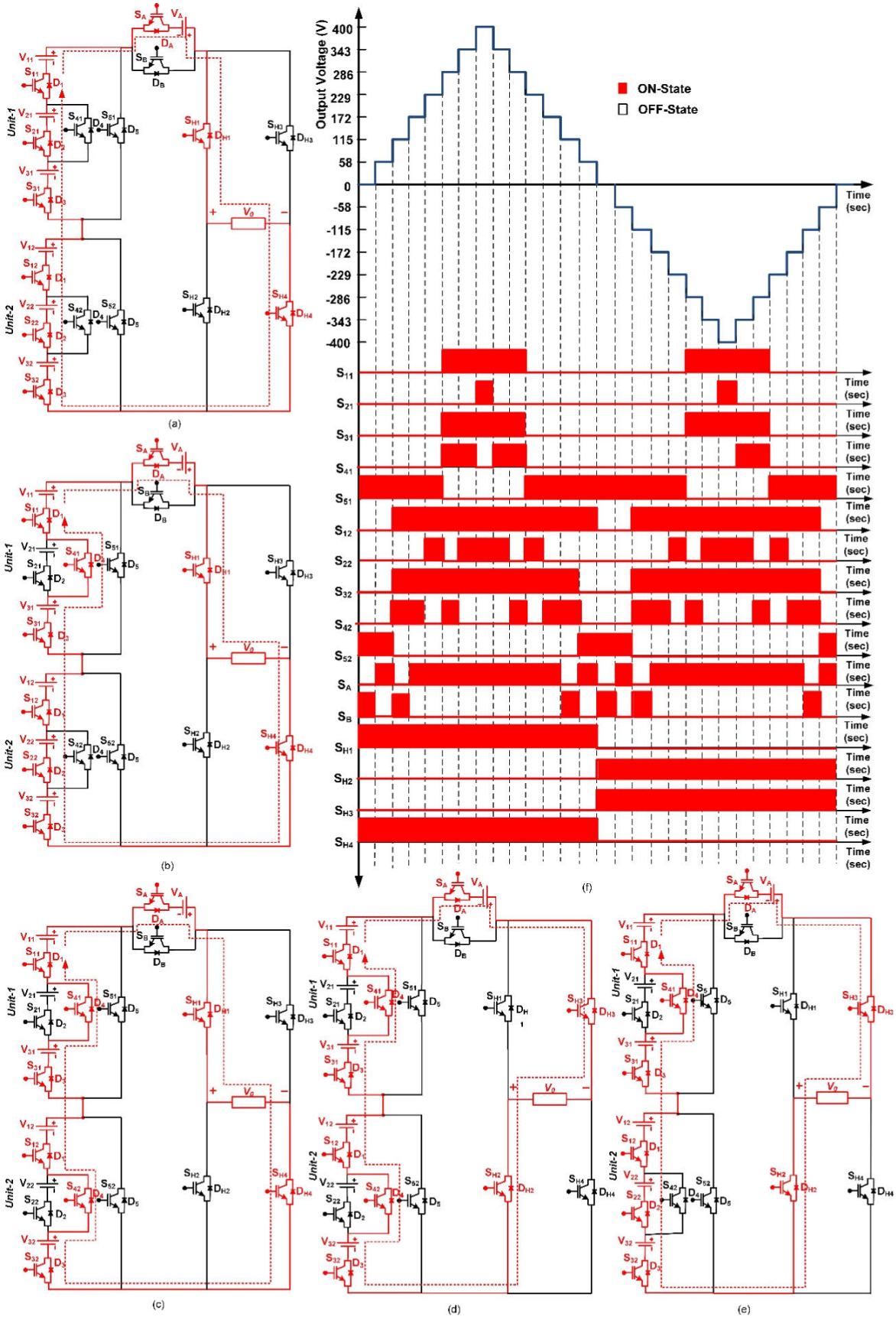

FIGURE 14. Few modes of operation for the developed 15-Level MLI topology. (a): Mode-1, (b): Mode-2, (c): Mode-3, (d): Mode-13, (e): Mode-14, (f): 15-Level expected output voltage waveform.

TABLE 4. Switching states for the developed 15-Level MLI.

Mode	Output Voltage (V_o) Volts	Switch State															
		S_{11}	S_{21}	S_{31}	S_{41}	S_{51}	S_{12}	S_{22}	S_{32}	S_{42}	S_{52}	S_A	S_B	S_{H1}	S_{H2}	S_{H3}	S_{H4}
1	$7V_{dc}$	1	1	1	0	0	1	1	1	0	0	1	0	1	0	0	1
2	$6V_{dc}$	1	0	1	1	0	1	1	1	0	0	1	0	1	0	0	1
3	$5V_{dc}$	1	0	1	1	0	1	0	1	1	0	1	0	1	0	0	1
4	$4V_{dc}$	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	1
5	$3V_{dc}$	0	0	0	0	1	1	0	1	1	0	1	0	1	0	0	1
6	$2V_{dc}$	0	0	0	0	1	1	0	1	1	0	0	1	1	0	0	1
7	V_{dc}	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	1
8	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	1
		1	1	1	0	0	1	1	1	0	0	1	0	0	1	1	0
9	$-V_{dc}$	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	0
10	$-2V_{dc}$	0	0	0	0	1	1	0	1	1	0	0	1	0	1	1	0
11	$-3V_{dc}$	0	0	0	0	1	1	0	1	1	0	1	0	0	1	1	0
12	$-4V_{dc}$	0	0	0	0	1	1	1	1	0	0	1	0	0	1	1	0
13	$-5V_{dc}$	1	0	1	1	0	1	0	1	1	0	1	0	0	1	1	0
14	$-6V_{dc}$	1	0	1	1	0	1	1	1	0	0	1	0	0	1	1	0
15	$-7V_{dc}$	1	1	1	0	0	1	1	1	0	0	1	0	0	1	1	0

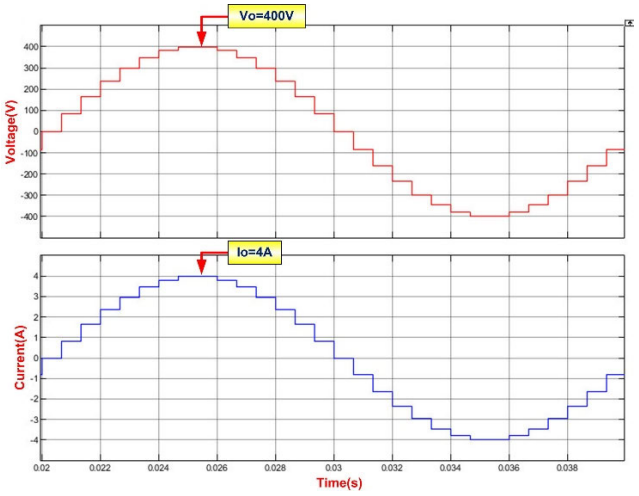

FIGURE 15. Simulation output voltage and current waveforms of a fifteen-level inverter.

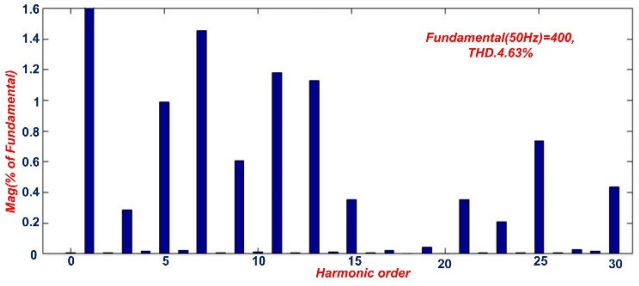

FIGURE 16. Simulation THD.

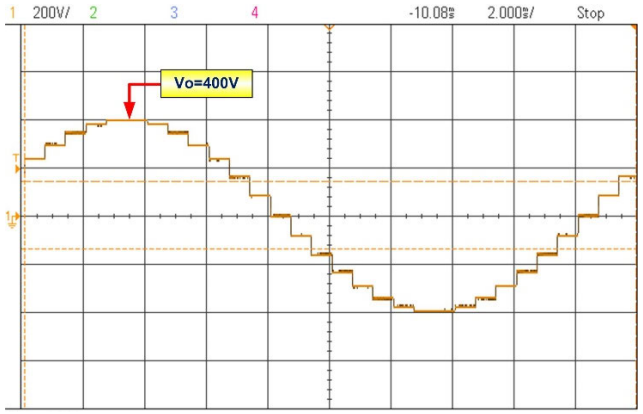

FIGURE 17. Experimental output waveform (Vo).

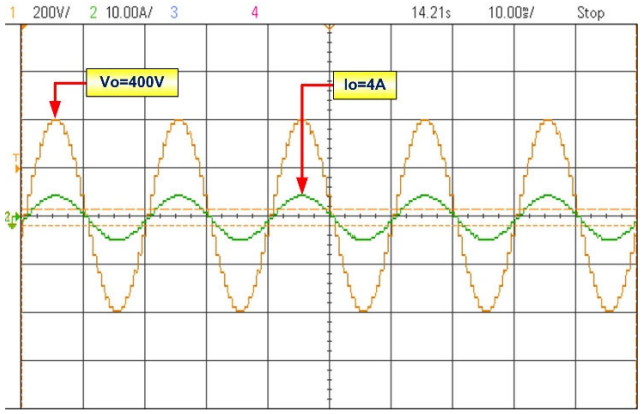

FIGURE 18. Experimental output waveform with R Load.

conduction losses dominate high switching frequencies are more effective in low switching frequency. Conduction loss of IGBT with antiparallel diode is because of the on-state condition of resistance and voltages of both transistors and diode. When V_S is applied to switches, R_S, R_d is the internal resistances of the transistor, diode respectively and V_d is the on-state voltage. The conduction losses (P_c) of diode P_{cd} and transistor P_{cs} are determined as follows [18], [39]

$$\boldsymbol{P_{cd}}(t) = V_d i(t) + R_d\, i2(t) \tag{18}$$

$$\boldsymbol{P_{cs}}(t) = V_s i(t) + [R_s\, i\beta(t)]i(t) \tag{19}$$

where β is a constant calculated from characteristics of a power switch.

Assuming, there are $N_{s,on}$ switches and $N_{d,on}$ diodes are conduction at the time of instant 't' then the multilevel

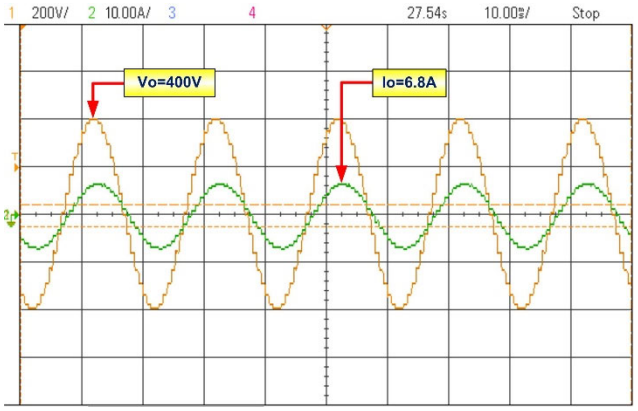

FIGURE 19. Experimental output waveform with L Load.

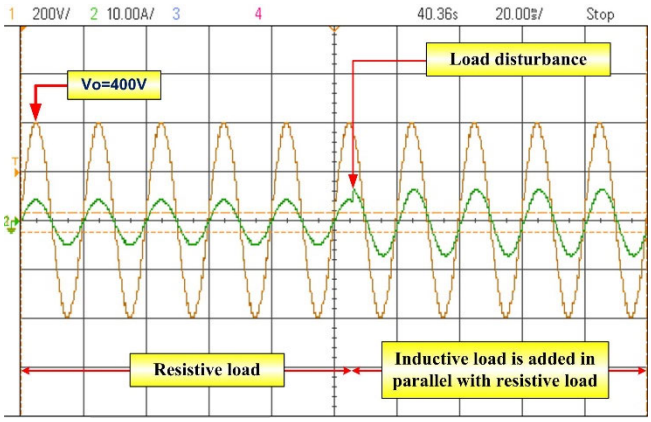

FIGURE 20. Experimental output waveform with R||L load.

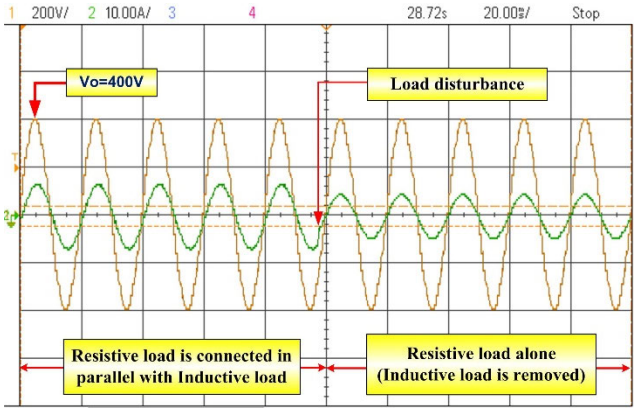

FIGURE 21. Experimental output waveform with L||R load.

average conduction power losses are [18], [39]

$$P_{CU} = \frac{1}{\pi}\int_0^{\pi}\left[N_{s,on}(t)\,P_{cs}(t) + N_{d,on}(t)\,P_{cd}(t)\right]dt$$

$$P_{CU} = \frac{1}{\pi}\int_0^{\pi}\Big[N_{s,on}(t)\{V_s i(t) + R_s i^{\beta}(t)\} + N_{d,on}(t)\{V_d i(t) + R_d i(t)\Big]i(t)dt \quad (20)$$

In the proposed MLI topology there is a bi-directional switch S_a, and it conducts at the time of instant't' then the average

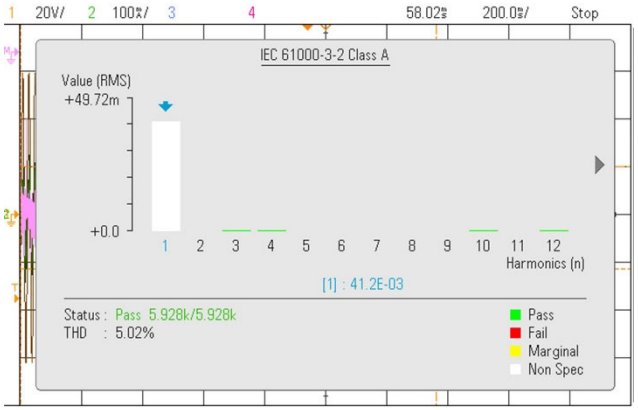

FIGURE 22. Experimental THD.

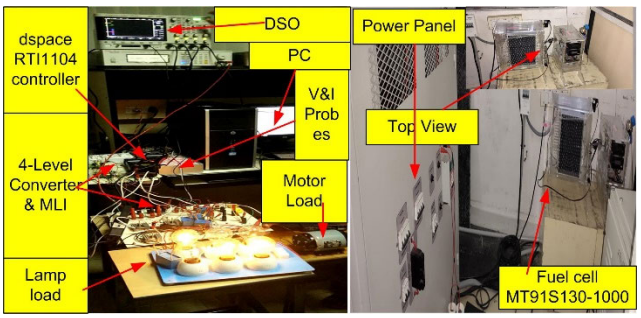

FIGURE 23. Experimental setup.

conduction losses are [18], [39]

$$P_{CB} = \frac{1}{\pi}\int_0^{\pi}\left[V_s(t) + V_d(t) + R_s i^{\beta}(t) + R_d i(t)\right]i(t)\,d(t) \quad (21)$$

Consider the output current is sinusoidal, then

$$i(t) = i_m \sin(t) \quad (22)$$

The simplified average conduction losses of a bi-directional switch can be calculated from equation (20) and (21)

$$P_{CB} = \frac{2}{\pi} i_m [V_s(t) + V_d(t)] + \frac{R_d i_m^2}{2} + \frac{R_s i_m^{\beta+1}}{\pi} \times \int_0^{\pi} \sin^{\beta+1}(t)\,d(t) \quad (23)$$

Therefore, total conduction losses P_c of MLI topology is obtained as equation (20) and (23)

$$P_C = P_{CU} + P_{CB} \quad (24)$$

The energy losses especially during on and off-states of the switches results in switching losses for a switching period of a switch. Hence there is a linear variation in voltage and current are related as follows [12], [17]

$$P_{sw,on} = \frac{1}{T}\int_0^{t_{on}} V(t)\,.i(t)\,dt = \frac{1}{T}\int_0^{t_{on}} [(\frac{V_{sw}}{t_{on}}t)(-\frac{I}{t_{on}}(t - t_{on}))]dt$$

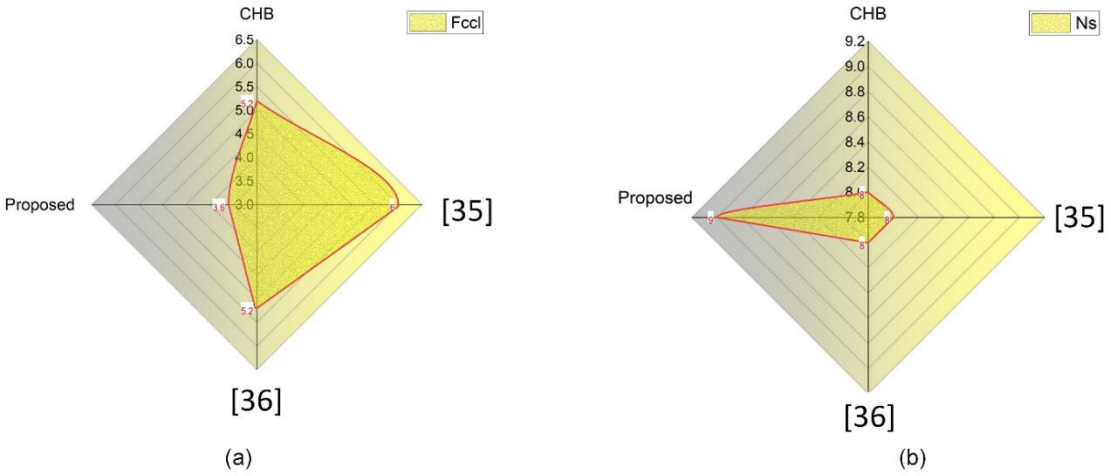

FIGURE 24. (a) Comparison of components count per level of proposed MLI with other topologies. (b) Comparison of Number of Switches to the proposed MLI with other topologies.

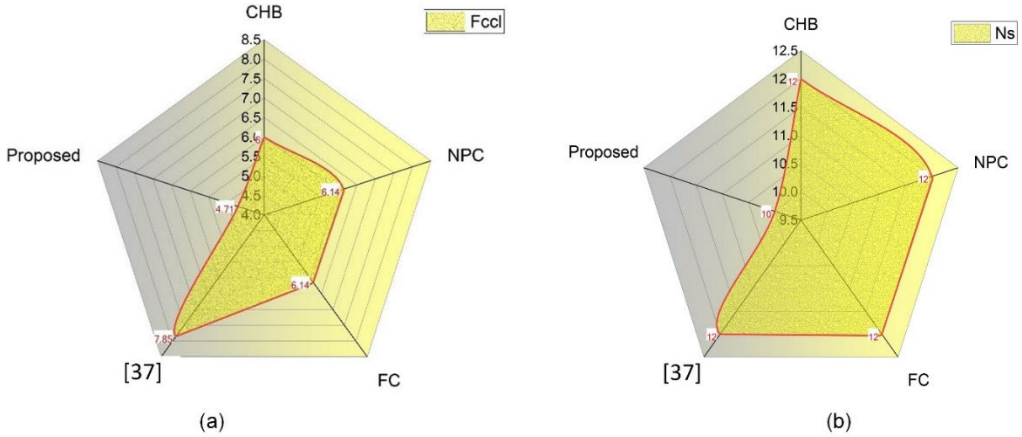

FIGURE 25. (a) Comparison of components count per level of proposed MLI with other topologies. (b) Comparison of Number of Switches to the proposed MLI with other topologies.

$$P_{sw,on} = \frac{1}{6T}[V_{sw}.I.t_{on}] \tag{25}$$

$$P_{sw,off} = \frac{1}{T}\int_0^{t_{off}} V(t).i(t)\,dt = \frac{1}{T}\int_0^{t_{off}} [(\frac{V_{sw}}{t_{off}}t)(-\frac{I}{t_{off}}(t-t_{off}))]dt$$

$$\mathrm{P_{sw,off}} = \frac{1}{6\mathrm{T}}[\mathrm{V_{sw}}.\mathrm{I}.\mathrm{t_{off}}] \tag{26}$$

where T is a total time period and $P_{sw,on}$, $P_{sw,off}$ are on-state, and off-state switching losses, t_{on}, t_{off} are the on, and off-state time periods respectively, and $V_{sw.}$ is the peak voltage of the switch hence total switching losses P_{sw} of multilevel inverter is expressed as

$$\mathrm{P_{SW}} = \mathrm{P_{SW,ON}} + \mathrm{P_{SW,OFF}} \tag{27}$$

Thus, the combination of conduction and switching losses gives the total power loss P_L; it can be expressed as

$$\mathrm{P_L} = \mathrm{P_C} + \mathrm{P_{SW}} \tag{28}$$

Further, the efficiency η for the proposed inverter is calculated as [18], [39]

$$\eta = \frac{P_{Out}}{P_{in}} = \frac{P_{Out}}{P_{Out} + P_L} \tag{29}$$

We can get the output power:

$$P_{out} = V_{rms} * I_{rms} \tag{30}$$

VI. COMPARISON STUDIES

The symmetrical configuration of the presented MLI is compared with various levels like 5 level, 7 levels, 15 levels symmetrical configuration of the multilevel inverters such as Cascaded H-bridge (CHB), Flying capacitors (FC), Neutral point clamped (NPC) and the several topologies presented. The components with their output voltage levels for correspondent topologies considered is calculated from the equations in Table IV and tabulated in the respective levels of operation tables. And the components count per level factor

TABLE 5. The variance of variant 7 level MLI topologies with regards number of output levels Nlev.

Components required	CHB	NPC	FC	[35]	[38]	[20]	[38]	Proposed
Number of switches (Ns)	$2(N_{Lev}\text{-}1)$	$2(N_{Lev}\text{-}1)$	$2(N_{Lev}\text{-}1)$	$(N_{Lev}+3)$	$(N_{Lev}+2)$	$(N_{Lev}+1)$	$(N_{Lev}\text{-}1)$	$\frac{N_{Lev}+19}{4}$
Number of diodes (Nd)	$2(N_{Lev}\text{-}1)$	$2(N_{Lev}\text{-}1)$	$2(N_{Lev}\text{-}1)$	$(N_{Lev}+3)$	$(N_{Lev}+2)$	$(N_{Lev}+1)$	$(N_{Lev}\text{-}1)$	$(N_{Lev}\text{-}1)$
Dc link capacitors (Ncap)	0	$(N_{Lev}\text{-}1)$	$(N_{Lev}\text{-}1)$	$\frac{N_{Lev}-1}{4}$	$\frac{N_{Lev}-1}{4}$	$\frac{N_{Lev}-1}{4}$	$\frac{N_{Lev}-1}{4}$	$\frac{N_{Lev}-1}{4}$
Dc sources (n)	$\frac{N_{Lev}-1}{2}$	$\frac{N_{Lev}-1}{8}$	$\frac{N_{Lev}-1}{8}$	$\frac{N_{Lev}-1}{8}$	$\frac{N_{Lev}-1}{8}$	$\frac{N_{Lev}-1}{8}$	$\frac{N_{Lev}-1}{4}$	$\frac{N_{Lev}-1}{4}$
Number of driver board circuits (Ndk)	$2(N_{Lev}\text{-}1)$	$2(N_{Lev}\text{-}1)$	$2(N_{Lev}\text{-}1)$	$(N_{Lev}+3)$	$(N_{Lev}+2)$	$(N_{Lev}+1)$	$(N_{Lev}\text{-}2)$	$\frac{N_{Lev}+19}{4}$

TABLE 6. The variance of variant 5 level MLI topologies with regards number of output levels.

Components required	CHB	[35]	[36]	Proposed
Number of switches (Ns)	8	8	8	5
Number of diodes (Nd)	8	8	8	5
Dc link capacitors (Ncap)	0	3	0	0
Dc sources (n)	2	1	2	3
Number of other components (nx)	0	2	0	0
Number of driver board circuits (Ndk)	8	8	8	5
Components count per level (Fccl)	5.2	6	5.2	3.6

F_{ccl} is calculated from equation 31.

$$F_{ccl} = \frac{N_s + N_d + N_{cap} + N_{dk} + n}{N_{Lev}} \tag{31}$$

Form Table VI, even though the number of power switches needed to produce five-level staircase outputs for designed topology is nominally high as considered with other topologies, the ambiguousness of the inverter, THD, power losses gets decreased. Considering that the components count per level factor $\boldsymbol{F_{ccl}}$ value is more; then the topology requires more components to build the desired voltage level thus in the recent investigations, the primary aim is to decrease components count per level factor in the design of multilevel inverter. It is noticed that from Table V the proposed MLI is having fewer components count per level factor $\boldsymbol{F_{ccl}}$ as related to other nine-level multilevel inverter topologies. Fig. 24 presents the comparison of the number of switches requires producing five-level output voltage steps. From Fig. 24, the introduced topology utilizes fewer switches to correspondence topologies. Minimization of switches reduces the requirement of gate driver circuits for switches and limits components count per level factor $\boldsymbol{F_{ccl}}$ hence reduce the complexity of the inverter. Fig. 24 represents the comparison result of the components count per level factor $\boldsymbol{F_{ccl}}$ to develop a nine-levels of output. From Fig. 24, the proposed topology uses fewer components count per level factor $\boldsymbol{F_{ccl}}$ in correlation with the different topologies.

A. COMPARISON STUDIES FOR 5 LEVEL MLI

B. COMPARISON STUDIES FOR 7 LEVEL MLI

Form Table VII the number of power switches needed to produce seven-level staircase outputs for designed topology is less as considered with other topologies. Hence there is a reduction of gate driver circuits, so the ambiguousness of the inverter gets decreased. Considering that the components count per level factor F_{ccl} value is more; then the topology requires more components to build the desired voltage level thus in the recent investigations, the primary objective is to decrease components count per level factor in the design of multilevel inverter. It is noticed that from Table III the proposed MLI is having fewer components count per level factor F_{ccl} as related to other seven-level multilevel inverter topologies. Fig. 10 presents the comparison of the number of switches requires producing seven-level output voltage steps. From Fig. 10, the introduced topology utilizes fewer switches to correspondence topologies. Minimization of switches reduces the requirement of gate driver circuits for switches and limits components count per level factor F_{ccl} hence reduce the complexity of the inverter. Fig. 28 represents the comparison result of the components count per level factor F_{ccl} to develop a seven-level output. From Fig. 28, the proposed topology utilizes fewer components count per level factor F_{ccl} in correlation with the different topologies.

C. COMPARISON STUDIES FOR 15 LEVEL MLI

Form Table VIII the number of power switches needed to produce 15-level staircase outputs for designed topology is less as considered with other topologies. Hence there is a reduction of gate driver circuits, so the ambiguousness of the inverter gets decreased. Considering that the components count per level factor F_{ccl} value is more; then the topology requires more components to build the desired voltage level thus in the recent investigations, the primary objective is to decrease components count per level factor in the design of multilevel inverter. It is noticed that from Table VIII the proposed MLI is having fewer components count per level factor F_{ccl} as related to other nine-level multilevel inverter topologies. Fig. 4 presents the comparison of the number of switches requires producing 15-level output voltage steps. From Fig. 26, the introduced topology utilizes fewer switches to correspondence topologies. Minimization of switches reduces the requirement of gate driver circuits for switches and limits components count per level factor

TABLE 7. The variance of variant 7 level MLI topologies with regards number of output levels.

Components required	CHB	NPC	FC	[37]	Proposed
Number of switches (Ns)	12	12	12	12	10
Number of diodes (Nd)	12	12	12	15	10
Dc link capacitors (Ncap)	3	6	6	6	0
Dc sources (n)	3	1	1	3	3
Number of other components (nx)	0	0	0	7	0
Number of driver board circuits (Ndk)	12	12	12	12	10
Components count per level (Fccl)	6	6.14	6.14	7.85	4.71

TABLE 8. The variance of variant 15 level MLI topologies with regards number of output levels.

Components required	FC	NPC	[38]	CHB	Proposed
Number of switches (Ns)	28	28	28	28	16
Number of diodes (Nd)	28	28	28	28	16
Dc link capacitors (Ncap)	14	14	0	7	0
Dc sources (n)	1	1	7	7	7
Number of driver board circuits (Ndk)	28	28	28	28	16
Components count per level (Fccl)	6.6	6.6	6.06	6.53	3.66

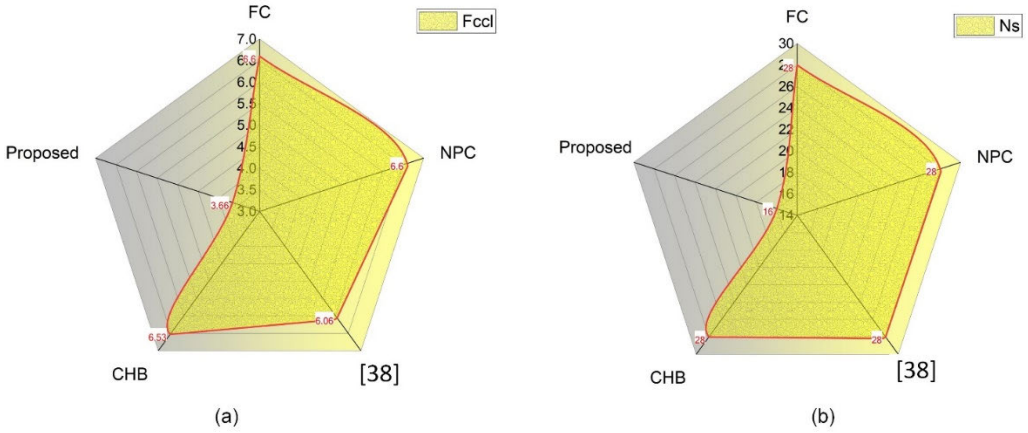

FIGURE 26. (a) Comparison of components count per level of proposed MLI with other topologies. (b) Comparison of Number of Switches to the proposed MLI with other topologies.

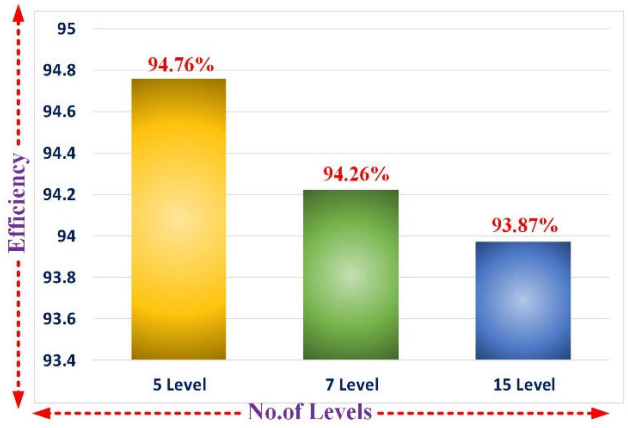

FIGURE 27. Efficiency for various MLI.

F_{ccl} hence reduce the complexity of the inverter. Fig. 26 represents the comparison result of the components count per level factor F_{ccl} to develop a 15-level output. From Fig. 26, the proposed topology utilizes fewer components count per level factor F_{ccl} in correlated with the different topologies.

Therefore, the power losses and efficiency are calculated from equations 28 and 29. The total losses of five, seven and fifteen level MLI are 44.12W, 49.05W and 77.6W respectively, which includes conduction losses of 44.072W, 48.96W and 77W and switching losses of 0.054W, 0.088W and 0.315W respectively. The efficiencies of five, seven and fifteen level MLI are calculated as 94.76%, 94.26% and 93.87% respectively and represented in Fig. 27.

VII. CONCLUSION

The hybrid cascaded multilevel inverters with five, seven and fifteen levels with PEMFC powered systems are developed mathematically with simulation and experimental verification. A new control strategy, an adaptive neuro-fuzzy interference system (ANFIS) is implemented for the boost converter with which the output is accurate with the learning ability of the controller and is designed and realized. Efficiency and power loss for each multilevel inverter are calculated mathematically. The proposed topology gives good results in the reduction of power switching components, THD, driver circuits, stress on the devices and switching losses compared

with the other topologies of multilevel inverters and generalized representation of these factors is illustrated. Simulation of boost converter for PEMFC input is presented to regulate the fuel flow input to meet the desired output voltage with proper care on the transients occurring in the fuel stack. Single-phase multilevel inverters with hardware prototypes of five, seven, and fifteen levels and a boost converter with a fuel cell input are developed. The hardware results under dynamic loads are validated. To test the robustness of the proposed topology load disturbance test is conducted and observed that it is well stabilized for these conditions. Five, seven, and fifteen level MLI are compared with various existing topologies and provide many advantages in various factors in the design of MLI. The proposed topologies provide efficient results with a fuel cell stack.

REFERENCES

[1] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm with switching state redundancy," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 792–804, Mar. 2009.
[2] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
[4] J.-S. Lai and F. Zheng Peng, "Multilevel converters–A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, Jun. 1996.
[5] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. Ángeles MartÌn Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
[6] Wu, Jinn-Chang, "Diode-clamped multilevel power converter with a zero-sequence current loop for three-phase three-wire hybrid power filter," *Electr. Power Syst. Res.*, vol. 81, no. 2, pp. 263–270, 2011.
[7] S. S. Wale and S. K. Patil, "A developed single phase cascaded multilevel inverter with reduced number of power switches," in *Proc. 2nd Int. Conf. Electr., Comput. Commun. Technol. (ICECCT)*, Feb. 2017, pp. 1–5.
[8] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on Neutral-Point-Clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
[9] Carmo, Marcelo, "A comprehensive review on PEM water electrolysis," International journal of hydrogen energy vol. 38.12, no. 2013, pp. 4901–4934.
[10] D. Guilbert, S. M. Collura, and A. Scipioni, "DC/DC converter topologies for electrolyzers: State-of-the-art and remaining key issues," *Int. J. Hydrogen Energy*, vol. 42, no. 38, pp. 23966–23985, Sep. 2017.
[11] J. E. Valdez-Resendiz, V. M. Sanchez, J. C. Rosas-Caro, J. C. Mayo-Maldonado, J. M. Sierra, and R. Barbosa, "Continuous input-current buck-boost DC-DC converter for PEM fuel cell applications," *Int. J. Hydrogen Energy*, vol. 42, no. 51, pp. 30389–30399, Dec. 2017.
[12] K. Jyotheeswara Reddy and S. Natarajan, "Energy sources and multi-input DC-DC converters used in hybrid electric vehicle applications – a review," *Int. J. Hydrogen Energy*, vol. 43, no. 36, pp. 17387–17408, Sep. 2018.
[13] D. Gao, Z. Jin, J. Zhang, J. Li, and M. Ouyang, "Development and performance analysis of a hybrid fuel cell/battery bus with an axle integrated electric motor drive system," *Int. J. Hydrogen Energy*, vol. 41, no. 2, pp. 1161–1169, Jan. 2016.
[14] R. O'hayre, *Fuel Cell Fundamentals*. Hoboken, NJ, USA: Wiley, 2016.
[15] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922–929, Feb. 2015.
[16] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-Bridge," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3932–3939, Aug. 2014.
[17] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.
[18] C. Dhanamjayulu and S. Meikandasivam, "Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads," *IEEE Access*, vol. 6, pp. 738–746, 2018.
[19] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Electr. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.
[20] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.
[21] A. Saadi, M. Becherif, D. Hissel, and H. S. Ramadan, "Dynamic modeling and experimental analysis of PEMFCs: A comparative study," *Int. J. Hydrogen Energy*, vol. 42, no. 2, pp. 1544–1557, Jan. 2017.
[22] Harrag, Abdelghani, and Hamza Bahri, "Novel neural network IC-based variable step size fuel cell MPPT controller: Performance, efficiency and lifetime improvement," *Int. J. Hydrogen Energy* vol. 42, no. 5, pp. 3549–3563, 2017.
[23] A. S. Samosir and A. H. M. Yatim, "Dynamic evolution control of bidirectional DC-DC converter for interfacing ultracapacitor energy storage to Fuel Cell Electric Vehicle system," in *Proc. Australas. Univ. Power Eng. Conf.*, 2008, pp. 1–5.
[24] S. Mekhilef, R. Saidur, and A. Safari, "Comparative study of different fuel cell technologies," *Renew. Sustain. Energy Rev.*, vol. 16, no. 1, pp. 981–989, Jan. 2012.
[25] O. Z. Sharaf and M. F. Orhan, "An overview of fuel cell technology: Fundamentals and applications," *Renew. Sustain. Energy Rev.*, vol. 32, pp. 810–853, Apr. 2014.
[26] D. Rekioua, S. Bensmail, and N. Bettar, "Development of hybrid photovoltaic-fuel cell system for stand-alone application," *Int. J. Hydrogen Energy*, vol. 39, no. 3, pp. 1604–1611, Jan. 2014.
[27] K. Jyotheeswara Reddy and N. Sudhakar, "High voltage gain interleaved boost converter with neural network based MPPT controller for fuel cell based electric vehicle applications," *IEEE Access*, vol. 6, pp. 3899–3908, 2018.
[28] A. Harrag and S. Messalti, "How fuzzy logic can improve PEM fuel cell MPPT performances?" *Int. J. Hydrogen Energy*, vol. 43, no. 1, pp. 537–550, Jan. 2018.
[29] Q. Niu, L. Zhang, and K. Li, "A biogeography-based optimization algorithm with mutation strategies for model parameter estimation of solar and fuel cells," *Energy Convers. Manage.*, vol. 86, pp. 1173–1185, Oct. 2014.
[30] M. Becherif and D. Hissel, "MPPT of a PEMFC based on air supply control of the motocompressor group," *Int. J. Hydrogen Energy*, vol. 35, no. 22, pp. 12521–12530, Nov. 2010.
[31] N. Benyahia, H. Denoun, M. Zaouia, T. Rekioua, and N. Benamrouche, "Power system simulation of fuel cell and supercapacitor based electric vehicle using an interleaving technique," *Int. J. Hydrogen Energy*, vol. 40, no. 45, pp. 15806–15814, Dec. 2015.
[32] T. Elmer, M. Worall, S. Wu, and S. B. Riffat, "Fuel cell technology for domestic built environment applications: State of-the-art review," *Renew. Sustain. Energy Rev.*, vol. 42, pp. 913–931, Feb. 2015.
[33] H. Tania, J. Patra, V. John, D. Elangovan, and G. Arunkumar, "Four level boost converter for linear loads," in *Emerging Trends in Electrical Communications and Information Technologies*. Singapore: Springer, 2017, pp. 369–376.
[34] K. J. Reddy and N. Sudhakar, "ANFIS-MPPT control algorithm for a PEMFC system used in electric vehicle applications," *Int. J. Hydrogen Energy*, vol. 44, no. 29, pp. 15355–15369, Jun. 2019.
[35] J. V. Missula, R. Adda, and P. Tripathya, "Pulse width modulation and SRF based closed-loop control of stand-alone single-phase 5L-ANPC inverter," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDES)*, Dec. 2018, pp. 1–5.
[36] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Convers. Manage.*, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.
[37] S. Birundha and V. Saravanan, "Design and development of z source cascaded seven level inverter for solar photovoltaic system," in *Proc. Int. Conf. Comput. Power, Energy, Inf. Commun. (ICCPEIC)*, Apr. 2015, pp. 1–5.
[38] A. R. Beig, U. Kumar, and R. Y. V. T. Ranganathan, "A novel fifteen level inverter for photovoltaic power supply system," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf.*, 2004, pp. 1–5.

[39] C. Dhanamjayulu, "Design and implementation of a novel asymmetrical multilevel inverter optimal hardware components," *Int. Trans. Elect. Energy Syst.*, vol. 30, no. 2, 2020, Art. no. e12201.

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