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Common Mode Current Mitigation for Medium Voltage Half Bridge SiC Modules

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Keywords

≪Wide bandgap devices≫, ≪Silicon Carbide (SiC)≫, ≪EMC/EMI≫, ≪Noise≫, ≪New switching devices≫.

Abstract

Medium voltage 10 kV Silicon Carbide MOSFETs, introduce challenges regarding converter design. Very high rate of voltage change and capacitive couplings to for example cooling systems cause increased electromagnetic interference. The aim of this paper is to accurately model the capacitive coupling to a heat sink and experimentally validate the model. An analytic model of the heat sink is developed which is demonstrated to be in excellent agreement with experimental results. The experimental result validates the modelled heat sink network allowing engineers to choose a suitable grounding impedance to comply with the electromagnetic compatibility regulations.

Introduction

The emergent wide-band gap semiconductor devices, such as Silicon Carbide (SiC) MOSFETs introduce new opportunities for converter designers. Key advantages of SiC MOSFET are their low switching losses and medium voltage withstand capability [1]-[3].The low switching losses at medium voltage are obtained by achieving very fast switching. The focus of this paper is on the rate of change in voltage (dv/dt), which typically may reach 30 kV/µs [4]. This is an order of magnitude larger compared to Si IGBT. The combination of parasitic capacitancens, high dv/dt and grounding the heat sink introduces some challenges when building a medium voltage SiC converter in practice [7],[8]. The effect of the device and module parasitic capacitive coupling is therefore crucial to understand if the common mode currents need to be addressed to obtain reliable operation and compliance with the electromagnetic compatibility (EMC) regulations. Common mode currents are desired to be attenuated to prevent excessive stress on components and maintaining fidelity of control signals. Failing to do so early in the design phase could result in a need to reduce the dv/dt and as a consequence also reduce switching frequency and power rating of the converter. The half bridge parasitics are key parameters in the design phase to calculate the magnitude of common mode currents. The aim of this work is to address and analyse it. A double pulse test setup was built with the purpose of experimentally validating an impedance network model of the heat sink.

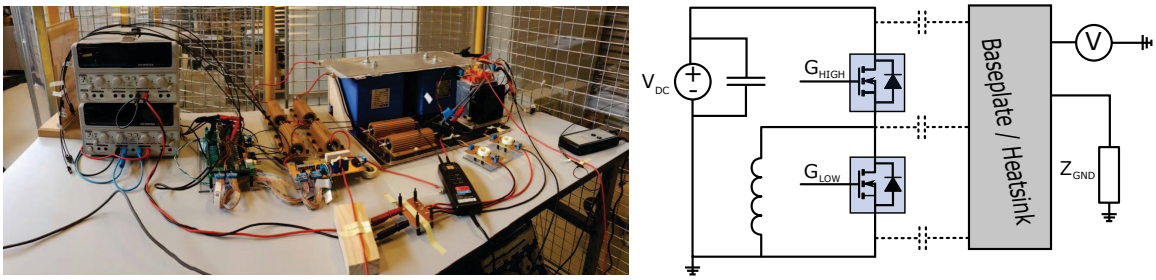

Fig. 1: Double pulse setup with half bridge module and grounded heat sink

Experimental and model details

The double pulse test setup and its schematic are shown in Fig 1.

The problem identification performed in this paper is focusing on a half bridge module with first generation 10 kV SiC MOSFETs and SiC JBS diodes. The specific half bridge module used is shown in Fig. 2 and was custom packaged at the Department of Energy Technology, Aalborg University. The parasitic

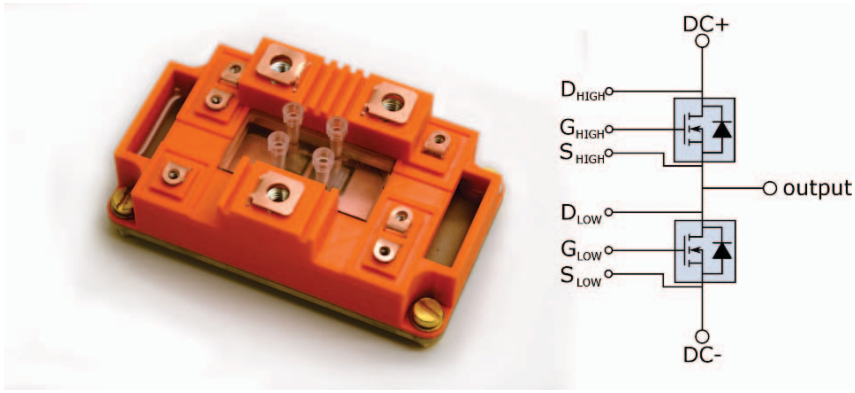

Fig. 2: Image and schematic of the half bridge power module consisting of 10 kV SiC MOSFETs and external SiC JBS diodes

capacitances of the module is listed in Table I. According to ANSYS Q3D, a capacitive coupling of 149 pF is present between the output of the half bridge module and the heat sink due to the layout and thickness of direct bonded copper (DBC) substrate.

A gate driver is required to drive the half bridge power module. A gate driver with low isolation capacitance of the isolating transformer was therefore developed for the experimental setup [5]. The gate driver is shown in Fig. 3.

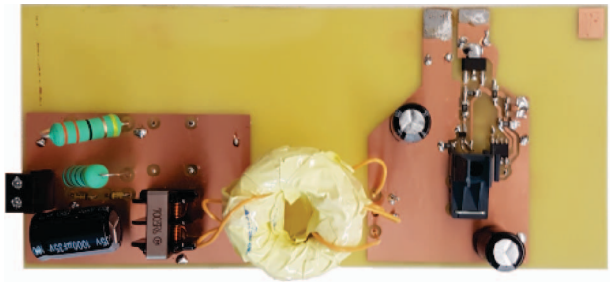

Fig. 3: Gate driver with active Miller clamping circuit for medium voltage SiC MOSFET

The isolation transformer has a coupling capacitance from primary to secondary of only 2.6 pF, attenuating the common mode currents flowing through the isolation boundary [6], ensuring fidelity in control

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signals. The capacitive coupling of the gate driver is neglected in this work due to its insignificant impact on achieving an accurate parasitic network representation of the heat sink.

Modelling of heat sink

With a given dv/dt the impact of external capacitive couplings on control signal fidelity and EMI is quantitatively analyzed. The parasitic network of the heat sink is displayed in Fig. 4 with values of parasitics presented in Table I. The stray inductance of the power module is not included in the analysis due to the relative low rate of current change and value of inductances contributing with a negligible voltage oscillation in the midpoint voltage compared to the medium voltage switching transient. The module parasitics were numerically simulated and extracted in [9] utilizing ANSYS Q3D on the module design. The simulated values were supplemented by external parasitics, obtained by measuring the impedance of the surrounding components using a Keysight E4990A impedance analyser.

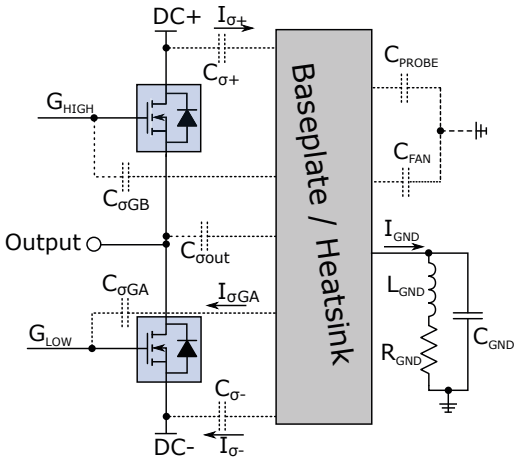

Fig. 4: Impedance network coupling the heat sink and half bridge power module

Table I: Parasitic parameter values for heat sink modelling

Parameter	Value	Determination
$C_{\sigma+}$	100.5 pF	ANSYS Q3D
$C_{\sigma GB}$	21.6 pF	...
$C_{\sigma out}$	149 pF	...
$C_{\sigma GA}$	18.7 pF	...
$C_{\sigma-}$	45 pF	...
C_{PROBE}	8 pF	Impedance analyser
C_{FAN}	80 pF	...
R_{GND}	235 Ω	...
L_{GND}	25 µH	...
C_{GND}	50 pF	...

A floating heat sink minimizes the current transfer from output to heat sink. The current returns as common mode current through the DC+ and DC- plane of the module. The DC+ and DC- common mode currents find their return path predominantly through the MOSFET's drain-source capacitance and the DC-link capacitor. The floating potential of the heat sink works as a medium voltage antenna and is a source of radiated EMI. If the heat sink is shorted to ground it is equivalent to inserting a snubber capacitance in parallel to the MOSFET's containing parasitic stray inductance as an effect of grounding the heat sink with a wire. The effect of shortening the heat sink to ground is an increase in inrush currents, and thereby an amplification of switching losses, and unintended high frequency current oscillation through the DC-link as common mode currents and to the gate of the MOSFET's. The effects are caused by the undamped resonance circuit consisting of the parasitic capacitances and the inductance of the heat sink grounding. To quantify this two selected grounding impedances are simulated using LTspice. In one case a stray inductance of 500 nH (L_{GND}) and a resistance of 0.5 Ω (R_{GND}) is inserted when shortening the heat sink to ground, which emulates a piece of grounding wire. The effect of inserting an inductance with low resistance is a high frequency resonance circuit with low damping factor as shown in Fig. 5. Allowing a parasitic high frequency resonant circuit is not desirable from an EMC or switching loss perspective. One solution is grounding the heat sink through a resistor, which dampens the oscillations. As an example a grounding impedance of 235 Ω is simulated as shown in Fig 5. The results shows a decrease in switching loss and a resonant circuit with a large damping, dampening the current oscillations to the DC potentials and the gate driver. The subscript of the current are referring to Fig. 4 representing the parasitic network. It is important to consider connected auxiliary equipment, such as a cooling fan and, the contribution to the parasitic network.

To choose a suitable grounding impedance, an analytical model has been developed based on Fig. 4 circuit and experimentally validated. When developing a small signal model for the heat sink, some

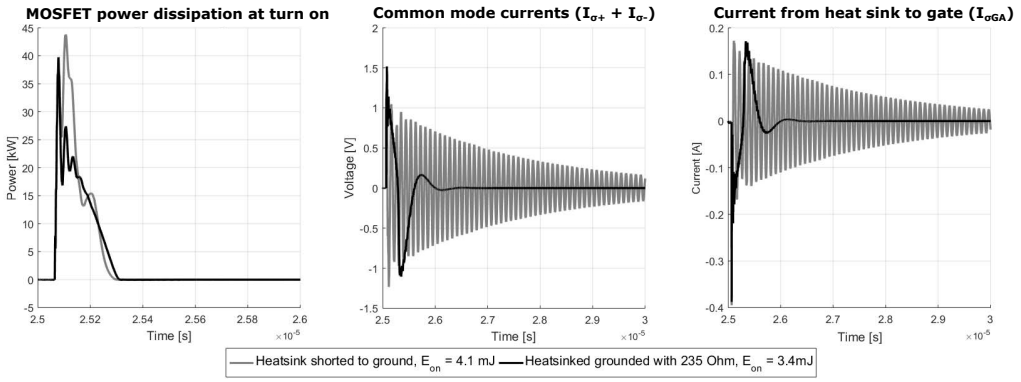

Fig. 5: Simulated effect of connecting the heat sink to ground with and without resistance

assumption are made. Since the signal of interest is in the MHz range, a 50 Hz voltage source supplying for example a cooling fan can be neglected in a small signal model. The impedances in Fig. 4 are combined into three equivalent impedances based on their connections and signals that are desired as outputs. Equation (1) is the impedance of the floating point to heat sink. (2) is from heat sink to the fixed potentials as DC+, DC- and ground. (3) is the impedance of the grounding connection of the heat sink.

$$\frac{1}{Z_1(s)} = \frac{(C_{\sigma out} + C_{\sigma GB}) \cdot s}{R_{EQ} \cdot (C_{\sigma out} + C_{\sigma GB}) \cdot s + 1} \tag{1}$$

$$\frac{1}{Z_2(s)} = \frac{(C_{\sigma+} + C_{\sigma-} + C_{\sigma GA} + C_{PROBE} + C_{FAN}) \cdot s}{R_{EQ} \cdot (C_{\sigma+} + C_{\sigma-} + C_{\sigma GA} + C_{PROBE} + C_{FAN}) \cdot s + 1} \tag{2}$$

$$Z_{GND}(s) = \frac{\frac{1}{C_{GND}} \cdot s + \frac{R_{GND}}{L_{GND} \cdot C_{GND}}}{s^2 + \frac{R_{GND}}{L_{GND}} \cdot s + \frac{1}{L_{GND} \cdot C_{GND}}} \tag{3}$$

Including the equivalent series resistance (ESR) of DC-link, R_{ds-on} of MOSFET's, resistance of connections would drastically increase the complexity of the model with limited impact. The impact will be small because the dominant part of the damping is being contributed by the heat sink resistor. An equivalent resistance representing all the other parasitic resistors apart from the heat sink grounding, is therefore chosen to be R_{EQ} = 5 mΩ to neglect it in the simulation and allowing parallel connection of parasitic capacitances. With the simplifications implemented, the equations can be converted into a simple block diagram structure for the heat sink voltage and currents. The block diagram is given in Fig. 6.

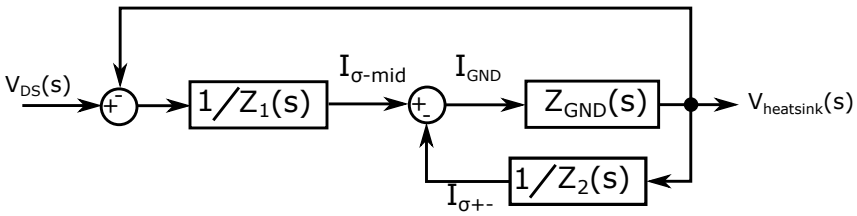

Fig. 6: Block diagram of the heat sink impedance network related to grounding (Z_{GND}) and power module (Z_1, Z_2).

$I_{\sigma-mid}$ is the current flowing through the DBC from the floating plane to the heat sink. The current $I_{\sigma+-}$ is the current conducted from the heat sink through the plane connected to DC+, DC−, C_{FAN} and C_{PROBE}, which is the common mode current flowing as an effect of the chosen grounding impedance. The I_{GND} is the current through the grounding impedance, usable for determining the power dissipation and choosing the ratings of the grounding impedance. The common mode current depends on the impedance network of the module, heat sink grounding as well as the dv/dt. The dv/dt should be limited due to the

Miller current flowing through the gate-drain capacitance C_{GD}. Due to the very high dv/dt, a large Miller current will be flowing through a MOSFET during its off state as a result of switching the complementary transistor in the half bridge module. The Miller current causes a voltage rise, potentially causing a false turn on even though a negative gate bias is applied. The controlling factors for the highest allowable dv/dt are V_{GS-th}, C_{GD}, C_{GS}, R_{G-INT}, L_{G-INT}. In order to quantify this, the voltage rise is analysed using the model shown in Fig. 7.

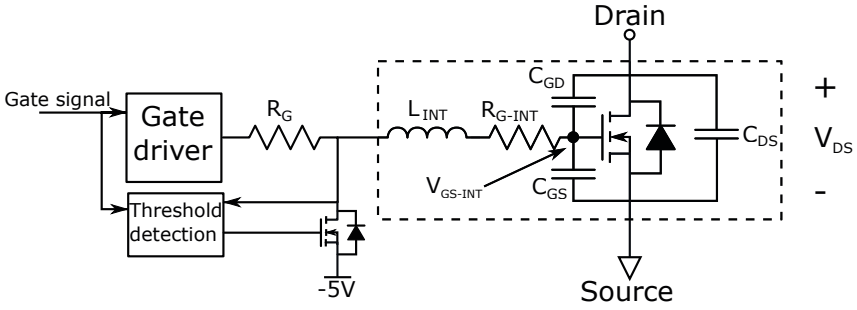

Fig. 7: Model of SiC MOSFET and gate driver circuit with active Miller clamp

The method of calculating Miller current is well documented in [10] and [11]. The purpose of mentioning it in this paper is to determine a dv/dt which prevents false turn on when considering safety margins, device parameters and their dependencies. Equation (4) describes the relationship between the imposed Drain-Source voltage (V_{DS}) and the rise of the internal gate voltage (V_{GS-INT}). The equation is used to determine a maximum $\mathrm{d}v_{DS}/\mathrm{dt}$ of 20 kV/µs when considering a safety margin for temperature dependency. The minimum value of external gate resistor is therefore chosen to comply with the upper limit of imposed $\mathrm{d}v_{DS}/\mathrm{dt}$.

$$\frac{V_{GS-INT}(s)}{V_{DS}(s)} = \frac{L_{INT}\cdot C_{GD}\cdot s^2 + C_{GD}\cdot(R_G + R_{G-INT})\cdot s}{1 + (R_G + R_{G-INT})\cdot(C_{GD} + C_{GS})\cdot s + L_{INT}\cdot(C_{GD} + C_{GS})\cdot s^2} \tag{4}$$

The safety margin of the dv/dt is imposed by the negative temperature coefficient of the threshold voltage. When the temperature increases, the threshold voltage decreases [12]. A clear requirement of a Miller clamp and negative gate bias for high dv/dt operation is identified by the simulation performed with (4).

Experimental results

In Fig. 8 a test at a DC-link voltage of 5 kV is presented, comparing output voltage and heat sink voltage of the experimental results to the simulation results. The purpose of comparing is to evaluate on the correlation between simulation and experiment. The measurements are performed with a Teledyne Lecroy PPE 6 kV high voltage probe and a CP030 current probe. The probes have a bandwidth of 400 MHz and 50 MHz, respectively.

Fig. 8 shows a close correlation between measured heat sink voltage and the response simulated using the model in Fig. 6. Excellent agreement is present in regards to amplitude, damping and oscillation frequency. The damping introduced to the system is dominated by the grounding resistor, which is implemented by a LCR circuit matching its measured frequency response. To corroborate the validity of the model it was also tested at different voltages. As an example measurements at 3.5 kV are shown in Fig. 9.

General for the simulated current through the impedance network I_{GND} is a rapid increase at 0.1 µs and decrease at 0.3 µs which diverges from the experimental results by an offset. The deviation is a result of the circuit representation for the grounding impedance. The grounding impedance is represented by a resistor and an inductor in parallel with a capacitor. Better agreement can be obtained if a more detailed representation of the grounding impedance is chosen.

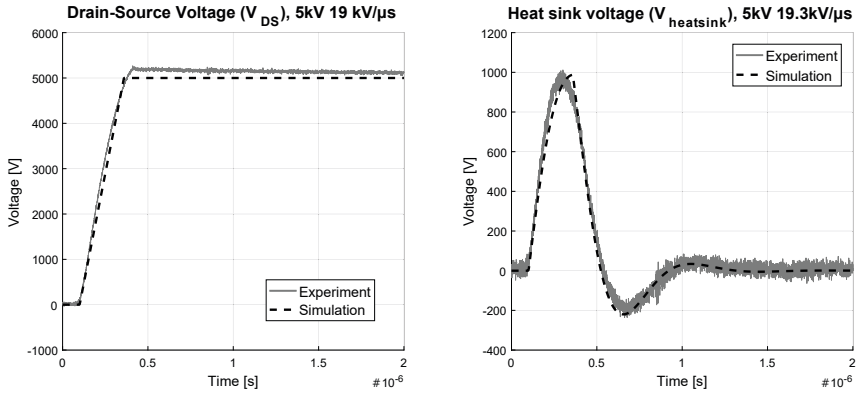

Fig. 8: Comparison between simulation and experiment results at 5 kV with 19 kV/µs.

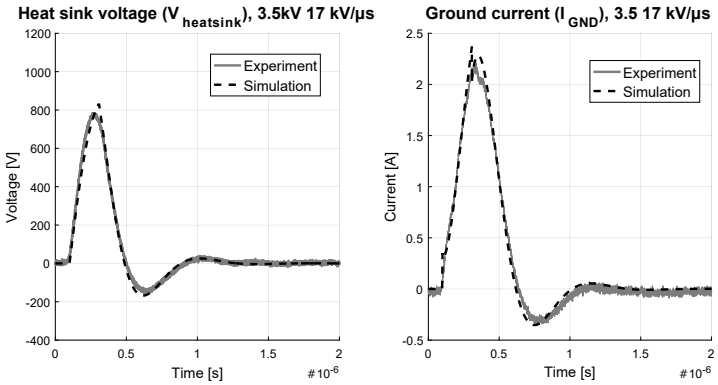

Fig. 9: Comparison between simulation and experimental results at 3.5 kV with 17 $kV/\mu s$.

The time period of oscillation is significantly affected by the capacitor values connected to the heat sink. The sensitivity to changes in capacitance values is demonstrated by removing the 80 pF and 8 pF of coupling capacitance contributed by the fan and probe, respectively. The responses with and without auxiliary capacitances are shown in Fig. 10.

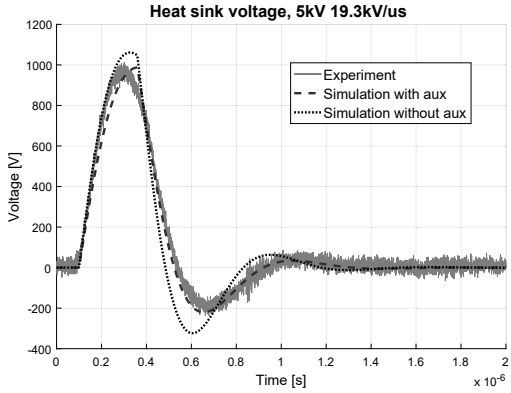

Fig. 10: The effect of omitting the auxiliary connected capacitances contributed by the fan and voltage probe.

Table II: Effect on heat sink voltage of an increase in capacitance with the subscript referring to the impedance transfer function

$$C_1 = C_{\sigma-} + C_{\sigma GA}$$
$$C_2 = C_{\sigma+} + C_{\sigma-} + C_{\sigma GA} + C_{PROBE} + C_{FAN}$$

Parameter	Amplitude	Period
$C_1 \uparrow$	$\uparrow$	$\uparrow$
$C_2 \uparrow$	$\downarrow$	$\uparrow$

By comparing the response in Fig. 10 it is clearly visible that omitting the fan and probe capacitances decreases the time period of the ringing and increases the amplitude, causing the simulation result to deviate from the measured response. The parameter sensitivity of the response verifies a high accuracy of the modelled impedance network for the heat sink. Combined with the excellent agreement between experimental results and impedance network in amplitude, frequency and dampening at all voltage levels tested, the usefulness of the model is validated. It demonstrates clearly the ability to determine the

common mode currents flowing through the heat sink to the DC-link, the ground current and the effect on the gate driver circuit.

With the model accuracy validated the impedance network can be used to explore the effects of a parasitic capacitance increase on the heat sink voltage. The qualitative relationships are given in Table II. The reduction of C_2 will reduce the ringing period and diminish the duration of noise. The penalty of reducing the capacitance will be an increase in heat sink voltage. A reduction of C_1 and C_2 will significantly reduce the ringing period and may also reduce the amplitude, depending on the relative distribution of their capacitance values.

Revised power module design

A new power module design with reduced capacitive couplings was developed [9] and experimentally tested. To reduce coupling capacitances, the area of the copper planes are reduced, with special focus on minimizing the area of the output plane, while monitoring the penalty in stray inductance and resistance introduced. The modification details in [9] are performed to the extend that manufacturing and parasitic penalties are at an acceptable level. The parasitics of the revised module are given in Table III. The revised module contains a never generation of SiC MOSFET dies, resulting in different dv/dt. The revised module was tested in a similar manner as in Fig. 1 and the heat sink voltage measured at 5 kV is presented in Fig. 11.

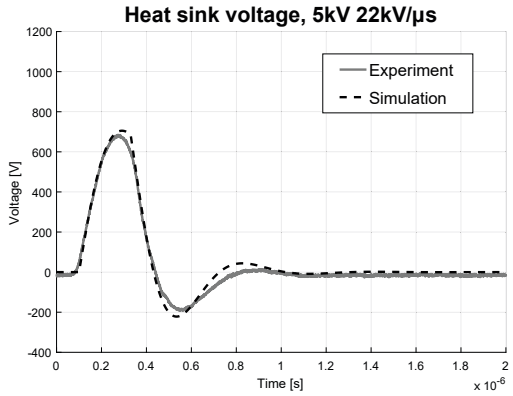

Fig. 11: Experimental test of the new generation of power module with reduced coupling capacitances to the baseplate.

Table III: Parasitic parameter values for the new generation of power module.

Parameter	Value	Determination
$C_{\sigma+}$	63.3 pF	Ansys Q3D
$C_{\sigma GB}$	11 pF	...
$C_{\sigma out}$	74.5 pF	...
$C_{\sigma GA}$	33.4 pF	...
$C_{\sigma-}$	33.4 pF	...
C_{PROBE}	8 pF	Impedance analyser
$C_{FAN-spaced}$	2.6 pF	...
R_{GND}	276 Ω	...
L_{GND}	25 µH	...
C_{GND}	50 pF	...

As can be seen in Fig. 11 good agreement is observed between measurement and simulation. Because of the reduction of the capacitance, the ringing period is reduced from 777 ns to 605 ns. The voltage amplitude is also reduced from 1000 V to 685 V with a grounding resistance of 276 Ω (R_{GND}), which is higher compared to the previous experiment. The duration and magnitude of the heat sink voltage oscillation is therefore effectively attenuated by reduced parasitic capacitances in the revised module design.

The validation of Table II and the heat sink model enables an experimental determination of the combined capacitance for (1) and (2) respectively by fitting the response of the heat sink voltage. The experimental determination of the parasitic coupling capacitances will only provide the capacitance sum (C_1 and C_2), thus some detail is not obtained. But the experimental determination of the coupling capacitance provides an alternative to a finite element method (FEM) software. An experimental determination will also include the auxiliary equipment which might be unknown prior to the construction of an initial prototype, and which may not be included in the software. It can also help, to identify parasitic effects of auxiliary equipment.

A double pulse test with a power module attached to a heat sink can then be used to determine switching losses and the capacitive coupling. The measurement requires a grounding impedance and an additional

voltage probe. By using the experimentally obtained information an accurate impedance model of the ground currents introduced by the heat sink can be developed.

Conclusion

The modelled heat sink voltage and current response shows excellent agreement with the experimental measurements, validating the presented understanding of the parasitic heat sink network. The impedance network can be used to accurately model the conducted EMI produced by the parasitic couplings to the heat sink. It also allows the designer to identify critical parameters and to choose a grounding impedance, that is beneficial in achieving compliance with EMC regulations. A preliminary double pulse test of a power module can be utilized to experimentally obtain an impedance network omitting the need of a finite element method simulation.

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