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A Mitigation Strategy for the Short-Circuit Degradation in SiC MOSFETs

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***Abstract*—The demand for highly reliable SiC MOSFETs is growing in the field applications, especially considering the short-circuit conditions. With the development of faster protection, short-circuit faults may occur many times within its expected service life, which only causes short-circuit degradation, rather than destructive failure. Based on finite element method simulation and experimental waveforms, this paper investigates the thermal and mechanical behavior of SiC MOSFET during short-circuit conditions, aiming to propose a package-level strategy to mitigate this short-circuit degradation and the results indicate that the front package design with sintered copper foil could be an effective approach.**

Keywords—Silicon Carbide (SiC), power MOSFET, short circuit, reliability, simulation, package

I. Introduction

Silicon Carbide (SiC) MOSFETs have emerged into the industrial market, offering promising performance compared to the Si counterparts, especially for the power electronics applications from 650 V to 1700 V [1]. Considering the safety-critical applications, such as electrical vehicles, uninterruptible power supplies, the robustness and reliability of SiC MOSFETs attract extensively concern, particularly short-circuit conditions [2].

At present, the state-of-the-art commercial SiC MOSFETs still have weaker short-circuit capability than Si IGBTs due to the smaller chip size and higher power density [3] and two separate failure mechanisms have been investigated, i.e. thermal runaway and gate dielectric breakdown [4]. The former one occurs several microseconds after the device turns off and it is mainly caused by the thermally-generated drain leakage current in the depletion region [5]. The latter one is newly found in SiC MOSFETs and it manifests as a short circuit between gate and source terminals as a consequence of damages in the gate structure [6]. The larger switch-off gate voltage and thicker gate oxide could be the approach to enhance the short-circuit capability [7].

On the other hand, the achievement of faster short-circuit detection techniques enables to limit the short-circuit pulse time duration below short-circuit capability and thereby avoid device destruction [8]. In this case, the device may withstand many times short-circuit events along within its expected service life, and the degradation induced by non-destructive short circuits is still inevitable, showing as increased gate leakage current and higher on-state resistance, which affects the long-term reliable operation of SiC MOSFETs [9]. Therefore, a reasonable approach to mitigate this degradation effect needs to be investigated.

Considering very fast temperature transient, the thermal measurement cannot be easily approached during short-circuit conditions, thereby, many works have been devoted to simulating the thermal behavior of SiC MOSFETs under short-circuit conditions [10]. Since the heat flux diffuses for a limited distance towards the substrate, the backside packaging material and external cooling system have little impact on the short-circuit capability [5]. Although increasing the heat capacity at the front side of the chip (e.g. thick copper metallization) has been used to improve the short-circuit capability in Si IGBTs [11], its influence on the SiC MOSFET is not fully understood due to the unique gate reliability issues. This paper investigates the impact of die top connection on the short-circuit degradation of SiC MOSFETs.

II. Short-Circuit Degradation

In this section, the degradation under short-circuit stress is described to ensure the proper simulation model. Repetitive short-circuit tests have been performed on the SiC MOSFETs to evaluate the variation of electrical characteristics [12]. As the number of repetitions increases, the on-state gate-source voltage during short-circuit tests (V_{GS_on}) becomes lower than the output voltage of the gate driver, leading to the reduction in the drain current (I_D). This V_{GS_on} drop is strongly correlated to the increased gate leakage current (I_{GSS}), which has been verified through static characteristics measurement. Besides, the threshold voltage (V_{th}) shift and the increase in on-state resistance (R_{DS_on}) have also been observed after repetitive short-circuit tests.

Further analysis of the degraded devices reveals the underlying mechanisms. One is gate degradation, such as damages in poly-silicon, gate oxide, and SiO_2 dielectric. The Scanning Electron Microscope (SEM) image after Focused Ion Beam (FIB) process in Fig. 1 shows a SiO_2 dielectric crack after tests [13]. During the short-circuit period, the dissipated high energy increases the internal temperature significantly. The mechanical stress on the Al/SiO_2 interface induced by the

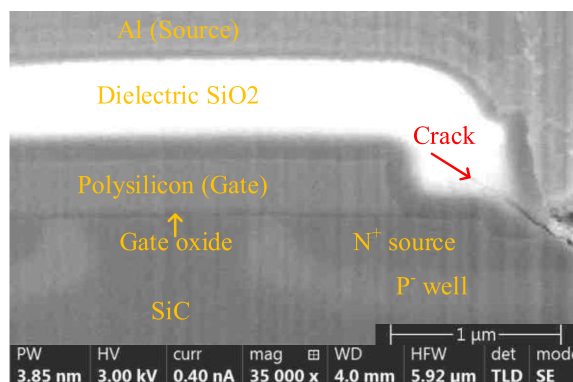

Fig. 1. Cross-sectional SEM image of the damaged cell. The red arrow identifies the SiO_2 dielectric crack [13].

Coefficient of Thermal Expansion (CTE) mismatch may exceed its limits and cause the crack. Meanwhile, the maximum temperature in the metallization layer might be higher than 1000 K based on the TCAD simulation [10]. In this case, the molten metal may flow through the crack [14] and form a conductive path between the gate and source terminal, showing as the I_{GSS} increase. The other one is Al metallization reconstruction. As pointed out above, the high temperature in the metallization layer could result in large voids due to the local heating and the R_{DS_on} further increase [15].

III. Approach and Simulation Model

The discrete 1000-V / 22-A SiC MOSFET with 3rd generation planar technology from CREE is used as a reference and a 2-D cell-level Finite Element Method model is built in COMSOL Multiphysics. To ensure an accurate simulation, the geometry of the gate structure is measured by the SEM image from [13]. Fig. 2 (a) shows the schematic of the structure and it is encapsulated in conventional TO-247 packaging design. For comparison, another model is built with the same size, but a 50 µm copper foil is sintered on top of the die surface metallization, which is similar to the Danfoss Bond Buffer technology [16], as shown in Fig. 2 (b) and the sintered layer has a thickness of 20 µm.

The physical density, thermal conductivity, and specific heat of SiC material are listed as (1) – (3) [17]. The thermal properties of the other materials are summarized in Table I [18]. Table II provides the mechanical properties of the materials [19].

$$\rho_{\mathrm{SiC}} = 3.211\ (\mathrm{g/cm^3}) \quad (1)$$

$$\lambda(T)_{\mathrm{SiC}} = (0.0003 + 1.05 \times 10^{-5}T)^{-1}\ \ (\mathrm{W/m \cdot K}) \quad (2)$$

$$c(T)_{\mathrm{SiC}} = 925.65 + 0.3772T - 7.929 \times 10^{-5}T^2 - 3.1946 \times 10^7/T^2\ (\mathrm{J/kg \cdot K}) \quad (3)$$

The top side of the epoxy resin material and the bottom side of the solder layer are set to the fixed temperature boundary condition (which is equal to 25 ºC). At the same time, the bottom side is applied as the fixed constraint boundary condition. To ensure inputting a realistic short-circuit energy, the experimental short-circuit tests have been performed to the same device with 2.2 µs pulse time duration at 25 ºC case temperature. The SiC drift region is set as the heat source, whose value $Q(t)$ is derived from the drain-source voltage V_{DS} and drain current I_D waveforms, as presented in Fig. 3. To be specific, the actual active area factor of the die, A can be calculated first by (4), which has a unit of 1. Then the heat source $Q(t)$ can be expressed as (5). Where S_H is the size of the heat source area, D represents the depth of the model, which is set to 1 µm by default, S_T is the total active area of

TABLE I. Thermal Properties of the Materials

Material	Density	Thermal conductivity	Specific heat
	kg/m3	*W/(m·K)*	*J/(kg·K)*
Epoxy Resin	1250	0.3	900
Copper Foil	8700	400	385
Sintered Silver	9500	170	200
Aluminum	2700	$239 \times f(T)$ [18]	910
SiO_2	2200	1.4	730
Polysilicon	2320	$(-2.2\times10^{-11}\times T^3 + 9\times10^{-8}\times T^2 - 1\times10^{-5}\times T + 0.014)^{-1}$	678
Solder	7400	60	160

TABLE II. Mechanical Properties of the Materials

Material	CTE	Young's modulus	Poisson's ratio
	$\times10^{-6}$ 1/K	*GPa*	*1*
Epoxy Resin	24	17	0.3
Copper Foil	17	110	0.35
Sintered Silver	19.75	12 ~ 32	0.3
Aluminum	23.2	70.3	0.346
SiO_2	0.5	75	0.17
Polysilicon	2.8	169	0.22
SiC	4.3	500	0.157
Solder	28.7	13.79	0.35

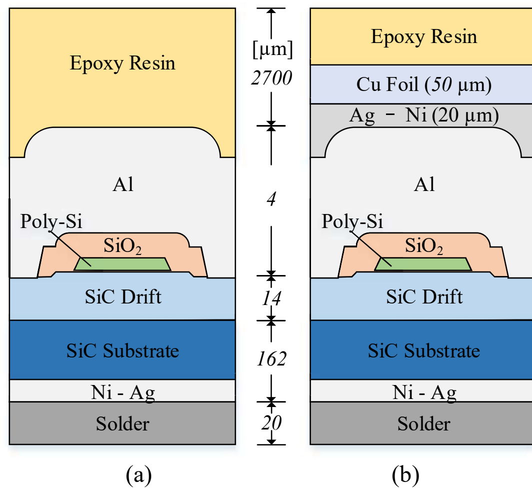

Fig. 2. Simulated structures (not to scale) (a) model 1: conventional package; (b) model 2: Ag sintered with Cu foil.

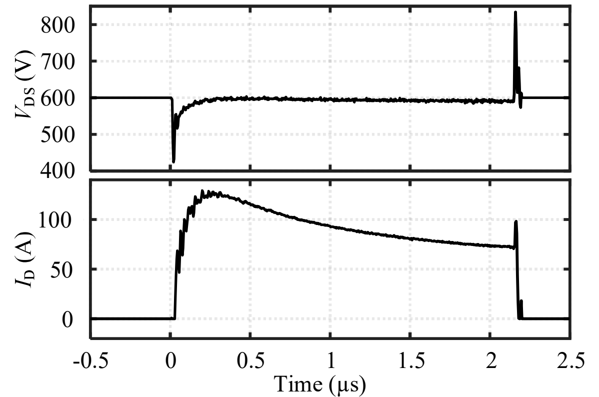

Fig. 3. Drain-source voltage (V_{DS}) and drain current (I_D) waveforms derived from the experimental short-circuit test.

the die, and W is the width of a single cell. Since the FEM model only includes a single cell width, its left and right side are set to symmetry for both thermal and mechanical boundary conditions.

$$Q = \frac{V_{DS}(t) \times I_D(t)}{A \times S_H \times D} \quad (W/m^3) \tag{4}$$

$$A = \frac{S_T}{W \times D} \quad (1) \tag{5}$$

Then, the transient thermo-mechanical simulation is performed from 0 µs to 5 µs in the step of 4 ns. The heat transfers from the SiC drift region to the top and bottom side of the model. Due to thermal expansion, mechanical stress can be calculated.

IV. Results and Discussion

To evaluate the simulation results, the maximum temperature inside three different layers is considered, i.e. Al metallization region, SiO_2 region, and SiC drift region. Fig. 4 shows the maximum temperature evolution with time in both conventional package model, hereinafter referred to 'without Cu foil', and the model with Cu foil sintered, which is referred to 'with Cu foil'.

The Al region in the case with Cu foil shows a decrease of the maximum temperature at the end of the short-circuit pulse time, i.e. t = 2.2 µs (from 829 °C to 569 °C), which indicates that the Al metallization damage induced by high temperature can be mitigated. This means that the die top connection with Cu foil may play a role in two aspects of short-circuit degradation. One aspect is to mitigate the Al metallization reconstruction and reduce the R_{DS_on} increase caused by short-circuit events. The other aspect is to avoid the melting of Al, which could reduce the possibility of molten Al flowing into the SiO_2 dielectric cracks.

Since the maximum temperature of the Al region is still below its melting point, which is around 660 °C, the pulse time duration is increased in the step of 0.2 µs and its corresponding short circuit waveforms are used to update the applied heat source in the model. As can be seen in the blue dotted line in Fig. 5, the short-circuit pulse time duration can be increased from 2.2 µs to 2.8 µs.

Apart from the Al metallization region, the rise of the maximum temperature inside the SiO_2 and SiC drift region also reduce owing to the Cu foil. Since the thermal runaway failure mode might come from the non-negligible thermally-induced leakage current in the depletion region, the decreased maximum temperature could also improve the short-circuit capability. Furthermore, the temperature distribution at the end of the short-circuit pulse (t = 2.2 µs) of two models are compared, as shown in Fig. 6 (a) and (b), respectively. Fig. 7 presents the temperature distribution along with the 2-D cut line which is shown as the dotted line in Fig. 6.

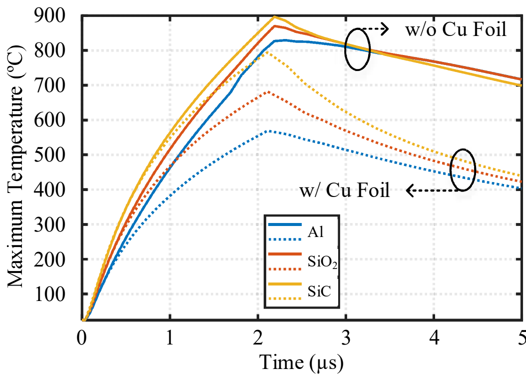

Fig. 4. Maximum temperature variation in Al, SiO_2, and SiC drift regions for the model with and without Cu foil.

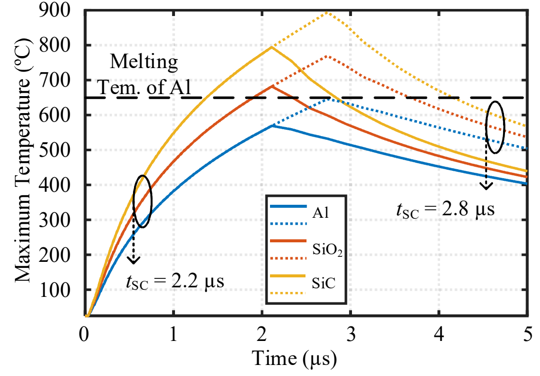

Fig. 5. Maximum temperature variation of Al, SiO_2, and SiC regions in the model with Cu foil and the short-circuit pulse time duration increase (from 2.2 µs to 2.8 µs).

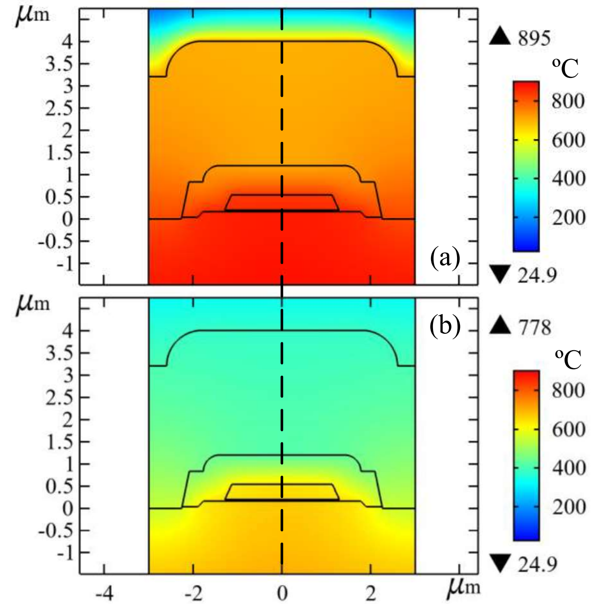

Fig. 6. Temperature distribution in the model (a) without and (b) with Cu foil.

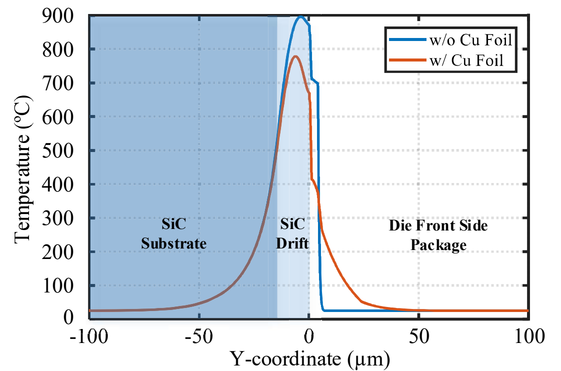

Fig. 7. Temperature distribution along with the 2-D cut line in the model without and with Cu foil.

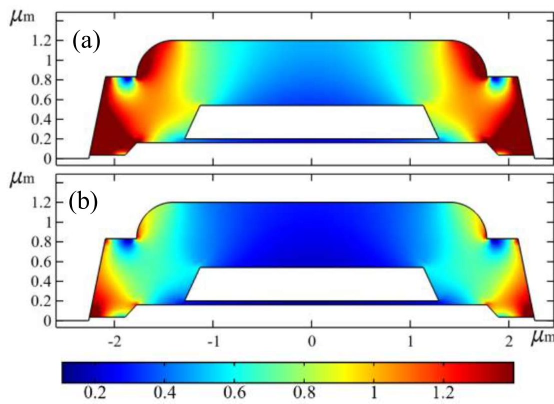

Fig. 8. Stress distribution within SiO_2 region: (a) without Cu foil; (b) with Cu foil.

Thanks to the lower temperature rise in the SiO_2 dielectric and Al metallization layer, the mechanical stress induced by the thermal expansion could be reduced in the model with Cu foil, compared to the model without Cu foil. The stress distribution within the SiO_2 dielectric region of both models is provided in Fig. 8 (a) and (b), respectively. Considering the strength limit for SiO_2 material is 1.4 GPa [14], it is worth noting that the crack location observed from the SEM image in Fig. 1 shows consistent with the location undergoing the highest stress in Fig. 8. Therefore, the SiO_2 crack risk caused by the CTE mismatch between Al and SiO_2 could be mitigated by applying the Cu foil.

V. Conclusions

In this paper, a 2-D FEM cell-level model of planar-gate SiC MOSFET is built and the transient thermo-mechanical FEM simulation is performed combined with the experimental waveforms. The impact of front side packaging on the short-circuit degradation is investigated by comparing two models. The simulation results indicate that the front packaging design with sintered thin copper foil can be an effective approach to mitigate this short-circuit degradation, mainly for two aspects: First, the Al metallization reconstruction could be extenuated due to its lower temperature rise. Second, the gate leakage current increase caused by the formed conductive path between gate and source could be decreased, which is achieved by reducing the stress on SiO_2 dielectric to mitigate the crack risk, and avoiding molten Al to flow through the crack.

Acknowledgment

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