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Analytical Modeling and Design of Capacitor Bank Considering Thermal Coupling Effect

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***Abstract*—The inevitable electro-thermal coupling among capacitors in a bank will lead to non-negligible errors to the temperature as well as the lifetime prediction of the individual capacitor. In this paper, the analytical thermal models with the corresponding design for capacitor banks are proposed considering the thermal coupling effect. Firstly, a measurement based lump thermal model and a physical model-based analytical thermal model are proposed. Then, with the help of the proposed thermal models, the design method for the thermal matching of capacitors in a bank is proposed by optimizing the parameters of individual capacitors, such as the rated parameters and actual loading. To validate the accuracy of the proposed design, case studies based on a capacitor bank with nine capacitors are presented.**

I. Introduction

Capacitors are widely used in power electronic converters to buffer the pulsating power, filter the harmonics, and support voltage for stable operation [1–3]. In some applications, they are also used to provide sufficient energy during the hold-up time [4, 5]. For these applications where a single capacitor can not fulfill the voltage rating or capacitance requirements, the capacitor bank is always used as the energy buffer by connecting several capacitors in parallel for larger capacitance or in series for higher voltage rating [6–8].

The design criteria of a capacitor bank depend on the applications and the user's requirements. For example, in the Photovoltaic (PV) applications, the minimum capacitance, maximum losses, and maximum volume are the essential factors should be considered [9, 10]. In power supply application, except for the factors mentioned above, the energy storage, differential-mode electromagnetic-interference level, and weight that should be considered [11, 12]. With more stringent constraints brought by automotive, aerospace, and energy industries, the design of capacitor bank encounters the reliability aspect challenges: a) capacitors are one kind of the stand-out components in terms of failure rate in field operation of power electronic systems [13–17]; b) constraints on volume and thermal dissipation of capacitors with the trends for high power density and high reliability capacitor banks [18–21]; c) cost reduction pressure from the global competition dictates the minimum design margin of capacitors without undue risk [22, 23].

In recent years, researchers and capacitor manufactures have devoted much effort to design for the reliability of capacitors in high-performance applications. From the research aspect, thermal modeling and lifetime prediction methods are proposed to obtain the health status of capacitors. For example, the physical structure of the capacitor is built to acquire the thermal model of capacitors [24–29]. Mission profile based evaluation method is proposed for lifetime prediction by accumulating damage from long-term loading profile [13, 30]. For reliability performance improvement, researchers propose the reliability-oriented capacitor sizing and derating design methods to release the electro-thermal stresses of the capacitors and fulfill different lifetime requirements [31, 32]. From the capacitor manufacturers aspect, different series products of capacitors (e.g. long lifetime series, downsize series, and cooling series) are provided by developing advanced material or packaging technologies [33]. By using the lower Equivalent Series Resistance (ESR), lower thermal resistance, or longer rated lifetime products, the thermal stress, as well as the failure rate, can be reduced.

All of these methods discussed above are effective and proposed for the single capacitor. But for capacitor bank, the direct application of the current methods can not bring the same benefit in the single capacitor, due to:

a) the capacitor bank is a system with multiple components, where the interactions among capacitors are existing. The thermal modeling methods in the literature assume the individual capacitor is standalone, so the temperature distribution is even in a symmetrical capacitor bank. It ignores the inevitable electro-thermal coupling effect among capacitors, which results in the estimation error on temperature and lifetime. In a real case, the electro-thermal interactions among capacitors will accelerate the degradation of partial capacitors in the middle and lead to more severe aging [25]. A few literature identified the uneven temperature distribution issue by using Finite Element Method (FEM) simulation and experimental testing [25, 29], but it is time-consuming. If the capacitors or layout of the capacitor bank are changed, the FEM model and testing setup need to be rebuilt, which consume more than tens of hours. In [34], the authors propose a thermal modeling method considering the thermal coupling effect, but the thermal model has to be implemented in the circuit simulator (e.g., PLECS, Simulink) to solve the nonlinear equations. It can not be integrated as a function into the model-based design and optimization. Therefore, the analytical

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thermal modeling method based on mathematical models is imperative;

b) In a typical capacitor bank implemented with the same capacitors and symmetrical layout, the uneven temperature distribution, as well as uneven lifetime distribution, is identified, due to partial capacitors in the middle have limited surface area to dissipate the heat. For these applications with partial capacitors aging severe, if all the capacitors in a bank apply the same derating design for longer lifetime, over-design will be seen from the other capacitors with less thermal stress. It would result in more material waste and higher costs. Different from a single capacitor, the capacitor bank has more than one design dimensions, such as the component rating, the stresses of individual capacitor, the layout of the capacitor bank, and so on. If these design dimensions can be utilized for optimization, it is possible to achieve higher reliability on the system-level with minimum extra cost.

Considering the electro-thermal coupling effect among capacitors, a lumped thermal model based on the measurement and a time-efficient analytical thermal model based on physical characteristics are proposed in this paper. Then, the design approach to achieve even temperature distribution is proposed by optimizing the rated parameters and the actual loading of the individual capacitor. Even though the part of results have already been presented in conference paper [35], it is worthwhile to have a comprehensive discussion on the modeling and optimization of the capacitor bank. Besides, new results are added including 1) a lumped thermal model for capacitor bank; 2) a circuit simulator based thermal model and its implementation for both string layout and rectangle layout; 3) a time-efficient analytical state-space thermal model for capacitor bank without the help of FEM simulation; and 4) thermal matching design case studies and benchmarking.

The rest of this paper is as follows: Section II discusses the existing evaluation and design method for capacitor banks and their challenges; Section III discusses the proposed thermal modeling method considering the thermal coupling effect; Based on the proposed thermal modeling method, Section IV proposes a thermal matching design for even temperature distribution; Section V validates the accuracy of the proposed modeling and design methods, followed by the discussions and conclusions.

II. Evaluation and Design Challenges of Capacitor Bank

This section presents the typical design and evaluation methods for capacitor bank. The design challenges and opportunities are discussed as follows.

A. Evaluation of Capacitor Bank

For a single capacitor, the hot-spot temperature is given as [13]

$$T_{\rm h} = T_{\rm a} + P_{\rm loss}(R_{\rm hc} + R_{\rm ca}) \tag{1}$$

where $T_{\rm h}$ is the hot-spot temperature, $T_{\rm a}$ is the ambient temperature, and $R_{\rm hc}$ and $R_{\rm ca}$ are the thermal resistances from hot-spot to case and from case to ambient, respectively. The ambient temperature $T_{\rm a}$ is measured at the initial condition before power injection to the capacitors, which depends on the global ambient temperature and heat transfer from other components around the capacitor bank. $P_{\rm loss}$ is the power loss of individual capacitor, which is estimated from ESR and capacitor current. Assuming there are two capacitors connected in parallel, the thermal model based on the extension of the single capacitor thermal model is shown in Fig. 1. $P_{\rm loss,i}$ and $P_{\rm loss,j}$, $T_{\rm h,i}$ and $T_{\rm h,j}$, and $T_{\rm c,i}$ and $T_{\rm c,j}$ are the power loss, hot-spot temperature, and case temperature of capacitor i and j, respectively. $R_{\rm hc,i}$ and $R_{\rm hc,j}$, $R_{\rm ca,i}$ and $R_{\rm ca,j}$ are the thermal resistances of capacitor i and j from the hot-spot to case and from case to ambient, respectively. Due to the thermal model of the individual capacitor in the existing literature is considered standalone, there is no heat transfer between the two capacitors. For the capacitor bank with the same capacitors connected in parallel, the temperature distribution is even from the existing evaluation method.

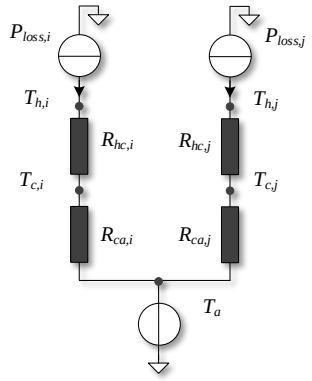

Fig. 1. Thermal model of a capacitor bank with two capacitors without consideration of thermal coupling effect.

The lifetime of capacitors can be derived from the following simplified model, which is popularly applied for electrolytic and film capacitors [13]:

$$L = L_0 \times (\frac{V}{V_0})^{-n} \times 2^{\frac{T_0 - T}{10}} \tag{2}$$

where L and L_0 are the lifetime under the using condition and testing condition, respectively. V and V_0 are the voltage at using condition and testing condition, respectively. T and T_0 are the temperature in Kelvin at using condition and testing condition, respectively. For electrolytic capacitors, the value of n typically varies from 3 to 5. For film capacitors, n is from around 7 to 9.4, which is used by leading capacitor manufacturers [1]. The application of the lifetime model results in fixed accumulated damage. It is far from reality since the capacitor parameter variations and the statistical properties of the lifetime model are not considered. In the field operations, the end-of-life of capacitors could vary within a range due to component parameter tolerances and differences in the experienced stresses. Therefore, a statistical approach based on Monte Carlo simulations is applied [13]. Finally, the distribution of the end-of-life of the capacitors can be obtained, allowing a lifetime analysis with a specified confidence level.

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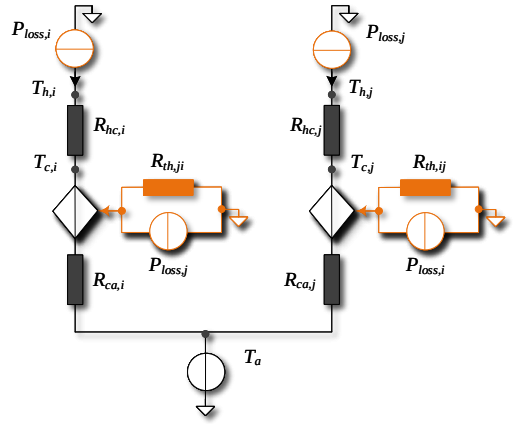

Fig. 2. The proposed lumped thermal model for a capacitor bank considering thermal coupling effect.

B. Challenges and Oppotunities

From the evaluation method presented above, it can be seen that the lifetime of the individual capacitor in a bank depends on the stresses of the capacitor itself, which ignores the heat transfer among the capacitors. When multiple capacitors are packaged in a bank, there will have heat flowing path among capacitors, which results in higher hot-spot temperature $T_{\mathrm{h,i}}$ and $T_{\mathrm{h,j}}$ as well as more severely aging. This phenomenon conflicts with the result obtained from the existing evaluation method in Section II.A., which should be modeled in a time-efficient way and considered in the design stage.

From the design aspect, all the rated parameters (e.g., L_0, T_0 and V_0) and actual stresses (e.g., T and V) in the lifetime model shown in (2) could be the design variables for the reliability of capacitor. It is possible to optimize these rated parameters or actual stresses of the individual component to achieve the even temperature in a bank, so that the lifetime of partial aging capacitors can be extended and better reliability performance on the system level can be obtained with the minimum extra cost.

III. Proposed Thermal Modeling Method Considering Thermal Coupling Effect

To acquire the even temperature distribution in a capacitor bank, two thermal models are proposed in this section considering the heat transfer among the capacitors: a lumped thermal model based on coefficients measurement, and an analytical thermal model based on the physical structure modeling.

A. A Lumped Thermal Model Based on Measurement

Based on the superposition theory, a lumped thermal model considering both the self-heating and thermal coupling effect in a capacitor bank is provided. Two capacitors i and j in a bank are taken as an example, which is shown in Fig. 2. The thermal coupling effects are represented by controlled voltage sources, which are added to the self-heating sources. The thermal coefficients of the lumped thermal model are extracted from the measurement in FEM simulation or experiment setup. $R_{\mathrm{hc,i}}$ and $R_{\mathrm{hc,j}}$ are the thermal resistances from hot-spot to case. $R_{\mathrm{ca,i}}$ and $R_{\mathrm{ca,j}}$ are the equivalent thermal resistances from case to ambient temperature. $R_{\mathrm{th_{ij}}}$ and $R_{\mathrm{th_{ji}}}$ are the equivalent thermal coupling resistances between capacitor i to j. Considering the self-heating and thermal coupling effects, the general lumped thermal model of the capacitor bank can be written in the matrix form as

$$\begin{bmatrix} T_{\mathrm{h},1} \\ T_{\mathrm{h},2} \\ \dots \\ T_{\mathrm{h,m}} \end{bmatrix} = \begin{bmatrix} R_{\mathrm{th}_{11}} & R_{\mathrm{th}_{12}} & \dots & R_{\mathrm{th}_{1\mathrm{n}}} \\ R_{\mathrm{th}_{21}} & R_{\mathrm{th}_{22}} & \dots & R_{\mathrm{th}_{2\mathrm{n}}} \\ & & \dots & \\ R_{\mathrm{th}_{\mathrm{m}1}} & R_{\mathrm{th}_{\mathrm{m}2}} & \dots & R_{\mathrm{th}_{\mathrm{mn}}} \end{bmatrix} \begin{bmatrix} P_{\mathrm{loss},1} \\ P_{\mathrm{loss},2} \\ \dots \\ P_{\mathrm{loss,n}} \end{bmatrix} + \begin{bmatrix} T_{\mathrm{a},1} \\ T_{\mathrm{a},2} \\ \dots \\ T_{\mathrm{a,m}} \end{bmatrix} \quad (3)$$

where $T_{\mathrm{h,m}}$, $T_{\mathrm{a,m}}$, $P_{\mathrm{loss,n}}$ are the hot-spot temperature, local ambient temperature, and power loss injection of individual capacitor, respectively. $R_{\mathrm{th_{mn}}}$ are the coupling thermal resistance between capacitors obtained from the measurement. In particular, $R_{\mathrm{th_{mn}}}$ $(m = n)$ is the self-heating thermal resistance from hot-spot to ambient. To extract these equivalent thermal resistances, a step power loss input is applied to each capacitor individually, and the temperature responses from the intended monitoring points are extracted. The methodology to find the thermal response of the capacitor bank is detailed in the following:

a) The geometry and material information of the capacitor bank are imported to or drawn in a FEM simulation tool;

b) A step response analysis is performed for all the capacitors, by applying the step current as well as the power loss to individual capacitor, respectively;

c) Measure the node temperature of interest, such as case temperature and hot-spot temperature. Identify the self-heating response of the individual capacitor and its thermal coupling effect to other capacitors;

d) The extracted temperature response is divided by the power loss of individual capacitor to calculate the thermal resistance or thermal impedance between two nodes. The thermal resistance and thermal impedance are given by

$$R_{\mathrm{th_{ab}}} = \frac{T_{\mathrm{a}} - T_{\mathrm{b}}}{P_{\mathrm{loss,i}}} \quad (4)$$

$$Z_{\mathrm{th_{ab}}}(t) = \frac{T_{\mathrm{a}}(t) - T_{\mathrm{b}}(t)}{P_{\mathrm{loss,i}}} \quad (5)$$

where T_{a} and T_{b} are the temperatures in two adjacent points and $P_{\mathrm{loss,i}}$ is the power loss of capacitor under testing.

B. An Analytical Thermal Model Based on Physical Modeling

To obtain the temperature distribution more time-efficient, an analytical model based on the physical structure modeling of the capacitor bank is provided. In this section, the basic diagram of the analytical thermal model is introduced at the beginning. Then, two solutions to obtain the steady-state temperature of the capacitor bank are provided, which are the circuit simulator-based method and state-space model-based method.

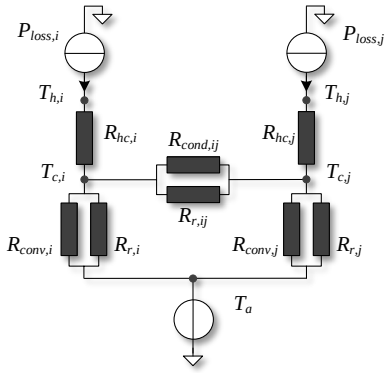

Fig. 3. The proposed analytical thermal model for capacitor bank considering thermal coupling effect.

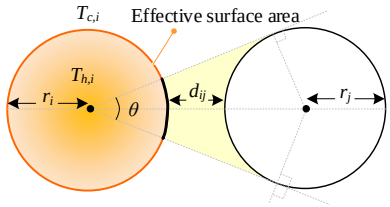

Fig. 4. Description of effective surface area for heat transfer between capacitors.

1) Structure Diagram of the Analytical Model: The diagram of the proposed analytical thermal model is shown in Fig. 3. For the individual capacitor, $R_{\mathrm{hc,i}}$ and $R_{\mathrm{hc,j}}$ are the thermal resistances from hot-spot to case, which are determined by the physical structure of capacitor and assumed constant in different operating conditions (e.g., electrical loading and thermal loading) and locations. $R_{\mathrm{conv,i}}$ and $R_{\mathrm{conv,j}}$ are the thermal resistances from case to ambient for convection heat transfer, which are loading conditions dependent. The thermal resistance of convection heat transfer can be written as

$$R_{\mathrm{conv}} = \frac{1}{h_{\mathrm{conv}} A_{\mathrm{effect}}} \tag{6}$$

h_{conv} is usually given as a function of ΔT, $h_{\mathrm{conv}} = 1.42\left(\frac{\Delta T}{H}\right)^{1/4}$, where ΔT is the temperature difference between two hot points T_{a} and T_{b}; H is the height of the capacitor. A_{effect} is the effective surface area for heat dissipation, which is a key parameter to estimate the transfer heat in a capacitor bank. For a single capacitor, all the surfaces are exposed in the ambient air, so that the effective surface area for heat convection is the whole surface. For the capacitor i in a bank with two capacitors, only a part of the surface is exposed in ambient air, while the other parts are faced to the capacitor j. The effective surface area is defined in Fig. 4, which can be written as

$$A_{\mathrm{effect}} = 2\pi r_{\mathrm{i}}^2 + 2\pi r_{\mathrm{i}} H - k\theta r_{\mathrm{i}} H \tag{7}$$

where k is the number of surrounding capacitors with heat exchange. A view factor θ is considered as a ratio to obtain the effective surface area from the lateral area, which can be written as

$$\theta = 2\arcsin\left(\frac{r_{\mathrm{j}}}{r_{\mathrm{i}} + d_{\mathrm{ij}} + r_{\mathrm{j}}}\right) \tag{8}$$

where r_{i} and r_{j} are the radius of the capacitor i and j, respectively. d_{ij} is the distance between capacitors.

Beside the convection heat transfer, radiation heat transfer is also considered as shown in Fig. 3. $R_{\mathrm{r,i}}$ and $R_{\mathrm{r,j}}$ are the thermal resistances for radiation heat transfer from case to ambient. The radiant energy exchange between a hot body with the absolute temperature T_{a} and an enclosing body with the absolute temperature T_{b} is proportional to the difference in the absolute temperatures to the fourth power

$$q = \varepsilon\sigma A_{\mathrm{effect}}(T_{\mathrm{a}}^4 - T_{\mathrm{b}}^4) \tag{9}$$

ε is the emissivity of the surface material. σ is the Stephan-Boltzman constant.

To represent the heat transfer among capacitors, a new path for heat transfer, which contains heat conduction and radiation thermal resistances connected in parallel from capacitor i to capacitor j, is considered in this thermal structure. $R_{\mathrm{cond,ij}}$ and $R_{\mathrm{r,ij}}$ are the thermal coupling resistances for conduction and radiation heat transfer through the air. The heat conduction can be described as

$$R_{\mathrm{cond}} = \frac{1}{h_{\mathrm{cond}} A_{\mathrm{coupling}}} \tag{10}$$

h_{cond} is the conduction heat transfer coefficient of the air. A_{coupling} is the coupling surface area between capacitors, which is

$$A_{\mathrm{coupling}} = \theta r_{\mathrm{i}} H \tag{11}$$

The radiation heat transfer between capacitors can be obtained from (9) with coupling surface area A_{coupling}.

From the above discussion, it can be seen that the thermal coefficients of the proposed thermal model are the node temperature and power loss dependent. Therefore, the fixed linear thermal resistances can not be used anymore. In order to solve the nonlinear model and obtain the steady-state temperature distribution, the circuit based method and state-space model-based method are proposed and discussed in the following two sections.

2) Circuit Based Method: Building the thermal model in circuit simulation (e.g., Simulink and PLECS) is an efficient way to represent the nonlinear thermal impedance and solve the nonlinear thermal model to obtain the steady-state temperature distribution. Due to the thermal coefficients for heat conduction, convection, and radiation in the proposed thermal model are nonlinear and temperature-dependent, the commonly used constant thermal resistor in the circuit simulation can not be used anymore. The proposed circuit based thermal model is shown in Fig. 5, which can be represented in two forms depending on the implementation of nonlinear thermal resistances. In Fig. 5(a), a current control voltage source is used to represent $R_{\mathrm{ca,i}}$ and $R_{\mathrm{ca,j}}$. Based on the power loss flowing through the nonlinear resistors, the case temperature can be calculated from the nonlinear equations in (6) and (9). The thermal coupling resistance $R_{\mathrm{th_{ij}}}$ $(i \neq j)$ is also temperature and power loss dependent, which should be a nonlinear resistor. The possible choices to represent the nonlinear resistors in the circuit simulation are the voltage control current source and current control voltage source. Due to $T_{\mathrm{c,i}}$ and $T_{\mathrm{c,j}}$ have already been represented by the

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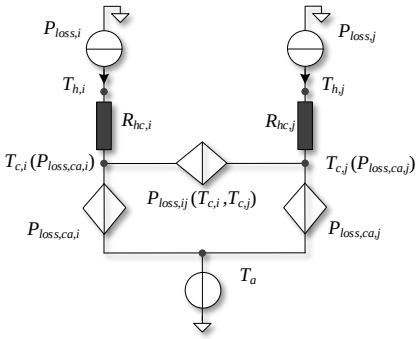
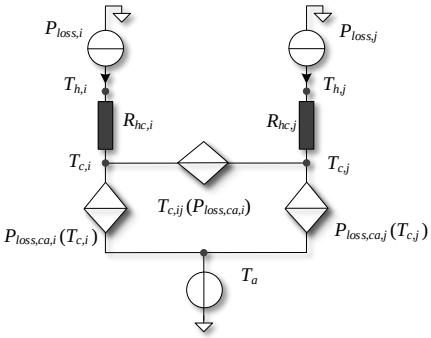
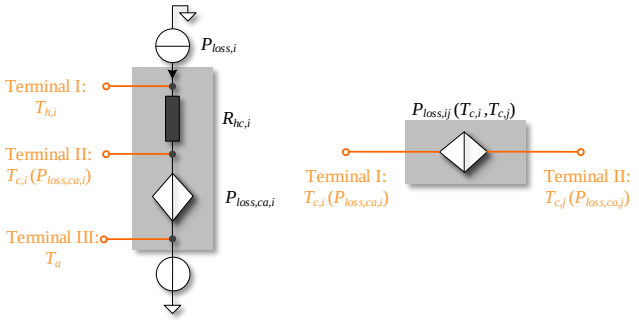


(a) Circuit based thermal model type I.



(b) Circuit based thermal model type II.

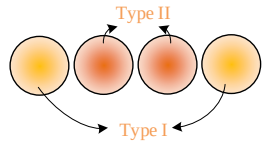
Fig. 5. Circuit based thermal models for capacitor bank by using controllable voltage source and current source to represent the nonlinear thermal resistances.



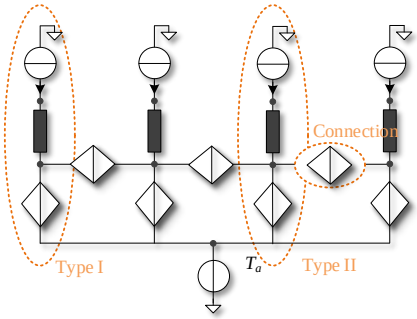
(a) Three-terminal thermal model for single capacitor.

(b) Two-terminal thermal model for thermal coupling connection.

Fig. 6. Basic modules of capacitors and connection to implement the circuit based thermal model in circuit simulation.

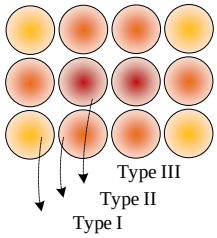


(a) Types of cell in thermal model for string layout.

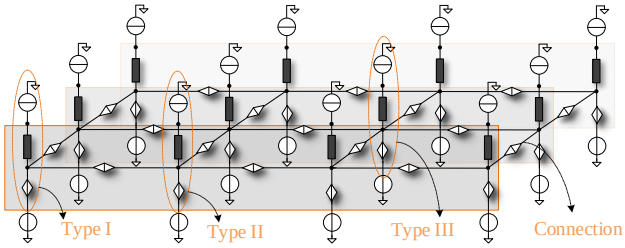


(b) Circuit based thermal model for string layout.

Fig. 7. Scalable circuit based thermal model for string layout capacitor bank.



(a) Types of cell in thermal model for rectangle layout.



(b) Circuit based thermal model for rectangle layout.

Fig. 8. Scalable circuit based thermal model for rectangle layout capacitor bank.

voltage source, the terminal temperatures of $R_{\mathrm{th_{ij}}}$ are clamped. Therefore, $R_{\mathrm{th_{ij}}}$ could only be a voltage control current source as shown in Fig. 5(a). On the other way, if the thermal resistances from case to ambient are represented by voltage control current sources as shown in Fig. 5(b), the transfer heat for self-heating of the individual capacitor, and the transfer heat among capacitors are determined. At this time, the thermal coupling resistances $R_{\mathrm{th_{ij}}}$ could only be a current control voltage source, as shown in Fig. 5(b). In the following discussion, the structure in Fig. 5(a) is taken as an example to study the implementation of a thermal model for the different layout of capacitor bank.

In circuit simulation, the thermal model of a single capacitor is packaged as a three-terminal module as shown in Fig. 6(a). It can extend for a capacitor bank by using multiple modules connected through a two-terminal thermal coupling resistor module as shown in Fig. 6(b). In different physical implementations, the basic simulation modules have different thermal coefficients depending on the locations and layout. For the string layout capacitor bank as shown in Fig. 7, three basic modules are packaged for the scalable implementation. The first two, Type I and Type II, are the thermal models of capacitors for the corner and middle locations as shown in Fig. 7(a). They have the same structure as the one in Fig. 5(a), but the effective surface area and the coupling surface area are different. The corner capacitor has one side faced to the neighbor capacitor, and the middle capacitor has two sides. The corresponding $A_{\mathrm{effective}}$ and A_{coupling} can be acquired from (7) and (11). The other basic module is the connection to represent the thermal coupling effect between capacitors from

case to case. By using these three basic modules, the thermal model of the string layout capacitor bank with different numbers of capacitors can be built as shown in Fig. 7(b). For the rectangle layout capacitor bank, four basic simulation modules to represent the thermal models are implemented as shown in Fig. 8(a). The corner capacitor, border capacitor, and middle capacitor have one side, three sides, and four sides faced to the neighbor capacitors, respectively, therefore, the coupling surface area should be updated accordingly. By using these capacitor modules and connection module, the thermal model of the rectangle layout capacitor bank with scalable numbers of capacitors can be built as shown in Fig. 8(b). After running the circuit simulation, the temperature distribution can be obtained.

3) State-space Model-based Method: The temperature distribution can also be described in the state-space thermal model and acquired from iterative computations, because the nonlinear thermal resistances need to be updated with instantaneous temperature. In this section, firstly, the state-space model for thermal dynamics is proposed. Then, the flowchart for iterations is provided to derive the steady-state temperature distribution.

For capacitor j, an energy balance equation can be built at the case temperature node, which is shown as

$$C_{\mathrm{th,j}}\frac{dT_{\mathrm{ca,j}}}{dt}=\sum_{\mathrm{i=1,i\neq j}}^{n}\frac{1}{R_{\mathrm{th_{i,j}}}}(T_{\mathrm{ca,i}}-T_{\mathrm{ca,j}})+P_{\mathrm{loss,j}} \quad (12)$$
$$(j=1,...,m)$$

where $P_{\mathrm{loss,j}}$ represents the heat injection related to the node. $T_{\mathrm{ca,j}}$ represents the case temperature. $R_{\mathrm{th_{i,j}}}$ represents the thermal resistance between cases. $C_{\mathrm{th,j}}$ represents the equivalent heat capacity of the node, which is ignored for the steady-state temperature estimation. For the capacitor bank with m order differential equations, the thermal dynamics of the case temperature can be expressed with a matrix representation,

$$\frac{dT}{dt}=AT+BU \quad (13)$$

where T represents the node temperatures from case to ambient. U represents the power loss injection. A and B represent the system matrices.

$$T=\begin{bmatrix}T_{\mathrm{ca,1}}\\T_{\mathrm{ca,2}}\\...\\T_{\mathrm{ca,m}}\end{bmatrix}\ U=\begin{bmatrix}P_{\mathrm{loss,1}}\\P_{\mathrm{loss,2}}\\...\\P_{\mathrm{loss,n}}\end{bmatrix}\ B=\begin{bmatrix}1&0&...&0\\0&1&...&0\\...&&&\\0&0&...&1\end{bmatrix} \quad (14)$$

$$A=\underbrace{\begin{bmatrix}-\frac{1}{R_{\mathrm{ca_{1,1}}}}&0&...&0\\0&-\frac{1}{R_{\mathrm{ca_{2,2}}}}&...&0\\...&...&...&...\\0&0&...&-\frac{1}{R_{\mathrm{ca_{m,n}}}}\end{bmatrix}}_{\mathrm{A_1:Self-heating}} \quad (15)$$

$$+\underbrace{\begin{bmatrix}-\sum_{\mathrm{j=1}}^{n}\frac{1}{R_{\mathrm{ca_{1,j}}}}&-\frac{1}{R_{\mathrm{ca_{1,2}}}}&\cdots&\frac{1}{R_{\mathrm{ca_{1,n}}}}\\-\frac{1}{R_{\mathrm{ca_{2,1}}}}&-\sum_{\mathrm{j=1}}^{n}\frac{1}{R_{\mathrm{ca_{2,j}}}}&\cdots&\frac{1}{R_{\mathrm{ca_{2,n}}}}\\...&...&...&...\\-\frac{1}{R_{\mathrm{ca_{m,1}}}}&-\frac{1}{R_{\mathrm{ca_{m,2}}}}&\cdots&-\sum_{\mathrm{j=1}}^{n}\frac{1}{R_{\mathrm{ca_{m,n}}}}\end{bmatrix}}_{\mathrm{A_2:Thermal-coupling}}$$

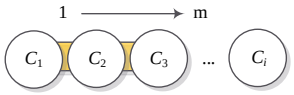


Fig. 9. Diagram of thermal coupling capacitors in string layout.

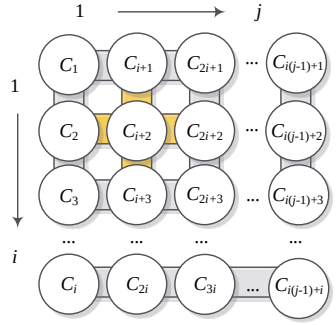


Fig. 10. Diagram of thermal coupling capacitors in rectangle layout.

where $R_{\mathrm{ca_{m,n}}}$ is the coupling thermal resistance between capacitors. In particular, $R_{\mathrm{ca_{m,n}}}$ $(m=n)$ is the self-heating thermal resistance from the case to ambient. The temperature distribution of the capacitor bank can be derived as

$$\begin{bmatrix}T_{\mathrm{h,1}}\\T_{\mathrm{h,2}}\\...\\T_{\mathrm{h,m}}\end{bmatrix}=\begin{bmatrix}T_{\mathrm{ca,1}}\\T_{\mathrm{ca,2}}\\...\\T_{\mathrm{ca,m}}\end{bmatrix}+\begin{bmatrix}R_{\mathrm{hc_1}}&0&...&0\\0&R_{\mathrm{hc_2}}&...&0\\...&&&\\0&0&...&R_{\mathrm{hc_m}}\end{bmatrix}\begin{bmatrix}P_{\mathrm{loss,1}}\\P_{\mathrm{loss,2}}\\...\\P_{\mathrm{loss,n}}\end{bmatrix} \quad (16)$$

where $R_{\mathrm{hc_m}}$ is the thermal resistance from the hot-spot to case. $T_{\mathrm{h,m}}$ is the hot-spot temperature of the capacitor. The key challenge in the state-space thermal model is to identify the thermal matrix A in (13) for different layouts.

For the string layout of the capacitor bank as shown in Fig. 9, C_1 and C_{m} are the corner capacitors, which have the same effective surface area (one side faced to neighbor capacitor) and the same self-heating thermal resistance for $R_{\mathrm{ca_{1,1}}}$ and $R_{\mathrm{ca_{m,m}}}$. C_{i} $(1<i<m)$ are the middle capacitors with the same effective surface area (two sides faced to neighbor capacitor) and the same thermal resistance for $R_{\mathrm{ca_{i,i}}}$ $(1<i<m)$. Then, the self-heating thermal matrix A_1 can be obtained by inserting corner capacitor thermal coefficients to $A_1(1,1)$ and $A_1(m,m)$, and middle capacitor thermal coefficients to $A_1(i,i)$. From the string layout as shown in Fig. 9, it can be seen that C_{i} has heat transfer with $C_{\mathrm{i-1}}$ and $C_{\mathrm{i+1}}$. Therefore, by inserting the thermal coupling coefficient to $A_2(i,i-1)$ and $A_2(i,i+1)$, the thermal coupling matrix A_2 can be obtained, which is shown in Appendix. For the rectangle layout as shown in Fig. 10, three types of capacitor thermal models need to be identified for the thermal matrix according to the effective surface area. The capacitor located at (i,j) in Fig. 10 is the capacitor $C_{i(j-1)+i}$. The corner capacitors located in $(1,1)$, $(1,j)$, $(i,1)$ and (i,j) have two sides faced to neighbor capacitors, the border capacitors located in $(1,:)$, $(j,:)$, $(:,1)$ and $(:,j)$ have three sides faced to neighbor capacitors, and the middle capacitors at the other locations have four sides faced to neighbor capacitors. Then, the self-heating thermal matrix A_1 can be obtained depending on the corresponding locations. According to Fig. 10, it can be seen that capacitor $C_{(j-1)+i}$

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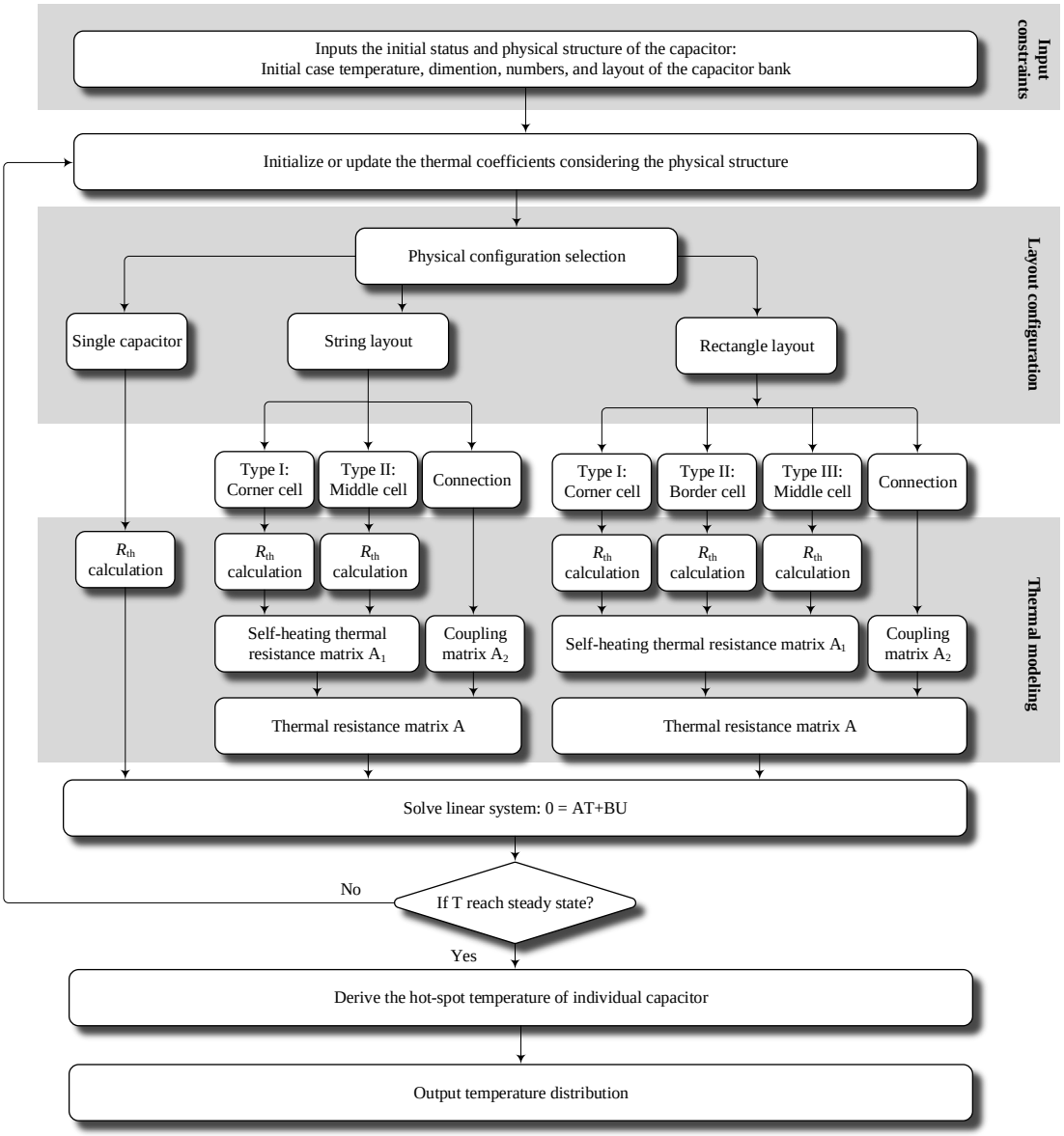


Fig. 11. Flowchart for iterations of the state-space thermal model to obtain the steady-state temperature distribution of capacitor bank.

has four surrounding capacitors for heat transfer, which are the capacitors $C_{i(j-1)+i-1}$, $C_{i(j-1)+i+1}$, $C_{i(j-1)+i-j}$ and $C_{i(j-1)+i+j}$. Therefore, by inserting the thermal coupling resistances to the interact locations, the thermal coupling matrix A_2 can be obtained and shown in the Appendix.

The state-space model discussed above describes the instantaneous temperature distribution of the capacitor bank. To derive the steady-state temperature distribution, a flowchart based on the state-space thermal model for iterations is provided as shown in Fig. 11. The input of the flowchart is the physical characteristics of the individual capacitor, the layout of the capacitor bank, and the initial temperature of the system. By loading the system parameters, the state-space thermal model can be constructed for a specific layout. Through a number of iterations, the case temperature and hot-spot temperature will be stabilized, and then the steady-state temperature distribution can be obtained.

IV. Design for Thermal Matching Considering the Thermal Coupling Effect

Thermal modeling of the capacitor bank describes the uneven temperature distribution in the capacitor bank, which will result in partial capacitors aging earlier. From the lifetime model shown in (2), it can be seen that the rated parameters (e.g, rated lifetime, rated voltage, rated testing temperature) and the actual stresses (e.g., voltage stress and thermal stress) are the key factors to the lifetime. By optimizing the rated parameters or actual stresses of the individual capacitor, it is possible to balance the temperature as well as the lifetime in a bank.

For a capacitor bank with specified rated voltage V_0, rated testing temperature T_0, rated lifetime L_0, and actual voltage V, the thermal loading T_h is the only design variable to the lifetime, which is determined by the current spectrum and the ESR of the capacitor. The current flowing through individual

capacitor depends on the capacitance (or impedance at the specified frequency) of each, because of the current sharing among capacitors. The current of capacitor i is written as

$$I_{\mathrm{C_i}} = I_{\mathrm{AB}} \frac{C_{\mathrm{i}}}{C_1 + C_2 + ...C_{\mathrm{m}}} \tag{17}$$

where m is the number of capacitors in a bank, C_{i} is the capacitance, and I_{AB} is the total current of the capacitor bank. ESR can be written as a function of capacitance, which is given as

$$ESR_{\mathrm{i}} = \frac{1}{C_{\mathrm{i}} s} \tan \delta_{\mathrm{i}} \tag{18}$$

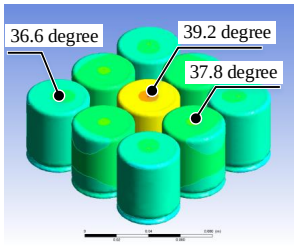
where $\tan \delta_{\mathrm{i}}$ is the Dissipation Factor (DF) and δ_{i} is the loss angle. Based on above equations, the power loss of individual capacitor can be derived as

$$P_{\mathrm{loss,i}} = I_{\mathrm{C_i}}^2 ESR_{\mathrm{i}} = C_{\mathrm{i}} \frac{\tan \delta_{\mathrm{i}} \times I_{\mathrm{AB}}^2}{(C_1 + C_2 + ...C_{\mathrm{m}})^2 s} \tag{19}$$

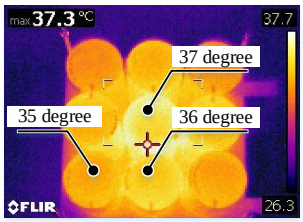
It can be seen that the power loss of capacitor is linear with C_{i}. By changing the capacitance of the individual capacitor, the corresponding heat injection will change accordingly as well as the temperature distribution. Worth to be noticed, in the same series of products, the size of capacitor is normally changed with the capacitance, which will affect the thermal impedance because of the heat dissipation area variation. Therefore, the thermal matching method should hybrid different downsize series products, which can provide various capacitance products with the same size. At this time, power loss is the only design variable corresponding to the hot-spot temperature of the individual capacitor. From above discussion, the thermal matching optimization model and the design constraints can be defined as

$$\begin{cases} \min.\{X\} \\ X = \dfrac{[T_{\mathrm{ca,1}}(C_1, C_2...C_{\mathrm{m}}) - \bar{T}]^2 + [T_{\mathrm{ca,2}}(C_1, C_2...C_{\mathrm{m}}) - \bar{T}]^2}{+...[T_{\mathrm{ca,m}}(C_1, C_2...C_{\mathrm{m}}) - \bar{T}]^2} \\ \bar{T} = \dfrac{T_{\mathrm{ca,1}}(C_1, \overset{m}{C_2}...C_{\mathrm{m}}) + T_{\mathrm{ca,2}}(C_1, C_2...C_{\mathrm{m}})}{+...T_{\mathrm{ca,m}}(C_1, C_2...\overset{m}{C_{\mathrm{m}}})} \\ P_{\mathrm{loss,i}} = \left(I_{\mathrm{AB}} \times \dfrac{C_{\mathrm{i}}}{C_1 + C_2 + ...C_{\mathrm{m}}} \right)^2 ESR_{\mathrm{i}} \quad (i = 1, 2...m) \\ P_{\mathrm{loss}} = P_{\mathrm{loss,1}} + P_{\mathrm{loss,2}} + ...P_{\mathrm{loss,m}} \end{cases} \tag{20}$$

where X is the temperature variances of the capacitors. $\bar{T}$ is the average temperature. The optimization variables are the capacitance of the individual capacitor. The optimization target is to minimize the temperature difference among capacitors. The constraint is to keep the same total power loss, which can also be to keep the same capacitance depending on applications. When the temperature difference among capacitors is zero, the capacitance for the individual capacitor in a bank can be acquired for even temperature distribution as well as even lifetime. Worth to notice, the voltage-dependent characteristics of the capacitor have an impact on the component sizing of the proposed design method. Therefore, the capacitance used in this method should be based on a specified voltage, which needs to be calibrated first and then taken into the model.

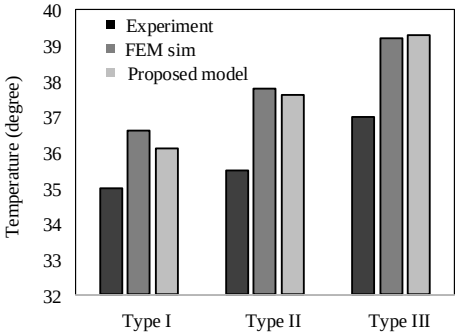


(a) FEM simulation results of temperature distribution.

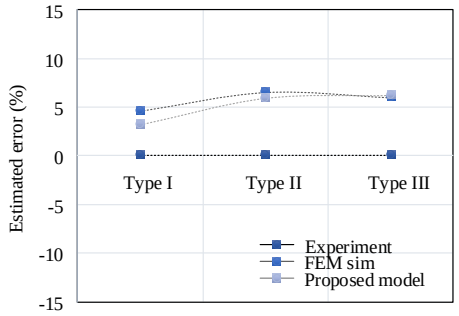


(b) Experimental results of temperature distribution.

Fig. 12. Temperature distribution of a capacitor from experiment and simulation testing.



(a) Comparison of temperature.



(b) Comparison of temperature estimation error.

Fig. 13. Comparison of temperature estimation among experiment, FEM simulation and proposed analytical thermal model.

V. Validation of the Proposed Thermal Modeling and Design Method for Thermal Matching

A. Thermal Model Verification

In order to verify the effectiveness of the proposed thermal model considering the thermal coupling effect, a capacitor bank with nine capacitors is investigated as a case study. NCC-KMQ series 450 V/ 470 μF/ 2000 hours electrolytic capacitors from Nippon Chemi-Con are used to implement the capacitor

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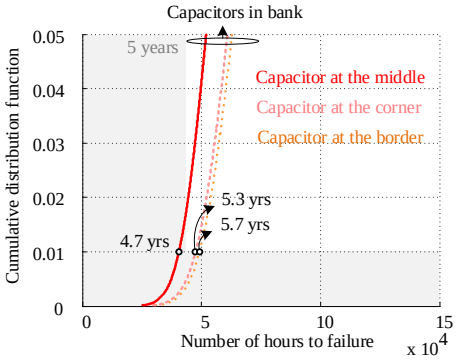


Fig. 14. Lifetime estimation results of the capacitor bank with nine capacitors (NCC-KMQ series 450 V/ 470 μF/ 2000 hours) based on the method in [13], where n=8.

bank. For the individual capacitor, the diameter is 40 mm and the height is 45 mm. The distance between the two capacitors is 2 mm. Chroma 11800 capacitor ripple current tester is used to inject 100 Hz ripple current to the capacitor bank. The current is shared among the nine capacitors connected in parallel, and the power dissipation for the individual capacitor is 0.96 W. The ambient temperature during the test is 25 $^{\circ}C$.

The proposed analytical thermal model is implemented in Matlab R2018a. The temperature distribution from the analytical model can be obtained in 5 seconds, while the FEM simulation takes 12 minutes. The results from the experiment and FEM simulation are shown in Fig. 12. The capacitors in the middle have the highest temperature in both cases, and the temperature difference between the middle and corner capacitors is around 2.5 degrees. The comparison between the proposed analytical model and the testing results are shown in Fig. 13 (a). Type I, II, and III are the corner, border, and middle capacitors in the capacitor bank. It can be seen that the estimated temperature from the proposed model is compatible with the simulation and experimental results. The deviation comparison among the three cases are shown in Fig. 13 (b), where the errors are within 10 %. The reason for the estimated error could be that the heat conduction from the pins of the capacitor to PCB board is ignored in simulation and analytical model, which could result in higher thermal resistance as well as higher temperature.

B. Verification of Design Method for Thermal Matching

Applying the same ripple current to the capacitor bank, the temperature distribution of the capacitor bank with a symmetrical layout and the same capacitors are shown in Fig. 12, where the difference between the highest and the lowest temperature is 2.5 degree, which leads to 17.5 % lifetime difference as shown in Fig. 14. By applying the proposed thermal matching design, the capacitance for the individual capacitor is able to be optimized for even temperature distribution, while the total power loss still keeps on the same level. Fig. 15 shows the capacitance of the individual capacitor in conventional design and proposed thermal matching design. The "Optimized solution" in Fig. 15 is the ideal capacitance used for the individual capacitor, and the "Practical solution" is based on

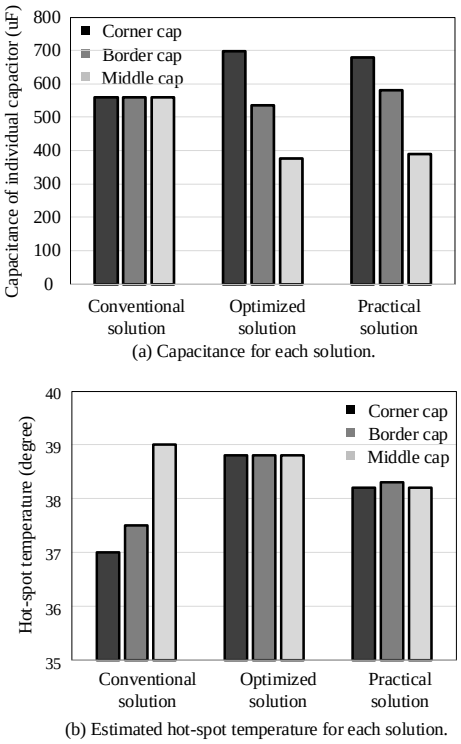


Fig. 15. Capacitance and hot-spot temperature of individual capacitor in conventional symmetrical design and the proposed thermal matching design.

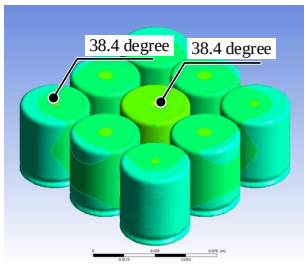


Fig. 16. Simulation results of a capacitor bank with proposed thermal matching design.

the available product in the market which can also fulfill the ideal optimization results. The capacitor bank with NCC-KMZ (EKMZ451VSN681MR50S) 450 V/ 680 μF$\times$4, NCC-KMW (EKMW451VSN561MR50S) 450 V/ 560 μF$\times$4 and NCC-KMQ (EKMQ451VSN391MR50S) 450 V/390 μF$\times$1 capacitors are implemented for simulation and experiment, where the results are shown in Fig. 16 and Fig. 17, respectively. It shows that the temperature distribution among capacitors is even and the physical characteristics of the capacitor bank are on the same level.

VI. Discussions

The thermal modeling method based on measurement in Section III. A is a generic method, which can be applied to different power electronic components and systems to acquire the temperature distribution, due to the measurement-based method to extract the thermal coefficients is independent with

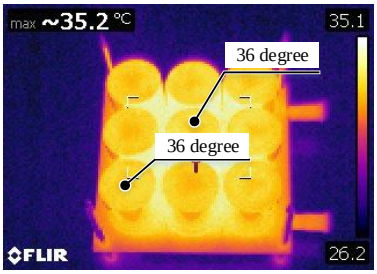


Fig. 17. Experimental results of a capacitor bank with the proposed thermal matching design.

the system structures, cooling system, and component parameters. Different from that, the analytical thermal modeling method proposed in Section III.B is effective for the capacitor bank with a cylinder capacitor and nature cooling only. It can be extended to other package capacitors, but the thermal resistances need to be updated based on the shape, surface area, surface material, and so on. For the forced air cooling or other cooling solutions, the model needs to be rebuild based on the cooling mechanisms and system structure.

In order to balance the temperature as well as the lifetime distribution, the design method is proposed in Section IV and demonstrated in a capacitor bank with natural cooling. But this method is not limited in the natural cooling condition. For example, in the capacitor bank with forced air cooling, the capacitors far away from the fans are stressed with higher temperatures and vice versa. By optimizing the parameters of the individual capacitor in a bank, it is able to reduce the temperature as well as the failure rate of the capacitors which are far away from the cooling source, to achieve even temperature and lifetime distribution. Future research efforts are expected, in terms of modeling and design for the reliability of capacitor bank with different cooling solutions.

VII. Conclusions

This paper proposes the modeling and design methods for the capacitor bank considering the thermal coupling effect. A lumped thermal model based on the measurement is proposed firstly, which is independent with the system structures, cooling system, and component parameters. For more time-efficient thermal modeling, an analytical model is proposed with programmable capability. Moreover, the design method for thermal matching is provided by optimizing the rated parameters or the actual stresses of individual capacitor. From the case study, the following conclusions can be drawn:

1) The proposed thermal model can be used to estimate the temperature distribution in a capacitor bank with natural cooling. It takes 5 seconds only, which is more time-efficient compared with FEM simulation with tens of minutes. Meanwhile, the estimation error is lower than 10 % with acceptable accuracy;

2) The thermal matching design is able to balance the thermal stresses as well as the lifetime among capacitors in a bank by optimizing the capacitance of individual capacitors, while still keep the total power loss on the same level.

Appendix A
Thermal Matrix

References

[1] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters-an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014.

[2] H. Wang and H. Wang, "Capacitive dc links in power electronic systems-reliability and circuit design," *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 29–36, Sep. 2018.

[3] H. Wang, H. Wang, G. Zhu, and F. Blaabjerg, "An overview of capacitive dc-links-topology derivation and scalability analysis," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1805–1829, 2020.

[4] Y. Jang, M. M. Jovanovic, and D. L. Dillman, "Hold-up time extension circuit with integrated magnetics," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 394–400, Mar. 2006.

[5] Y. Lai, Z. Su, and W. Chen, "New hybrid control technique to improve light load efficiency while meeting the hold-up time requirement for two-stage server power," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4763–4775, Sep. 2014.

[6] R. Moxley, J. Pope, and J. Allen, "Capacitor bank protection for simple and complex configurations," in *Proc. 65th Annual Conference for Protective Relay Engineers*, Apr. 2012, pp. 436–441.

[7] D. Zhou, Y. Song, Y. Liu, and F. Blaabjerg, "Mission profile based reliability evaluation of capacitor banks in wind power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4665–4677, May 2019.

[8] F. J. Nepveux, "Protection of tuned capacitor banks," *IEEE Trans. Ind. App.*, vol. 44, no. 4, pp. 973–978, Jul. 2008.

[9] C. Collins and L. Ran, "Optimized selection and utilization of dc-link capacitor in a single-phase pv grid inverter system," in *Proc. IEEE ECCE Asia*, May 2018, pp. 1931–1937.

[10] Jilong Yao and T. Green, "Dc-link capacitors sizing for three-level neutral-point-clamped inverters in four-wire distributed generation systems," in *Proc. International Conference on Future Power Systems*, Nov. 2005, pp. 5 pp.–5.

[11] P. Pelletier, J. Guichon, J. Schanen, and D. Frey, "Optimization of a dc capacitor tank," *IEEE Trans. Ind. App.*, vol. 45, no. 2, pp. 880–886, Mar. 2009.

[12] F. Zare, "Harmonics issues of three-phase diode rectifiers with a small dc link capacitor," in *Proc. IEEE IPEMC*, Sep. 2014, pp. 912–917.

[13] H. Wang, P. Davari, H. Wang, D. Kumar, F. Zare, and F. Blaabjerg, "Lifetime estimation of dc-link capacitors in adjustable speed drives under grid voltage unbalances," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4064–4078, May 2019.

[14] X. Wang, M. Karami, and R. M. Tallam, "Test fixtures to apply variable dc bias and ac ripple current for reliability testing of electrolytic capacitors," *IEEE Trans. Ind. App.*, vol. 55, no. 4, pp. 4073–4079, Jul, 2019.

[15] K. Lee, T. M. Jahns, G. Venkataramanan, and W. E. Berkopec, "Dc-bus electrolytic capacitor stress in adjustable-speed drives under input voltage unbalance and sag conditions," *IEEE Trans. Ind. App.*, vol. 43, no. 2, pp. 495–504, Mar, 2007.

[16] A. Lahyani, P. Venet, G. Grellet, and P. . Viverge, "Failure prediction of electrolytic capacitors during operation of a switchmode power supply," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1199–1207, Nov. 1998.

[17] B. Sun, X. Fan, C. Qian, and G. Zhang, "Pof-simulation-assisted reliability prediction for electrolytic capacitor in led drivers," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6726–6735, Nov. 2016.

[18] M. Chen, K. K. Afridi, and D. J. Perreault, "Stacked switched capacitor energy buffer architecture," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5183–5195, Nov. 2013.

[19] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase pwm rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[20] H. Wang and H. Wang, "A two-terminal active capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5893–5896, Aug. 2017.

[21] H. Wang, Y. Liu, and H. Wang, "On the practical design of a two-terminal active capacitor," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10 006–10 020, Oct. 2019.

[22] H. Wang and H. Wang, "A reliability-oriented component sizing procedure for cost benchmarking of capacitive dc-links," in *Proc. IEEE EPE*, Sep. 2017, pp. P.1–P.9.

[23] R. M. Burkart and J. W. Kolar, "Comparative life cycle cost analysis of si and sic pv converter systems based on advanced η- ρ-σ multiobjective

$$A_2 = \begin{bmatrix} -\sum_{j=1}^{n} \frac{1}{R_{ca_{1,j}}} & -\frac{1}{R_{ca_{1,2}}} & 0 & \dots & 0 \\ -\frac{1}{R_{ca_{2,1}}} & -\sum_{j=1}^{n} \frac{1}{R_{ca_{2,j}}} & -\frac{1}{R_{ca_{2,3}}} & \dots & 0 \\ 0 & -\frac{1}{R_{ca_{3,2}}} & -\sum_{j=1}^{n} \frac{1}{R_{ca_{3,j}}} & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & -\sum_{j=1}^{n} \frac{1}{R_{ca_{m,j}}} \end{bmatrix} \tag{A.1}$$

$$A_2 = \begin{bmatrix} -\sum_{j=1}^{n} \frac{1}{R_{ca_{1,j}}} & -\frac{1}{R_{ca_{1,2}}} & \dots & -\frac{1}{R_{ca_{1,i+1}}} & 0 & \dots & 0 \\ -\frac{1}{R_{ca_{2,1}}} & -\sum_{j=1}^{n} \frac{1}{R_{ca_{2,j}}} & \dots & 0 & -\frac{1}{R_{ca_{2,i+2}}} & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ -\frac{1}{R_{ca_{i+1,1}}} & 0 & \dots & -\sum_{j=1}^{n} \frac{1}{R_{ca_{i+1,j}}} & -\frac{1}{R_{ca_{i+1,i+2}}} & \dots & 0 \\ 0 & -\frac{1}{R_{ca_{i+2,2}}} & \dots & -\frac{1}{R_{ca_{i+2,i+1}}} & -\sum_{j=1}^{n} \frac{1}{R_{ca_{i+2,j}}} & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & 0 & 0 & \dots & -\sum_{j=1}^{n} \frac{1}{R_{ca_{m,j}}} \end{bmatrix} \tag{A.2}$$

optimization techniques," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4344–4358, Jun. 2017.

[24] P. Freiburger, "Transient thermal modeling of aluminum electrolytic capacitors under varying mounting boundary conditions," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2015, pp. 1–5.

[25] Z. Wang, F. Yan, M. Xu, Z. Wang, X. Wang, and Z. Xu, "Influence of external factors on self-healing capacitor temperature field distribution and its validation," *IEEE Trans. Plasma Sci.*, vol. 45, no. 7, pp. 1680–1688, Jul. 2017.

[26] H. Wang, R. Zhu, H. Wang, M. Liserre, and F. Blaabjerg, "A thermal modeling method considering ambient temperature dynamics," *IEEE Trans. Power Electron.*, 2019,(in press).

[27] Y. Yang, K. Ma, H. Wang, and F. Blaabjerg, "Instantaneous thermal modeling of the dc-link capacitor in photovoltaic systems," in *Proc. IEEE APEC*, Mar. 2015, pp. 2733–2739.

[28] J. Rajmond and P. Dan, "Thermal modeling of through hole capacitors," in *Proc. IEEE SIITME*, Oct. 2012, pp. 227–232.

[29] M. L. Gasperi and N. Gollhardt, "Heat transfer model for capacitor banks," in *Proc. IEEE Industry Applications Conference*, vol. 2, Oct. 1998, pp. 1199–1204.

[30] D. Zhou, H. Wang, and F. Blaabjerg, "Lifetime estimation of electrolytic capacitors in a fuel cell power converter at various confidence levels," in *Proc. IEEE SPEC*, Dec. 2016, pp. 1–6.

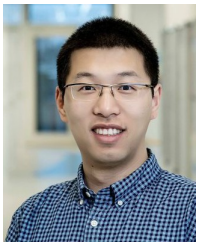
[31] Y. Liu, M. Huang, H. Wang, X. Zha, J. Gong, and J. Sun, "Reliability-oriented optimization of the lc filter in a buck dc-dc converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6323–6337, Aug. 2017.

[32] W. Liu, K. Wang, H. S. Chung, and S. T. Chuang, "Modeling and design of series voltage compensator for reduction of dc-link capacitance in grid-tie solar inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2534–2548, May 2015.

[33] Nippon-Chemi-con, "Aluminum capacitors group chart," Available: https://www.chemi-con.co.jp/e/catalog/pdf/al-e/al-sepa-e/001-guide/al-groupchart-e-171001.pdf, 2017.

[34] H. Wang and H. Wang, "An analytical circuit based nonlinear thermal model for capacitor banks," in *Microelectronics Reliability*, vol. 88-90, Sep. 2018, pp. 524–527.

[35] H. Wang and H. Wang, "Reliability evaluation and optimization of capacitor bank," in *Proc. IEEE ECCE*, Sep. 2018, pp. 7386–7390.



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