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Capacitor Voltage Balancing Control Scheme for 2/3-Level DAB Converters

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***Abstract*—Two-three (2/3)-level dual-active-bridge (DAB) DC-DC converters have high potential to be applied in the high-voltage (HV) applications due to their higher voltage blocking capability compared to the two-level DAB converters. However, capacitor voltage balancing will be a crucial issue for the neutral-point-clamped (NPC) bridge in the HV side. In order to regulate the capacitor voltages, this paper proposes a complementary-small-vector (CSV) balancing control scheme. According to the relationships among the polarity of the neutral-point current, the small vectors, and the polarity of the transformer current, two CSV pairs are obtained. In the proposed scheme, if a small vector is diagnosed as an adverse small vector for the capacitor voltage balance, it will be replaced by its CSV. After that, the polarity of the neutral-point current can be changed to increase the required charge injected into or drawn from the neutral point. Meanwhile, the waveforms of the current and voltage during the balancing process will remain unchanged. Therefore, the power fluctuation and current overshoot can be avoided. Furthermore, the implementation of the proposed scheme under different operating modes are demonstrated. Finally, the simulation results verify the performances of the proposed balancing control scheme.**

***Index Terms*—DAB converters, neutral-point-clamped bridge, capacitor voltage balancing control, dynamic performances.**

I. Introduction

The dual-acitve-bridge (DAB) converters were originally proposed for the high-power-density applications in 1980s [1]. Due to many advantages, such as soft-switching capability, galvanic isolation, and high efficiency, the DAB converters have been widely applied in different applications. Compared with the two-level DAB converters, the two-three (2/3)-level DAB converters, as shown in Fig. 1, is a promising solution for interconnecting the low-voltage (LV) DC input side with a high-voltage (HV) DC-link voltage, e.g., 1500Vdc PV application due to the three-level neutral-point-clamped (NPC) bridge in the HV side. Besides, the 2/3-level DAB converters can provide more degrees of freedom (DoFs) to further improve the performances of the converters [2], [3].

The phase-shift control is the most popular control scheme for the DAB converters. The most simplest modulation scheme is the single-phase-shift control, in which the power magnitude and direction is controlled by the phase-shift angle between the two full bridges. However, when the terminal voltages of the transformer mismatch, the soft-switching range will be limited and the root-mean-square (RMS) current will be increased [4], [5]. To overcome these drawbacks, the multi-phase-shift (MPS) control schemes were proposed. The five-level control scheme is one of the most advantageous MPS schemes for the NPC-type DAB converters, which can increase the soft-switching capability and improve the efficiency by applying more DoFs. However, the capacitor voltage unbalance issues will appear in the five-level control scheme due to the tolerances in component values, and perturbation in the phase shifts or duty cycles of the gate driving signals. When the capacitor voltage unbalance occurs, the voltage stress on some components will increase, and the uneven stress on the capacitors will accelerate the failure of the components. Furthermore, the capacitor voltages unbalance will reduce the accuracy of the power transfer model of the converters, and deteriorate the optimal operating conditions [6]–[9].

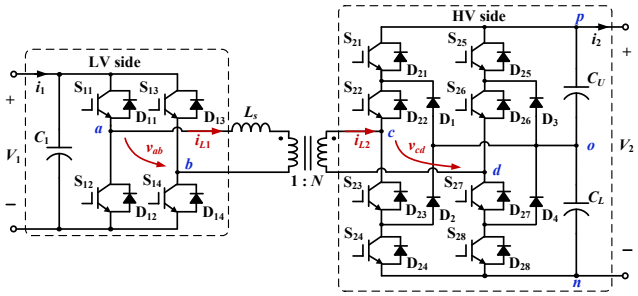


Fig. 1. A two-three (2/3)-level dual-active-bridge (DAB) DC-DC converter.

To regulate the capacitor voltages, some balancing control schemes have been proposed. In [7]–[9], the intervals where the small vectors being utilized are dramatically regulated by a PI controller according to the capacitor voltage unbalance conditions and the polarity of the transformer current. In [6], the authors choose certain small vectors to decouple the polarity of the neutral-point current from the polarity of the transformer current (i_{L1} and i_{L2} in Fig. 1). However, all of the mentioned schemes suffer from the current overshoot and power fluctuation during the voltage balancing process, which increase the current stress on the power components and limit the dynamic performances of the DAB converters.

In order to overcome the capacitor voltage balancing issues and improve the dynamic performances, this paper proposes a complementary-small-vector (CSV) method. The CSV pairs are firstly introduced in this method. In each CSV pair, the two small vectors can achieve the same waveforms of the transformer current and voltage, and opposite polarity

of the neutral-point current. Therefore, after replacing an adverse small vector by using its CSV, the waveforms of the transformer current and voltage can be reconfigured, and thus no current or voltage fluctuation occurs during the balancing process. Meanwhile, due to the opposite polarity of the neutral-point current, the CSV can be used to assist the capacitor voltage balancing. Therefore, the required neutral-point charge can be increased during each switching cycle to accelerate the capacitor voltage balancing process. The rest of the paper will be organized as follows. The analysis of the five-level modulation and small vectors are given in Section II. The definition of the CSVs and the implementation of the proposed scheme are given in Section III. Section IV presents the simulation results to verify the effectiveness of the theoretical analysis. Finally, a conclusion is given in Section VI.

II. Modulation

A. Five-level control scheme

As shown in Fig. 1, V_1 and V_2 are the LV-side and HV-side DC-link voltages, respectively. v_{ab} and v_{cd} are the input and output voltages of the transformer, respectively. L_s is the series inductor, and i_{L1} and i_{L2} are the two terminal currents of the transformer. $1:N$ denotes the turns ratio of the transformer. i_o denotes the neutral-point current. Fig. 2 shows the typical waveforms of the gate driving signals, voltages and current of the 2/3-level DAB converters with the five-level control scheme, where T_{hs} is a half of the switching cycle. For the LV side, the two diagonal switches (e.g., S_{11} and S_{14}) turn on and off synchronously with the duty cycle of 50%. For the HV side, α_i $(i = 1, 2, 3, 4)$ denotes the phase shifts between the gate driving signals of the HV-side switches and that of S_{11}, and φ_i $(i = 1, 2, 3, 4)$ denotes the duty cycles of the gate driving signals of the HV-side switches. The ranges of the phase shifts and duty cycles are: $0 \le \alpha_i \le T_{hs}$, $0 \le \varphi_1, \varphi_4 \le T_{hs}$, and $T_{hs} \le \varphi_2, \varphi_3 \le 2T_{hs}$. To obtain symmetrical waveforms and simplify the modulation scheme, some constraints should be fullfilled: $\alpha_1 - \alpha_2 = \alpha_4 - \alpha_3 = \triangle\alpha$, $\varphi_1 = \varphi_4$, $\varphi_2 = \varphi_3$, $\varphi_1 + \varphi_2 = \varphi_3 + \varphi_4 = 2T_{hs}$, and $\varphi_1 + \triangle\alpha = T_{hs}$. Therefore, the modulation scheme is determined by three control variables, i.e., α_2, α_3, and $\triangle\alpha$. It should be noted that the waveforms of the voltages and current for the $\alpha_2 \le \alpha_3$ and $\alpha_2 \ge \alpha_3$ cases are identical. A similar condition applies also in the relationships between α_1 and α_3. Therefore, only $\alpha_2 \le \alpha_3 \le \alpha_1$ is under consideration.

From Fig. 2, it can be seen that there are five levels on the HV-side voltage v_{cd}, i.e., $v_{cd} \in \{0, \pm 0.5V_2, \pm V_2\}$. The switching states corresponding to $v_{cd} = 0, \pm 0.5V_2, \pm V_2$ are defined as the zero vectors, small vectors, and large vectors, respectively. Only during the intervals where the small vectors are employed, the current will flow through the neutral point o. Due to the symmetry of the waveforms, the charge injected into and drawn from the neutral point is equal during one switching cycle in ideal operation. However, when there is an initial capacitor voltage unbalance cause by the tolerances in component values or other issues, or perturbation in the phase shifts, the neutral-point balancing condition can be

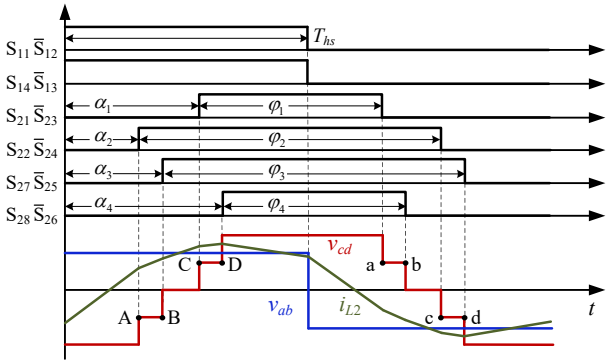


Fig. 2. Typical waveforms of the five-level control scheme for the 2/3-level DAB converters.

deteriorated, leading to capacitor voltage unbalance, which will increase the voltage stress on the power components, deteriorate the optimal operating conditions, and affect the safety of the system. To balance the capacitor voltages, the small vectors utilization should be modified to change the polarity or duration of i_o.

B. Small vectors analysis

From Fig. 2, it can be seen that there are four intervals where the small vectors are employed, i.e., [A, B], [C, D], [a, b], and [c, d], and the corresponding small vectors are $\{S_{22}, S_{23}, S_{25}, S_{26}\}$, $\{S_{21}, S_{22}, S_{26}, S_{27}\}$, $\{S_{22}, S_{23}, S_{27}, S_{28}\}$, and $\{S_{23}, S_{24}, S_{26}, S_{27}\}$, respectively. Note that the small vectors denote the switches with high-level gate driving signals. During the four intervals, i_o will flow through the neutral point. However, the direction of i_o is not only dependent on the applied small vectors, but also affected by the polarity of i_{L2}. For instance, at the interval [A, B], the small vector is applied as $\{S_{22}, S_{23}, S_{25}, S_{26}\}$. When the polarity of i_{L2} is positive (from the LV side to the HV side), the current flows through S_{25}, S_{26}, S_{23}, D_2, and injects into the neutral point o, as shown in Fig. 3 (a). Therefore, the upper capacitor C_U will discharge in this condition. However, when the polarity of i_{L2} is negative (from the HV side to the LV side), the current will draw from the neutral point o, and flow through D_1, S_{22}, D_{26}, and D_{25}, as shown in Fig. 3 (b), and the voltage of the capacitor C_U will increase. By analyzing the current conduction paths of the four intervals with different polarities of i_{L2}, the relationships between the polarity of i_o and the polarity of i_{L2} can be obtained, as shown in Table I. In Table I, $\bar{i}_{L2}$ and $\bar{i}_o$ are the mean value of i_{L2} and i_{Lo} during each interval, respectively. $\bar{i}_o > 0$ denotes the current injects into the neutral point, while $\bar{i}_o < 0$ denotes the current draws from the neutral point. From Table I, it can be seen that for each small vector, with different polarities of $\bar{i}_{L2}$, the polarities of $\bar{i}_o$ will also be opposite.

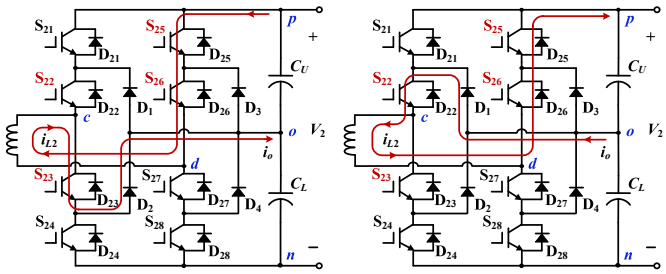
III. Capacitor Voltage Balancing Control Scheme

A. Complementary-small-vector pairs

When the capacitor voltage unbalance occurs, the phase shifts or duty cycles should be adjusted to increase or decrease

TABLE I
SMALL VECTORS WITH RESPECT TO THE POLARITY OF $\bar{i}_o$

Intervals	Small vectors	Polarity of $\bar{i}_{L2}$	Value of v_{cd}	Current conduction Path	Polarity of $\bar{i}_o$
[A, B]	$\{S_{22}, S_{23}, S_{25}, S_{26}\}$	$\bar{i}_{L2} > 0$	-0.5V_2	$S_{25} \rightarrow S_{26} \rightarrow S_{23} \rightarrow D_2$	$\bar{i}_o > 0$
		$\bar{i}_{L2} < 0$		$D_1 \rightarrow S_{22} \rightarrow D_{26} \rightarrow D_{25}$	$\bar{i}_o < 0$
[C, D]	$\{S_{21}, S_{22}, S_{26}, S_{27}\}$	$\bar{i}_{L2} > 0$	0.5V_2	$D_3 \rightarrow S_{26} \rightarrow D_{22} \rightarrow D_{21}$	$\bar{i}_o < 0$
		$\bar{i}_{L2} < 0$		$S_{21} \rightarrow S_{22} \rightarrow S_{27} \rightarrow D_4$	$\bar{i}_o > 0$
[a, b]	$\{S_{22}, S_{23}, S_{27}, S_{28}\}$	$\bar{i}_{L2} > 0$	0.5V_2	$D_{28} \rightarrow D_{27} \rightarrow S_{23} \rightarrow D_2$	$\bar{i}_o > 0$
		$\bar{i}_{L2} < 0$		$D_1 \rightarrow S_{22} \rightarrow S_{27} \rightarrow S_{28}$	$\bar{i}_o < 0$
[c, d]	$\{S_{23}, S_{24}, S_{26}, S_{27}\}$	$\bar{i}_{L2} > 0$	-0.5V_2	$D_3 \rightarrow S_{26} \rightarrow S_{23} \rightarrow S_{24}$	$\bar{i}_o < 0$
		$\bar{i}_{L2} < 0$		$D_{24} \rightarrow D_{23} \rightarrow S_{27} \rightarrow D_4$	$\bar{i}_o > 0$



(a) (b)

Fig. 3. Current conduction paths of the small vector $\{S_{22}, S_{23}, S_{25}, S_{26}\}$. (a) When i_{L2} is positive. (b) When i_{L2} is negative.

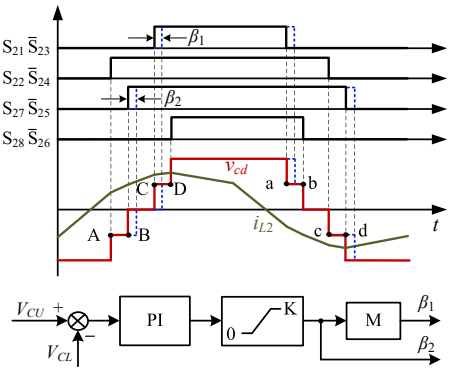


Fig. 4. A capacitor voltage balancing control scheme when $V_{CU} > V_{CL}$.

the intervals [A, B], [C, D], [a, b], and [c, d], and thus to regulate the neutral-point voltage. If the voltage of the capacitor C_U is higher than that of C_L, a positive $\bar{i}_o$ is required to charge the lower capacitor. Otherwise, a negative $\bar{i}_o$ is required to charge the upper capacitor. Fig. 4 demonstrates a traditional capacitor voltage balancing control scheme with a PI controller when the upper capacitor voltage V_{CU} is higher than the lower capacitor voltage V_{CL}, in which β_1 and β_2 are the regulated phase shifts, K is the upper threshold for the output of the PI controller, and M is the multiplier. In order to avoid the waveforms distortion, the regulated phase shifts should satisfy that $\beta_1 \leq \triangle\alpha$ and $\beta_2 \leq \triangle\alpha$. In Fig. 4, during [A, B] and [C, D], the polarity of the transformer current $\bar{i}_{L2}$ is positive, while that during [a, b] and [c, d] is negative. According to Table I, $\bar{i}_o$ is positive during [A, B] and [c, d], and negative during [a, b] and [C, D]. Therefore, the small vectors during [A, B] and [c, d] are beneficial to assist the neutral-point voltage balancing, which are defined as beneficial small vectors, while the small vectors during [a, b] and [C, D] are defined as adverse small vectors. To increase the charge injected into o, the intervals [A, B] and [c, d] are increased while the intervals [a, b] and [C, D] are decreased by increasing the phase shifts of the gate driving signals of S_{21} and S_{22}. However, from the power and current expression

$$P = \frac{1}{T_{hs}} \int_0^{T_{hs}} v_{cd}(t) i_{L2}(t) dt \tag{1}$$

$$\frac{i_{L2}(t)}{dt} = \frac{N v_{ab}(t) - v_{cd}(t)}{L_s} \tag{2}$$

it can be seen that because the waveform of V_{cd} changes during the balancing process, the transferred power will also change, and the current fluctuation will occur, resulting in higher current stress and longer dynamic process. To overcome these problems, this paper proposes a capacitor voltage balancing control scheme based on the CSVs.

From (1), it can be seen that if the waveforms of v_{cd} and i_{L2} remain unchanged during the balancing process, the transferred power will also keep constant, and the dynamic performances of the converters can be improved. Therefore, the CSV pairs are defined as: for two small vectors, under the same polarity of $\bar{i}_{L2}$, the value of v_{cd} should be the same, while the polarity of $\bar{i}_o$ should be opposite. In this way, when a small vector is identified as an adverse small vector in a certain operating condition, it can be replaced by its CSV. Since the replacement of the small vector does not affect the voltage v_{cd}, the dynamic waveforms of the current and voltage will be identical to the steady-state waveforms. Hence, the current fluctuation can be avoided. Furthermore, the changed polarity of $\bar{i}_o$ can guarantee the CSV is beneficial to the capacitor voltage balance. With the above analysis, according to Table I, $\{S_{22}, S_{23}, S_{25}, S_{26}\}$ and $\{S_{23}, S_{24}, S_{26}, S_{27}\}$, $\{S_{21}, S_{22}, S_{26}, S_{27}\}$ and $\{S_{22}, S_{23}, S_{27}, S_{28}\}$ are two pairs of CSVs. For instance, if V_{CU} is higher than V_{CL}, and the polarity of $\bar{i}_{L2}$ is positive, according to Table I, it can be seen that $\bar{i}_o$ will inject into the neutral point during the interval [A, B], and thus $\{S_{22}, S_{23}, S_{25}, S_{26}\}$ is a beneficial small vector. Therefore, this small vector should be remained. On the con-

trary, when the polarity of i_{L2} is negative, $\{S_{22}, S_{23}, S_{25}, S_{26}\}$ is an adverse small vector, which should be replaced by its CSV $\{S_{23}, S_{24}, S_{26}, S_{27}\}$. Hence, the small vector applied at the interval [A, B] becomes a beneficial small vector.

B. Complementary-small-vector method

From the above analysis, the capacitor voltage balancing control scheme should be divided into three steps: 1. Based on the deviation of the capacitor voltages, the required polarity of $\bar{i}_o$ can be determined; 2. Based on the polarity of $\bar{i}_{L2}$, which can be calculated by (2), the beneficial and adverse small vectors can be identified; 3. Replacing the adverse small vectors by using their CSVs to change the polarity of $\bar{i}_o$. Due to the symmetry, the current $\bar{i}_{L2}$ during [A, B] and [a, b] have opposite polarities, so do that during [C, D] and [c, d]. Therefore, we only discuss the polarity of $\bar{i}_{L2}$ during [A, B] and [C, D]. For instance, if $V_{CU} > V_{CL}$, the implementation of the proposed balancing control scheme under different operating modes can be divided as follows.

(1) $\bar{i}_{L2}$ [A, B] > 0, $\bar{i}_{L2}$ [C, D] > 0: According to Table I, it can be seen that $\bar{i}_o$ [A, B] > 0, $\bar{i}_o$ [C, D] < 0, $\bar{i}_o$ [a, b] < 0, and $\bar{i}_o$ [c, d] > 0. During $V_{CU} > V_{CL}$, $\bar{i}_o > 0$ is required. Therefore, in this mode, the two small vectors during [A, B] and [c, d], i.e., $\{S_{22}, S_{23}, S_{25}, S_{26}\}$ and $\{S_{23}, S_{24}, S_{26}, S_{27}\}$, are beneficial small vectors, while the vectors during [C, D] and [a, b], i.e., $\{S_{21}, S_{22}, S_{26}, S_{27}\}$ and $\{S_{22}, S_{23}, S_{27}, S_{28}\}$, are adverse small vectors. Hence, the two adverse small vectors should be replaced by their complementary small vectors, i.e., in the interval [C, D], $\{S_{22}, S_{23}, S_{27}, S_{28}\}$ should replace $\{S_{21}, S_{22}, S_{26}, S_{27}\}$, and in the interval [a, b], $\{S_{21}, S_{22}, S_{26}, S_{27}\}$ should replace $\{S_{22}, S_{23}, S_{27}, S_{28}\}$. Therefore, the implementation of the balancing control in this mode is shown in Fig. 5, in which $T_s = 2T_{hs}$ is the switching cycle. $\alpha_i^{'}$ and $\varphi_i^{'}$ $(i = 1, 2, 3, 4)$ denote the phase shifts and duty cycles after applying the balancing control. During the balancing process, the dotted lines denote the gate driving signals in the previous steady state, while the solid lines denote those after applying the balancing control. The relationships of the control variables between the balancing control and the steady-state control are

$$\begin{cases} \alpha_1^{'} = \alpha_1 + (\alpha_3 - \alpha_2), \alpha_2^{'} = \alpha_2 \\ \alpha_3^{'} = \alpha_3, \alpha_4^{'} = \alpha_1 - (\alpha_3 - \alpha_2) \\ \varphi_i^{'} = \varphi_i (i = 1, 2, 3, 4) \end{cases} \tag{3}$$

Therefore, to achieve the balancing control in this condition, only the phase shifts of α_1 and α_4 are modified. As a result, all of the four small vectors during the balancing process are beneficial small vectors, which accelerate the dynamic response. Meanwhile, because the waveform of v_{cd} remains unchanged, according to (2), the waveform of i_{L2} will also keep constant, and thus the power fluctuation during the balancing process will be eliminated.

(2) $\bar{i}_{L2}$ [A, B] > 0, $\bar{i}_{L2}$ [C, D] < 0: According to Table I, it can be seen that $\bar{i}_o$ [A, B] > 0, $\bar{i}_o$ [C, D] > 0, $\bar{i}_o$ [a, b] < 0, and $\bar{i}_o$ [c, d] < 0. Therefore, the small vectors during the intervals

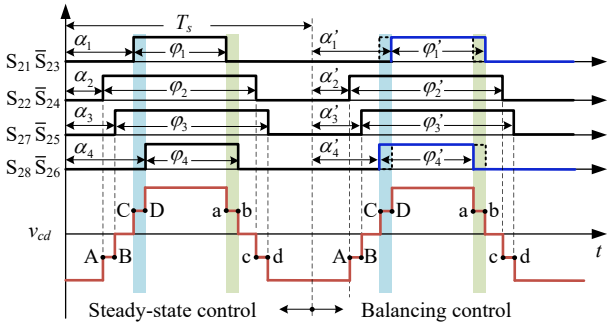


Fig. 5. The proposed CSV balancing control scheme when $\bar{i}_{L2}$ [A, B] > 0 and $\bar{i}_{L2}$ [C, D] > 0 under the condition $V_{CU} > V_{CL}$.

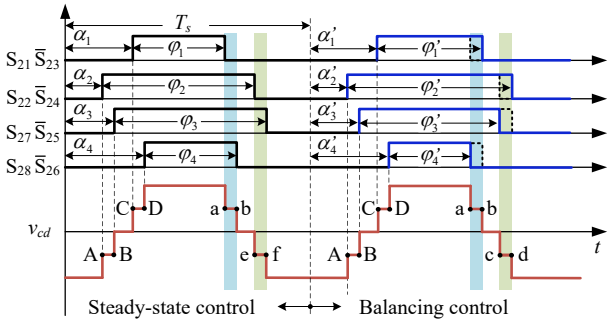


Fig. 6. The proposed CSV balancing control scheme when $\bar{i}_{L2}$ [A, B] > 0 and $\bar{i}_{L2}$ [C, D] < 0 under the condition $V_{CU} > V_{CL}$.

[a, b] and [c, d] are adverse small vectors, which should be replaced by their CSVs. The implementation of the balancing control in this mode is shown in Fig. 6. The relationships of the control variables between the balancing control and the steady-state control are

$$\begin{cases} \alpha_i^{'} = \alpha_i (i = 1, 2, 3, 4) \\ \varphi_1^{'} = \varphi_1 + (\alpha_3 - \alpha_2), \varphi_2^{'} = \varphi_2 + (\alpha_3 - \alpha_2) \\ \varphi_3^{'} = \varphi_3 + (\alpha_3 - \alpha_2), \varphi_4^{'} = \varphi_4 + (\alpha_3 - \alpha_2) \end{cases} \tag{4}$$

(3) $\bar{i}_{L2}$ [A, B] < 0, $\bar{i}_{L2}$ [C, D] > 0: In this mode, the neutral-point current during the four intervals satisfies that $\bar{i}_o$ [A, B] < 0, $\bar{i}_o$ [C, D] < 0, $\bar{i}_o$ [a, b] > 0, and $\bar{i}_o$ [c, d] > 0. Therefore, the small vectors during the intervals [A, B] and [C, D] are adverse small vectors, which should be replaced by their complementary small vectors $\{S_{23}, S_{24}, S_{26}, S_{27}\}$ and $\{S_{22}, S_{23}, S_{27}, S_{28}\}$, respectively. The implementation of the balancing control scheme is shown in Fig. 7, and the relationships of the control variables between the balancing control and the steady-state control are

$$\begin{cases} \alpha_1^{'} = \alpha_1 + (\alpha_3 - \alpha_2), \alpha_2^{'} = \alpha_2 + (\alpha_3 - \alpha_2) \\ \alpha_3^{'} = \alpha_3 - (\alpha_3 - \alpha_2), \alpha_4^{'} = \alpha_4 - (\alpha_3 - \alpha_2) \\ \varphi_1^{'} = \varphi_1 - (\alpha_3 - \alpha_2), \varphi_2^{'} = \varphi_2 - (\alpha_3 - \alpha_2) \\ \varphi_3^{'} = \varphi_3 + (\alpha_3 - \alpha_2), \varphi_4^{'} = \varphi_4 + (\alpha_3 - \alpha_2) \end{cases} \tag{5}$$

(4) $\bar{i}_{L2}$ [A, B] < 0, $\bar{i}_{L2}$ [C, D] < 0: Based on Table I, it can be seen that $\bar{i}_o$ [A, B] < 0, $\bar{i}_o$ [C, D] > 0, $\bar{i}_o$ [a, b] > 0, and

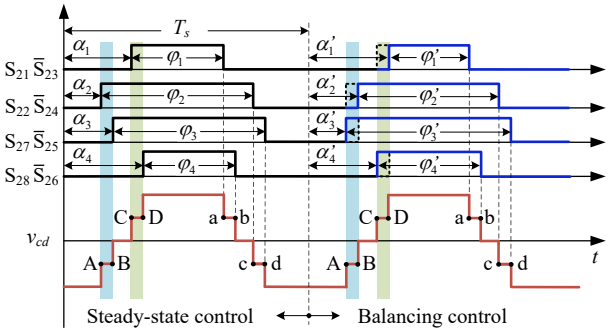


Fig. 7. The proposed CSV balancing control scheme when $\bar{i}_{L2}$ [A, B] < 0 and $\bar{i}_{L2}$ [C, D] > 0 under the condition $V_{CU} > V_{CL}$.

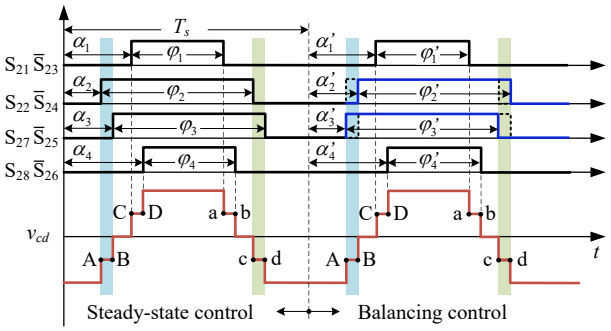


Fig. 8. The proposed CSV balancing control scheme when $\bar{i}_{L2}$ [A, B] < 0 and $\bar{i}_{L2}$ [C, D] < 0 under the condition $V_{CU} > V_{CL}$..

$\bar{i}_o$ [c, d] < 0. Therefore, the small vectors during [A, B] and [c, d] should be replaced by the complementary small vectors $\{S_{23}, S_{24}, S_{26}, S_{27}\}$ and $\{S_{22}, S_{23}, S_{25}, S_{26}\}$, respectively. The balancing control scheme in this mode is shown in Fig. 8, and the relationships of the control variables between the balancing control and the steady-state control are

$$\begin{cases} \alpha_1^{'} = \alpha_1, \alpha_2^{'} = \alpha_2 + (\alpha_3 - \alpha_2) \\ \alpha_3^{'} = \alpha_3 - (\alpha_3 - \alpha_2), \alpha_4^{'} = \alpha_4 \\ \varphi_i^{'} = \varphi_i, (i = 1, 2, 3, 4) \end{cases} \tag{6}$$

The balancing control scheme under different modes when $V_{CU} > V_{CL}$ has been demonstrated above, and the analysis for the condition when $V_{CU} < V_{CL}$ can be done in a similar way, where the negative $\bar{i}_o$ is required for neutral-point voltage regulation. For the four modes of $\bar{i}_{L2}$ [A, B] > 0 and $\bar{i}_{L2}$ [C, D] > 0, $\bar{i}_{L2}$ [A, B] > 0 and $\bar{i}_{L2}$ [C, D] < 0, $\bar{i}_{L2}$ [A, B] < 0 and $\bar{i}_{L2}$ [C, D] > 0, $\bar{i}_{L2}$ [A, B] < 0 and $\bar{i}_{L2}$ [C, D] < 0, the balancing scheme will be the same as Fig. 8, Fig. 7, Fig. 6, and Fig. 5, respectively.

IV. Simulation Results

To verify the effectiveness of the proposed capacitor voltage balancing control scheme, simulations are performed. The main parameters are: the input voltage V_1 is 200 V, the reference output voltage V_{2ref} is 300 V, the DC load R is 18 Ω, the transformer turns-ratio N is 1, the series inductor

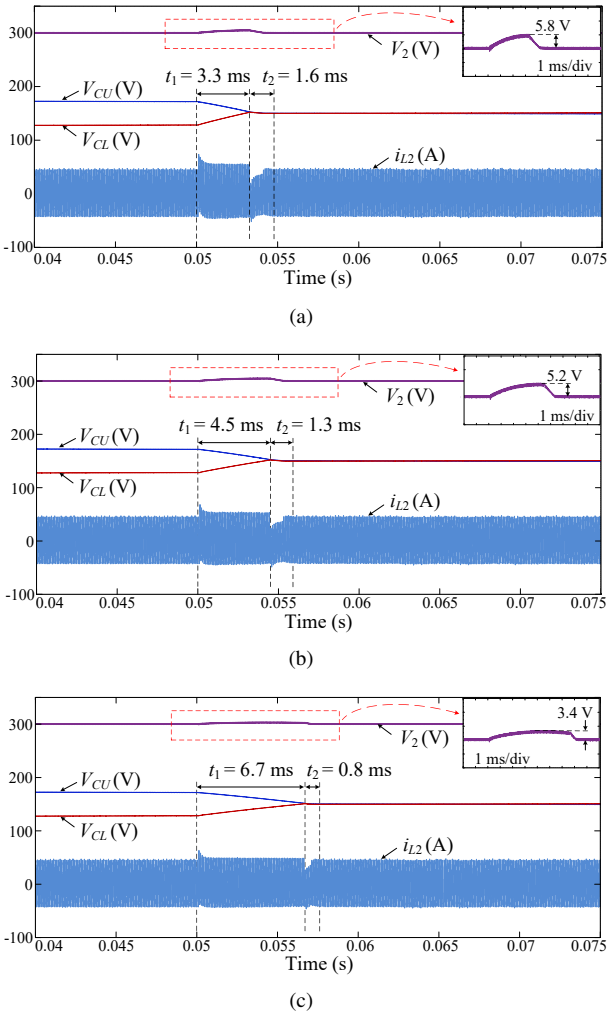


Fig. 9. Simulation results with the traditional capacitor voltage balancing control scheme when $V_{CU} - V_{CL} = 50$V with: (a) K = 0.3. (b) K = 0.2. (a) K = 0.1.

L_s is 100 μH, the capacitors C_1, C_U and C_L are 1000 μF, and the switching frequency f_s is 10 kHz.

The simulation results by using the traditional balancing scheme as shown is given in Fig. 9, in which the control variables $\alpha_3 = 0.22T_{hs}$, $\triangle\alpha = 0.3T_{hs}$, and α_2 is set as the output of the PI controller in the closed-loop control system to regulate the output voltage. From the modulation analysis in Section II, the phase shifts and duty cycles of all the gate driving signals can be determined by these three control variables. In the traditional balancing control scheme, the multiplier M is set as 1. Since $\beta_1 \leq \triangle\alpha$ and $\beta_2 \leq \triangle\alpha$, the maximum value of K is $0.3T_{hs}$, and the simulation results are shown in Fig. 9 (a). In Fig. 9 (a), an initial voltage unbalance of 50 V is given ($V_{CU} - V_{CL} = 50$V), and at $t = 0.05$s, the balancing control scheme is activated. It can be seen that during the balancing process, current fluctuation occurs in i_{L2}, causing the current overshoot. Compared with the steady-state peak current 48 A, the peak value of the current overshoot reaches 74 A. From the zoom-in waveform of V_2, it can be

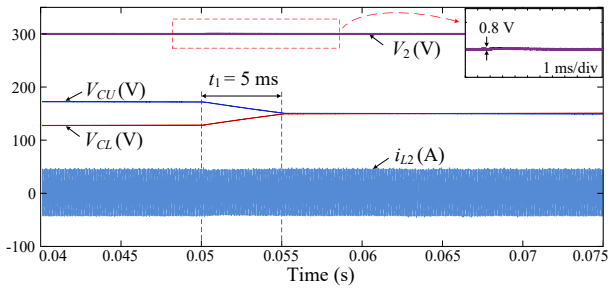


Fig. 10. Simulation results with the proposed CSV scheme when $V_{CU} - V_{CL} = 50$V.

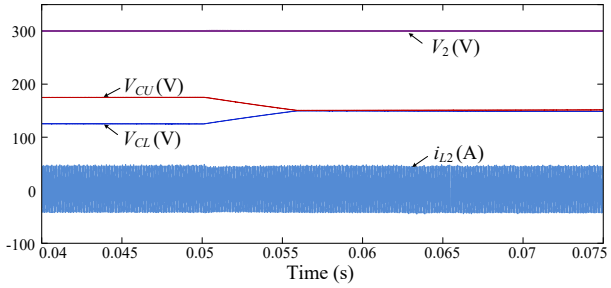


Fig. 11. Simulation results with the proposed CSV scheme when $V_{CL} - V_{CU} = 50$V.

seen the output voltage will also fluctuate during the balancing process. The capacitor voltages balance after $t_1 = 3.3$ ms. After that, it will take another time interval $t_2 = 1.6$ ms to reach the steady state due to the output voltage fluctuation during the balancing process. That is to say, t_1 is the time for balancing the two capacitor voltages, and t_2 is the time for achieving the reference output voltage. Therefore, in the traditional balancing control scheme, the total settling time is 4.9 ms (i.e., $t_1 + t_2 = 4.9$ms). When decreasing the value of K, the peak current will be reduced. For instance, in Fig. 9 (b) and (c), K is set as 0.2 and 0.1, respectively. It can be seen that the peak current is reduced to 66 A in Fig. 9 (b), and to 60 A in Fig. 9 (c). However, the settling time will be increased with the decreased K, which is 5.8 ms and 7.5 ms in Fig. 9 (b) and (c), respectively.

With the same parameters, the simulation results by using the proposed CSV scheme are shown in Fig. 10. It can be seen that there is no obvious current fluctuation during the balancing process, and the output voltage almost keep constant. The capacitor voltages become equal after 5 ms, which is also the total settling time due to no output voltage fluctuation. From Fig. 9 and Fig. 10, it can be seen that compared with the traditional balancing control scheme, the proposed balancing control scheme can smooth the dynamic current and output voltage waveforms, which avoid the current overshoot and improve the dynamic performances. Besides, the total settling time of the proposed scheme only slightly increases compared to that of the traditional balancing scheme with the maximum K. However, when the value of K is decreased to reduce the peak value, the dynamic process can be longer than that of the proposed scheme. Overall, the proposed balancing scheme can eliminate the power fluctuation, and obtain a relatively short dynamic time. Besides, Fig. 11 gives the simulation results when $V_{CL} - V_{CU} = 50$V. It can be seen that when V_{CU} is lower than V_{CL}, the proposed scheme can also balance the capacitor voltages without output voltage fluctuation and current overshoot.

V. Conclusion

This paper proposed a capacitor voltage balancing control scheme based on the CSVs for the 2/3-level DAB converters. The relationships among the polarity of the neutral-point current, the small vectors, and the polarity of the transformer current were summarized. Based on the analysis, two CSV pairs were obtained. In the proposed balancing control scheme, according to the operating condition, once a small vector is identified as an adverse small vector, it should be replaced by its CSV. After that, the waveforms of the current and voltage remain unchanged while the polarity of the neutral-point current changes. Therefore, the capacitor voltages can be regulated, and the current and output voltage fluctuation will be suppressed during the balancing process. Simulation results have verified that the proposed balancing scheme can eliminate the current overshoot and smooth the dynamic waveforms.

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