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Published in:
2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)

DOI (link to publication from Publisher):
10.23919/IPEC-Himeji2022-ECCE53331.2022.9806839

Publication date:
2022

Document Version
Accepted author manuscript, peer reviewed version

Statistical Performance Verification of the FS-MPC Algorithm Applied to the Matrix Converter

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***Abstract*—In recent publications statistical model checking (SMC) has been proposed as a method for verifying the performance of finite-set model predictive control (FS-MPC) algorithms applied to power electronics converters. SMC is a powerful method originating from statistics, which can provide statistical evidence of a system's performance in a stochastic environment. In this paper, SMC is applied to a direct matrix converter, which operates in a grid with different harmonic distortion levels and voltage sags. Using the proposed method it is possible to evaluate not only the performance of the control algorithm in terms of the output current distortion but also evaluate the effects of the weighting factor selection and grid distortions on the device utilization. The obtained results show that high grid distortions and voltage sags increase the number of switching cycles. This information can be of great importance to identify the most stressed devices and how the control algorithm can be adapted to extend the lifetime of the devices and thereby the system during different grid conditions at the very early stage of the converter system design.**

***Index Terms*—finite-set model predictive control, matrix converter, performance verification, statistical model checking**

I. Introduction

In the design of grid-connected power electronics converter systems, verification of the control algorithm is an important design stage as improper design might have a high influence on other units operating in the grid [1]. Moreover, nowadays the importance of design for reliability (DfR) has increased [2], the influence of the control algorithm on the stress of the components becomes more relevant and it should be explored before implementing the control algorithm. For linear control based algorithms, methods for evaluating the performance and stability are well established, while for control algorithms like model predictive control (MPC), whose popularity in power electronic converter applications is increasing, the methods for verifying the performance and stability are still under development [3].

Available control algorithm verification methods in power electronics systems [4] include simulations, symbolic model checking (MC), statistical model checking (SMC), hardware-in-the-loop (HiL) and experiments. Each of them has its advantages and disadvantages, providing at the same time different kinds of feedback information and it is typically applied at different stages of converter system development. Formal verification methods (e.g. symbolic MC and SMC), which use mathematical models, can be applied at the early stages of system development to increase the quality of the final product and to decrease the costs of design correction [5]. Symbolic MC [6] allows the analysis of dynamical systems modeled by state-transition systems and has been widely used for the verification of hardware and software in the industry. A system model is typically compared with user-defined requirements. As a result, an answer is given stating which properties are satisfied and which are not, in the second case - also supplemented with counter-examples. Symbolic model checking was applied for a direct matrix converter (DMC) in [7] for verification of structural properties, e.g., whether all system locations are reachable. Symbolic MC gives a 100% confidence, but it suffers from the state space explosion problem and it is not suitable for systems with stochastic components. Therefore, in many cases the system model has to be some kind of abstraction.

As an alternative, SMC was introduced, which can be treated as a combination of simulation and statistical methods [8], [9]. Instead of exploring the whole state space of the system, the distribution of samples obtained by simulating the stochastic system is used to obtain an estimated probability of the system having a certain property. It allows gaining statistically valid results that predict system behaviour with high confidence. Guidelines for applying SMC for control algorithm performance verification in power electronics applications were presented in [10], where the verification was focused on the effects of a stochastic load, weighting factor design and parameter mismatch on the reference tracking performance.

In this paper it will be demonstrated how an SMC approach can provide valuable information about the performance of the grid connected converters operating with the FS-MPC algorithm. The direct matrix converter with FS-MPC algorithm was selected as the application topology. Predictive control has been reported as the most promised alternative to control the matrix converter. However, due to the lack of performance verification tools, it was not possible to complete the benchmarking to other conventional methods in [11]. The SMC approach applied in this paper can provide the necessary information on how a grid connected matrix converter performs under different levels of harmonic distortions and types of voltage sags. In order to ensure safe operation of a grid-connected converter, algorithm performance in these conditions should

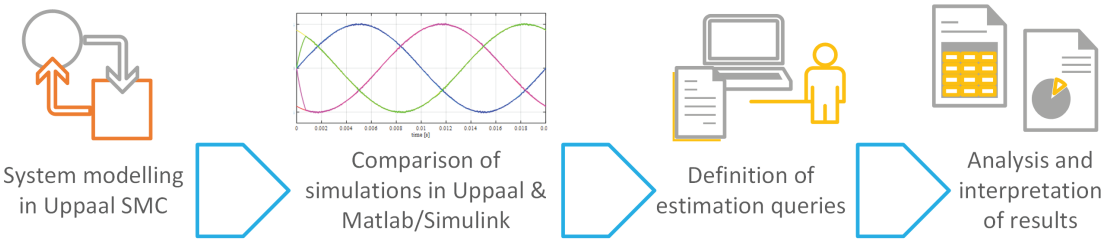


Fig. 1: Workflow of the control algorithm performance verification using UPPAAL SMC.

be analysed. On top of that, using SMC, the distribution of device thermal stress can be checked at the same time. Due to the fact that the FS-MPC algorithm has a variable switching frequency, it cannot easily be performed using conventional simulations. Different grid conditions paired with different weighting factors used in the algorithm will provide different stress distributions. Methods that explore a single run of the system, like simulations or experiments, will be unable to cover all the converter operating points or easily gain insight into the statistical evidence of the system performance.

Both modelling and verification of the matrix converter system are performed using UPPAAL SMC, a model checker toolbox, whose essential building blocks are timed automata structures (state machines). This fact makes it partially easy for implementation as the behaviour of FS-MPC algorithm can be represented using a state machine. Each stage of the verification workflow is illustrated in Fig. 1 and will be presented in detail in the following sections.

The rest of the paper is structured as follows. Section II provides some general information about the system model. Section III explains how the system can be modelled in the UPPAAL SMC toolbox to enable SMC. Section IV shows the results of the performed SMC, focusing on the effects of a stochastic grid behavior on the device stress and control performance and, additionally, the effects of the cost function on the device stress. Finally, section V concludes the paper.

II. SYSTEM MODEL

A direct matrix converter (DMC) [12] can be described as a power electronic system with a complex structure and with a large number of power electronic devices, responsible for a direct AC/AC conversion. Statistical model checking will be presented on the example of a direct matrix converter with a simplified load model. The load is modelled as a typical impedance with series connected R and L elements. The structure of the converter is a matrix of bidirectional semiconductor devices directly switching the three-phase power grid to the inductive load as shown in Fig. 2. It is possible to independently control the output currents and the input power factor. The converter is connected to the source through a low-pass input filter to eliminate high-frequency harmonics in the input currents and overvoltages from the network.

The converter will be operated using the FS-MPC algorithm presented in [11], [12], thus only a short algorithm description will be provided here. The FS-MPC algorithm control actions

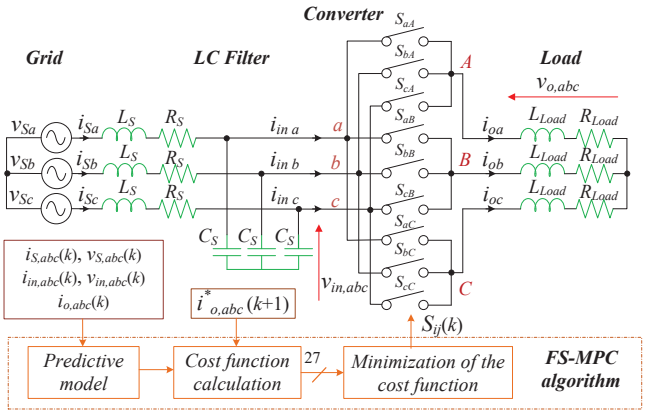


Fig. 2: Simplified direct matrix converter topology with FS-MPC algorithm.

are based on predicted values of the system variables. The predictions are calculated for all allowed converter operation states (27 in total) using the system model and afterward evaluated in the cost function. The converter state that will provide the minimum cost function value is selected among the allowed converter operation states. The source filter system model can be described by the state space equations in (1) and the load model by the equation (2), where L_F, R_{LF} and C_F represent the output filter inductance, resistance and capacitance, L_{Load} and R_{Load} are load inductance and resistance, respectively. The DMC model is defined by equations (3)-(4) describing the voltage and current relationships at the output and input:

$$\begin{bmatrix} \frac{dv_{in,\ abc}}{dt} \\ \frac{di_{S,\ abc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C_S} \\ \frac{-1}{L_S} & \frac{-R_S}{L_S} \end{bmatrix} \begin{bmatrix} v_{in,\ abc} \\ i_{S,\ abc} \end{bmatrix} + + \begin{bmatrix} 0 & \frac{-1}{C_S} \\ \frac{1}{L_S} & \frac{-R_S}{L_S} \end{bmatrix} \begin{bmatrix} v_{S,\ abc} \\ i_{in,\ abc} \end{bmatrix} \quad (1)$$

$$L_{Load} \frac{di_{o,\ abc}}{dt} = v_{o,\ abc} - R_{Load} i_{o,\ abc} \quad (2)$$

$$\begin{bmatrix} v_{oa} \\ v_{ob} \\ v_{oc} \end{bmatrix} = \begin{bmatrix} s_{aA} & s_{bA} & s_{cA} \\ s_{aB} & s_{bB} & s_{cB} \\ s_{aC} & s_{bC} & s_{cC} \end{bmatrix} \begin{bmatrix} v_{in\ a} \\ v_{in\ b} \\ v_{in\ c} \end{bmatrix} \quad (3)$$

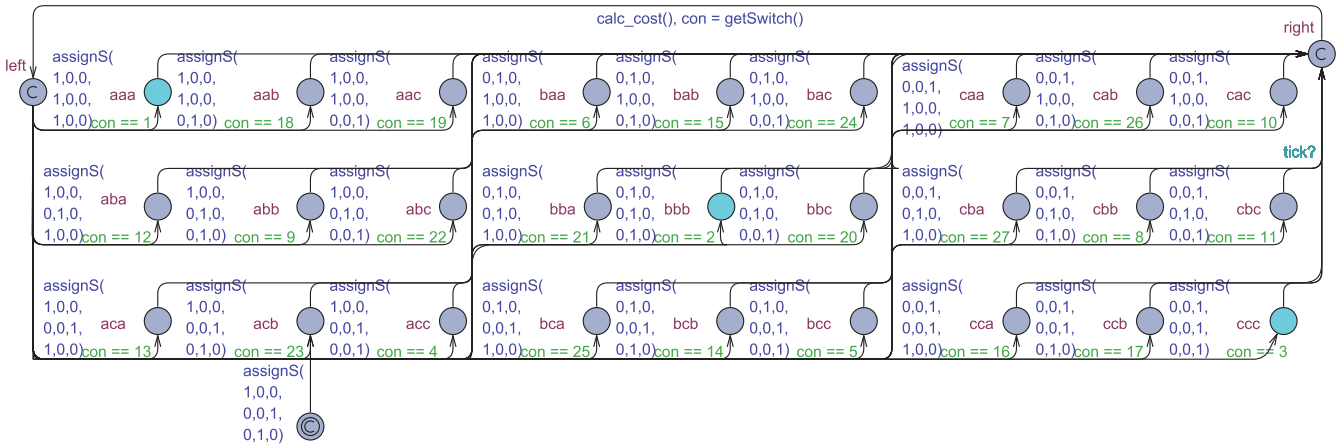


Fig. 3: Controller model in UPPAAL SMC.

$$\begin{bmatrix} i_{in\ a} \\ i_{in\ b} \\ i_{in\ c} \end{bmatrix} = \begin{bmatrix} s_{aA} & s_{aB} & s_{aC} \\ s_{bA} & s_{bB} & s_{bC} \\ s_{cA} & s_{cB} & s_{cC} \end{bmatrix} \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \tag{4}$$

where $v_{S,\ abc}$ and $i_{S,\ abc}$ are the grid voltages and currents, $v_{in,\ abc}$ and $i_{in,\ abc}$ are the converter input voltages and currents, $v_{o,\ abc}$ and $i_{o,\ abc}$ are the load voltages and currents and $s_{xy} \in (0, 1)$ define the switching states of the converter devices shown in Fig. 2 for $x, y \in a, b, c$. Using the forward Euler method, equations (1) and (2) are discretized and used to calculate the predictions. New measurements of signals $v_{S,\ abc}$, $i_{S,\ abc}$ and $v_{in,\ abc}$ and $i_{o,\ abc}$ are obtained for each sampling period. Accurately tracking the reference output current $i^*_{o,\ abc}$ by shaping the appropriate output voltage of the converter is the main goal of the algorithm. A secondary control objective with the goal of maintaining unity input power factor is also defined. For these purposes, the cost function is defined as:

$$g = \lambda_1 \left(|i^*_{o\alpha} - i^p_{o\alpha}| + |i^*_{o\beta} - i^p_{o\beta}| \right) + \lambda_2 |v_{S\beta} i^p_{S\alpha} - v_{S\alpha} i^p_{S\beta}| \tag{5}$$

where indices α and β - are the real and imaginary part of the respective three-phase voltages and currents described in the complex reference plane, $i^p_{S,\ abc}$ and $i^p_{o,\ abc}$ are the predicted values obtained using the system model, λ_1 and λ_2 are the weighting factors.

III. MODELING THE SYSTEM IN THE UPPAAL TOOLBOX

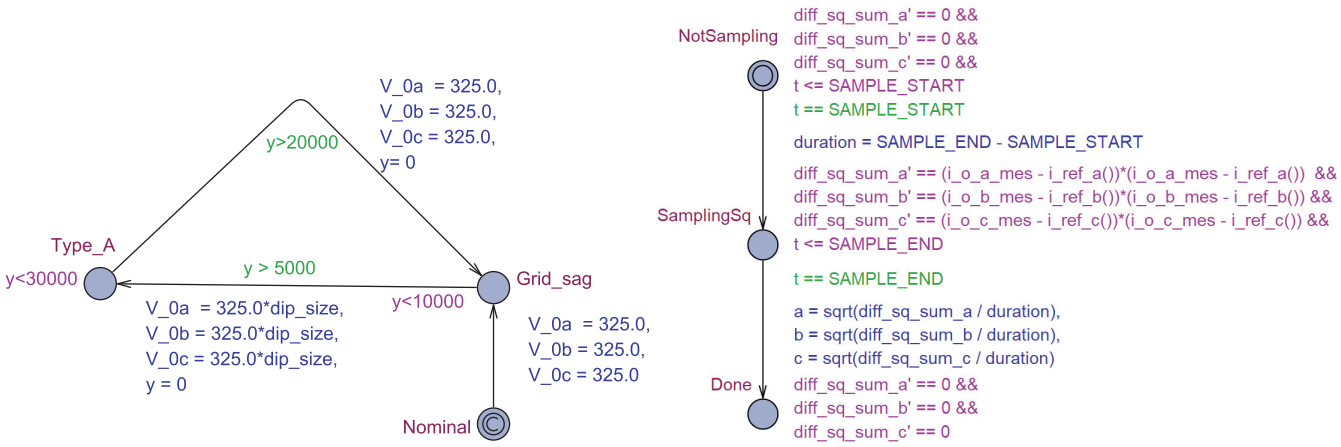
In order to formally verify the performance of a designed matrix converter, it is first necessary to present it as a network of timed automata (Figs. 3-5). The core component is the Controller model (shown in Fig. 3), with 27 available locations, which are chosen based on the result of calculating the cost function (5). The model represents two components from Fig. 2: converter and the control algorithm. Each location of the controller model has a unique name related to the switch configuration. For example: location aac indicates that in this location the output terminals of the matrix converter *A* and *B* are connected to the input terminal *a* and the output terminal *C* is connected to the input terminal *c*. Before reaching the location, to each switch of the matrix converter will be assigned to appropriate values (switching signals 1 or 0, i.e., ON and OFF) that can realize the state defined in that location (e.g. $assignS(1, 0, 0, 1, 0, 0, 0, 0, 1)$ for location aac). On each transition edge there is a guard for choosing the particular location, resulting from calculating the cost function (e.g. $con == 19$ for location aac). The transition from one location of a controller to the next is triggered by a synchronization component. The synchronization component sends the *tick* signal to the Controller model every 25 time units, which equals to sampling time of 25 μs. The system voltages and currents are defined in a physical system automaton (Fig. 5) as a system of first-order differential equations. They are obtained from the system model equations given in (1)-(4) and multiplied by the GLOBAL FACTOR = 10^{-6}, so the system will have the same dynamics as an equivalent simulation model with a sample time of T_s = 1 μs.

One of the metrics that will be used to evaluate the performance of the algorithm is the root mean square difference of the load current (RMSD), defined by the equation:

$$RMSD = \sqrt{\frac{\sum_{j=1}^{N} (i_j - i^*_j)}{N}} \tag{6}$$

where N represents the number of samples, i_j is the measured load current and i^*_j is the reference current. The RMSD model in UPPAAL SMC is shown in Fig. 4b. It can be noticed that three values are calculated, namely a, b and c, which represent the RMSD of each phase. These values will be compared under various combinations of grid sag types and distortion levels.

To assess the performance of the algorithm, a stochastic grid model is used. Three levels of grid distortions (no/low/high distortion) are modelled separately. The structure of the low/high distortion models is the same (leading from a perfect grid), the values and equations are adjusted for the particular distortion. The low distortion grid corresponds to the compatibility level of harmonics defined by the IEC 61000-2-4 [13], while the high distortion grid – to the immunity level of



(a) Grid sag type A. (b) RMSD.

Fig. 4: Model of grid sag type A and root mean square difference (RMSD) in UPPAAL SMC where V_{0a}, V_{0b}, V_{0c} are the amplitudes of the grid voltages and a, b, c are the load current RMSD values for each phase.

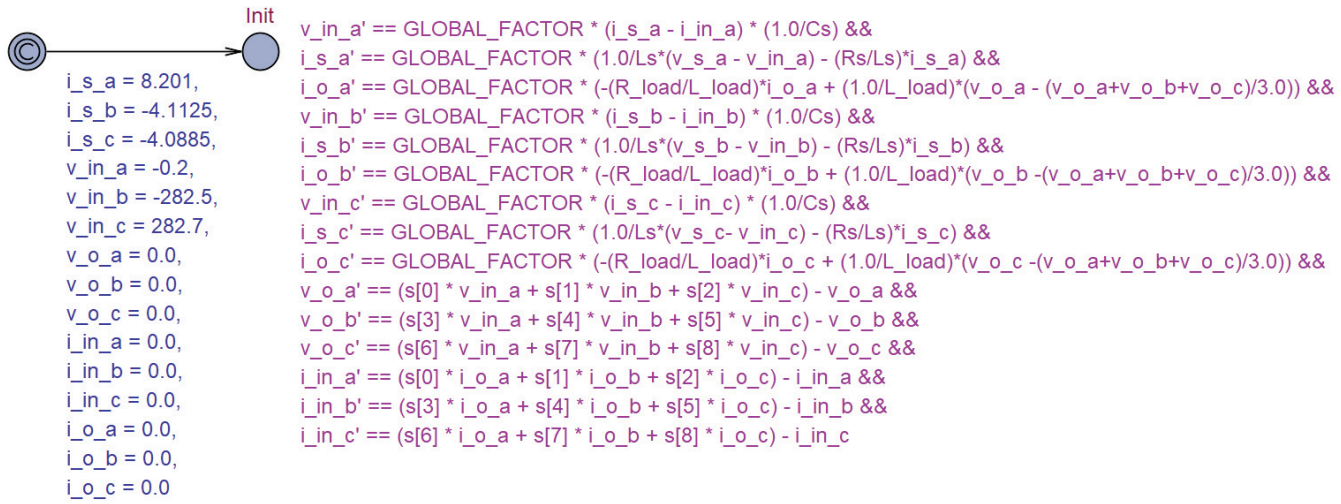


Fig. 5: Model of the physical system in Uppaal SMC.

harmonics defined by the IEC 61800-3 [14]. The grid voltage waveforms are shown in Fig. 6.

In the ABC classification, seven grid sag types are defined based on the fault type, transformer winding connection and load connection [15]. For the application presented in this paper, grid sag types - A, B and E - were selected. As an illustration, a model of grid sag type A in UPPAAL SMC is shown in Fig. 4a. Initially, the nominal grid parameter values are used and then randomly changed to model the stochastic behaviour of the grid, also depending on the depth of the sag size. In Fig.7a the voltage waveform during sag type A and low level of grid distortion can be observed. This type of sag influences all three grid phases by reducing the voltage amplitude for a certain period. Sag type B influences only one phase, selected randomly as shown in Fig.7b. Finally, sag type E shown in Fig. 7c, will influence two phases, also chosen randomly (during one simulation all phases have the same likelihood to experience a voltage sag).

Any combination of distortion and grid sag type can be modeled, thus e.g. perfect grid and grid sag type A, low distortion and grid sag type B, or high distortion and grid sag type E. This allows comparing the performance of the FS-MPC algorithm under various conditions and can be checked as it is demonstrated in the next section.

IV. STATISTICAL MODEL CHECKING

Performance verification has been carried out using the UPPAAL SMC toolbox [16]. Before evaluating various queries, multiple simulations have been performed and compared with Simulink simulation results to make sure that the system has been correctly modelled. Only after successful checking (and comparison) of simulation results, the results obtained in SMC can be treated as correct and representative. Two

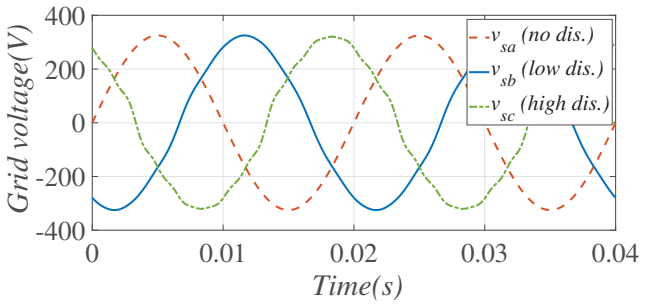
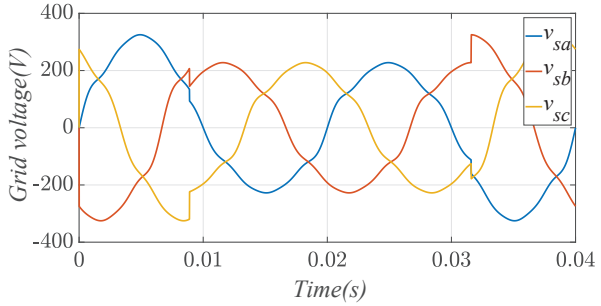
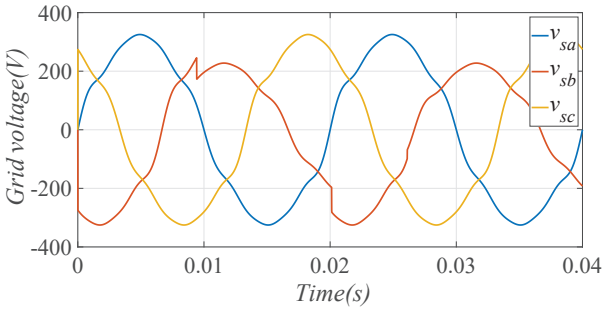


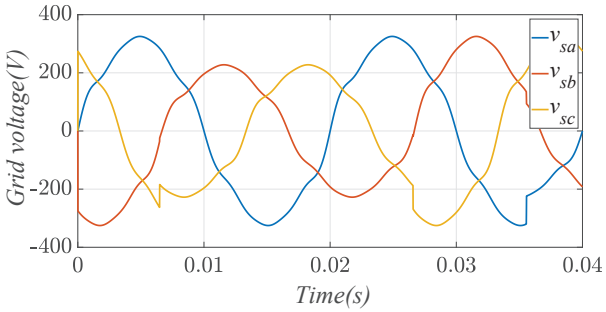
Fig. 6: Grid voltage waveforms: no distortion (no dis.), low distortion (low dis., compatibility level), high distortion (high dis., immunity level).



(a) Grid sag A.



(b) Grid sag B.



(c) Grid sag E.

Fig. 7: Waveforms of the grid voltage sag types. Sag duration and location are selected randomly in each simulation run.

types of queries have been defined, i.e. probability and value estimation. Probability estimation (quantitative model checking) returns the probability of a path expression being true in the defined interval of the simulation (0, END) given that the predicate in probability brackets is true (e.g., $Pr[<= END](<> (Rmsd.a > 0.1))$). Value estimation returns the expected mean value of an expression (e.g., $E[<= END](max : Rmsd.a)$) by running a given number of simulations. The duration of a single simulation was set to END = 4400, which corresponds to 44 ms. The number of simulations affects directly the verification time. Afterward, the obtained results can be compared, analysed and interpreted to show how they influence the performance. The verification of stochastic models is much more time-consuming than for fully deterministic models, but all defined queries could be verified within a reasonable time for this application.

A. *Effects of the stochastic grid on the device stress*

SMC was first applied to verify how different levels of grid distortion affect the utilization of the devices. For this purpose two performance metrics were monitored for each device of the matrix converter: the number of switching cycles (Fig. 8), and the conduction time during 20 fundamental cycles (0.2 s) (Fig. 9). The mentioned metrics are connected to device switching and conduction losses. Device switching losses depend on the load current, junction temperature and duty cycles, while switching losses depend on the load current, load type, DC-link voltage, junction temperature and switching frequency [17]. Both the duty cycle and switching frequency are in the case of the used FS-MPC algorithm variable, thus it is not easy to connect the expected thermal stress to the operation of the converter. What is also common for both loss types is the dependency on the current amplitude. As low amplitude currents do not produce high switching losses when counting the number of switching cycles for the purpose of comparing the switching stress during different distortions, the cycles where the device current was below 60% of the reference were not included in the stress analysis. Similar, the time intervals where the current flowing through the device was below 60% were not included in the conduction time.

In the presented case, the λ_2 was set to 0, i.e., the reactive power compensation was not active. It can be observed that three devices in each phase (S_1, S_5, S_9) have a significantly larger switching and conduction stress. For the conduction intervals, the grid level distortion did not have an impact, but a higher number of switching cycles was observed for almost all devices when the grid distortion was high. This means that the converter had to increase the switching effort to supply the load with a sinusoidal current, thus the switching stress applied to the devices was also increased.

B. *Effects of the cost function on the device stress*

The device utilization has also been evaluated for the cost function with reactive power compensation ($\lambda_2 = 0.01$) in Fig. 8 and Fig. 9. It can be observed, that for both cost functions, the amount of switching cycles is the highest for a high grid distortion, and the lowest for a grid without distortion, but the absolute values for $\lambda_2 = 0.00$ and $\lambda_2 = 0.01$

differ a lot. For example, the number of switching cycles of the S_1 switch is almost 3000 when $\lambda_2 = 0.00$, in comparison to half of the value when $\lambda_2 = 0.01$ (taking into account the same time period). Moreover, for the conduction interval it can be noticed that the distribution is even more unbalanced, e.g., devices (S_1, S_5, S_9) for $\lambda_2 = 0.00$ conduct approximately for the same amount of time, while for $\lambda_2 = 0.01$ this is no longer the case. It can be concluded that by tuning the weighting factor λ_2, the number of switching cycles can be reduced. In this way, SMC can be used to assess if the weighting factor, which was selected in the steady state using some of the available weighting factor design methods, does also provide the required performance metrics in a stochastic environment with high harmonic distortion and voltage sags.

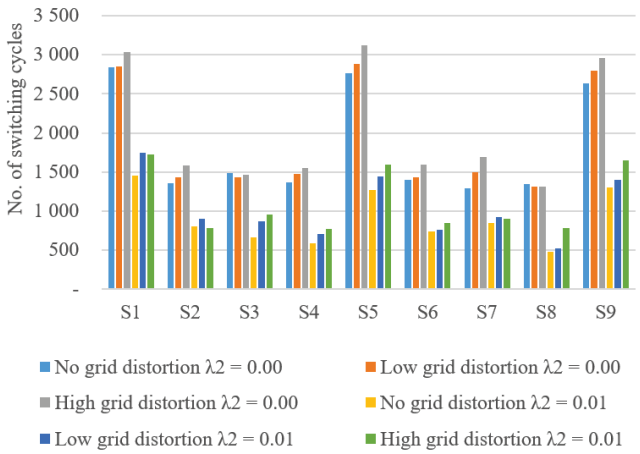


Fig. 8: Number of device switching cycles for different levels of grid distortion and λ_2.

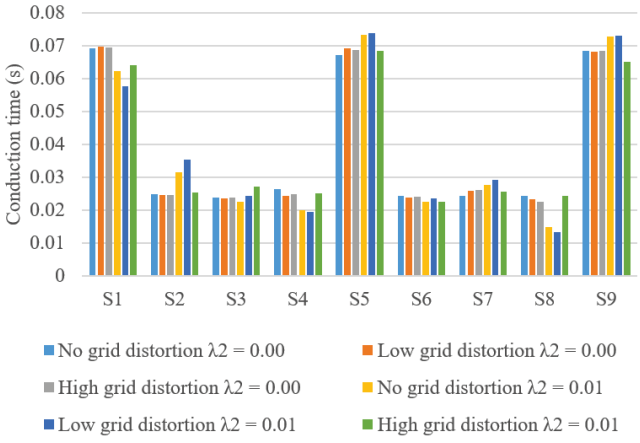


Fig. 9: Device conduction time for different levels of grid distortion and λ_2.

C. Effects of the stochastic grid on the control performance

The average $RMSD$ of the converter output current ($i_{o,abc}$), expressed as an % of the reference current value, has been evaluated for various combinations of grid voltage sags and grid distortions. The results are summarized in Fig. 10. It can be observed that for all grid distortion combinations and sag types, which reduce the grid voltage amplitude for only 0.1 pu, the $RMSD$ will preserve a low value. For larger voltage sags (0.3 pu) the A type and E type voltage sags significantly degrade the performance of the control algorithm, as the results indicate 4% RMSD (two to three times larger than for 0.1 pu). It is interesting to observe that B type voltage sag, which is shown in Fig. 7 effects only one phase at a time, and does not significantly degrade the controller performance.

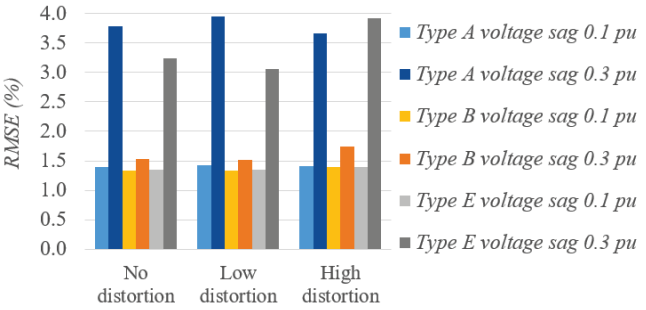


Fig. 10: Average root mean square difference ($RMSD$) obtained for different grid level distortions and voltage sags.

D. Experimental validation

In the experimental verification the FS-MPC control algorithm has been implemented using a DSP card with Analog Devices Sharc processor (ADSP-21369) and 12 A/D converters. The matrix converter is powered by programmable multi-functional power source NETWAVE 20.2, which is used to apply various types of low-frequency distortions to the three-phase supply voltage. Parameters of the experimental set-up shown in Fig. 11 are the following: $L_S = 1\ mH$, $R_S = 0.01\ \Omega$, $C_S = 60\ \mu F$, $L_{Load} = 44\ mH$ and $R_{Load} = 69\ \Omega$. FS-MPC algorithm cost function (5) was used with weighting factors λ_1 = 1 and λ_2 = 0.01.

The experiments were performed for the case of unbalanced source voltages where $U_{Sa} = 100\%$, $U_{Sb} = 90\%$, $U_{Sc} = 95\%$ of U_n as presented in Fig. 12 and for the case of high harmonic distortion of the source voltage in Fig. 13. It was observed in both cases that the output currents can follow the defined set of sinusoidal reference currents even with distorted source voltage and voltages dips.

V. Conclusion

SMC is proposed as an approach to verify the performance of the FS-MPC algorithm controlling a direct matrix converter connected to a stochastic grid model. The proposed converter system model, modelled in UPPAAL SMC, was used to verify how the controller performance and device stress distribution is affected by the different level of harmonic grid voltage distortion and voltage sags. It was observed that a higher level of distortion will increase the switching stress, thus it is important to include different levels of grid distortions in

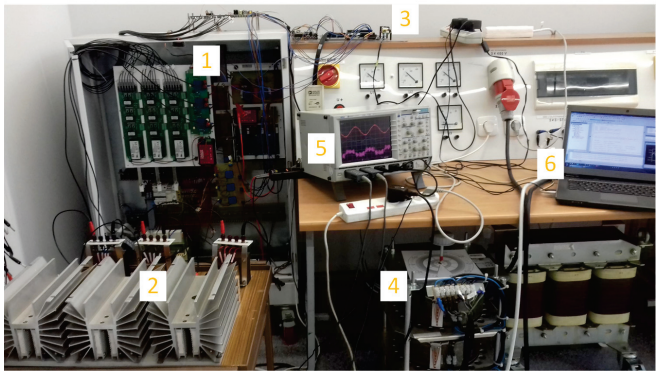


Fig. 11: Experimental set-up: matrix converter (1), RL load (2), DSP and FPGA control board (3), autotransformer (4), oscilloscope (5), PC (6).

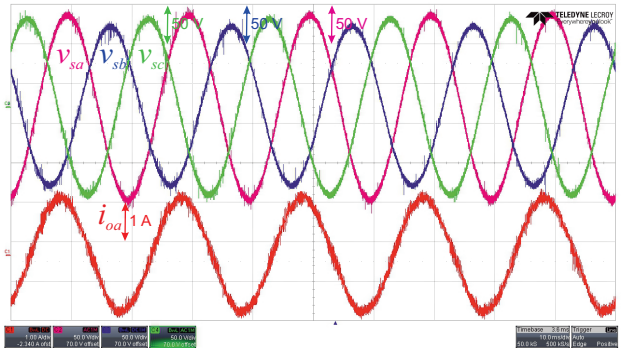


Fig. 12: Experimental results with voltage sags in the source voltages.

the verification. Moreover, device stress was not the same for different cost functions. This offers the possibility to define the weighting factors in the cost function for a different level of grid voltage distortion and reduce the degradations of the most stressed devices. Finally, it was demonstrated that not all types of voltage sags significantly degrade the performance of the control algorithm. As the proposed method requires most time to be invested in the modeling of the power electronics system, in future work we will focus on simplifying this procedure by providing building blocks for fast modeling of power electronics systems.

ACKNOWLEDGMENT

The work is supported by the Reliable Power Electronic-Based Power System (REPEPS) project at the AAU Energy, Aalborg University as a part of the Villum Investigator Program funded by the Villum Foundation.

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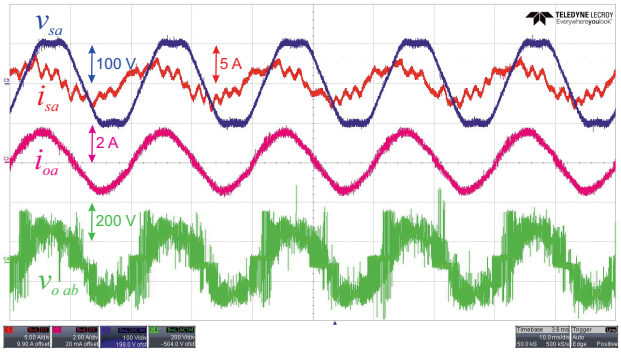

Fig. 13: Experimental results with harmonic distortion in the source voltages.

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