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# Parasitic Capacitance Modeling of Inductors Without Using the Floating Voltage Potential of Core

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***Abstract*—The analytical modeling of parasitic capacitances in inductors is commonly based on the energy-conservation law. Yet, in order to calculated the equivalent capacitances of inductors, the floating voltage potential of magnetic core is required to be pre-known in all previous modeling methods. This letter proposes an analytical method for calculating the parasitic capacitances of the inductors with low-resistivity cores, which does not require any prior knowledge of the floating core potential. The proposed modeling method can be extended to the transformers as well as multi-terminal magnetic devices. The experimental results verify the effectiveness of the proposed method.**

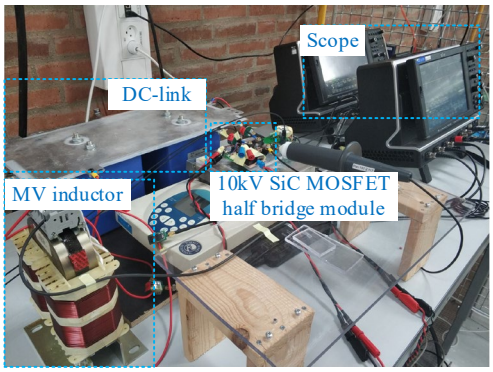
***Index Terms*— *Parasitic capacitance, inductor, floating core potential, analytical method*.**

## I. Introduction

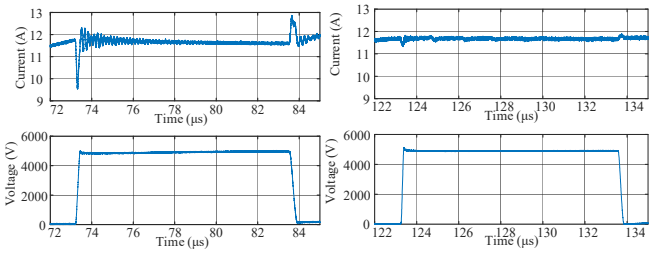
The modeling of parasitic capacitance in magnetic devices attracts increasing attention in modern power electronics applications [1-3]. Under the high $dv/dt$ operations, the parasitic capacitance of inductors contributes with the additional capacitive current circulating in the circuit and result in more switching noises, aggravating electromagnetic interference issues [4], [5] and worsening the reliability of power modules [6]. The setup and experimental waveforms of two different inductors used in 5000V/12A double pulse tests are shown in Fig. 1, where the inductor with air core (10 pF parasitic capacitance) has a smaller current spike compared to the inductor with amorphous core (60 pF parasitic capacitance), since the smaller parasitic capacitances contribute to less capacitive currents. Therefore, it is important to model and reduce the parasitic capacitance of inductors and transformers [7]-[12].

The physics-based modeling methods that are based on the energy conservation law have been widely used in deriving the equivalent parasitic capacitance of inductors and transformers [8]-[11]. The inductor with a floating core is modeled as a two-terminal component, where only one parasitic capacitance is aimed to be identified [8], [10]. In order to simplify the models, the low-resistivity cores, e.g., nanocrystalline core, silicon steel core, and amorphous core, are usually assumed to be perfect conductors without any ohmic voltage drops in previous research works [8], [10], [11].

Although effective, the previous methods have a common restriction, that is, the floating voltage potential on the inductor core needs to be known before modeling. The floating core potential on the core can be identified by applying Kirchhoff's current law into a simplified lumped circuit of inductors [10], but with limitations in characterizing the three-terminal equivalent circuit of inductors. Finite-element-method (FEM) simulations are also applicable to simulate the floating core potential of inductors, yet it requires a 3-dimensional computer-aided design model for initiating the simulations [10], where the model complexity is still high for engineers.




(a)




(b) (c)

Fig. 1 Inductor current and output voltage in 5000V/12A double pulse tests with two different inductors. (a) a picture of the DPT setup; (b) 30 mH inductor with amorphous core, equivalent parasitic capacitance is 60 pF; (c) 49 mH inductor with an air core, equivalent capacitance is 12 pF.

The inductor with a grounded core can be described as a three-terminal component, where the three capacitances between the each of these terminals can be characterized individually [11]. A similar method for characterizing the six

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parasitic capacitances in a four-terminal circuit is also introduced for the planar transformer design [12]. However, the method given in [12] is only applicable for analysis using the FEM simulations as well as in final measurements, which is not an analytical solution, and thus, the floating core potential is simulated by FEM software directly (it is unnecessary to know the floating core potential in practice measurements). Therefore, it is still a challenge to find a general representation of the parasitic capacitance in inductors without using the floating voltage potentials of the cores.

Thus, this letter proposes a modeling method to analytically calculate the parasitic capacitances in the inductors, which, in contrast to conventional methods, offers one prominent feature: no prior knowledge on the floating voltage potential of the core is required. The inductor is characterized as a three-terminal component first, where the floated core is regarded as an individual terminal. Further, three equivalent capacitances between the two terminals and the core are derived without having a prior knowledge of the floating core potential, where the parasitic capacitances between the terminals and core are derived. Upon the three identified capacitances, a three-terminal equivalent circuit of the inductor is built, which can be readily simplified to a two-terminal equivalent circuit. Then, the parasitic capacitance in the inductor with a floating core is obtained. Finally, experimental results verify the theoretical analysis.

## II. Limitation of the Conventional Approach

In this section, the limitation of the conventional approach for calculating parasitic capacitances of the inductors with floating low-resistivity cores is addressed.

### *A. Static and dynamical capacitances*

This paper classifies the parasitic capacitances into two types: i) static capacitance $C_{sta}$ and ii) dynamical capacitance $C_{dyn}$. The static capacitance is only dependent on the geometrical structure and the physical properties of the materials, thus with given geometrical structure and material of the inductors, the static capacitance is constant. When the inductor is being used in the circuit, the voltage drop occurs across the winding due to the current flow, which gives rise to capacitive couplings across different segments. Such capacitive couplings will store the electrical field energy, where the equivalent capacitance to represent the actual stored electrical field energy is named as dynamical capacitance in this letter. Both static capacitance and the voltage potential distribution will determine the stored electrical field energy. The concept is in line with the approach reported representations for the final calculated capacitance. The dynamical capacity under dynamic load can be a complex situation to handle but as will be shown later can be managed using the energy-based approach which gives an effective way of solving for the equivalent dynamic capacitance [3], [8], [9]-[11], [15].

In this letter, the voltage potential in the winding is assumed to be distributed linearly with the equal ohmic voltage drop $\Delta V$ contributed by resistance and inductance, before the first resonant point when the inductor is in active use. The voltage potential on the core is equal due to the perfect conductor assumption, where the low-resistivity cores are using.

### *B. Example of a two-dimension inductor*

In order to intuitively elaborate the principle of both static and dynamical capacitances in this letter, an inductor in two-dimension (2D) is used as the example in this letter, where the schematic is given in Fig. 2. It is noted that the modeling method can also be applied to 3D structures. Here the 2D inductor is chosen for the sake of simplicity.

Three static parasitic capacitances are considered in this letter: i) Static capacitance between two adjacent layers $C_{stall}$, ii) Static capacitance between the inner layer and core $C_{stalc}$, and iii) Static capacitance between the adjacent turns $C_{statt}$.

It is mature to analytically calculate the static capacitances $C_{stalc}$, $C_{stall}$, and $C_{statt}$, with using the known geometrical structures and material information [8], [10], [11]. Detailed derivations of $C_{stalc}$, $C_{stall}$, and $C_{statt}$ are also given in Appendix A. The values of these capacitances depend on geometrical and material parameters. The static capacitances mentioned in this paper are also named “inherent capacitances” in [10], “lumped capacitances” in [11], and “disconnected capacitances” in [8].

In order to calculate the dynamical capacitance, an accurate voltage potential of the floating core is required to be pre-known, which will significantly influence the calculated dynamical capacitance $C_{dynlc}$ between the winding and core.

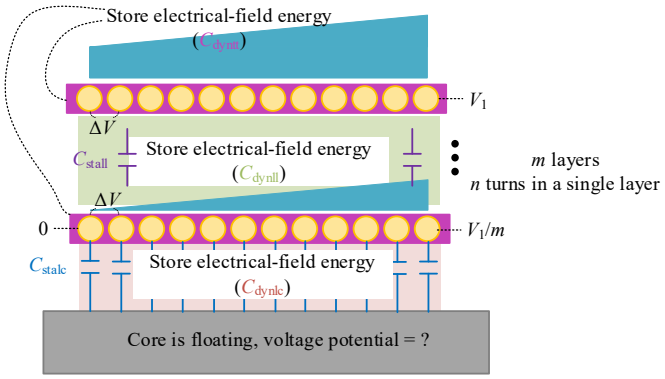



Fig. 2 Schematic of the electrical-field energy stored in between the winding and core (Blue triangles represent the voltage potential distribution in the winding)

It is assumed in the following that the voltage potential on the core is $V_{core}$, the voltage potential at the terminal of the inner layer is 0, and the voltage potential at the terminal of the outer layer is $V_1$, where $V_1=nm\Delta V$. $C_{dynlc}$ is derived as (1) according to [11]. The edge effects (fringe electrical field) are neglected in order to reduce the complexities the analytical model of the exampled 2D inductor.

$$C_{dynlc}=\frac{1}{3V_1^2}\left(\frac{V_1^2}{m^2}-\frac{3V_1V_{core}}{m}+3V_{core}^2\right)C_{stalc}$$

$$C_{dynll}=\frac{4(m-1)}{3m^2}C_{stall} \tag{1}$$

$$C_{dyntt}=\frac{m(n-1)}{(nm)^2}C_{statt}$$

where $m$ is the number of layers. The detail derivations of $C_{\text{dynlc}}$ and $C_{\text{dynll}}$ are attached in Appendix B.

According to (1), both $C_{\text{dynll}}$, $C_{\text{dynlc}}$, and $C_{\text{dyntt}}$ depend on $m$, but it is noted that $C_{\text{dynlc}}$ additionally depends on the floating core potential.

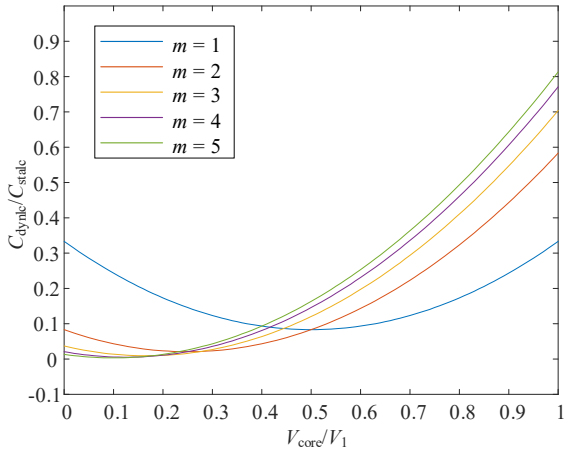
Using $C_{\text{dynlc}}/C_{\text{stalc}}$, $C_{\text{dynll}}/C_{\text{stall}}$, $C_{\text{dyntt}}/C_{\text{statt}}$, $V_{\text{core}}/V_1$, and $m$ as the variables, (1) are represented by three figures given in Fig.3 (here $n$ is assumed as 1). It can be seen that $C_{\text{dynlc}}/C_{\text{statlc}}$ will significantly change under different core potential and the different number of layers, whereas $C_{\text{dynll}}/C_{\text{stall}}$ and $C_{\text{dyntt}}/C_{\text{statt}}$ are independent of the different core potential.

If the inductors with floating low-resistivity cores are represented as two-terminal equivalent circuits, only one total equivalent parasitic capacitance is needed whcih can be expressed addressed as (2).

$$C_{\text{total}} = C_{\text{dynlc}} + C_{\text{dynll}} + C_{\text{dyntt}} \tag{2}$$

### C. Limitation

It can be found that different floating core voltage potential finally results in a different dynamical capacitance between the winding and core, which will also influence the total equivalent capacitance of the inductor.

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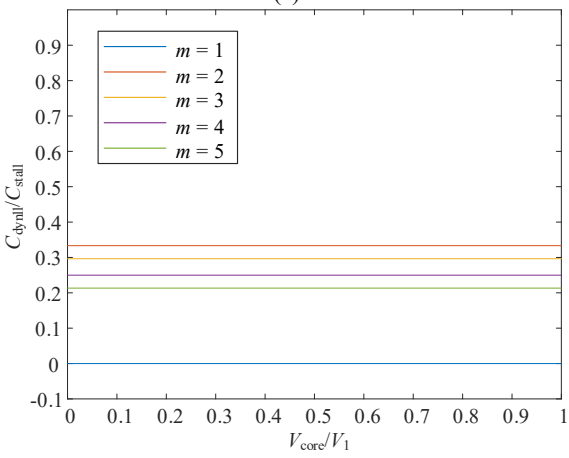


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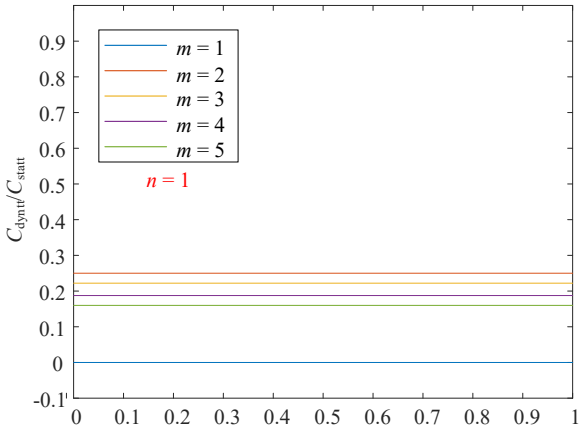



(c)

Fig. 3 Variation of (a) $C_{\text{dynlc}}/C_{\text{stalc}}$; (b) $C_{\text{dynll}}/C_{\text{stall}}$; (c) $C_{\text{dyntt}}/C_{\text{statt}}$($n$=1) with respect to different core voltage potential and number of layers.

In practice, with a given geometrical structure and input voltage of inductors, there is only a single deterministic value of the floating core potential. Thus, it is significant to get an accurate value of the floating core potential before modeling, where this value is calculated by estimations, simplifications or simulations in all previous research, which are either time consuming or inaccurate.

## III. Proposed Modeling Method

In contrast to using a two-terminal equivalent circuit to characterize the inductors with floating cores in previous research, this letter proposes using a three-terminal equivalent circuit, where the core is regarded as the third terminal of the circuit. Therefore, three capacitances, instead of one capacitance in the conventional method, need to be modeled in the proposed modeling method. The same two-dimension inductor illustrated in Fig. 2 is used in this section for elaborating the principle of the method.

Three different configurations given in Fig. 4 are used for numerical calculations, where the floating core potential is not needed in any of the three configurations.The terminal at the inner layer is defined as hot terminal $\text{P}_{\text{hot}}$ with a given voltage potential $V_0$, where the terminal at the outer layer is defined as cold terminal $\text{P}_{\text{cold}}$ with a given voltage potential $V_1$.

### A. Configuration 1

In this configuration, the current flows through the winding due to the different voltage potential at the terminals $\text{P}_{\text{hot}}$ and $\text{P}_{\text{cold}}$. Therefore, the voltage potential on the winding is linearly distributed. The core is connected to $\text{P}_{\text{hot}}$, then the voltage potential on the core is clamped to the same voltage potential as $\text{P}_{\text{hot}}$ due to the "perfect conductor" assumption.

Using the inductor given in Fig. 2 as an example, the total equivalent capacitance $C_{\text{total1}}$ in Configuration 1 is calculated as (3). The derivations of the dynamical capacitances are given in Appendix C.

$$\begin{aligned} C_{\text{total1}} &= C_{\text{dynlc}} + C_{\text{dynll}} + C_{\text{dyntt}} \\ &= \frac{1}{3m^2}C_{\text{stalc}} + \frac{4(m-1)}{3m^2}C_{\text{stall}} + \frac{m(n-1)}{(nm)^2}C_{\text{statt}} \end{aligned} \tag{3}$$

According to the right figures in Fig. 4(a), the total equivalent capacitance $C_{\text{total1}}$ in Configuration 1 is also given as (4) from the circuit model. $C_{\text{tt}}$ is the equivalent capacitance between $\text{P}_{\text{hot}}$ and $\text{P}_{\text{cold}}$. $C_{\text{tc2}}$ is the equivalent capacitance between $\text{P}_{\text{cold}}$ and Core.

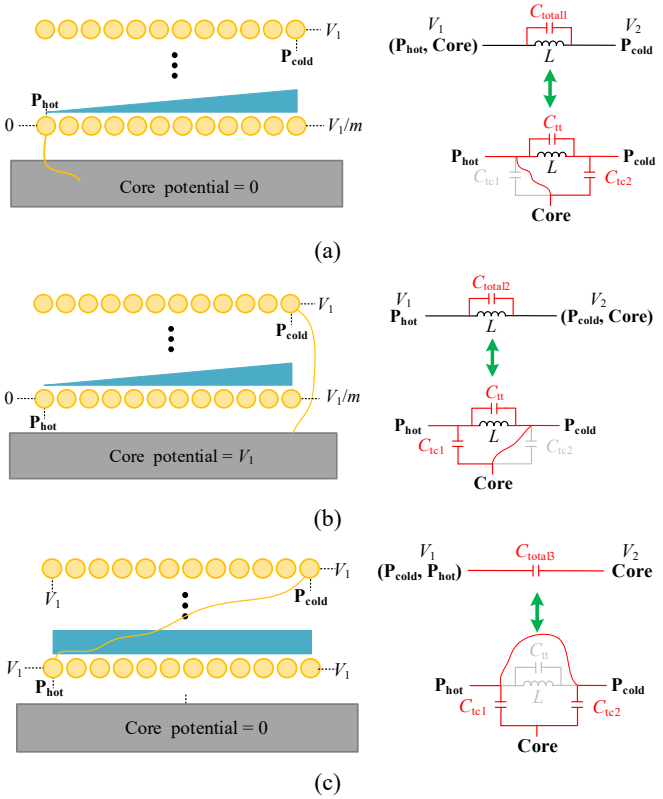



Fig. 4 Schematics for the three configurations. a) Configuration 1; b) Configuration 2; c) Configuration 3.

$$C_{\text{total1}} = C_{\text{tt}} + C_{\text{tc2}} \tag{4}$$

## B. Configuration 2

Since the current flows through the winding, the voltage potential on the winding is also linearly distributed in this case. However, the core is connected to $\text{P}_{\text{cold}}$, then the voltage potential on the core is $V_1$. Similarly, the total equivalent capacitance $C_{\text{total2}}$ of the inductor in Configuration 2 is derived as (5) and (6) in physics and circuit levels, respectively. $C_{\text{tc1}}$ is the equivalent capacitance between $\text{P}_{\text{hot}}$ and Core. The derivations of the coefficients of dynamical capacitances are given in Appendix D.

$$C_{\text{total2}} = \frac{3m^2-3m+1}{3m^2}C_{\text{stalc}} + \frac{4(m-1)}{3m^2}C_{\text{stall}} + \frac{m(n-1)}{(nm)^2}C_{\text{statt}} \tag{5}$$

$$C_{\text{total2}} = C_{\text{tt}} + C_{\text{tc1}} \tag{6}$$

## C. Configuration 3

The terminal $\text{P}_{\text{hot}}$ and $\text{P}_{\text{cold}}$ are shorted and clamped to the voltage potential $V_1$. The voltage potential on the core is clamped to the voltage potential 0. Therefore, there is no current flow through the winding, which means there is no ohmic voltage drop. Then the total equivalent capacitance $C_{\text{total3}}$ of the inductor in Configuration 3 is derived as (7) and (8), respectively. The derivations of the coefficients of dynamical capacitances are given in Appendix E.

$$C_{\text{total3}} = C_{\text{stalc}} \tag{7}$$

$$C_{\text{total3}} = C_{\text{tc1}} + C_{\text{tc2}} \tag{8}$$

It is worth mentioning that the voltage drops between segments of the same winding are zero, since there is no current flow through the winding. Thus, the dynamical capacitance s contributed by neighbour layers and neighbour turns are zero in this configuration. Moreover, according to the derivations in Appendix E, the coefficient for $C_{\text{dynlc}}$ is only one. Thus in (7), the total equivalent capacitance is exactly equal to $C_{\text{stalc}}$.

## D. Combination

By using (3), (5) and (7), the total capacitances are analytically calculated based on the geometrical structure and material information. Then, $C_{\text{tt}}$, $C_{\text{tc1}}$, and $C_{\text{tc2}}$ in the three-terminal equivalent circuit are derived by using the calculated $C_{\text{total1}}$, $C_{\text{total2}}$, $C_{\text{total3}}$, (4), (6), and (8). Once the three-terminal equivalent circuit shown in Fig. 5 is obtained, it is also able to be converted to a two-terminal equivalent circuit, which represents the same inductor when its core is floating. The total equivalent capacitance of inductors with a floating core is calculated as (9).

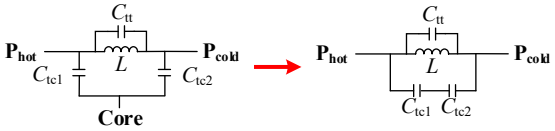



Fig. 5 Converting the three-terminal equivalent circuit to the corresponding two-terminal equivalent circuit when the core is floating

$$C_{\text{float}} = C_{\text{tt}} + \frac{C_{\text{tc1}}C_{\text{tc2}}}{C_{\text{tc1}}+C_{\text{tc2}}} \tag{9}$$

Throughout the calculation of capacitance in (3)-(8), the equivalent capacitances of the inductors with a floating core or grounded core is calculated, where the floating voltage potential on the core $V_{\text{core}}$ is not required.

It is worth mentioning that the(1), (3), (5), and (7) are dependent on the geometrical structures and material of inductors. Thus, (1), (3), (5), and (7) are only valid for the inductors with the inductor shown in Fig. 2 and Fig. 4. However, the (4), (6), (8), and (9) are general for all inductors, which are the equivalent representations of three-terminal equivalent circuits, and not limited by the geometrical structures and material of inductors. The calculated parasitic capacitances are valid up to the first resonant frequency of inductors, due to the assumption made before the derivation [8], [11], [15].

# IV. Experimental Verifications

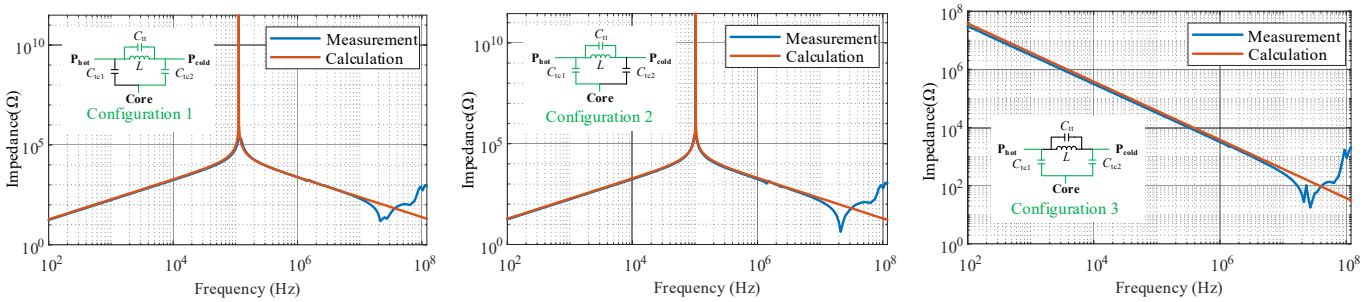
An MV copper-foiled filter inductor is used as the case study for verifying the principle in this letter. The impedance of the inductor in the above three different configurations are measured by using a Keysight E4990A impedance analyzer and its adaptor 16047 [13], from 20 Hz to 120 MHz [14] . Then a circuit model ($LC$ parallel circuit in Configuration 1 and 2, single $C$ circuit in Configuration 3) is applied to fit the

Table I Numerical comparisons of the experimentally measured and calculated parasitic capacitances of the inductor

| | $C_{dylc}$ | $C_{dyll}$ | $C_{total}$(Calculations) | $C_{total}$(Measurements) |
|---|---|---|---|---|
| Configuration 1 | 11.6 pF | 53.7 pF | 65.3 pF | 65.5 pF |
| Configuration 2 | 26.4 pF | 53.7 pF | 80.0 pF | 84.9 pF |
| Configuration 3 | 42.1 pF | 0 pF | 42.1 pF | 44.9 pF |

Table II Numerical comparisons of the parasitic capacitances for the different modeling methods

| Methods | Model in [11] | Model in [15] | Model in [10] | Model in this letter |
|---|---|---|---|---|
| Floating core potential | By estimating the value as the average potential in the inner layer | By estimating the value as 25% of the total winding voltage drop | By calculating the value based on the simplified circuit model and charge-conservation law | Not needed |
| Two-terminal equivalent circuit | 65.3 pF; $P_{hot}$, $L$, $P_{cold}$ | 61.1 pF; $P_{hot}$, $L$, $P_{cold}$ | 60.9 pF; $P_{hot}$, $L$, $P_{cold}$ | 60.8 pF; $P_{hot}$, $L$, $P_{cold}$ |
| Three-terminal equivalent circuit | 65.2 pF; $P_{hot}$ 14.7 pF; $P_{cold}$ 0 pF; $L$; Core | 52.1 pF; $P_{hot}$ 27.8 pF; $P_{cold}$ 13.2 pF; $L$; Core | Not valid | 51.6 pF; $P_{hot}$ 28.4 pF; $P_{cold}$ 13.7 pF; $L$; Core |




(a) (b) (c)

Fig. 8 Comparison between the measured and calculated impedance. (a) Configuration 1; (b) Configuration 2; (c) Configuration 3

Table III Measurements of the parasitic capacitances by using an impedance analyzer

| Methods | Floating core potential | Two-terminal equivalent circuit | Three-terminal equivalent circuit |
|---|---|---|---|
| Measurement results | Not needed | 62.0 pF; $P_{hot}$, $L$, $P_{cold}$ | 52.8 pF; $P_{hot}$ 32.2 pF; $P_{cold}$ 12.8 pF; $L$; Core |

measured impedance, where either $L$ or $C$ values are obtained as results [10], [11]. The calculated capacitances are only valid before the first resonant frequency of inductors, due to the assumptions made for deriving the static and dynamical capacitances [3], [8], [10], [11], [15]. A picture of the measurement setup is given in Fig. 7.

This inductor is constructed by two U-type amorphous cores, which are electrically connected by the steel belt [15]. The two windings are in parallel, where 190 layers of copper-foil are used in a single winding [15]. Since the total capacitances derived in Section II is only valid for the exampled 2D inductor, (3), (5), and (7) cannot be used for calculating the total capacitances of the copper-foiled inductor. However, the total capacitances of three configurations can be calculated by using the same method proposed in the letter and the derived static capacitances for copper-foiled inductor in [15]. Then, with using (4), (6), and (8), the three equivalent capacitances of the three-terminal equivalent circuit are obtained.

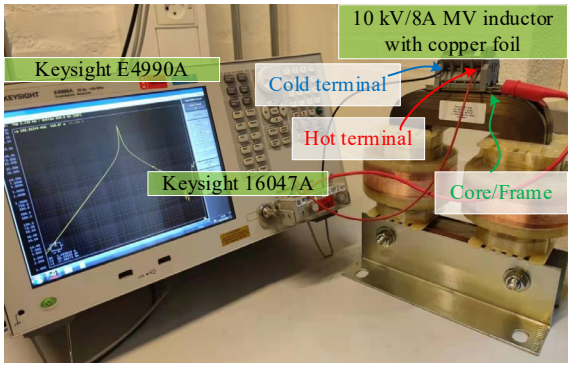


Fig. 7 A picture of the setup for measuring the impedance and parasitic capacitances of inductors

With using (9), the equivalent capacitance of the copper-foiled inductor with a floating core is obtained. The calculated capacitances are listed in Table I and II. In order to plot the equivalent impedance for three configurations, the inductance of the copper-foiled inductor used in calculations is assumed to be known as 30 mH as the designed value, where the impedance is given in Fig. 8.

The total equivalent capacitances of the inductor in these three configurations are measured by using the setup shown in Fig. 7, where the measured impedances of the inductor under three configurations are compared to the calculated impedance.

Fig. 8 compares the calculated impedances (red curve) with the measured impedances (blue curve). In Fig. 8(a) and (b), the calculated impedance has a large magnitude at the resonant frequency since the damping resistance is not modeled in this letter. With using the parallel LC circuit fitting analysis together with the Keysight E4990A impedance analyzer, the equivalent parasitic capacitances of the inductor with three configurations are measured and listed in Table. I, where the fitted inductance is 27.5 mH from the impedance analyzer.

The calculated parasitic capacitance is compared to three conventional modeling methods and measurement methods in Table I, which require to estimate or calculate the floating core potential before calculating the total equivalent capacitance of inductors. The first two columns by using the modeling methods proposed in [11] and [15] are based on the estimations of the floating core potential, where both two-terminal and three-terminal equivalent circuits of the inductor can be obtained. The third column is calculated by using the modeling method proposed in [10], where the floating core potential is analytically calculated. However, the modeling method [10] can only obtain the two-terminal equivalent circuit. The last column is calculated by using the proposed modeling method of this letter, where both two-terminal and three-terminal equivalent circuits are obtained without knowing the voltage potential of the floating core.

The two-terminal and three-terminal equivalent circuits of the MV copper-foiled inductor by using the measured results are given in Table III. By comparing Table II and III, the calculation by using the method in [11] has the largest error since it only uses the average potential of the inner layer. The calculation by using the method in [10] and [15] has similar results to the calculation by using the proposed method. However, the method in [10] does not reveal the parasitic coupling between the terminals and core, where [11] and [15] need to estimate the floating core potential.

## V. Extend the Proposed Method to Transformers

Although the research subject of this letter is an MV inductor with a grounded core and frame, which is a three-terminal component, the proposed modeling method is possible to be extended for the in transformers with more than four terminals. Some suggestions are given by using an example of a transformer with two windings (a four-terminal component) as:

1) The static capacitance of the transformer can be calculated by using the same method in Appendix, based on the geometrical structure and material information of the transformers.
2) There are six equivalent capacitances in a four terminal transformer with six different configurations. The first four configurations can be obtained by modeling the dynamical capacitance between one of the terminals and the rest, where the rest of the three terminals are shorted toghther. The last two configurations can be selected by modeling the dynamical capacitance between the two pairs of the shorted terminals. Each of these configuration can be regarded as a two-terminal configuration, which is the same as Section III of this letter. Finally, the six equivalent capacitances can be calculated by the dynamical capacitances for each of these six configurations.

For a magnetic component with $x$ number of terminals, $x(x-1)/2$ configurstions are needed for deriving the equivalent capacitances between any of these two terminals.

## VI. Conclusions

This letter proposed a modeling method to analytically calculate the parasitic capacitances for the inductors without having the prior knowledge on the floating voltage potential of the magnetic cores, while maintaining the comparable accuracy as with previous methods. It is known that requring to obtain the foating core potential is a complex procedure and this letterr proposed a method to calculate capacitance without having the prior knowledge of that. Experimental measurements verify the proposed modeling method. The proposed modeling method provides a general flowchart for modeling the parasitic capacitances in magnetics with multiple terminals, which can be further implemented to inductors and transformers with arbitrary number of terminals

## Acknowledgement

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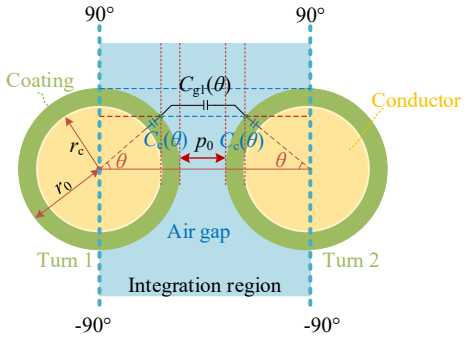
## Appendix

### *A. Derivations of the static capacitances in the exampled 2D inductor*

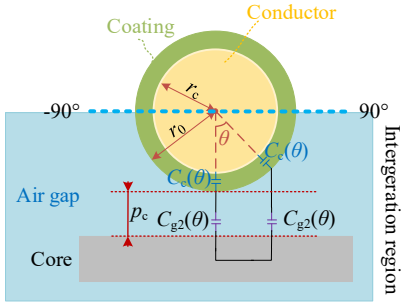
The elementary capacitances should be derived first [10]. In the researched 2D inductor given in Fig. 2, there are two elementary capacitances: 1) Elementary coating capacitance between two turns $dC_c(\theta)$; 2) Elementary air gap capacitance $dC_g(\theta)$. These two elementary capacitances contributed to elementary turn-to-turn capacitance and turn-to-core capacitance, where their schematics are given in Fig. A1. Only the elementary capacitance between the two adjacent turns are considered since the capacitive couplings between two non-adjacent turns are relatively small, which is neglected in this research. This is a common concept in [3], [10], [11], [15].

Then the elementary coating and air-gap capacitance can be presented as (A1), based on the geometrical information given in Fig. A1. $\varepsilon_r$ is the relative permittivity of the coating, where $\varepsilon_o$ is the vacuum permittivity.

In Fig. A1 (a), if the length $p_0$ in $dC_{g1}(\theta)$ is replaced by $p_1$, then (A2) is obtained.




(a)




(b)

Fig. A1 Schematic of the two basic elementary capacitances

$$dC_c(\theta)=\frac{\varepsilon_r\varepsilon_0}{\ln\frac{r_0}{r_c}}d\theta$$

$$dC_{g1}(\theta)=\frac{\varepsilon_0 r_0}{p_0+2r_0(1-\cos\theta)}d\theta \quad \text{(A1)}$$

$$dC_{g2}(\theta)=\frac{\varepsilon_0 r_0}{p_c+r_0(1-\cos\theta)}d\theta$$

$$dC_{g3}(\theta)=\frac{\varepsilon_0 r_0}{p_1+2r_0(1-\cos\theta)}d\theta \quad \text{(A2)}$$

where (A1) will be used for calculating the static capacitance between the inner layer and the core, (A2) will be used for calculating the static capacitance between two adjacent layers.

The schematic of the researched 2D inductor is shown in Fig. A2, which is composed by static turn-to-turn capacitance $C_{statt}$, equivalent layer-to-layer capacitance $C_{stall}$, and equivalent layer-to-core capacitance $C_{stalc}$.

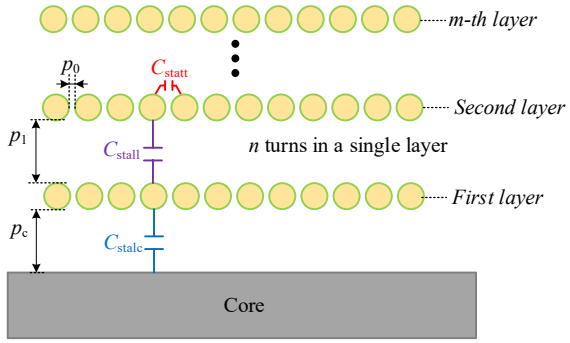



Fig. A2 Schematic of the 2D inductor with main geometrical parameters and static capacitances

These static capacitances are composed by the elementary coating capacitance and air-gap capacitance. It is assumed that each layer has the same number $n$ of turns. The edge effects (electrical fringe field) is neglected for simplifying the model.

Then $C_{statt}$, $C_{stall}$ and $C_{stalc}$ are presented as (A3), (A4), and (A5), respectively. The integrated angle is [-π/2, π/2].

$$\frac{1}{dC_{ele\_turn\text{-}to\text{-}turn1}(\theta)}=\frac{2}{dC_c(\theta)}+\frac{1}{dC_{g1}(\theta)}$$

$$C_{statt}=\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}dC_{ele\_turn\text{-}to\text{-}turn1}(\theta) \quad \text{(A3)}$$

$$\frac{1}{dC_{ele\_turn\text{-}to\text{-}turn2}(\theta)}=\frac{2}{dC_c(\theta)}+\frac{1}{dC_{g3}(\theta)}$$

$$C_{stall}=n\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}dC_{ele\_turn\text{-}to\text{-}turn2}(\theta) \quad \text{(A4)}$$

$$\frac{1}{dC_{ele\_turn\text{-}to\text{-}core}(\theta)}=\frac{1}{dC_c(\theta)}+\frac{1}{dC_{g2}(\theta)}$$

$$C_{stalc}=n\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}dC_{ele\_turn\text{-}to\text{-}core}(\theta) \quad \text{(A5)}$$

*B. Derivations of the dynamical capacitances in the exampled 2D inductor*

The dynamical capacitances are dependent by both static capacitances and voltage potential difference. A schematic for illustrating the voltage potential distribution is given in Fig. B1. In this part, the current is assumed to flow through the winding, where the derivations are only valid for Configuration 1 and 2 of this letter.

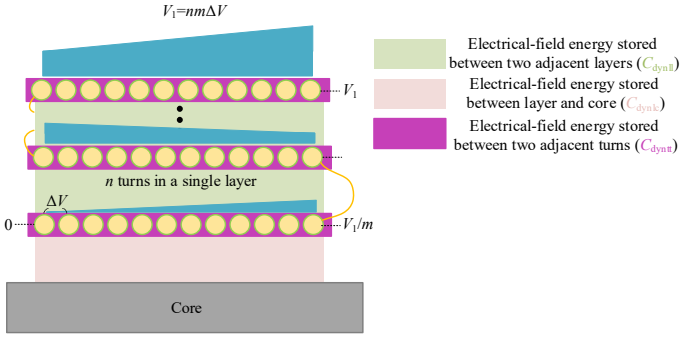



Fig. B1 Schematic of the 2D inductor with three different stored electrical-field between adjacent surfaces

Then the energy stored between the inner layer and core can be written as (B1), based on the energy-conservation law [8]. The first line of (B1) acts as the defining quantity of the dynamical capacitance Cdynlc.

$$W_{\text{E-field\_lc}} = \frac{1}{2} C_{\text{dynlc}} (V_1\text{-}0)^2$$

$$W_{\text{E-field\_lc}} = \frac{C_{\text{stalc}}}{6}\left( (0 - V_{\text{core}})^2 + (0 - V_{\text{core}})(\frac{V_1}{m} - V_{\text{core}}) + (\frac{V_1}{m} - V_{\text{core}})^2 \right) \quad \text{(B1)}$$

Thus, the dynamical capacitance $C_{\text{dynlc}}$ contributed by the electrical field energy stored between the inner layer and core is obtained as (B2).

$$C_{\text{dynlc}} = \frac{1}{3V_1^2}\left( \frac{V_1^2}{m^2} - \frac{3V_1 V_{\text{core}}}{m} + 3V_{\text{core}}^2 \right) C_{\text{stalc}} \quad \text{(B2)}$$

Similarly, the dynamical capacitances $C_{\text{dynll}}$ and $C_{\text{dyntt}}$ are defined and derived as (B3) and (B4), respectively.

$$\begin{aligned} W_{\text{E-field\_ll}} &= \frac{1}{2} C_{\text{dynll}} (V_1\text{-}0)^2 \\ W_{\text{E-field\_ll}} &= \frac{(m-1)C_{\text{stall}}}{6}\left( (\frac{2V_1}{m})^2 \right) \\ \Rightarrow C_{\text{dynll}} &= \frac{4(m-1)C_{\text{stall}}}{3m^2} \end{aligned} \quad \text{(B3)}$$

$$\begin{aligned} W_{\text{E-field\_tt}} &= \frac{1}{2} C_{\text{dyntt}} (V_1\text{-}0)^2 \\ W_{\text{E-field\_tt}} &= \frac{m(n-1)C_{\text{statt}}}{6}\left( 3(\frac{V_1}{mn})^2 \right) \\ \Rightarrow C_{\text{dyntt}} &= \frac{m(n-1)C_{\text{statt}}}{m^2 n^2} \end{aligned} \quad \text{(B4)}$$

*C. Derivations of total equivalent capacitance in Configuration 1*

In Configuration 1, the core is connected to the hot terminal with 0 voltage potential. By substituting $V_{\text{core}}$=0 to (B2), $C_{\text{dynlc}}$ of Configuration 1 is derived as (C1).

$$C_{\text{dynlc}} = \frac{1}{3m^2} C_{\text{stalc}} \quad \text{(C1)}$$

Since the current is flowing through the winding in Configuration 1 due to the different potential at the terminals, the distribution of the voltage potential within the winding is still the same as Fig. B1, before the first resonant frequency of the inductor. Thus, $C_{\text{dynll}}$ and $C_{\text{dynll}}$ are the same as (B3) and (B4), respectively.

Based on (2), the total equivalent capacitance of Configuration 1 is obtained as (C2).

$$C_{\text{total1}} = \frac{1}{3m^2} C_{\text{stalc}} + \frac{4(m-1)}{3m^2} C_{\text{stall}} + \frac{m(n-1)}{(nm)^2} C_{\text{statt}} \quad \text{(C2)}$$

*D. Derivations of total equivalent capacitance in Configuration 2*

By substituting $V_{\text{core}}$=$V_1$ to (B2), $C_{\text{dynlc}}$ of Configuration 1 is derived as (D1).

$$C_{\text{dynlc}} = \frac{3m^2 - 3m + 1}{3m^2} C_{\text{stalc}} \quad \text{(D1)}$$

Since the current is flowing through the winding in Configuration 2 due to the different voltage at the terminals, the distribution of the voltage potential within the winding is still the same as Fig. B1, before the first resonant frequency of the inductor. Thus, $C_{\text{dynll}}$ and $C_{\text{dyntt}}$ are still the same as (B3) and (B4), respectively.

Based on (2), the total equivalent capacitance of Configuration 2 is obtained as (D2).

$$C_{\text{total2}} = \frac{3m^2 - 3m + 1}{3m^2} C_{\text{stalc}} + \frac{4(m-1)}{3m^2} C_{\text{stall}} + \frac{m(n-1)}{(nm)^2} C_{\text{statt}} \quad \text{(D2)}$$

*E. Derivations of total equivalent capacitance in Configuration 3*

As opposed to Configuration 1 and 2, the voltage at the inductor terminals are equal in Configuration 3. Thus, there is no current flow through the winding, where the voltage potential is always the same within the winding, before the first resonant frequency of the inductor. Thus, the electrical-field energy stored between two adjacent layers is zero, where $C_{\text{dynll}}$ is also zero. Similarly, the electrical-field energy stored between two adjacent turns is also zero, where $C_{\text{dyntt}}$ is zero.

The electrical-field energy stored between the inner layer and core is also different with (B1), which is re-written as (E1).

$$\begin{aligned} W_{\text{E-field\_lc}} &= \frac{1}{2} C_{\text{dynlc}} (V_1\text{-}0)^2 \\ W_{\text{E-field\_lc}} &= \frac{C_{\text{stalc}}}{6}\left( (V_1\text{-}0)^2 + (V_1\text{-}0)(V_1\text{-}0) + (V_1\text{-}0)^2 \right) \end{aligned} \quad \text{(E1)}$$

Thus, the dynamical capacitance between the inner layer and core of Configuration 3 is derived as (E2).

$$C_{\text{dynlc}} = C_{\text{stalc}} \quad \text{(E2)}$$

Finally, to sum $C_{\text{dynll}}$, $C_{\text{dyntt}}$, and $C_{\text{dynlc}}$, the total equivalent capacitance of Configuration 3 is obtained as (E3).

$$C_{\text{total3}} = C_{\text{stalc}} \quad \text{(E3)}$$

## REFERENCE


[1] Z. Ouyang et al., "Optimal design and tradeoff analysis of planar transformer in high-power DC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2800-2810, Mar. 2010.

[2] M. Aghaei et al., "On the effect of disorder on stray capacitance of transformer winding in high-voltage power supplies," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3608-3618, May 2017.

[3] J. Biela et al., "Using transformer parasitic for resonant converters-a review of the calculation of the stray capacitance of transformers," *IEEE Transactions on Industrial Applications*, vol. 44, no. 1, pp. 223-233, Jan. – Feb. 2008.

[4] S. Wang et al., "Analysis and applications of parasitic capacitance cancellation techniques for EMI suppression," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3109-3117, Dec. 2009.

[5] B. Zhang and S. Wang, "A Survey of EMI Research in Power Electronics Systems With Wide-Bandgap Semiconductor Devices," *IEEE Journal of*

*Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626-643, Mar. 2020.

[6] A. Anurag, S. Acharya, S. Bhattacharya and T. Weatherford, "Thermal performance and reliability analysis of a medium voltage three-phase inverter considering the influence of high dv/dt on parasitic filter elements," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 486-494, Mar. 2020.

[7] P. Thummala, H. Schneider, Z. Zhang and M. Andersen, "Investigation of transformer winding architectures for high voltage (2.5 kV) capacitor charging and discharging applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5786-5796, Aug. 2016.

[8] E. Snelling, SoftFerrites: Properties and Applications. London, U.K.: Iliffe Books Ltd., 1988.

[9] X. Liu et al., "Calculation of capacitance in high-frequency transformer windings," *IEEE Transactions on Magnetics*, vol. 52, no. 7,2003204, Jul. 2016.

[10] Z. Shen, H. Wang, Y. Shen, Z. Qin and F. Blaabjerg, "An improved stray capacitance model for inductors," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11153-11170, Nov. 2019.

[11] H. Zhao et al., "Physics-based modeling of parasitic capacitance in medium-voltage filter inductors," *IEEE Transactions on Power Electronics*, early access, doi: 10.1109/TPEL.2020.3003157. [Online]. Available: https://ieeexplore.ieee.org/document/9119860

[12] M. Saket et al., "LLC converters with planar transformers: issues and mitigation," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4524-4542, Aug. 2016.

[13] Keysight Technologies, "Keysight Technologies Impedance measurement handbook" [Online], Available: https://literature.cdn.keysight.com/litweb/pdf/5950-3000.pdf

[14] Keysight Technology, "E4990A Impedance Analyze" [Online]. Available: https://www.keysight.com/us/en/assets/7018-04256/data-sheets/5991-3890.pdf

[15] H. Zhao et al., "Parasitic Capacitance in Copper-Foiled Medium-Voltage Filter Inductors Considering Fringe Electrical Field," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8181-8192,Jul. 2021.