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Capacitor Voltage Balancing for Multi-Level Dual-Active-Bridge DC-DC Converters

Chaochao Song, *Student Member, IEEE*, Ariya Sangwongwanich, *Member, IEEE*, Yongheng Yang, *Senior Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Capacitor voltage balancing is a critical issue for neutral-point-clamped (NPC)-based converters, including the two-three (2/3)-level dual-active-bridge (DAB) DC-DC converters. The unbalanced capacitor voltage will increase the voltage stress on power devices and negatively affect the reliability of the converters. Two typical problems during the capacitor voltage balancing process should be solved, i.e., power fluctuation minimization and determination of the transformer current polarity. Accordingly, this paper proposes a balancing control scheme based on the complementary-switching-state (CSS) method. In the CSS method, the switching states which are identified to be adverse for balancing will be replaced by their corresponding CSSs to control the neutral-point current while keeping the voltage and current waveforms unchanged. By doing so, the power fluctuation and current overshoot during the balancing process can be significantly reduced. Moreover, since the dynamic voltage and current waveforms are identical to the steady-state waveforms, the transformer current polarity during the balancing process can be identified based on the steady-state power and current models. Therefore, the determination of the transformer current polarity can be simplified compared to the traditional balancing control scheme. Finally, experimental results are carried out to verify the performance of the proposed balancing control scheme.**

***Index Terms*—DAB converters, multi-level converters, capacitor voltage balancing control, dynamic performances.**

I. Introduction

THE dual-active-bridge (DAB) converter is one of the most promising interfacing DC-DC converters for various applications, e.g., solid state transformers (SST), distributed generation systems, and electric vehicles, due to its merits of high power density and efficiency, inherent soft-switching capability, and galvanic isolation [1]–[4]. A two-three (2/3)-level DAB converter, as shown in Fig. 1, was proposed for the applications with higher voltage rating [5], e.g., medium-voltage photovoltaic systems (Fig. 2), where the two-level H-bridge of the secondary side is replaced by a three-level neutral-point-clamped (NPC) bridge. In addition to the higher voltage blocking capability, the 2/3-level DAB converters can realize a higher step-up ratio, enable the utilization of lower voltage-rating devices to save the cost to some extent, and present more control degrees of freedom (DoFs) to improve the performances of the DAB converters [6]–[8].

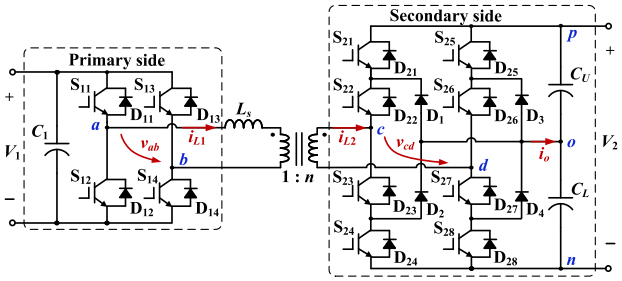

Fig. 1. A two-three (2/3)-level dual-active-bridge (DAB) converter: V_1 and V_2 are the DC-link voltages, v_{ab} and v_{cd} are the terminal voltages of the transformer with the turns-ratio being $1:n$, i_{L1} and i_{L2} are the terminal currents of the transformer, and L_s is the series inductor.

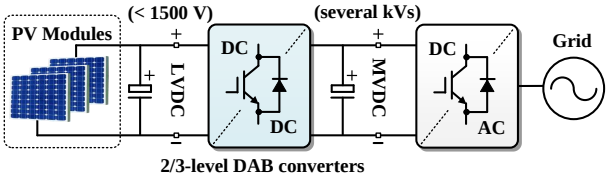

Fig. 2. A typical medium-voltage DC (MVDC) photovoltaic (PV) system.

As for the modulation for the 2/3-level DAB converters, five-level control is one of the most advantageous phase-shift control schemes, where the transferred power is controlled by the phase-shift angles and duty cycles. By employing the five-level control scheme, the performance of DAB converters in terms of the soft-switching capability, current stress, and efficiency can be improved [9]–[11]. However, the capacitor voltage imbalance exists in the five-level control scheme, which can occur due to: 1) the tolerances in different power components, e.g., the DC-link capacitors, and 2) synchronization failure of the gate-driving signals [12]–[16]. Under the voltage unbalanced condition, the voltage stress on power devices will increase, especially when the gate-driving signals fail to synchronize, which could exceed the voltage blocking capability and eventually damage the devices. Moreover, the capacitor voltage imbalance will affect the accuracy of the

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Chaochao Song, Ariya Sangwongwanich, and Frede Blaabjerg are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: chso@energy.aau.dk, ars@energy.aau.dk, fbl@energy.aau.dk).

Yongheng Yang is with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: yang_yh@zju.edu.cn).

power transfer model of the DAB converters, and affect the optimal operating conditions, e.g., efficiency [15].

To address these issues, a balancing control scheme is required. In [12]–[14], capacitor voltage balancing control schemes have been proposed for the NPC-based DAB converters by dynamically modifying the dwell time of the switching states where the current is injected into/drawn from the neutral point o. However, the waveforms of the voltage v_{cd} and the current i_{L2} will be affected during the balancing process. Consequently, the 2/3-level DAB converters will suffer from power fluctuation and current overshoot, which will deteriorate the dynamic performance of the converters by the increased current stress and settling time. Besides, the determination of the transformer current is another issue for the above balancing methods. For the NPC-based DAB converters, under the same switching state, the direction of the neutral-point current i_o will be affected by the polarity of the transformer current i_{L2}. In each modulation strategy, the polarity of the transformer current i_{L2} in the steady state can be calculated by the transferred power and current models. However, due to the change in voltage and current waveforms during the voltage balancing dynamic, the determination of the transformer current polarity is challenging. Accordingly, another capacitor voltage balancing control scheme was proposed in [15] to decouple the neutral-point current from the transformer current polarity by means of switching-sequence reconfiguration. Nevertheless, this scheme also fails to maintain the dynamics of the DAB converters due to the changed dynamic voltage and current waveforms. Furthermore, a capacitor voltage balancing control scheme was proposed to improve the dynamic performance during the balancing process by reconfiguring the waveform of v_{cd} [17]. However, besides certain theoretical errors, the relationship between the direction of the neutral-point current and transformer current was not analyzed. Consequently, the method may fail to balance the capacitor voltages in practice due to the uncertain direction of the neutral-point current.

In all, two major issues need to be addressed in the capacitor voltage balancing control: 1) the power fluctuation and current overshoot and 2) the determination of the transformer current polarity during the balancing process. Thus, this paper proposes a capacitor voltage balancing control scheme based on complementary-switching-state (CSS) method. The CSS pairs are two switching states that can achieve the same voltage v_{cd}, but have an opposite direction of the neutral-point current i_o. Specifically, when a switching state is identified to be adverse for balancing (the direction of the neutral-point current under this switching state is not required for balancing), it should be replaced by its corresponding CSS. In this way, the CSS can be used to assist the capacitor voltage balancing due to the presence of the opposite neutral-point current. Meanwhile, the dynamic waveforms will not be affected, since the voltage v_{cd} remains unchanged after the replacement of the CSS. Therefore, the polarity of the transformer current during the balancing process can be determined by using the steady-state power and current models. Notably, this paper is extended from [18] with the following major improvements by including typical examples to show the utilization of the proposed CSS method, a thorough characteristics comparison of the proposed method and the traditional balancing method, and extensive experimental tests.

TABLE I
SWITCHING STATES FOR NPC BRIDGE

Switching state	ON switches (first arm)	ON switches (second arm)	v_{cn}/v_{dn}
[P]	$\{S_{21}, S_{22}\}$	$\{S_{25}, S_{26}\}$	V_2
[O]	$\{S_{22}, S_{23}\}$	$\{S_{26}, S_{27}\}$	$0.5V_2$
[N]	$\{S_{23}, S_{24}\}$	$\{S_{27}, S_{28}\}$	0

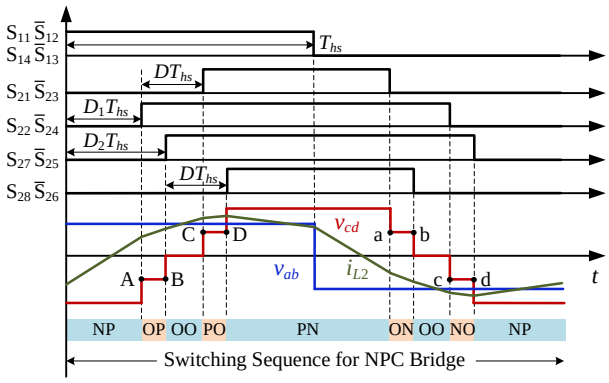


Fig. 3. Typical waveforms of the 2/3-level DAB converters with the five-level control scheme.

The rest of the paper is organized as follows. The analysis of switching states with the five-level control is presented in Section II. The proposed CSS method is detailed in Section III with two typical examples to show its application. Section IV presents the experimental results to verify the theoretical analysis. Finally, conclusions are provided in Section V.

II. MODULATION FOR 2/3-LEVEL DAB CONVERTERS

A. Five-level control scheme

Considering the NPC bridge, there are three switching states for each bridge arm, i.e., [P], [O], and [N], as shown in Table I, where the midpoint voltage v_{cn}/v_{dn} (i.e., the voltage between the midpoint c/d of each arm and the negative pole n in Fig. 1) is equal to V_2, $0.5V_2$, and 0, respectively. Thus, the terminal voltage v_{cd} $(= v_{cn} - v_{dn})$ can be five-level ($v_{cd} \in \{0, \pm 0.5V_2, \pm V_2\}$). Fig. 3 shows the typical waveforms of v_{ab}, v_{cd}, i_{L2}, and the gate-driving signals with the five-level control scheme for the 2/3-level DAB converters, where T_{hs} is a half of the switching cycle, D_1 and D_2 denote the phase-shift ratios between the gate-driving signals of S_{22} and S_{11}, S_{27} and S_{11}, respectively. D denotes the duty-cycle ratio, where the duty cycle of S_{21} and S_{28} is 1-D, and that of S_{22} and S_{27} is 1+D. The transferred power of the 2/3-level DAB converters is controlled by the three control variables, i.e., D_1, D_2 and D. It should be noted that the waveforms of v_{ab}, v_{cd}, and i_{L2} for the cases of $D_1 < D_2$ and $D_1 > D_2$ are identical. A similar condition also applies to the relationships between $D_1 + D$ and D_2. For convenience, only the condition of $D_1 \leq D_2 \leq D_1 + D$ is discussed in this paper.

TABLE II
SWITCHING STATES WITH RESPECT TO THE DIRECTION OF THE NEUTRAL-POINT CURRENT i_o

Intervals	Switching States	Polarity of i_{L2}	Value of v_{cd}	Current Conduction Path	Direction of i_o
[A, B]	[OP]	$i_{L2} > 0$	$-0.5V_2$	$S_{25} \rightarrow S_{26} \rightarrow S_{23} \rightarrow D_2$	$i_o > 0$
		$i_{L2} < 0$		$D_1 \rightarrow S_{22} \rightarrow D_{26} \rightarrow D_{25}$	$i_o < 0$
[C, D]	[PO]	$i_{L2} > 0$	$0.5V_2$	$D_3 \rightarrow S_{26} \rightarrow D_{22} \rightarrow D_{21}$	$i_o < 0$
		$i_{L2} < 0$		$S_{21} \rightarrow S_{22} \rightarrow S_{27} \rightarrow D_4$	$i_o > 0$
[a, b]	[ON]	$i_{L2} > 0$	$0.5V_2$	$D_{28} \rightarrow D_{27} \rightarrow S_{23} \rightarrow D_2$	$i_o > 0$
		$i_{L2} < 0$		$D_1 \rightarrow S_{22} \rightarrow S_{27} \rightarrow S_{28}$	$i_o < 0$
[c, d]	[NO]	$i_{L2} > 0$	$-0.5V_2$	$D_3 \rightarrow S_{26} \rightarrow S_{23} \rightarrow S_{24}$	$i_o < 0$
		$i_{L2} < 0$		$D_{24} \rightarrow D_{23} \rightarrow S_{27} \rightarrow D_4$	$i_o > 0$

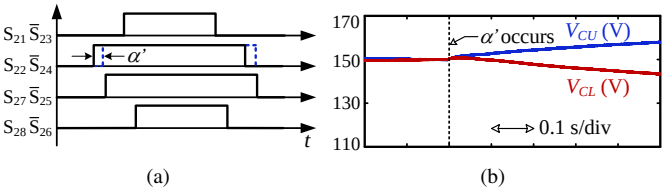


Fig. 4. Capacitor voltage imbalance due to the asynchronization of the gate-driving signals. (a) Waveforms of the gate-driving signals when an extra phase-shift angle α' occurs on S_{22} and S_{24}. (b) Waveforms of the two capacitor voltages.

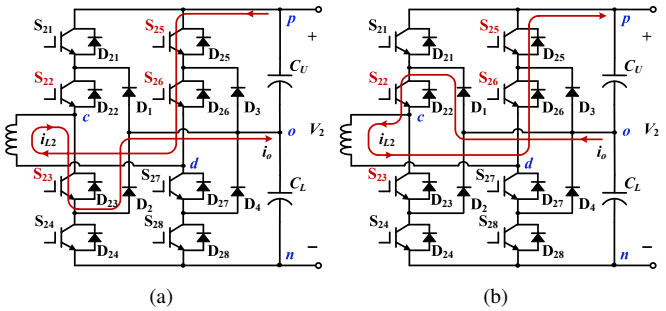


Fig. 5. Current conduction paths of the switching state [OP] when i_{L2} is: (a) positive, and (b) negative.

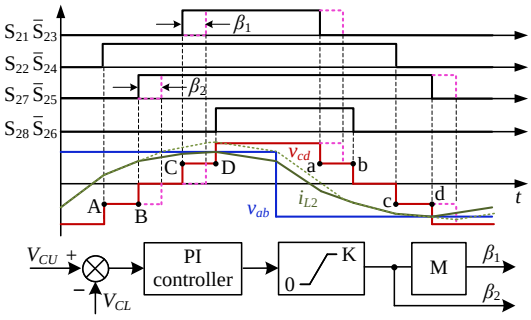


Fig. 6. A traditional capacitor voltage balancing control scheme under the condition $V_{CU} > V_{CL}$ when I_{L2} [A, B] > 0, and I_{L2} [C, D] > 0.

B. Analysis of Switching States

It is clear that only during the intervals where the voltage v_{cd} is $\pm 0.5V_2$, i.e., [A, B], [C, D], [a, b], and [c, d] in Fig. 3, the current can flow through the neutral point o. In normal state, the charges injected into and drawn from the neutral point during each switching cycle are identical. Thus, the voltages of the two capacitors C_U and C_L are balanced. However, if the gate-driving signals are not perfectly synchronized, the balanced condition will be broken, resulting in an unbalanced capacitor voltage. Fig. 4 illustrates an unbalanced condition when an extra phase-shift angle α' appears on the gate-driving signals of S_{22} (i.e., the gate-driving signals of S_{21} and S_{22} fail to synchronize), where $\alpha' = 0.01T_{hs}$ (i.e., 1.8°). To overcome the capacitor voltage imbalance caused by the asynchronization of the gate-driving signals and the tolerances in the power components, the utilization of the switching states during the four intervals, i.e., [OP], [PO], [ON], and [NO] in Fig. 3, should be modified to change the direction or dwell time of the neutral-point current i_o.

In order to do so, the direction of the neutral-point current i_o under the four switching states should be identified. For each switching state, the direction of the neutral-point current i_o will be affected by the polarity of the transformer current i_{L2}. For instance, during the interval [A, B], the switching state [OP] is applied, which means the gate-driving signals of S_{22}, S_{23}, S_{25}, and S_{26} are at high level. When the transformer current i_{L2} is positive (from the primary side to the secondary side), the current will flow through S_{25}, S_{26}, S_{23}, D_2, and will be injected into the neutral point o (i.e., $i_o > 0$), as shown in Fig. 5 (a). Therefore, the upper capacitor C_U will be discharged during this condition. On the other hand, when the transformer current i_{L2} is negative, the current will be drawn from the neutral point o (i.e., $i_o < 0$), as shown in Fig. 5 (b), and C_U will be charged. With a similar analysis, the switching states with respect to the direction of the neutral-point current i_o can be obtained, as summarized in Table II.

III. CAPACITOR VOLTAGE BALANCING CONTROL

A. Traditional Balancing Method

If the voltage of the upper capacitor C_U is higher than that of the lower capacitor C_L, a positive neutral-point current i_o is required to charge the lower capacitor. Otherwise, a negative neutral-point current i_o is required to charge the upper capacitor. Fig. 6 demonstrates a traditional balancing method under the condition I_{L2} [A, B] > 0, and I_{L2} [C, D] > 0 when $V_{CU} > V_{CL}$ [12], in which I_{L2} [A, B] and I_{L2} [C, D] denote the average transformer current during the intervals [A, B] and [C, D], respectively. Note that due to the symmetry of the voltage and current waveforms, the direction of I_{L2} [a, b] and I_{L2} [c, d] is opposite to that of I_{L2} [A, B] and I_{L2} [C, D], respectively. In Fig. 6, β_1 and β_2 are the regulated phase-shift angles, K is the upper threshold for the output signal of

the proportional-integral (PI) controller, and M is a multiplier. During the balancing process, the switching sequence should remain unchanged to avoid the waveform distortion. Thus, the regulated phase-shift angles should satisfy that $\beta_1 \leq DT_{hs}$ and $\beta_2 \leq DT_{hs}$. According to Table II, it can be seen that the neutral-point current i_o will be positive during the intervals [A, B] and [c, d], and negative during the intervals [C, D] and [a, b]. Therefore, for the condition $V_{CU} > V_{CL}$ (i.e., $i_o > 0$ is required), the switching states during the intervals [A, B] and [c, d], i.e., [OP] and [NO], are beneficial for the capacitor voltage balancing, which are defined as beneficial switching states. On the other hand, the switching states [PO] and [ON] during the intervals [C, D] and [a, b] are defined as adverse switching states since they will accelerate the imbalance. To increase the charges injected into the neutral point, the intervals [A, B] and [c, d] should be increased while the intervals [C, D] and [a, b] should be decreased by increasing the phase-shift angles for S_{21} and S_{27}, as shown in Fig. 6, where the dotted lines denote the waveforms after applying the capacitor voltage balancing control scheme.

However, from the expression of the transformer current:

$$\frac{di_{L2}(t)}{dt} = \frac{nv_{ab}(t) - v_{cd}(t)}{n^2 L_s} \tag{1}$$

it can be seen that when the voltage v_{cd} changes during the balancing process, the transformer current i_{L2} will also be affected. This will lead to current fluctuation and may cause large overshoots, which will increase the current stress of the power devices. If the peak current exceeds the rated and activates the protection system, the DAB converter may be shut down completely. Furthermore, from the power expression:

$$P = \frac{1}{T_{hs}} \int_0^{T_{hs}} nv_{ab}(t) i_{L2}(t) dt \tag{2}$$

it can be seen that the transferred power will also fluctuate along with the changed current i_{L2}, which will negatively affect the dynamics. The dynamic performance of the DAB converters will be related to β_1 and β_2. That is, with larger β_1 and β_2, the balancing period can be accelerated, but the current/power fluctuation will be increased. Besides, the beneficial and adverse switching states should be identified according to the polarity of the dynamic transformer current during [A, B], [C, D], [a, b], and [c, d], which is difficult to be determined due to the changed dynamic waveforms.

B. Proposed CSS Balancing Method

To overcome the above challenging issues, a capacitor voltage balancing control scheme based on a CSS method is proposed in this section. From (1) and (2), it can be seen that if the waveform of the voltage v_{cd} remains unchanged during the balancing process, the transferred power will also remain constant, and the dynamic performance of the converters can be improved due to no power fluctuation and overshoot current. Therefore, when a switching state is identified to be adverse for the balancing control, if it can be replaced by another switching state which can change the direction of the neutral-point current i_o, and realize the identical voltage v_{cd} at the same time, the capacitor voltages can be balanced without any current/power fluctuation. Those are the CSS pairs, defined as: with the same polarity of the transformer current i_{L2}, two switching states that can realize: 1) the same voltage v_{cd}, and 2) the opposite direction of the neutral-point current i_o. Under such principles, it can be seen from Table II that there are two pairs of CSSs: [OP] and [NO], [PO] and [ON]. Due to the symmetry of the voltage and current waveforms, there will be two beneficial switching states and two adverse ones during each switching cycle. After the two adverse switching states are replaced by their CSSs, the employed four switching states will all be beneficial switching states, which can improve the capacitor voltage balancing process.

TABLE III
CHARGING/DISCHARGING CONDITION OF THE CAPACITORS DURING EACH INTERVAL UNDER MODE I

Intervals	Steady State		Balancing State	
	Formed Capacitor	Condition	Formed Capacitor	Condition
[A, B]	C_U	Discharge	C_U	Discharge
[C, D]	C_U	Charge	C_L	Charge
[a, b]	C_L	Discharge	C_U	Discharge
[c, d]	C_L	Charge	C_L	Charge

According to the above analysis, with different transformer current polarity during the four intervals [A, B], [C, D], [a, b], and [c, d], the two adverse switching states will change. Thus, the implementation of the proposed CSS method under different transformer current polarity should be discussed.

For the condition $V_{CU} > V_{CL}$, during I_{L2} [A, B] > 0 and I_{L2} [C, D] > 0, it can be seen from Table II that the neutral-point current during [A, B] and [c, d] is positive, and that of [C, D] and [a, b] is negative. Since $i_o > 0$ is required for charging the lower capacitor, [OP] and [NO], which are employed in the intervals [A, B] and [c, d], are beneficial switching states. On the other hand, [PO] and [ON] during the intervals [C, D] and [a, b] are adverse switching states. This can also be confirmed according to the charging/discharging condition of each capacitor. Under the switching state [OP] during the interval [A, B], the current conduction path is the same as Fig. 5 (a). It can be seen from Fig. 5 (a) that the voltage v_{cd} is formed by the upper capacitor C_U, and the capacitor C_U will be discharged during [A, B]. Thus, [OP] is identified as a beneficial switching state since it can assist the capacitor voltage to achieve balancing. With a similar analysis, the charging/discharging condition of each capacitor during the other three intervals can be obtained, as shown in Table III. It can be seen from Table III that the two switching states during [C, D] and [a, b] are adverse switching states, which should be replaced by their CSSs, i.e., [PO] should be replaced by [ON] during the interval [C, D], and [ON] should be replaced by [PO] during the interval [a, b], respectively. After the replacement, the upper capacitor C_U will be discharged, and the lower capacitor C_L will be charged during each switching cycle, which can be seen in Table III. Therefore, the switching states after applying the CSS method are all beneficial for capacitor voltage balancing. In all, the implementation of the CSS method in this condition is shown in Fig. 7, which is defined as Mode I. The shaded areas in Fig. 7 denote the

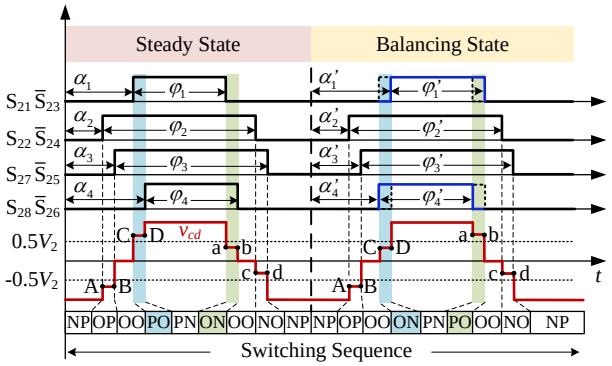


Fig. 7. Illustration of the proposed CSS method for Mode I: I_{L2} [A, B] > 0 and I_{L2} [C, D] > 0, under the condition $V_{CU} > V_{CL}$.

intervals where the switching states should be replaced by their CSSs. In Fig. 7, α_i and φ_i $(i = 1, 2, 3, 4)$ denote the phase-shift angles and duty cycles of the gate-driving signals, which can be expressed as

$$\begin{cases} \alpha_1 = (D_1 + D)T_{hs}, \alpha_2 = D_1 T_{hs} \\ \alpha_3 = D_2 T_{hs}, \alpha_4 = (D_2 + D)T_{hs} \\ \varphi_1 = \varphi_4 = (1 - D)T_{hs}, \varphi_2 = \varphi_3 = (1 + D)T_{hs} \end{cases} \tag{3}$$

Additionally, in Fig. 7, α_i' and φ_i' $(i = 1, 2, 3, 4)$ denote the phase-shift angles and duty cycles after applying the CSS method. During the balancing process, the dotted lines denote the steady-state gate-driving signals, while the solid lines denote those after applying the CSS method. The control variables during the capacitor voltage balancing process can be obtained as

$$\text{Mode I}: \begin{cases} \alpha_1' = \alpha_1 + (\alpha_3 - \alpha_2), \alpha_2' = \alpha_2 \\ \alpha_3' = \alpha_3, \alpha_4' = \alpha_4 - (\alpha_3 - \alpha_2) \\ \varphi_i' = \varphi_i (i = 1, 2, 3, 4) \end{cases} \tag{4}$$

Therefore, to achieve the CSS method in this mode, the gate-driving signal for S_{21} should be delayed by an angle of $\alpha_3 - \alpha_2$, i.e., $(D_2 - D_1)T_{hs}$, and that for S_{28} should be advanced by the same angle. In this way, the switching states during the intervals [C, D] and [a, b] are replaced by their CSSs. The waveform of the voltage v_{cd} is similar to the steady-state voltage waveform. In addition, according to Table III, the voltage v_{cd} is equal to V_{CU} during [A, B] and [C, D] in steady state, whose values are higher than $0.5V_2$, and v_{cd} is equal to V_{CL} during [a, b] and [c, d] , whose values are lower than $0.5V_2$. After replacing the switching states during [C, D] and [a, b], the voltage v_{cd} is equal to V_{CL} during [C, D], and equal to V_{CU} during [a, b]. As a result, the slopes of the transformer current will be different between steady state and balancing state during [C, D] and [a, b] according to (1). However, the severe capacitor voltage imbalance (e.g., V_{CU} = V_2 and V_{CL} = 0) is not prone to occur if the balancing control scheme is employed from the beginning. In addition, the dwell time of the four intervals is limited. Therefore, the current and power fluctuation caused by the difference between V_{CU} and V_{CL} will be limited, which can be ignored in practice.

With a similar analysis, the implementation of the CSS method under other three conditions, i.e., I_{L2} [A, B] > 0 and I_{L2} [C, D] < 0, I_{L2} [A, B] < 0 and I_{L2} [C, D] > 0, I_{L2} [A, B] < 0 and I_{L2} [C, D] < 0 can be obtained, as shown in Fig. 8, which are defined as Modes II - IV, respectively. The control variables during the balancing state can be given as

$$\begin{aligned} \text{Mode II}: &\begin{cases} \alpha_i' = \alpha_i (i = 1, 2, 3, 4) \\ \varphi_1' = \varphi_1 + (\alpha_3 - \alpha_2), \varphi_2' = \varphi_2 + (\alpha_3 - \alpha_2) \\ \varphi_3' = \varphi_3 + (\alpha_3 - \alpha_2), \varphi_4' = \varphi_4 + (\alpha_3 - \alpha_2) \end{cases} \\ \text{Mode III}: &\begin{cases} \alpha_1' = \alpha_1 + (\alpha_3 - \alpha_2), \alpha_2' = \alpha_2 + (\alpha_3 - \alpha_2) \\ \alpha_3' = \alpha_3 - (\alpha_3 - \alpha_2), \alpha_4' = \alpha_4 - (\alpha_3 - \alpha_2) \\ \varphi_1' = \varphi_1 - (\alpha_3 - \alpha_2), \varphi_2' = \varphi_2 - (\alpha_3 - \alpha_2) \\ \varphi_3' = \varphi_3 + (\alpha_3 - \alpha_2), \varphi_4' = \varphi_4 + (\alpha_3 - \alpha_2) \end{cases} \\ \text{Mode IV}: &\begin{cases} \alpha_1' = \alpha_1, \alpha_2' = \alpha_2 + (\alpha_3 - \alpha_2) \\ \alpha_3' = \alpha_3 - (\alpha_3 - \alpha_2), \alpha_4' = \alpha_4 \\ \varphi_i' = \varphi_i, (i = 1, 2, 3, 4) \end{cases} \end{aligned} \tag{5}$$

On the other hand, for the condition $V_{CU} < V_{CL}$, since the required neutral-point current i_o is negative, which is opposite to that of the condition $V_{CU} > V_{CL}$, the beneficial and adverse switching states will also be opposite. Thus, the implementation of the CSS method under the four conditions I_{L2} [A, B] > 0 and I_{L2} [C, D] > 0, I_{L2} [A, B] > 0 and I_{L2} [C, D] < 0, I_{L2} [A, B] < 0 and I_{L2} [C, D] > 0, I_{L2} [A, B] < 0 and I_{L2} [C, D] < 0 are similar to Modes IV, III, II and I, respectively.

C. Application of the CSS Method

According to the above analysis, the polarity of the transformer current in the CSS method can be obtained by using the steady-state current and power models due to the unchanged voltage and current waveforms during the balancing process. The dwell time of the intervals where the switching states should be modified (i.e., [A, B], [C, D], [a, b], and [c, d]) is $(D_2 - D_1)T_{hs}$, which is further determined by the modulation schemes and operating conditions. Two examples are given to exemplify the proposed CSS method in typical operating conditions.

• *Example 1:* Zero-voltage-switching (ZVS) modulation is employed in many applications to reduce the switching losses [19]–[21]. The ZVS constraints for the secondary side of the 2/3-level DAB converters have been discussed widely as [19]

$$i_{L2}(\text{A}) > 0, i_{L2}(\text{B}) > 0, i_{L2}(\text{C}) > 0, i_{L2}(\text{D}) > 0 \tag{6}$$

Thus, in the ZVS modulation strategies for the 2/3-level DAB converters, the current polarity during the intervals [A, B] and [C, D] is positive. In this way, the operating mode can be determined as Mode I for the condition $V_{CU} > V_{CL}$ and Mode IV for the condition $V_{CU} < V_{CL}$.

• *Example 2:* The DAB converters are generally expected to operate under the condition $k = 1$ ($k = nV_1/V_2$), especially when the two DC-link voltages are constant, since the soft-switching capability can be enhanced and the circulating power can be reduced in such a condition. For the condition of $k = 1$,

the transformer current of the four critical points A, B, C, D can be calculated based on (1) as

$$\begin{cases} i_{L2}(\mathrm{A}) = \dfrac{V_2 T_{hs}}{n^2 L_s}(1.5D_1 - 0.5D_2 - 0.5D) \\ i_{L2}(\mathrm{B}) = \dfrac{V_2 T_{hs}}{n^2 L_s}(D_2 - 0.5D) \\ i_{L2}(\mathrm{C}) = \dfrac{V_2 T_{hs}}{n^2 L_s}(D_1 + 0.5D) \\ i_{L2}(\mathrm{D}) = \dfrac{V_2 T_{hs}}{n^2 L_s}(0.5D_1 + 0.5D_2 + 0.5D) \end{cases} \tag{7}$$

Thus, the average current during the two intervals [A, B] and [C, D] can be obtained as

$$\begin{cases} I_{L2}[\mathrm{A,B}] = \dfrac{V_2 T_{hs}}{2n^2 L_s}(1.5D_1 + 0.5D_2 - D) \\ I_{L2}[\mathrm{C,D}] = \dfrac{V_2 T_{hs}}{2n^2 L_s}(1.5D_1 + 0.5D_2 + D) \end{cases} \tag{8}$$

where it can be seen that $I_{L2}[\mathrm{C,D}] > 0$ is satisfied with all combinations of the control variables D_1, D_2, and D. However, the polarity of the average transformer current during the interval [A, B] should be further analyzed. For each modulation strategy, the control variables can be determined under a certain reference power according to the power and current models. Based on it, the polarity of $I_{L2}[\mathrm{A,B}]$ can be calculated. This model-based method can be used to identify the current polarity in all operating conditions (in addition to the condition $k = 1$). On the other hand, it can be calculated from (8) that $I_{L2}[\mathrm{C,D}] - |I_{L2}[\mathrm{A,B}]| > 0$. Since the dwell time of the two intervals [A, B] and [C, D] is identical, there will be more charges injected into/drawn from the neutral point during the interval [C, D] than that during the interval [A, B]. Therefore, the switching state employed in the interval [C, D] is the dominant one for regulating the capacitor voltages. In this way, the polarity of $I_{L2}[\mathrm{A,B}]$ will not affect the direction of the neutral-point current during the entire switching cycle. Thus, one of Modes I and III can be applied for the condition $V_{CU} > V_{CL}$ and one of Modes II and IV can be applied for the condition $V_{CU} < V_{CL}$. Compared to the model-based method, this method simplifies the balancing process significantly. However, the balancing time may be increased due to the uncertain polarity of $I_{L2}[\mathrm{A,B}]$.

Furthermore, for other operating conditions, e.g., the two-side DC voltages are not matched (i.e., $k \neq 1$), the transformer current polarity can be obtained based on the model-based method, and then, the corresponding mode can be selected. In summary, the proposed CSS method can be realized by the following three steps: 1) Based on the unbalanced conditions ($V_{CU} > V_{CL}$ or $V_{CU} < V_{CL}$), the required direction of the neutral-point current can be determined; 2) The beneficial and adverse switching states can be identified based on the polarity of the transformer current; 3) The two adverse switching states are replaced by their CSSs, as shown in Fig. 9.

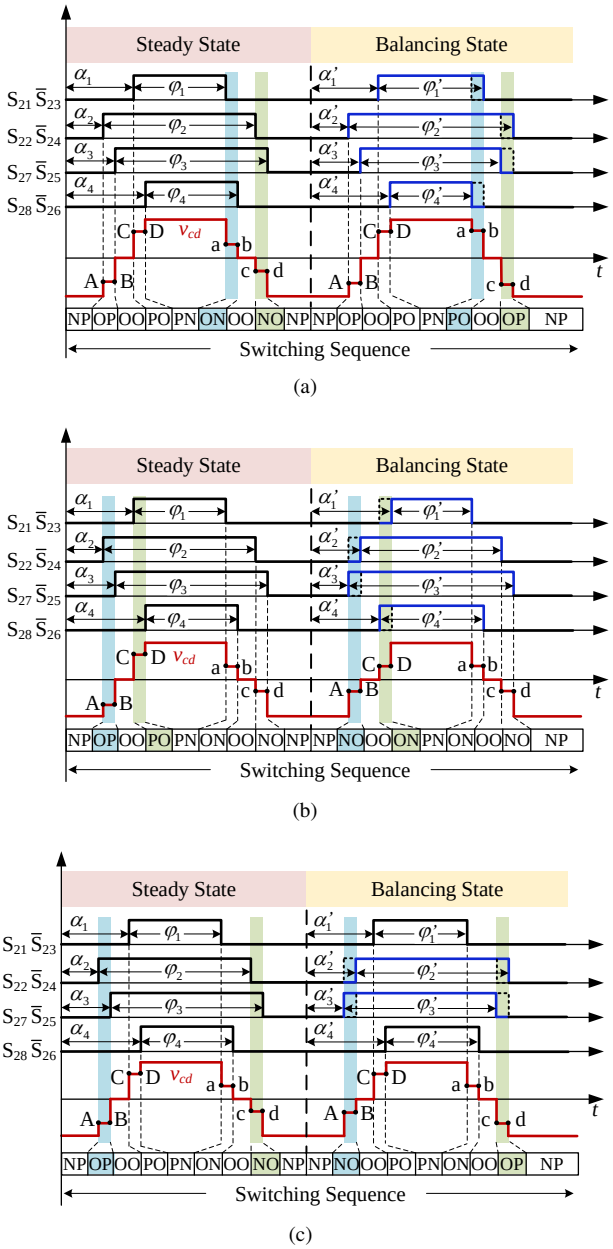


Fig. 8. Illustration of the proposed CSS method under the condition $V_{CU} > V_{CL}$ with: (a) Mode II: I_{L2} [A, B] > 0 and I_{L2} [C, D] < 0, (b) Mode III: I_{L2} [A, B] < 0 and I_{L2} [C, D] > 0, and (c) Mode IV: I_{L2} [A, B] < 0 and I_{L2} [C, D] < 0.

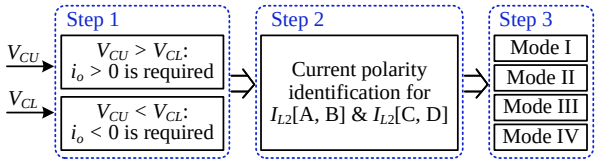


Fig. 9. Control structure for the proposed CSS method.

IV. Experimental Results

To verify the performance of the proposed capacitor voltage balancing control scheme based on the CSS method, experimental tests are performed based on a 2.5-kW setup, as shown in Fig. 10. A dSPACE MicroLabBox is employed as the control system, and the main parameters of the experimental system are shown in Table IV.

Fig. 11 shows the experimental results by using the traditional balancing (TB) method (i.e., Fig. 6), where the input

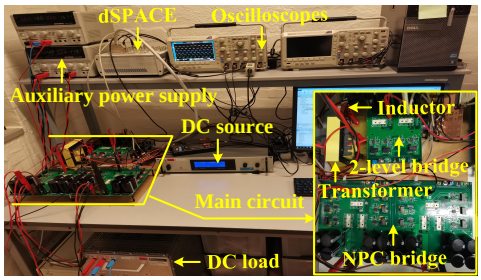
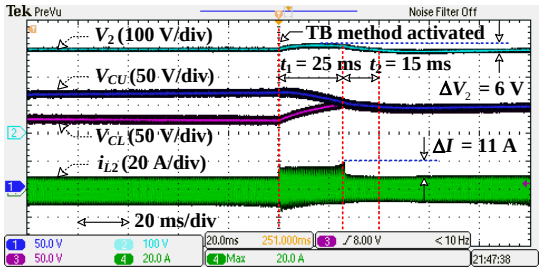


Fig. 10. Prototype of a 2/3-level DAB converter.

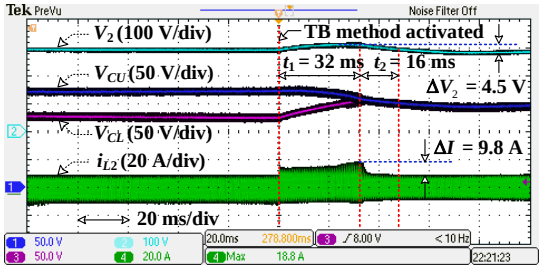
TABLE IV
MAIN PARAMETERS OF THE EXPERIMENTS

Parameters	Values
Rated power P	2.5 kW
Input voltage V_1	150 V
Reference output voltage V_{2ref}	300 V
Transformer turns-ratio n	2
Series inductor L_s	100 μH
DC capacitors C_1, C_U and C_L	680 μF
Switching frequency f_s	10 kHz
Power switches (IGBT)	Semikron SK35GB12T4

voltage is 150 V, the reference output voltage is 300 V, and the output DC load is 57.5 Ω. In addition, the steady-state control variables are: $D_2 = 0.2$, $D = 0.2$, and D_1 is regulated by a closed-loop control system to achieve the reference output voltage. The capacitor voltage imbalance is realized by shifting an extra angle for the gate-driving signal for S_{22} and S_{24} ($\alpha' = 0.05T_{hs}$ in Fig. 4 (a)), which is maintained after the balancing control schemes are enabled. When the deviation of the two capacitor voltages reaches 50 V, i.e., $V_{CU} - V_{CL}$ = 50 V, the balancing control scheme is employed. According to the analysis in Section III, the regulated phase-shift angles should satisfy that $\beta_1 \leq DT_{hs}$ and $\beta_2 \leq DT_{hs}$ (β_1 and β_2 can be seen in Fig. 6). Thus, the maximum value for these two regulated phase-shift angles is $0.2T_{hs}$, which is also the maximum value of the upper threshold K (see Fig. 6) when the multiplier M is applied as 1. From Fig. 11, it can be seen that with various K, the performance in terms of the increased peak current, and the settling time will be different. In Fig. 11 (a), K = $0.19T_{hs}$ is employed, and it can be seen that the two capacitor voltages can become balanced after a balancing period of t_1 = 25 ms. Meanwhile, the peak value of the transformer current i_{L2} will increase from 9 A in the steady state to 20 A, which leads to an overshoot current as $\triangle I$ = 11 A (122% increment). Besides, the output voltage will also fluctuate with an increased value $\triangle V_2$ = 6 V during the balancing process. After the capacitor voltage balancing process is completed, the DAB converter will realize the reference output voltage (i.e., 300 V), and enter the new steady state with another period of t_2 = 15 ms. Therefore, in the traditional balancing method, the total settling time t_s is 40 ms ($t_s = t_1 + t_2$). The overshoot current in the traditional balancing method can be reduced when K is decreased, which can be seen in Fig. 11 (b) and (c). However, the settling time will be increased in the meanwhile, being 48 ms and 53 ms, respectively, resulting in a slower dynamic of



(a)



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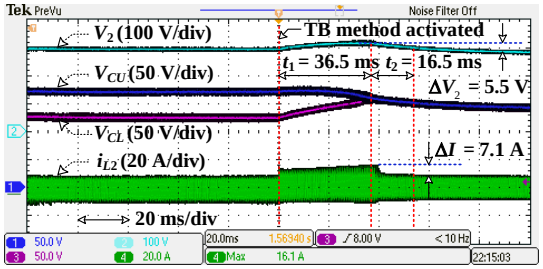

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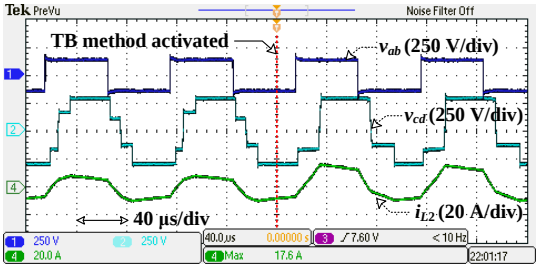
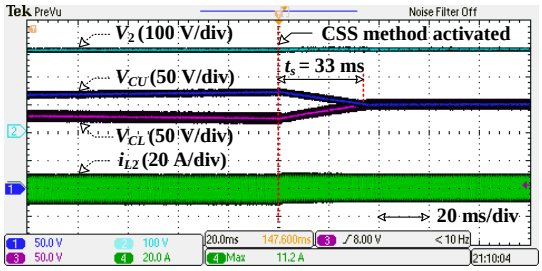


(d)

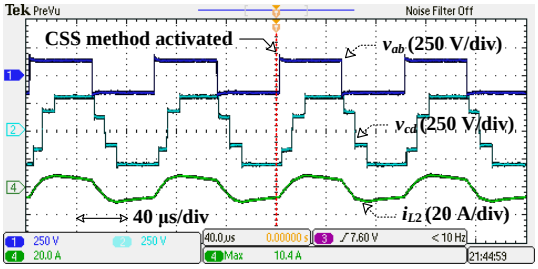
Fig. 11. Experimental results with the traditional balancing (TB) method for the condition $V_{CU} - V_{CL} = 50$ V with $D_2 = 0.2$, and $D = 0.2$ under: (a) K = $0.19T_{hs}$, (b) K = $0.15T_{hs}$, and (c) K = $0.1T_{hs}$. (d) Zoomed-in transient waveforms under K = $0.19T_{hs}$.

the balancing process. The zoomed-in experimental waveforms of v_{ab}, v_{cd}, and i_{L2} are shown in Fig. 11 (d), where the upper threshold K is applied as $0.19T_{hs}$. It can be seen from Fig. 11 (d) that when the traditional balancing method is employed, the waveform of the voltage v_{cd} will be affected during the transition due to the regulated phase-shift angles. Therefore, the peak value of the transformer current will increase, and the transferred power will also fluctuate.

On the other hand, with the same parameters, the dynamic performance of the 2/3-level DAB converter with the proposed CSS method is shown in Fig. 12, where Mode I is selected to regulate the capacitor voltages. It can be seen from the



(a)



(b)

Fig. 12. Experimental results with the proposed CSS method for the condition $V_{CU} - V_{CL} = 50$ V: (a) waveforms of the output voltage, capacitor voltages, and transformer current, and (b) zoomed-in transient waveforms of the transformer voltages and current.

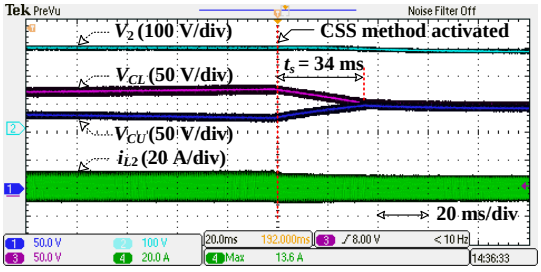


Fig. 13. Experimental results with the proposed CSS method for the condition $V_{CL} - V_{CU} = 50$ V.

results in Fig. 12 (a) that when the CSS method is employed under the condition $V_{CU} - V_{CL}$ = 50 V, the balancing control can be completed within t_s = 33 ms. During the balancing process, the overshoot current and output voltage fluctuation are effectively eliminated. The entire settling time is 33 ms without an extra regulating period (i.e., t_2 in Fig. 11). Fig. 12 (b) shows the zoomed-in transient waveforms of v_{ab}, v_{cd}, and i_{L2}, where it can be seen that the waveform of v_{cd} after employing the CSS method is similar to the steady-state voltage waveform. Therefore, the transformer current and power will also remain unchanged, which leads to smooth transition during the balancing process. Similarly, the experimental results for the condition $V_{CU} < V_{CL}$ are shown in Fig. 13, where the operating parameters are identical to those in Fig. 12. The initial capacitor voltage imbalance for $V_{CU} < V_{CL}$ is realized by adding an extra phase-shift angle of the gate-driving signal for S_{21} and S_{23}. Similar to the analysis for Fig. 12, the overshoot current and output voltage fluctuation can be significantly reduced when the proposed method is adopted.

The comparison between the proposed CSS method and

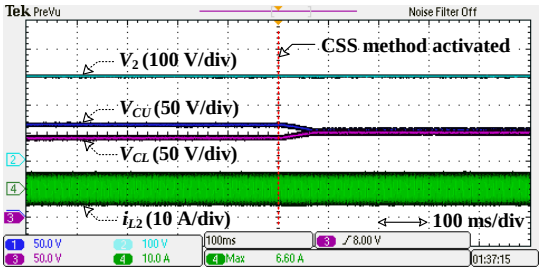


Fig. 14. Experimental results with the proposed CSS method under different capacitors $C_U = 680$ µF and $C_L = 1020$ µF with D_2 = 0.11 and D = 0.08.

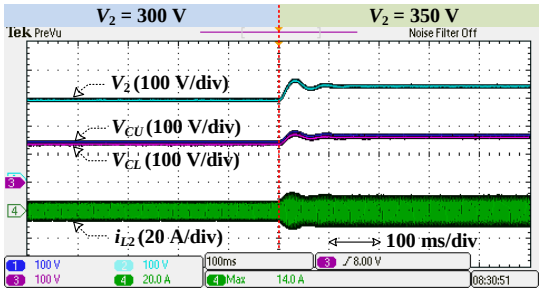
traditional balancing method under different transferred power and control variables for the condition $V_{CU} - V_{CL} = 50$ V is summarized in Table V. It can be seen from Table V that with the traditional balancing method, the current overshoot $\triangle I$ and output voltage fluctuation $\triangle V_2$ can be reduced when the upper threshold K decreases. However, the settling time t_s will be increased. By contrast, with the proposed CSS method, the current overshoot $\triangle I$ and output voltage fluctuation $\triangle V_2$ can be significantly reduced. Besides, although the capacitor voltage balancing time t_1 of the CSS method may be increased compared to that of the traditional balancing method with a large K, the total settling time t_s can be reduced due to no extra regulating time t_2 to realize the reference output voltage. Therefore, the overall dynamic performance of the converter is improved. Furthermore, since the voltage and current waveforms after employing the traditional balancing method are fluctuated during transient, the identification of the transformer current polarity will be more difficult compared to the proposed CSS method due to the unchanged dynamic waveforms. In addition, the value of the upper threshold K should be modified under different operating conditions to compromise the overshoot current and settling time in the traditional balancing method. Therefore, the balancing control can be simplified with the proposed CSS method.

In addition, different upper and lower capacitors will also lead to capacitor voltage imbalance. Fig. 14 shows the experimental results, where the upper capacitor C_U is 680 µF, and the lower capacitor C_L is 1020 µF. It can be seen from Fig. 14 that the deviation between V_{CU} and V_{CL} is around 20 V caused by the different capacitors. After applying the proposed balancing control scheme, the two capacitor voltages can be balanced without current/output voltage fluctuation. Thus, the unbalanced condition due to the tolerances in the capacitors or uneven degradation of the capacitors can be solved effectively by the proposed balancing method.

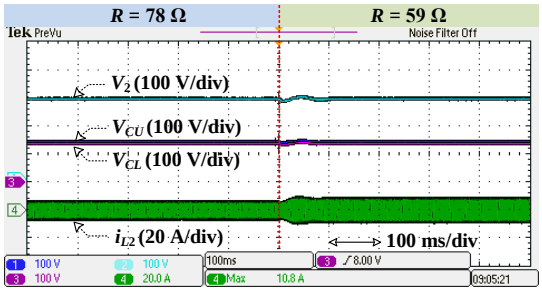
Furthermore, the experimental transient waveforms with step changes in the reference output voltage and load are shown in Fig. 15, where the proposed balancing control scheme is enabled from the beginning. In Fig. 15 (a), the input voltage is 150 V, and the output voltage changes from 300 V to 350 V. It can be seen from Fig. 15 (a) that the two capacitor voltages can be kept balanced during the transient process, which means the balancing control is retained during the transient. A similar condition applies to Fig. 15 (b), where

TABLE V
EXPERIMENTAL RESULTS FOR THE CAPACITOR VOLTAGE BALANCING CONTROL SCHEMES UNDER DIFFERENT OPERATING STATES

States	Control Variables	DC Load/Transferred Power	Balancing Methods	t_s	$\triangle I$	$\triangle V_2$
1	$D_2 = 0.35$ $D = 0.15$	$R = 45\Omega$ $P = 2000$W	Traditional method	K = $0.14T_{hs}$: $t_s = t_1 + t_2 = 5.8 + 12 = 17.8$ ms	10 A	4.5 V
				K = $0.1T_{hs}$: $t_s = t_1 + t_2 = 7.5 + 11.5 = 19$ ms	8 A	2.8 V
				K = $0.05T_{hs}$: $t_s = t_1 + t_2 = 14.5 + 13 = 27.5$ ms	4.5 A	2 V
			CSS method	$t_s = t_1 = 16.0$ ms	1.0 A	1.3 V
2	$D_2 = 0.30$ $D = 0.20$	$R = 57.5\Omega$ $P = 1565$W	Traditional method	K = $0.19T_{hs}$: $t_s = t_1 + t_2 = 6.6 + 16 = 22.6$ ms	12 A	5 V
				K = $0.15T_{hs}$: $t_s = t_1 + t_2 = 8.7 + 15 = 23.7$ ms	10 A	4.6 V
				K = $0.10T_{hs}$: $t_s = t_1 + t_2 = 14 + 18 = 32$ ms	7.5 A	4 V
			CSS method	$t_s = t_1 = 13.0$ ms	1.2 A	3.2 V
3	$D_2 = 0.15$ $D = 0.12$	$R = 80\Omega$ $P = 1125$W	Traditional method	K = $0.11T_{hs}$: $t_s = t_1 + t_2 = 35 + 23 = 58$ ms	8.5 A	16 V
				K = $0.07T_{hs}$: $t_s = t_1 + t_2 = 65 + 18 = 83$ ms	6 A	10 V
				K = $0.03T_{hs}$: $t_s = t_1 + t_2 = 120 + 15 = 135$ ms	2.5 A	7.5 V
			CSS method	$t_s = t_1 = 37.0$ ms	0.9 A	4.0 V
4	$D_2 = 0.11$ $D = 0.08$	$R = 95\Omega$ $P = 947$W	Traditional method	K = $0.07T_{hs}$: $t_s = t_1 + t_2 = 47 + 20 = 67$ ms	14 A	18 V
				K = $0.05T_{hs}$: $t_s = t_1 + t_2 = 65 + 18 = 73$ ms	7 A	13 V
				K = $0.03T_{hs}$: $t_s = t_1 + t_2 = 85 + 18 = 103$ ms	3.5 A	8.5 V
			CSS method	$t_s = t_1 = 58.0$ ms	0.8 A	4.2 V



(a)



(b)

Fig. 15. Transient response by applying the proposed CSS method with a step change in: (a) output voltage from 300 V to 350 V, and (b) load from 78 Ω to 59 Ω.

the reference output voltage keeps constant at 300 V, and the load changes from 78 Ω to 59 Ω (i.e., the transferred power changes from 1150 W to 1530 W). Therefore, the capacitor voltages can be balanced by employing the proposed balancing control scheme during the transients.

V. CONCLUSION

This paper proposed a capacitor voltage balancing control scheme based on the CSS method for the 2/3-level DAB converters. The relationships between the neutral-point current and the polarity of the transformer current under different switching states were analyzed first. As a result, two CSS pairs were obtained. In the proposed CSS method, the adverse switching states are replaced by their CSSs. After that, the voltage and current waveforms during the balancing process remain identical to the steady-state waveforms, and meanwhile, the direction of the neutral-point current can be controlled to achieve the voltage balancing. In this way, the four switching states during each switching cycle are all beneficial for regulating the capacitor voltages without dynamic power fluctuation and overshoot current. Furthermore, due to the unchanged dynamic waveforms, the transformer current polarity can be obtained based on the steady-state power and current models, which can simplify the identification for the current polarity. Experimental results have validated that the proposed CSS method can achieve better dynamics. In addition to the capacitor voltage imbalance caused by the asymmetries between capacitors or gating-driving signals, the proposed balancing control can also be applied in the bipolar DC systems, where the voltage imbalance can also occur due to different loads.

ACKNOWLEDGMENT

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REFERENCES

[1] F. Wu, F. Feng, and H. B. Gooi, "Cooperative triple-phase-shift control for isolated DAB DC-DC converter to improve current characteristics," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 7022-7031, Sept. 2019.

[2] S. Luo, F. Wu, and G. Wang, "Effect of dead band and transient actions on CTPS modulation for DAB DC-DC converter and solutions," *IEEE Trans. Transport. Electrific.*, vol. 7, no. 3, pp. 949-957, Sep. 2021.

[3] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148-3172, Mar. 2020.

[4] V. Karthikeyan and R. Gupta, "FRS-DAB converter for elimination of circulation power flow at input and output ends," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2135-2144, Mar. 2018.

[5] M. A. Moonem and H. Krishnaswami, "Analysis and control of multi-level dual active bridge DC-DC converter," in *Proc. ECCE*, Raleigh, NC, 2012, pp. 1556-1561.

[6] P. Liu, C. Chen, S. Duan, and W. Zhu, "Dual phase-shifted modulation strategy for the three-level dual active bridge DC-DC converter," *IEEE Trans. Ind. Electron*., vol. 64, no. 10, pp. 7819-7830, Oct. 2017.
[7] Y. Wang, H. Wen, Y. Zhu, H. Shi, Q. Bu, Y. Hu, and Y. Yang, "Minimum-current-stress scheme of three-level dual-active-bridge DC-DC converters with the particle swarm optimization," *IEEE Trans. Transport. Electrific*., vol. 7, no. 4, pp. 2067-2084, Dec. 2021.
[8] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A novel NPC dual-active-bridge converter with blocking capacitor for energy storage system," *IEEE Trans. Power Electron*., vol. 34, no. 11, pp. 10635-10649, Nov. 2019.
[9] P. Liu, C. Chen, and S. Duan, "An Optimized Modulation Strategy for the Three-Level DAB Converter With Five Control Degrees of Freedom," *IEEE Trans. Ind. Electron*., vol. 67, no. 1, pp. 254-264, Jan. 2020.
[10] C. Song, Y. Yang, A. Sangwongwanich, Y. Pan, and F. Blaabjerg, "Modeling and analysis of 2/3-level dual-active-bridge DC-DC converters with the five-level control scheme," in *Proc. IEEE APEC*, USA, 2021, pp. 1958-1963.
[11] A. F. Martínez, S. B. Monge, and J. Bordonau, "Modulation and capacitor voltage balancing control of a three-level NPC dual-active-bridge DC-DC converter," in *Proc. IECON*, Austria, 2013, pp. 6251-6256.
[12] M. A. Moonem, T. Duman, and H. Krishnaswami, "Capacitor voltage balancing in a neutral-point clamped multilevel dc-dc dual active bridge converter," in *Proc. PEDG*, Brazil, 2017, pp. 1-7.
[13] A. F. Martinez, S. B. Monge, and J. Bordonau, "Modulation and capacitor voltage balancing control of multilevel NPC dual active bridge DC-DC converters," *IEEE Trans. Ind. Electron*., vol. 67, no. 4, pp. 2499-2510, Apr. 2020.
[14] A. F. Martinez, S. B. Monge, J. N. Apruzzese, and J. Bordonau, "Operating principle and performance optimization of a three-level NPC dual-active-bridge DC-DC converter," *IEEE Trans. Ind. Electron*., vol. 63, no. 2, pp. 678-690, Feb. 2016.
[15] M. A. Awal, M. R. H. Bipu, O. A. Montes, H. Feng, I. Husain, W. Yu, and S. Lukic, "Capacitor voltage balancing for neutral point clamped dual active bridge converters," *IEEE Trans. Power Electron*., vol. 35, no. 10, pp. 11267-11276, Oct. 2020.
[16] C. Li, T. Yang, P. Kulsangcharoen, G. L. Calzo, S. Bozhko, C. Gerada, and P. Wheeler, "A modified neutral point balancing space vector modulation for three-level neutral point clamped converters in high-speed drives," *IEEE Trans. Ind. Electron*., vol. 66, no. 2, pp. 910-921, Feb. 2019.
[17] J. Lee, H. Choi, and J. Jung, "Three level NPC dual active bridge capacitor voltage balancing switching modulation," in *Proc. IEEE INTELEC*, Australia, 2017, pp. 438-443.
[18] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor voltage balancing control scheme for 2/3-Level DAB converters," in *Proc. IECON*, Canada, 2021, pp. 1-6.
[19] L. Jin, B. Liu, and S. Duan, "ZVS soft switching operation range analysis of three-level dual-active bridge DC-DC converter under phase shift control strategy," *IEEE Trans. Ind. Appl*., vol. 55, no. 2, pp. 1963-1972, Mar-Apr. 2019.
[20] P. Liu and S. Duan, "A ZVS range enhancement strategy for the DAB converter by using blocking capacitors," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 9, no. 2, pp. 1389-1398, Apr. 2021.
[21] Y. Lu, Q. Wu, Q. Wang, D. Liu, and L. Xiao, "Analysis of a novel zero-voltage-switching bidirectional DC/DC converter for energy storage system," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 3169-3179, Apr. 2018.

Chaochao Song (S'21) received the B.S. degree in automation and M.S. degree in power electronics from Shandong University, Jinan, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree at Aalborg University, Aalborg, Denmark.

His current research interests include multilevel converters and renewable power generation.

Ariya Sangwongwanich (S'15-M'19) received the M.Sc. and Ph.D. degree in energy engineering from Aalborg University, Denmark, in 2015 and 2018, respectively. He is currently working as an Assistant Professor at the Department of Energy Technology, Aalborg University, where he is a Vice-Leader of Photovoltaic Systems research program. His research interests include control of grid-connected converters, photovoltaic systems, reliability in power electronics, and multi-level converters.

He was a Visiting Researcher with RWTH Aachen, Aachen, Germany from September to December 2017. Dr. Sangwongwanich was the recipient of the Danish Academy of Natural Sciences' Ph.D. Prize and the Spar Nord Foundation Research Award for his Ph.D. thesis in 2019.

Yongheng Yang (SM'17) received the B.Eng. degree in electrical engineering and automation from Northwestern Polytechnical University, China, in 2009 and the Ph.D. degree in energy technology (power electronics and drives) from Aalborg University, Denmark, in 2014.

He was a postgraduate student with Southeast University, China, from 2009 to 2011. In 2013, he was a Visiting Scholar at Texas A&M University, USA. During 2014-2020, he was with the Department of Energy Technology, Aalborg University, where he became a tenured Associate Professor in 2018. In January 2021, he joined Zhejiang University, China, as a ZJU100 Professor. His research focuses on the grid-integration of photovoltaic systems and control of power converters, in particular, the grid-forming control technologies.

Dr. Yang was the Chair of the IEEE Denmark Section (2019-2020). He is an Associate Editor for several IEEE Transactions. He was the recipient of the 2018 IET Renewable Power Generation Premium Award and was an Outstanding Reviewer for the *IEEE TRANSACTIONS ON POWER ELECTRONICS* in 2018. He was the recipient of the 2021 Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society (PELS) and the 2022 Isao Takahashi Power Electronics Award. In addition, he has received two IEEE Best Paper Awards. He has been included on the list of Highly Cited Chinese Researchers by Elsevier in 2022. He is currently the Secretary of the IEEE PELS Technical Committee on Sustainable Energy Systems and a Council Member of the China Power Supply Society.

Frede Blaabjerg (S'86-M'88-SM'97-F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 33 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves as a President of IEEE Power Electronics Society. He has been Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014-2020 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.