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***Abstract*— Determining the reliability of 10 kV SiC-MOSFET power modules experimentally, is challenging due to the low number of samples available in the market. A digital design based on 3D thermal calculations is demonstrated to improve reliability capability in a 10 kV SiC-MOSFET power module. The module design was determined based on the calculation with digital twin modelling. The correctness of the digital twin model was confirmed by fabricating a 10kV SiC-MOSFETs power module sample and comparing the calculation temperature with the measured results. The design was focused on aluminum wires on chips, and the effect of the wire temperature by changing the wire layout was clarified. The results show that the improved wire layout reduces the wire temperature by 2.2-5.3% compared to the conventional design. This is expected to increase the power cycle capability by up to 31%, according to predictions based on the Coffin-Manson model.**

Keywords— —10 kV SiC MOSFET, power module, digital design, 3D thermal simulation, power cycle

I. INTRODUCTION

Power modules with Silicon Carbide metal-oxide-semiconductor field effect transistors (SiC-MOSFET) can be applied in higher voltage ranges than the currently mainstream Silicon insulated-gate bipolar transistor (Si-IGBT) power modules due to the material properties of SiC. For applications of 10kV or higher, SiC MOSFETs have superior output characteristics compared to Si IGBTs [1], which has led to increased interest in SiC MOSFET medium voltage power modules. However, there are currently only engineering samples of 10kV SiC-MOSFET chips available on the market. Therefore, it is challenging for module designers to obtain the necessary number of chips for their design verification of reliability. Thus, following a conventional procedure of several experimental power cycling tests, may result in high design costs and long design lead times. Instead, design optimization by "digital design" is very useful for products with such scarce devices, as it enables optimized design parameters without building many physical prototypes in a laboratory. Digital design is gaining attention as a next-generation product design method for power electronics [2]. This is a method of optimizing product structures using a digital twin of the target product. This enables high-quality products to be designed in a short time and reducing the number of physical prototypes in the laboratory.

The power module characteristics covered by the design process include electrical, thermal, mechanical, structural, and reliability [3, 4]. Reliability design, as typified by power cycle capability, is a process that requires many prototypes and much evaluation time. For example, five samples are required per one reliability test, so dozens of samples are needed for all reliability tests [4]. Moreover, each test takes about 2-3 months, which adds up as “design lead time” as the number of tests increases. In addition, it is difficult to prepare the required number of samples for reliability testing for modules with devices that are not widely available in the market, such as 10kV SiC-MOSFETs. In such reliability design, the product structure can be optimized before physical measurements are made by utilizing digital design. As a result, the number of physical prototypes and tests can be reduced compared to conventional trial-and-error design methods based on actual power cycling measurement results.

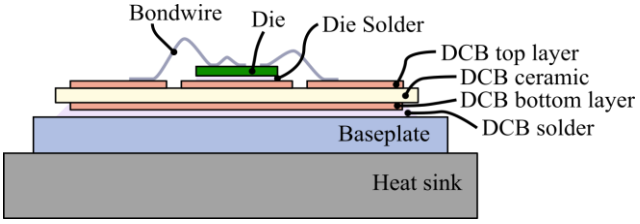

Fig. 1. Cross sectional image of power module structure

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The structure of a conventional power module (Direct Copper Bonding (DCB), solder, semiconductor chip and bondwire(Al)), which is shown in Fig. 1, typically has three weak points for long-term reliability tests. They are (1) Chip-wire interface, (2) Chip-solder interface, (3) DCB-base plate interface [5]. Especially, (1) occurs most frequently in semiconductor packages and requires special attention in power modules that handle high temperature and high power [6]. Therefore, what is studied in this paper is how to improve the chip-wire interface delamination capability. This failure is due to strain and stress caused during heat generation between materials with different coefficients of thermal expansion (CTEs). Therefore, mitigating the thermal stress of wires on the chip when the device is operated improves the power cycle capability. As an example, it has been shown that, in the case of Si PIN diodes, the temperature difference between the aluminum wires and the device is reduced by optimising the wire layout on the chip [7]. This is one of the simplest design optimisations to improve the reliability of wire bonds, which does not require more advanced material technologies for connections. For devices with new materials or structures, such as 10 kV SiC-MOSFETs, the temperature distribution model on the chip surface has not been sufficiently validated. Therefore, it is unclear to what extent reliability will be affected.

In this paper, 10kV SiC-MOSFET modules are investigated based on the 3D thermal calculation to improve the power cycle capability. First, a simulation framework for calculation of thermal parameters is experimentally verified through comparison with prototype measurements of existing 10kV SiC-MOSFET power modules. Second, the thermal distribution effect of the larger edge length in 10 kV SiC-MOSFETs is analyzed in the calculation. Finally, the module design is demonstrated in the digital twin, with particular focus on the wire layout on the chip source pad. The "digital design" method was evaluated by estimating the effect of the design on power cycle performance improvement.

II. METHODOLOGY

The target module in this research is a package with a half-bridge power module incorporating 10 kV SiC-MOSFETs [8, 9] which is the same structure in Fig. 1. The device installed is a Wolfspeed 3rd generation SiC-MOSFET CMP3-100000-035B (Ron=350mΩ). Thermal simulation was performed using ANSYS mechanical (Workbench 2021 R1) [10].

A. *3D Thermal modelling of 10kV SiC-MOSFET modules*

First, it was checked whether the thermal calculation results from the 3D model can be correctly reproduced by comparing the calculations with the actual measurements. The module and SiC-MOSFET 3D models in this calculation are shown in Fig. 2. The module layout detail is found in [9] [11]. In thermal calculations, the module model without the case, terminals and gel shown in Fig. 2-b was used. The components of the module and the various physical properties used in the calculations are shown in TABLE I [9, 12-15]. The SiC-MOSFET is modelled

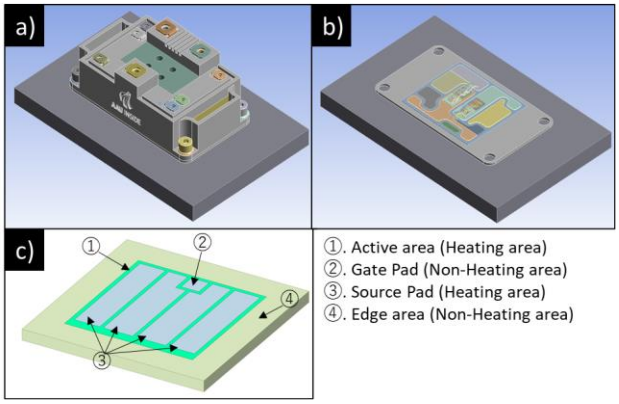


Fig. 2. 3D model of power modules and SiC-MOSFET

a). 3D model of the 10kV SiC-MOSFET power module package with a heat sink. b). 3D model for thermal calculations without the case, terminals, and isolation gel. c). 3D model of a 10 kV SiC-MOSFET device that consists of heating area (Active area, Source pad) and non-heating area (Gate pad, Edge area).

as four parts : active part, gate pad, source pad and edge part (i.e. Edge areas to reduce the concentration of electric fields generated at the perimeter of the chip), as shown in Fig. 2-c, and the active part and the source pad was calculated as the heating element [11]. For the operating conditions, a single DC constant power profile (on/off=2/3sec, T_0=23°C,) simulating a power cycle test was performed. In order to compare with the measurement results, the applied power value was determined so that the maximum chip surface temperature change $\Delta T_{\text{chip surface max}}$=100°C.

TABLE I. THICKNESS AND PROPERTIES OF MATERIALS[9, 12-15]

Structure	***Material***	***Thickness* [9]**	***Density [kg/m3]***	***Thermal conductivity [W/(m・K)]***	***Heat capacity [J/(kg・K)]]***
Bondwire	Al	250μm	2689*	237.5*	880*
Die	4H-SiC	500μm	3240 [12]	353.3 [12]	551.8 [12]
Die solder	96.5Sn-3Ag-0.5Cu	50μm	7370 [12]	57 [12]	220 [12]
DCB top layer	Cu	300μm	8960 [13]	400 [13]	385 [13]
DCB ceramic	AlN	630μm	3300 [14]	150 [14]	710 [14]
DCB bottom layer	Cu	300μm	8960	400	385
DCB Solder	96.5Sn-3Ag-0.5Cu	50μm	7370	57	220
Baseplate	AlSiC	1.5mm	2600 [15]	140 [15]	730 [15]
Heat sink	Al	10cm	2689	237.5	880

* General material properties in the ANSYS material library

For actual measurements, the test sample of 10 kV SiC-MOSFET module without gel was manufactured. The power was energized under the same conditions as the calculation, and the chip surface temperature was measured with an optical fiber (OTG-F type-10-62ST, from OpSens Solutions) as shown in Fig. 3.

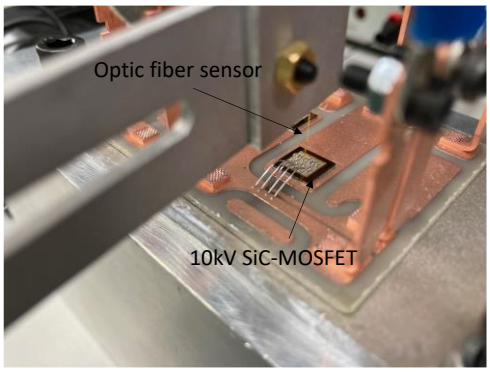


Fig. 3. The picture of chip surface temperature measurement by the optic fiber sensor

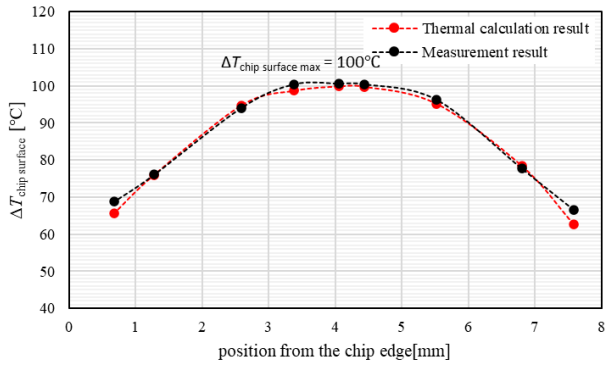


Fig. 4. Comparative results of 3D thermal calculations and measured 10kV SiC-MOSFET temperatures $\Delta T_{chip\ surface}$. (line profile on the chip)

B. *Temperature distribution for the SiC-MOSFET*

3D thermal calculations focusing on the chip edge length were performed to verify the surface temperature distribution of the 10kV SiC-MOSFET. SiC-MOSFETs with different edge length were analyzed. The temperature distribution of 10 kV SiC-MOSFETs was characterised by comparing the other edge length SiC-MOSFETs calculation results. The calculation conditions were DC constant power profile (on/off=2/3sec, T_0=25°C). Therefore, the applied power value was adjusted so that the maximum chip surface temperature $T_{chip\ surface\ max}$ = 175°C ($\Delta T_{chip\ surface\ max}$=150°C) since the temperature distribution of the chip is clearer at higher temperatures.

C. *Design of modules structures to improve the power cycle capabilities*

According to the thermal characteristics of the 10 kV SiC-MOSFETs shown in the above calculations, the module structures that improve power cycle capability were estimated and module design in 3D models were created. 3D thermal calculations were performed on these models to confirm the effect of improved power cycle performance. The calculation conditions were similar to methodology B.

III. RESULT

A. *Comparison of 3D thermal simulation and actual sample measurements*

The temperature distribution of the 10kV SiC-MOSFET surface by calculations is compared with the measured results. The one-dimensional profile of chip surface temperature ΔT_j with respect to position on the chip are shown in Fig. 4. The results show that the calculated surface temperature agree well with the measured results with a error value of less than 4 K. The simulated line profile is visualized in Fig. 5-a (bottom).

B. *The variation in surface temperature distribution of SiC-MOSFETs due to the edge length*

The variation in temperature distribution with geometry of the 10kV SiC-MOSFET was evaluated. As a comparison, three different edge widths SiC-MOSFET models with the same chip

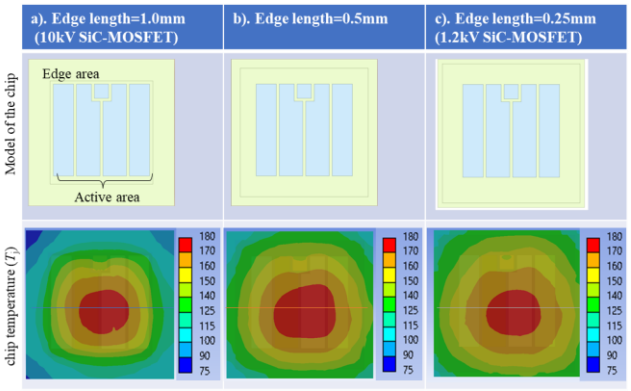


Fig. 5. Calculated surface temperature distribution of SiC-MOSFETs with different edge sizes.

a). Edge width 1 mm (10 kV SiC-MOSFET), b). Edge width 0.5 mm

c). Edge width 0.25 mm (1.2 kV SiC-MOSFET)

size (8.1×8.1 mm^2) were investigated and the temperature was calculated. In this calculation, all other module structures and operating conditions are the same. Fig. 5 a-c shows SiC-MOSFET models with edge widths of 1 mm (i.e. edge length of 10kV SiC-MOSFETs), 0.5 mm and 0.25 mm (i.e. edge length of 1.2kV SiC-MOSFETs) and the temperature calculation results. Fig. 6 shows a comparison of one-dimensional temperature profiles at the same line of Fig.5 a, b and c. The result shows that the 10kV SiC-MOSFET with

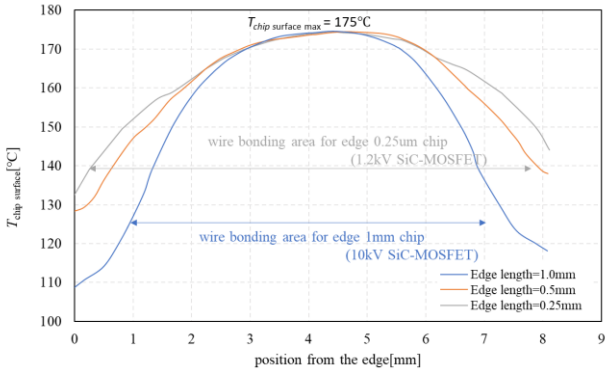


Fig. 6. Calculated temperature T_j (line profile on the chip) comparison between 10kV SiC-MOSFETs and different edge sizes.

1mm edge length has the largest temperature gradient on the chip surface ($T_{\text{chip surface}}$). These results show that the temperature gradient on the chip surface increases when the edge structure, which acts as a heat conductor, increases in relation to the active area, which is the heat-generating element. Therefore, for high-voltage devices such as 10kV SiC-MOSFETs where large edge isolation areas are used, optimising the wire bonding layout to suppress wire temperature is more effective than for low-voltage devices, due to the large surface temperature gradient across the device as will be shown below.

C. *Results of wire layout on 10kV SiC-MOSFET module to reduce the wire temperature in the digital twin*

According to the above results, 10kV SiC-MOSFETs have a comparatively large temperature gradient across the surface. Therefore, the Al wire temperature on the source pad of the chip is highly dependent on the bonding position on the chip source pads. From the module design point of view, it suggests that the wire temperature can be reduced by optimizing wire layout on source pads. In this section, the effect of wire temperature reduction was calculated when the wire layout was changed. The wire layout design of 10kV SiC-MOSFET modules is carried out in the 3D model to compare the maximum wire temperature swing ($=T_{\text{wire max}}$-T_0). Three wire layout patterns were considered, including a reference layout. Wire layouts and the temperature calculation results are shown in Fig. 7. The standard layout (Fig. 7-a) is the one in which the wires are placed in the center of source pads where wire bonding is possible. As modified wire layouts, two layouts were considered to avoid the center of source pads, which is the highest temperature on the chip surface (Fig. 7-b, c). The temperatures calculated for these three model patterns under the same power value (380W/chip) are shown in Fig. 8. The maximum chip heating $\Delta T_{\text{j max}}$ shown on the left side of Fig. 8 is almost constant regardless of the wire layout. In contrast, $\Delta T_{\text{wire max}}$ shown on the right side of Fig. 8 is smaller due to the wire layout modified. Compared to the standard layout, the improved layout reduced the maximum wire temperature swing by 2.7-8.0°C (1.9-5.5%). This is due to changing the wire bonding position on the chip to the source

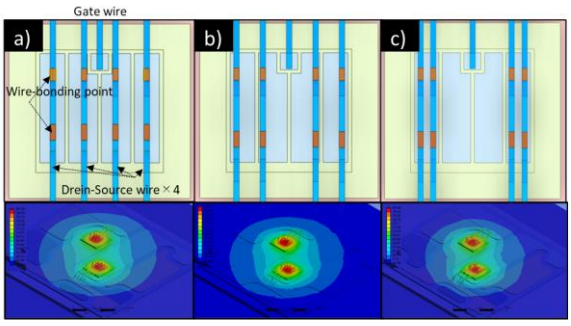
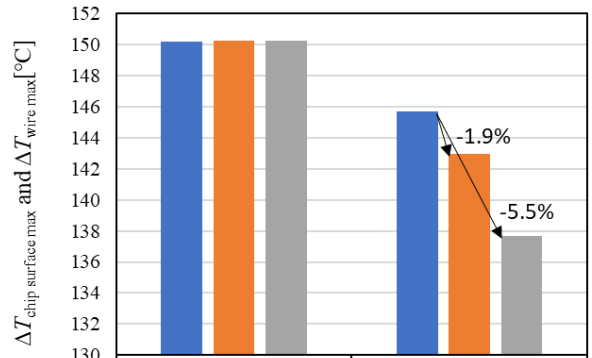


Fig. 7. SiC-MOSFET wire layout model and temperature calculation results.

a). Standard : Wire bonding position is the center of Al-source pads

b). Modified : Wire bonding located on the edge of Al-source pads

c). Further modified :Wire bonding only on Al-sorce pads at both edges.



	$\Delta T_{\text{chip surface max}}$	$\Delta T_{\text{wire max}}$
Wire layout a	150.19	145.67
Wire layout b	150.23	142.93
Wire layout c	150.25	137.65

Fig. 8. Calculate and compared results of $\Delta T_{\text{j max}}$ and $\Delta T_{\text{wire max}}$. All model were applied the same power value ($\Delta T_{\text{j max}}$=150°C).

pad end where the temperature is lower, as shown in Fig. 6.

IV. DISCUSSION

The expected power cycle capabilities improvement effect of reduced wire temperature is discussed using prediction model. The device temperature during operation and power cycle capability are described using the Coffin-Manson model [16] as follows. Here, focusing that the power cycle failure is caused by thermal expansion due to the maximum wire temperature swing ΔT_{wire} is incorporated in the Coffin-Manson model. Therefore, the relationship between the $\Delta T_{\text{wire max}}$ and power cycle capability N_{f} is described as follows :

$$N_{\text{f}} = \text{A}(\Delta T_{\text{wire max}})^{\alpha} \exp(\text{B}/T_{\text{j max}}) \quad (1)$$

N_{f} is the number of power cycles to failure, A, B and α are constants.

According to (1), the effect of the power cycle capability improvement due to the reduction of wire temperature swing is estimated. The constants A, B and α included in (1) are necessary for the calculation. Therefore, N_{f} was calculated using the various constants from the power cycle withstand capacity prediction models for power modules reported by other groups. A list of references and N_{f} calculation formulae used for this calculation is given in TABLE II below. [16-21] On the other hand, it has been reported that the respective constants required to accurately predict N_{f} depend on the device and module structure in higher detail [20], and in this case a power cycle test on a specific layout with a 10kV SiC-MOSFET is required. However, as mentioned earlier, by applying the wiring design method based on the results of the 3D thermal calculations, an improved structure of the module can be efficiently identified using the digital design approach.

TABLE II. LIFETIME MODELS AND CONSTANTS IN REFFERENCES

REF. NO.	*Target sample*	*Lifetime model equation*	*Constant Values*
16	Si-IGBT modules	$N_f = K \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{\beta_2}{T_j+273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4}$	β_1=-4.416 β_2=1.29×10^3 β_3=-0.463 β_4=-0.716
17	Si-IGBT modules	$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\frac{Q}{R \cdot T_m}}$	A=640 α=-5 Q=7.8×10^4 R=8.314
18	Si-IGBT modules	$N_f = C \times (\Delta T_{j,t})^{-\alpha} \cdot e^{\frac{E_a}{k_B \cdot T_{jm,t}}}$	C=97.2 α=-3.1 E_a=9.89×10^{-20} k_B=1.38×10^{-23}
19	Si-IGBT modules	$N_f = A \cdot (\Delta T)^{\alpha_0}$	A=1.41×10^{13} α=-4.3327
20	SiC-MOSFET TO-247	$N_f = A \cdot \Delta T^{\alpha} \cdot e^{\frac{\beta}{T_m}}$	A=1.34×10^{10} α=-2.7478 A=1.56×10^{13} α=-4.2991
21	SiC-MOSFET modules	$N_f = K' \cdot \Delta T_{vj}^{\beta_1} \cdot e^{\frac{\beta_2}{T_{vjmin}}} \cdot I_{bw}^{\beta_4}$	K'=1.31×10^{10} β_1=-3.775 β_2=1285 β_4=-0.387

Using these equations and constants in TABLE II, N_f values were calculated for each of the three wire layouts of $\Delta T_{\text{wire max}}$ and $\Delta T_{\text{j max}}$ obtained in this simulation. The results of the calculations are shown in Fig. 9. They are normalized with respect to N_f at the calculation result for the standard wire layout (Wire layout a). This means that the values on the vertical axis show the rate of change with respect to the standard.

・$\Delta T_{\text{wire max}}$=1.9% reduction : N_f=+4 ~ 9%

(Wire layout Fig. 7-a → Fig. 7-b)

・$\Delta T_{\text{wire max}}$=5.5% reduction : N_f=+16 ~ 31%

(Wire layout Fig. 7-a → Fig. 7-c)

The results show that N_f increases at a greater rate than the reduction rate of wire temperature $\Delta T_{\text{wire max}}$. This is due to the fact that, from (2), $\Delta T_{\text{wire max}}$ varies with an exponent of constant α (<2 in all references) with respect to N_f. This indicates that a slight reduction in wire temperature, has a significant impact on the power cycle capability N_f. Therefore designing a module structure that suppresses the wire temperature can effectively improve the power cycle capability without additional manufacturing complexity or cost. In this study, a design for improving power cycle was conducted based on thermal calculation. In actual product design, it is necessary to optimize the design by considering other electrical, thermal, and reliability characteristics. However, we have shown that wire layout design to minimize wire temperature for power cycle improvement can be performed on the digital twin. This method can determine the optimal structure for power cycle capability with a minimum number of physical prototypes, which previously required many actual samples and measurements, thus enabling efficient reliability design with a less cost and lead time.

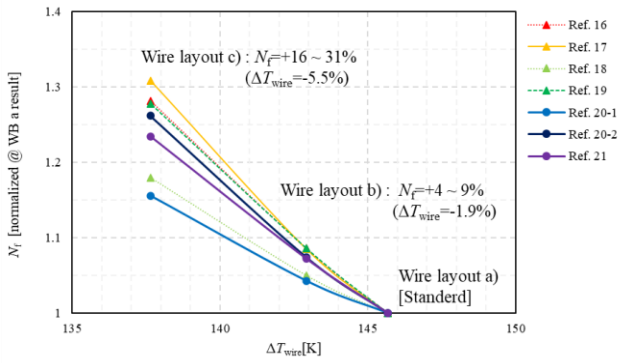


Fig. 9. Power cycle capability N_f calculation results for each wire bonding layout in Fig. 6 a-c when the same power value (380W/chip) was applied (ΔT_{wire}=144°C). The value of N_f is expressed as the percentage change in the value of WB a), normalized. Wire layout changes have reduced $\Delta T_{\text{wire max}}$ and increased N_f. Mark ▲ shows the results quoted from References. about Si-IGBTs and Mark ● shows the calculation results quoted from References about SiC-MOSFETs.

V. CONCLUSION

A digital design to improve the power cycle capability using 3D thermal calculations was demonstrated for 10kV SiC-MOSFET power modules.

First, it was confirmed that the thermal calculation results from the 3D model of the 10kV SiC-MOSFET matched well with the actual measurements.

Next, it was clarified that the spread of surface heat during energisation of 10kV SiC-MOSFETs is greater than for lower voltage devices such as 1.2kV due to the structure of the device, and the wire bonding points to the chip surface have a greater impact on the wire temperature.

An improved wire layout that avoids the hottest areas of the chip surface was proposed, and it was shown that the wire temperature swing during operation could be reduced by 1.9-5.5% compared to a standard layout.

Finally, the power cycle capability improvement due to the wire temperature reduction is estimated based on reference values, and the possibility of a larger power cycle capability improvement than the wire temperature reduction is shown. According to these results, an efficient design method for improving the power cycle using digital twin and 3D thermal simulation was proposed.

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