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Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2022.3231281

Publication date:
2023

Document Version
Accepted author manuscript, peer reviewed version

Voltage Balancing of Series Connected SiC MOSFETs with Adaptive-impedance Self-powered Gate Drivers

Rui Wang, *Student Member, IEEE*, Asger Bjørn Jørgensen, Wentao Liu, Hongbo Zhao, Zhixing Yan and Stig Munk-Nielsen, *Member, IEEE*

***Abstract*— Passive clamping snubbers for voltage balancing (VB) series connected power devices exhibit strong applicability and high robustness, moreover, they are particularly suitable for the emerging fast-switching silicon-carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs). However, the compromise still exists as a better VB performance comes at a penalty of a larger loss of snubber. Consequently, in this paper, novel adaptive-impedance "snubbers" are proposed for series connected SiC MOSFETs on the basis of converter-based self-powered gate driver design, and a better trade-off is achieved between loss and VB both in static and dynamic states. Further, the proposed passive VB strategy could be combined with an active delay control strategy by introducing an extra closed-loop controller. Benefiting from a more accurately established small-signal system model, the closed-loop numerical parameters are easier to design. As a result, well-balanced voltage distribution is realized during the continuously switching process of series connected SiC MOSFETs. To verify the effectiveness, a comprehensive analysis is firstly provided as guidance, followed by the corresponding detailed hardware and software design. Finally, the experiments are conducted by using two SiC MOSFETs, which show excellent VB performance at a 110 kV/μs switching speed.**

***Index Terms*—Series connection, SiC MOSFET, self-powered, small-signal.**

I. Introduction

For decades, silicon (Si) insulated-gate-bipolar-transistors (IGBTs) have been prevalent in medium-voltage (MV) applications due to their gradually improved performances, mature designs and standardized fabrications. However, the blocking voltage of commercial Si IGBT is limited to 6.5 kV due to the conduction loss, and its frequency is usually limited to a few kHz due to the switching loss caused by tail current, which becomes the obstacles of future high-performance MV applications. Therefore, in recent years, silicon-carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) has drawn extensive research attention due to its superior switching characteristics and becomes the most promising power device to replace the dominance of Si IGBT. However, the blocking voltage of a commercial single SiC MOSFET is still limited, maximum to 3.3 kV according to the data in [1]. As an alternative to satisfy high voltage requirement, using series connection of SiC MOSFETs is a valuable approach.

Nevertheless, there is a well-known constraint for the series connection of power devices, that is, the unbalanced voltage distribution among devices. Specifically, the dynamic voltage unbalancing, caused by inconsistencies of gate drivers (GDs), devices characteristics, etc. during the switching transients [2], is considered to be the most significant issue to solve, and thus making the corresponding dynamic voltage balancing (VB) strategy a research hotspot. In recent years, active VB strategies have been prevalent due to their good VB performances by actively adjusting the gate loop status of power device. Generally, they can be divided into four categories:

(1*) Active voltage control strategy*: by setting the same voltage trajectory as a reference to make a comparison with the collector-emitter voltage of each IGBT, the closed-loop is formed to control the gate driving process and VB can be achieved [3]-[4]. However, the VB performance is limited by the bandwidth of analog device on the GD, and it is rarely seen in series connected SiC MOSFETs.

(2) *Active clamping strategy*: by appending a clamping circuit between the power and gate sides, a current will flow into the gate loop of power device immediately after the over-voltage exceeds the clamping threshold, so that the voltage unbalancing is reduced [5], but the loss of power device is increased, and voltage unbalancing can not be avoided under lower voltage cases.

(3*) Active gate compensation strategy*: the core principle is compensating the gate charge of individual power device accurately for the VB purpose by online detecting the voltage unbalancing degree. To realize voltage unbalancing detection, one approach is using coupled inductors in resistor-capacitor (RC) snubbers to output the *dv/dt* difference [6]-[7]. Another approach is adopting analog-to-digital converters (ADCs) to sample the voltages and the digital controller to make the difference. Further, in [8], a three-level turn-off GD is designed and the turn-off gate-source voltage of SiC MOSFET can be adjusted accordingly by controlling the intermediate voltage. In [9]-[10], an extra voltage-dependent miller capacitor is added and the *dv/dt* of SiC MOSFET can get controlled accordingly. In [11]-[13], a controlled current

Manuscript received August 12, 2022; revised October 25, 2022 and December 6, 2022; accepted December 11, 2022. This work was supported in part by the Center of Digitalized Electronics (CoDE) project funded by Paul Due Jensen Foundation. *(Corresponding author: Wentao Liu.)*

Rui Wang, Asger Bjørn Jørgensen, Wentao Liu, Hongbo Zhao, Zhixing Yan and Stig Munk-Nielsen are with AAU energy, Aalborg University, Aalborg 9220, Denmark (e-mail: rwa@et.aau.dk; abj@et.aau.dk; wliu@energy.aau.dk; hzh@energy.aau.dk; zhya@energy.aau.dk; smn@et.aau.dk).

source is integrated with the conventional voltage source GD, and the current source compensation degree will determine the VB performance. Nevertheless, the system design becomes complex, and the robustness gets weakened.

(4) *Active delay control strategy*: on the basis of detecting the voltage unbalancing degree, accurately adjusting the switching signal delay by using time delay chips, etc. is another effective strategy to obtain good VB performance [14]-[17]. Since it does not impair the switching speed at all, it is considered the best strategy for series connection of SiC MOSFETs while taking full advantage of this emerging fast-switching power device. However, the utilization of closed-loop control still increases the design burden, and an accurate system model is required for parameter identification.

Comparatively, although passive VB strategies like using snubbers result in higher loss compared with the above active VB strategies, they are still widely applied in industrial applications thanks to their better reliability and robustness without any closed-loop controlling complexity [18]. Although some novel topologies and energy recycling approaches are put forward to reduce the loss of snubbers, they are still not attractive due to the complex structure, dedicated modulation and limited applicability [19]-[25]. When it comes to a general passive snubber strategy, a better VB performance still comes at a penalty of a larger loss of snubber, and thus a better trade-off of loss versus VB is being pursued. Besides, paralleling VB resistor is the common way to reduce static voltage unbalancing caused by the discrepancy of leakage currents of power devices, which could cause a large power loss in MV high-power applications [17], while few articles take into account the optimization of static VB performance.

In response to those issues, as a continuation of the previously published article where a scalable self-powered GD design was proposed for SiC MOSFET [26], this article makes two major contributions as follows:

(1) Based on the self-powered GD design, a novel adaptive-impedance "snubber" concept and its corresponding design are proposed for achieving a better trade-off between loss and VB of series connected SiC MOSFETs both in static and dynamic states.

Further, if well balanced voltage distribution performances of active VB strategies are preferred while caring less on the additional controlling complexity, a hybrid VB strategy will be a good solution.

(2) Owing to the proposed "snubber" design, the accurate small-signal model of this system can be established, and the voltage unbalancing degree can also be conveyed by signal multiplexing. Consequently, in order to obtain a well balanced voltage distribution performance, the proposed passive strategy is combined with active delay control strategy by introducing an extra closed-loop controller, where the numerical parameters are easier to design.

Next, in the following Section II of this article, the novel adaptive-impedance "snubber" concept is proposed. In Section III, the corresponding circuit design is given in detail. In Section IV, the novel "snubber" is combined with active delay control strategy, and the parameter design guideline is provided after giving the comprehensive analysis and establishing the small-signal system model. In Section V, the experimental results by using two SiC MOSFETs verify the effectiveness. Finally, the conclusion is given in Section VI.

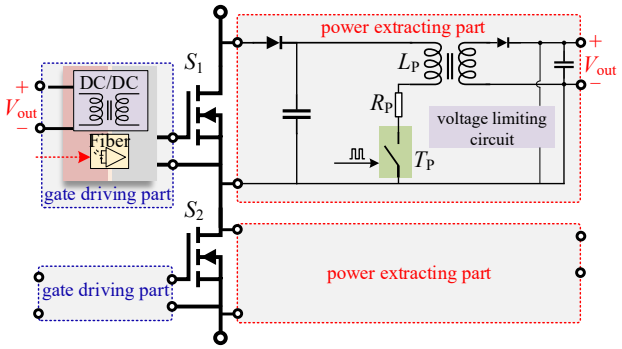

Fig. 1. Two series connected SiC MOSFETs with the individual converter-based self-powered GD

II. Proposed Adaptive-Impedance "Snubber" Concept for Better VB Performance

Analysis in this article is conducted in the case of two series connected SiC MOSFETs, where each SiC MOSFET is equipped with a scalable converter-based self-powered GD, and the schematic is depicted in Fig. 1. Similar to the conventional clamping resistor-capacitor-diode (RCD) snubber, its diode-capacitor clamping structure contributes to the feature of not influencing the switching speed of power device until the clamping voltage is reached, which is particularly suitable in the SiC MOSFET application to maintain its advantage of fast switching speed. Further, different from conventional external-powered GDs, the self-powered GDs partially recycle the energy of "snubbers" (the power extracting parts which extract and absorb the energy from the power loop) to supply the gate driving parts, which eliminates the need of external auxiliary power supply configuration. Beside this, the design burdens related to voltage isolation and common mode noise are eased drastically [26].

Owing to the converter-based design of the self-powered GD, there are more flexibilities and possibilities for obtaining a better VB performance by controlling the behavior of its power extracting part (i.e., the inside modified flyback converter), and thus making it operate as an adaptive-impedance "snubber". Next, the elaborations will be provided from the perspectives of static VB and dynamic VB, respectively.

A. Static VB

Generally, because of the leakage current discrepancy in the case of series connection, paralleling the same resistor r_S with each SiC MOSFET S_i (i = 1, 2) is a common approach for static VB purpose, as shown in Fig. 2(a). Beside this, r_S also greatly contributes to speed up the recovery of VB after an occurrence of dynamic VB. In conclusion, r_S plays an important role in VB design.

Hence, in order to calculate the appropriate value of r_S, the leakage current $i_{DSS(i)}$ of S_i during the static state is defined and $i_{DSS(2)}$ is assumed to be much larger than $i_{DSS(1)}$ in the worst case (i. e., $i_{DSS(1)} = 0$ and $i_{DSS(2)} = I_{DSS(max)}$, where $I_{DSS(max)}$ is the

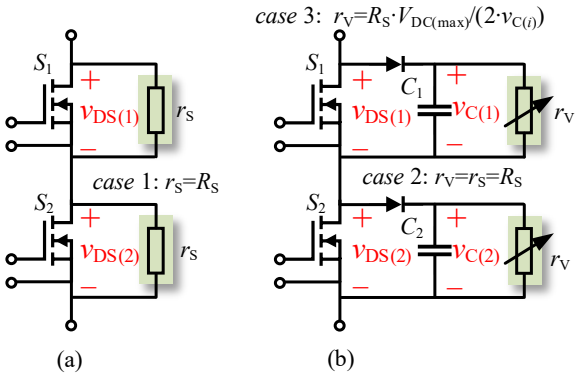

Fig. 2. Static VB (a) by paralleling resistors (b) by the proposed design

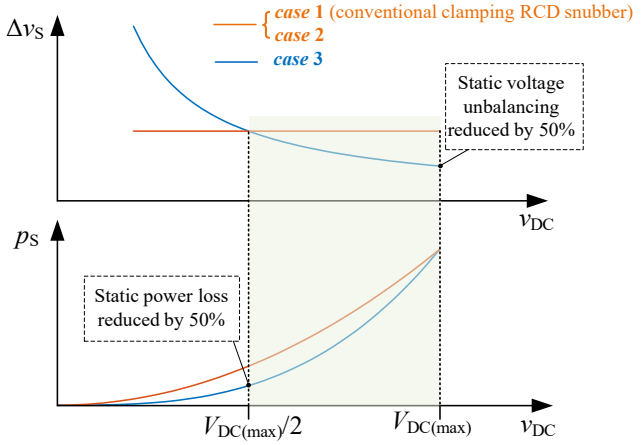

Fig. 3. Δv_S and p_S versus v_{DC} in *case* 1, *case* 2 and *case* 3

maximum leakage current of S_i at an extremely atrocious condition). Then following relationship exists:

$$\begin{cases} v_{DS(1)}/r_S - v_{DS(2)}/r_S = I_{DSS(max)} \\ v_{DS(1)} + v_{DS(2)} = v_{DC} \end{cases} \tag{1}$$

where $v_{DS(i)}$ (i = 1, 2) is the drain-source voltage of S_i and v_{DC} is the total blocking voltage.

Further, defining $\Delta v_S = v_{DS(1)} - v_{DS(2)}$ as the static voltage unbalancing degree and p_S as the static power loss in this situation, it is solved that:

$$\begin{cases} \Delta v_S = r_S \cdot I_{DSS(max)} \\ p_S = \dfrac{v_{DS(1)}^2}{r_S} + \dfrac{v_{DS(2)}^2}{r_S} = \dfrac{1}{2\cdot r_S}\cdot(v_{DC}^2 + \Delta v_S^2) \end{cases} \tag{2}$$

As $I_{DSS(max)}$ gets increased with multiple power device dies being in parallel to advance the current rating and power device aging at extreme operating conditions, if a smaller Δv_S is expected, r_S should be chosen smaller according to (2), whereas induced p_S will become larger. In consequence, there is a compromise between Δv_S and p_S.

Owing to the passive characteristic of resistor, once r_S is selected as R_S, no optimization measures could be taken to perform a better trade-off since R_S is a fixed value, which is also the bottleneck of the static VB strategy. In contrast, in this paper, r_S is substituted with a converter-based circuit as depicted in Fig. 1 (i.e., the power extracting part). By regulating the converter behavior in a specifical way, the possibility of breaking through the bottleneck appears as it could be represented by an adaptive resistor r_V to achieve a better trade-off between Δv_S and p_S, as shown in Fig. 2(b), and the analysis is given as follows.

During the static state, both S_1 and S_2 are in the constantly off state, in the meanwhile, the switch T_P is continuously switching to enable the power extracting part, so as to provide the required input power of the following gate driving part. The basic topology inside is a flyback converter, and the discontinuous conduction mode (DCM) is its working mode. Since the conveyed power is small and the efficiency is not much concerned, a resistor R_P is inserted into the primary side as a modification to damp the voltage/current oscillation during the switching transient and alleviate the noise issue. When T_P is turned on, the primary state is equivalent to the zero-state response of a RL circuit, and the primary current $i_{P(i)}$ (i = 1, 2) can be solved as:

$$i_{P(i)} = \frac{v_{C(i)}}{R_P}\cdot(1-e^{-\frac{t}{L_P/R_P}}) = \frac{v_{DS(i)}}{R_P}\cdot(1-e^{-\frac{t}{L_P/R_P}}) \tag{3}$$

where L_P is the inductance of the primary side, and the voltage $v_{C(i)}$ (i = 1, 2) across the clamping capacitor C_i is equal to $v_{DS(i)}$ in the static state.

When T_P is turned off after a constant on-time duration T_{on}, $i_{P(i)}$ decreases to zero rapidly and the stored power of the primary side is transferred to the secondary side. The secondary voltage limiting circuit and the following gate driving part will consume the transferred power so that the energy stored in this "snubber" will not get accumulated [26]. Therefore, by integrating $v_{C(i)}\cdot i_{P(i)}$ over time and combining it with (3), the extracting power $p_{(i)}$ (i = 1, 2) from power loop can be obtained as:

$$p_{(i)} = \frac{f_{(i)}\cdot\Delta t_{on}\cdot v_{DS(i)}^2}{R_P} - \frac{f_{(i)}\cdot L_P\cdot v_{DS(i)}^2}{R_P^2} + \frac{f_{(i)}\cdot L_P\cdot v_{DS(i)}^2}{R_P^2}e^{-\frac{\Delta T_{on}}{L_P/R_P}} \tag{4}$$

where $f_{(i)}$ (i = 1, 2) is the switching frequency of the modified flyback converter.

Similar to the conventional approach of paralleling resistors as described above, $p_{(1)}+p_{(2)}$ is also the static power loss p_S as defined above, which plays a dominant role in static VB process. Therefore, based on Fig. 2(b), the following equations can be obtained:

$$\begin{cases} p_{(1)}/v_{DS(1)} - p_{(2)}/v_{DS(2)} = I_{DSS(max)} \\ v_{DS(1)} + v_{DS(2)} = v_{DC} \end{cases} \tag{5}$$

If $f_{(i)}$ (i = 1, 2) is a fixed value as F_P, by combining (4) and (5), it can be solved that:

$$\begin{cases} \Delta v_S = K_1\cdot I_{DSS(max)} \\ p_S = \dfrac{1}{2\cdot K_1}\cdot(v_{DC}^2 + \Delta v_S^2) \end{cases}, \quad K_1 = \frac{R_P}{F_P\cdot[T_{on} - \frac{L_P}{R_P}\cdot(1-e^{-\frac{T_{on}}{L_P/R_P}})]} \tag{6}$$

where K_1 is a constant since all the parameters are predefined as fixed values in the design.

By contrast, if $f_{(i)}$ (i = 1, 2) is a not fixed value, for example $f_{(i)}=\alpha\cdot v_{C(i)}$, ($\alpha$ is a constant), by combining (4) and (5), it is solved that:

$$\begin{cases} \Delta v_S = \dfrac{K_2}{v_{DC}}\cdot I_{DSS(max)} \\ p_S = \dfrac{1}{4\cdot K_2}\cdot(v_{DC}^3 + 3\cdot v_{DC}\cdot\Delta v_S^2) \end{cases}, \quad K_2 = \frac{R_P}{\alpha\cdot[T_{on} - \frac{L_P}{R_P}\cdot(1-e^{-\frac{T_{on}}{L_P/R_P}})]} \tag{7}$$

where K_2 is also a constant value.

To facilitate the comparison, in this paper, an effective bond is established between (2), (6) and (7) (respectively defined as *case* 1, *case* 2 and *case* 3): when v_{DC} reaches the designed maximum blocking voltage $V_{DC(max)}$, the static power losses in these three cases are designed to be equal. By formula, it can be expressed as:

$$\begin{cases} K_1=R_S \\ K_1=2\cdot K_2 / V_{DC(max)} \end{cases} \tag{8}$$

Then (2), (6) and (7) can be unified as:

$$\begin{cases} \Delta v_S = R_S \cdot I_{DSS(max)} \\ p_S \approx \dfrac{v_{DC}^{\ 2}}{2\cdot R_S} \end{cases}, \quad case\ 1$$

$$\begin{cases} \Delta v_S = R_S \cdot I_{DSS(max)} \\ p_S \approx \dfrac{v_{DC}^{\ 2}}{2\cdot K_1} = \dfrac{v_{DC}^{\ 2}}{2\cdot R_S} \end{cases}, \quad case\ 2 \tag{9}$$

$$\begin{cases} \Delta v_S = \dfrac{R_S \cdot V_{DC(max)}}{2\cdot v_{DC}} \cdot I_{DSS(max)} \\ p_S \approx \dfrac{v_{DC}^{\ 3}}{4\cdot K_2} = \dfrac{v_{DC}^{\ 3}}{2\cdot R_S \cdot V_{DC(max)}} \end{cases}, \quad case\ 3$$

To analyze (9), the corresponding functional relation graphs of three cases are drawn, as shown in Fig. 3.

According to Fig. 3, *case* 1 is referring to the conventional clamping RCD snubber, whose working principle is the same as paralleling resistors in the static state. It is seen that the curves in *case 1* and *case* 2 are coincident, which proves that the converter could be controlled to behave as a resistor in the common static VB approach (i.e., r_V in Fig. 2(b) is equal to r_S (R_S) in *case* 2). More importantly, by comparing *case 2* and *case 3*, it is found that both Δv_S and p_S in *case* 3 are smaller than those in *case* 2 in the v_{DC} range from $V_{DC(max)}/2$ to $V_{DC(max)}$. It indicates that a better trade-off could be achieved by regulating the converter behavior as an adaptive-impedance "snubber" (i.e. r_V is equal to $R_S\cdot V_{DC(max)}/(2\cdot v_{DS(i)})$ in *case* 3). Although Δv_S in *case* 3 is larger than that in *case* 2 in the v_{DC} range from 0 to $V_{DC(max)}/2$, the determinate startup voltage could be set as $V_{DC(max)}/2$ to skip the unexpected operation points since the startup voltage of converter is always required for providing enough gate driving power during the startup of this self-powered GD. Specifically, when $v_{DC} = V_{DC(max)}/2$, the static power loss is reduced by 50% comparing *case* 3 with *case* 2; when $v_{DC} = V_{DC(max)}$, the static voltage unbalancing is reduced by 50% comparing *case* 3 with *case* 2.

With the same manner, $f_{(i)}$ (i = 1, 2) could be further set as: $f_{(i)} = \beta\cdot v_{DS(i)}^2$, or $f_{(i)} = \gamma\cdot v_{DS(i)}^3$ (β, γ are constants) and an even better trade-off between Δv_S and P_S could be obtained. However, the suitable v_{DC} range becomes much narrower, which is not practical in real applications. Consequently, this paper focuses on the conditions of fixed $f_{(i)}$ and $f_{(i)}=\alpha\cdot v_{DS(i)}$ (i.e., *case* 2 and *case* 3).

B. Dynamic VB

In addition to the benefit to static VB, the converter-based power extracting part also contributes to dynamic VB because of its voltage clamping characteristic. In *case* 2, the converter is controlled to behave as a pure resistor, and thus the power

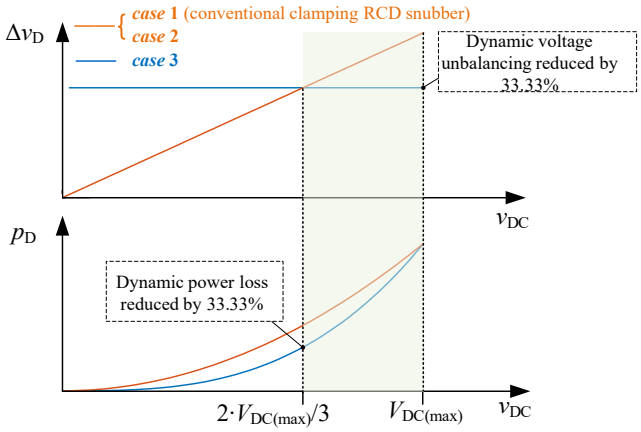

Fig. 4. Δv_D and p_D versus v_{DC} in *case* 1, *case* 2 and *case* 3

extracting part behaves the same as a conventional "clamping RCD snubber" circuit. In the stable state when S_1 and S_2 are continuously switching, $v_{C(1)}$ also as the clamping voltage value will be higher than $v_{C(2)}$ if the power extracting part for S_1 accumulates more energy than that for S_2 due to the inconsistencies of GDs, devices characteristics, etc., and vice versa ($i_{DSS(1)} = i_{DSS(2)}$ is assumed here, i.e. the influence of static voltage unbalancing is neglected). Since case 1 and case 2 are the same, only case 2 and case 3 are analyzed in this part. By defining the more accumulated energy during one switching cycle as $\Delta E_{(case i)}$ (i=2, 3) in both cases, following relationships exist as:

$$\begin{cases} \dfrac{v_{C(1)}^{\ 2}}{R_S} - \dfrac{v_{C(2)}^{\ 2}}{R_S} = \dfrac{v_{C(1)}^{\ 2}}{K_1} - \dfrac{v_{C(2)}^{\ 2}}{K_1} = f_s \Delta E_{(case2)} \\ v_{C(1)} - v_{C(2)} = \Delta v_D \end{cases}, \quad case\ 1\ \&\ case\ 2 \tag{10}$$

$$\begin{cases} \dfrac{v_{C(1)}^{\ 3}}{K_2} - \dfrac{v_{C(2)}^{\ 3}}{K_2} = f_s \Delta E_{(case3)} \\ v_{C(1)} - v_{C(2)} = \Delta v_D \end{cases}, \quad case\ 3\cdot \tag{11}$$

where f_s is the switching frequency of S_1 and S_2, and Δv_D is defined as the voltage unbalancing degree of $v_{C(i)}$ (i = 1, 2), which also indicates the dynamic voltage unbalancing degree of S_1 and S_2.

To facilitate the calculation, Δv_D is considered to be much smaller than v_{DC}, $v_{C(1)} + v_{C(2)} \approx v_{DC}$ and $\Delta E_{(case2)} \approx \Delta E_{(case3)} = K_e\cdot v_{DC}^2$, where K_e is a coefficient that relates energy to voltage. Further, f_s is a fixed value as F_s, and the dynamic power loss is defined as p_D. Combining (8), (10) and (11), it is solved that:

$$\begin{cases} \Delta v_D = \dfrac{K_1 \cdot F_s \cdot \Delta E_d}{v_{DC}} = K_e \cdot R_S \cdot F_s \cdot v_{DC} \\ p_D \approx \dfrac{v_{DC}^{\ 2}}{2\cdot K_1} = \dfrac{v_{DC}^{\ 2}}{2\cdot R_S} \end{cases}, \quad case\ 1\ \&\ case\ 2$$

$$\begin{cases} \Delta v_D \approx \dfrac{4\cdot K_2 \cdot F_s \cdot \Delta E_d}{3\cdot v_{DC}^{\ 2}} = \dfrac{2\cdot K_e \cdot V_{DC(max)} \cdot R_S \cdot F_s}{3} \\ p_D \approx \dfrac{v_{DC}^{\ 3}}{4\cdot K_2} = \dfrac{v_{DC}^{\ 3}}{2\cdot R_S \cdot V_{DC(max)}} \end{cases}, \quad case\ 3 \tag{12}$$

Similarly, the corresponding functional relation graphs are drawn in Fig. 4 to give an analysis.

According to Fig. 4, in addition to the consistent *case 1* and *case* 2, it is found that a better trade-off of Δv_D and P_D is achieved in *case* 3 with the adaptive-impedance "snubber" than that in *case* 2 with the linear impedance "snubber", in the v_{DC} range from $2 \cdot V_{DC(max)}/3$ to $V_{DC(max)}$. In *case* 3 compared with *case* 2, when $v_{DC} = 2 \cdot V_{DC(max)}/3$, the dynamic power loss is reduced by 33.3%; when $v_{DC} = V_{DC(max)}$, the dynamic voltage unbalancing is reduced by 33.3%.

III. Detailed Design of Adaptive-Impedance Self-Powered GD

Based on the above, hardware is designed according to the adaptive-impedance "snubber" (*case 3*) to achieve a better tradeoff between loss and VB, and the detailed circuitry of the key power extracting part is shown in Fig. 5. As described, the main topology is an open-loop modified flyback converter. The current rating requirement of T_P is low since the conveyed power is small, and the voltage limiting circuit works to regulate the output voltage V_{out} within the nominal input voltage range of the following gate driving part. For controlling the switching of T_P, resistors R_{X1}~R_{X3}, a capacitor C_X, a diode D_X and a Schmitt trigger U_X are adopted to form a voltage-dependent pulse generator, and its working principle is described as follows:

Once the voltage v_{CX} across C_X rises to the positive threshold voltage V_{th}^+ of U_X, the output pulse voltage is in "low" level; once v_{CX} across C_X falls to the negative threshold voltage V_{th}^- of U_X, the output pulse voltage is in "high" level. Therefore, t_{off} is the time interval of v_{CX} rising from V_{th}^- to V_{th}^+, and t_{on} is the time interval of v_{CX} falling from V_{th}^+ to V_{th}^-. From the schematic, when the output pulse voltage is in "high" level, v_{CX} is below V_{th}^+, and D_X is reversely blocking. $v_{C(i)}$ (i=1, 2) is scaled down by k with the resistor divider, and the rising of v_{CX} is caused by the charging from $k \cdot v_{C(i)}$ through R_{X1}, which could be depicted as shown in Fig. 6(a). Therefore, this process is equivalent to the complete response of a RC circuit, and t_{off} could be solved as:

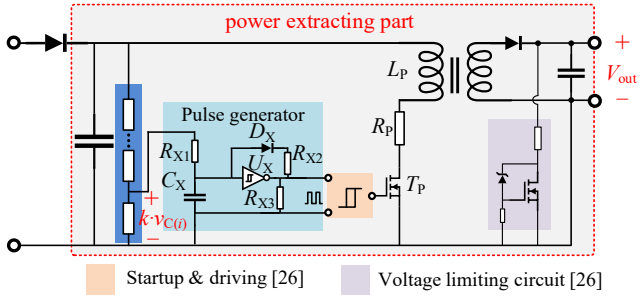

Fig. 5. Detailed design of the power extracting part

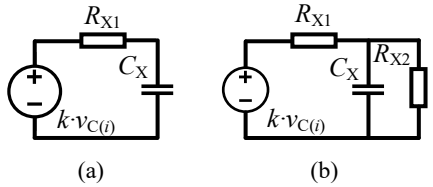

Fig. 6. Equivalent circuit of the pulse generator during (a) OFF period, (b) ON period

$$t_{off} = R_{X1} \cdot C_X \cdot \ln\left(1 - \frac{V_{th}^+ - V_{th}^-}{V_{th}^+ - k \cdot v_{C(i)}}\right) \tag{13}$$

When the output pulse voltage is in "low" level, v_{CX} is above V_{th}^+, and D_X is forward conducting. The falling of v_{CX} is caused by the discharging of C_X through R_{X2}, in the meantime, it is influenced by the charging from $k \cdot v_{C(i)}$ through R_{X1}. The state of the circuit could be described as shown in Fig. 6(b), and the following relationship exists:

$$k \cdot v_{C(i)} = R_{X1} \cdot (C_X \cdot dv_{CX}/dt + v_{CX}/R_{X2}) + v_{CX} \tag{14}$$

Considering v_{CX} is a variate which decreases from V_{th}^+ to V_{th}^- while $v_{C(i)}$ (i=1, 2) is relatively constant, t_{on} could be solved from (14) as:

$$t_{on} = \frac{R_{X1} \cdot R_{X2} \cdot C_X}{R_{X1} + R_{X2}} \cdot \ln\left\{1 + (V_{th}^+ - V_{th}^-)/\left(V_{th}^- - \frac{k \cdot v_{C(i)} \cdot R_{X2}}{R_{X1} + R_{X2}}\right)\right\} \tag{15}$$

Since $k \cdot v_{C(i)}$ is much larger than V_{th}^+ and V_{th}^-, it is further simplified from (13) as:

$$t_{off} \approx R_{X1} \cdot C_X \cdot \frac{V_{th}^+ - V_{th}^-}{k \cdot v_{C(i)}} \tag{16}$$

Similarly, since R_{X1} is set to be much larger than R_{X2}, and $V_{th}^-/R_{X2} >> k \cdot v_{C(i)}/(R_{X1}+R_{X2})$, t_{on} is solved from (15) to be a fixed value T_{on} as:

$$t_{on} \approx R_{X2} \cdot C_X \cdot \frac{V_{th}^+ - V_{th}^-}{V_{th}^-} = T_{on} \tag{17}$$

From (16) and (17), since t_{off} is much larger than t_{on}, the frequency of the output pulse voltage is approximately proportional to $v_{C(i)}$. In summary, the pulse generator is built in a simple way to satisfy the conditions in *case 3*: (1) $f_{(i)} = \alpha \cdot v_{C(i)}$; (2) fixed T_{on}. As for other parts such as the voltage limiting circuit in Fig. 5, their detailed descriptions have already been provided in [26]. Since this adaptive-impedance self-powered GD does not involve any closed-loop control, its optimized passive "snubber" characteristic makes it attractive if a less control complexity is expected in series connection.

IV. Potential Risk and Implementation

It is worth noting that, the proposed adaptive-impedance "snubber" could also be realized separately and further simplified if the GD has been reliably designed and does not need to extract power from the "snubber". Instead, once it is combined with the "self-powered design" as elaborated above, the potential safety issue of the driven device comes as it could experience the uncertainty of the GD output when $v_{C(i)}$ (i=1, 2) is too low to maintain the normal running. This issue also exists in some other self-powered applications, such as the internal auxiliary power supplies of submodules in the modular multilevel converter (MMC) [27]. As for the potential dip of DC bus voltage when the system is running, two approaches can be adopted to ensure the safety: (1) from the power side, $v_{C(i)}$ can be sampled by the controller, and once the tolerable lowest voltage threshold is reached, the controller will force the output PWM to be "low"; (2) from the gate driver side, the under-voltage detection function can be integrated into the gate driver part, once its input voltage (v_{out}) is below the threshold, an "error" signal will be sent to the controller and the output PWM is forced to be "low" immediately. Another issue exists during the system startup

process when v_{DC} is gradually increasing to the working voltage from zero. Before $v_{C(i)}$ reaches the startup voltage threshold, the input impedance of this proposed "snubber" is determined by the resistor divider as depicted in Fig. 5, and it is a large value. Only after the power extracting part is activated, the input impedance is changed to the designed smaller value. However, due to the parameter discrepancy, the startup out-of-sync of all the power extracting part could cause a temporary oscillation of $v_{C(i)}$. Therefore, the oscillation should be evaluated within the safe range. Since this paper focuses on VB during the normal working process, the comprehensive analysis of the startup process is outside the scope. In addition to the above two safety issues, a limitation of the self-powered GD design remains. Since the self-powered GD extracts the energy during the off state of SiC MOSFET, it can not be applied in the case where SiC MOSFET is constantly on for a long period.

Additionally, for the proposed design, it is worth considering the power rating of the power extracting part and the gate driving part. Generally, the power required by the gate driving part is only a few watts, while even with the adaptive-impedance optimization, the power extracting part as "snubber" should extract tens of watts to realize VB under a severe natural voltage unbalancing case (described in detail in Section VI), and the excess power is inevitably dissipated in R_P and the voltage limiting circuit in Fig. 5. Therefore, if a better dynamic VB performance with low loss of the active VB strategy is preferred while caring less about the additional controlling complexity, this proposed passive strategy can be further combined with active delay control strategy as illustrated in the following section.

V. Hybrid VB Strategy and Analysis

In fact, the output pulse of the above pulse generator carries the information of $v_{C(i)}$ (i = 1, 2) by frequency, therefore, it can not only be used to switch the modified flyback converter but can also convey $v_{C(i)}$ to an external controller through a fiber. In this manner, a hybrid VB strategy is proposed: based on the proposed adaptive-impedance "snubber" design, the added controller can calculate the voltage unbalancing degree of series connected SiC MOSFETs according to fiber feedbacks, and then online control the switching signal delay to achieve the dynamic VB [28].

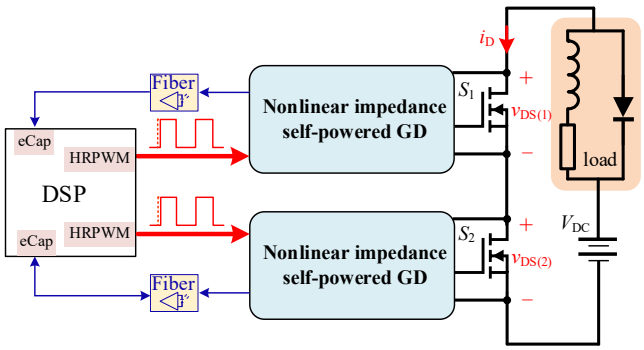

Fig. 7. Structure of the proposed hybrid VB strategy

As shown in Fig. 7, in this article, digital signal processor (DSP) is applied as the external controller. Its inside eCAP module is used to detect the input frequency, and $v_{C(i)}$ can be identified. Beside this, the time resolution of its inside HRPWM module can reach 150 ps, which is sufficient as a high-precision delay executor to adjust the dynamic VB in series connected SiC MOSFETs. Consequently, a closed-loop compensation is formed. To make it clear, the detailed system flowchart is presented in Fig. 8. In the $k_{(th)}$ switching cycle, $v_{C(1)}$ ($v_{C(2)}$) is converted into frequency $f_{(1)}$ ($f_{(2)}$), then it is captured when the PWM interrupt arrives and a calculation algorithm in the DSP is applied to generate a compensation delay Δt' for the next switching cycle. Hence, with a dynamic balance between charging and discharging of the clamping capacitor in the self-powered GD, $v_{C(1)}$ and $v_{C(2)}$ are nearly the same eventually, and $v_{DS(1)}$ and $v_{DS(2)}$ are well balanced.

In the key calculation part, proportional-integral (PI) control is applied as the algorithm in DSP, and how to properly choose the K_p and K_i parameters remains. Instead of using a method of trial and error, establishing the small-signal model of the whole closed-loop system is a more effective way to help choose parameters while maintaining the system stability. Therefore, the separate blocks presented in Fig. 8 should be modeled accordingly.

Among published literatures as [14], since $v_{DS(1)}$ and $v_{DS(2)}$ are generally considered as the judgements, the relationship between the derived delay and voltage unbalancing degree of series connected SiC MOSFETs is attained by an experimental method, which limits the design flexibility. Instead, thanks to the proposed passive "snubber" in this design, $v_{C(1)}$ ($v_{C(2)}$) is sampled as the control feedback, and the relationship between

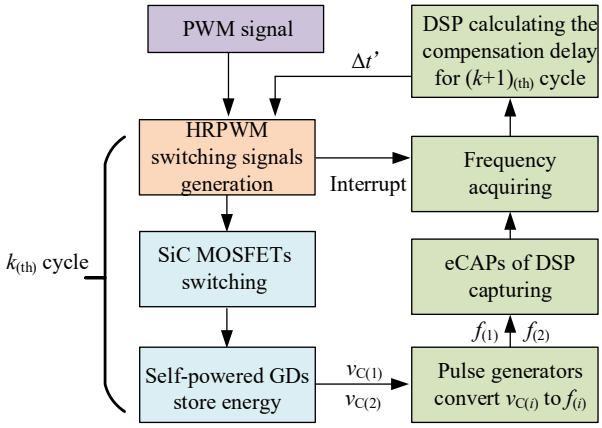

Fig. 8. The detailed system flowchart of the proposed hybrid VB strategy

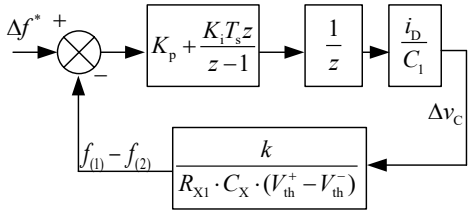

Fig. 9. The control block diagram of the proposed hybrid VB strategy

Δt' and the difference Δv_C of $v_{C(1)}$ and $v_{C(2)}$ is obtained as:

$$\Delta t' = \frac{C_1 \cdot (v_{C(1)} - v_{C(2)})}{i_D} = \frac{C_1 \cdot \Delta v_C}{i_D} \tag{18}$$

where i_D is the power loop current, and C_1 is equal to C_2.

In addition, the relationship between $f_{(1)}$ ($f_{(2)}$) and $v_{C(1)}$ ($v_{C(2)}$) can be solved from (16) and (17) as:

$$f_{(i)} \approx \frac{k \cdot v_{C(i)}}{R_X \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}, \qquad i=1, 2 \tag{19}$$

Since the closed-loop system is a discrete system, by defining the sample period as T_s and based on (18) and (19), the control block diagram can be drawn as in Fig. 9, and the closed-loop z-transfer function can be solved as:

$$G(z) = \frac{\frac{k \cdot i_D \cdot (K_p + K_i \cdot T_s)}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)} \cdot z - \frac{k \cdot i_D \cdot K_p}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}}{z^2 + (\frac{k \cdot i_D \cdot (K_p + K_i \cdot T_s)}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)} - 1) \cdot z - \frac{k \cdot i_D \cdot K_p}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}} \tag{20}$$

According to Routh–Hurwitz stability criterion, the stability conditions can be obtained as:

$$\begin{cases} \dfrac{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}{k \cdot i_D} > K_p > -\dfrac{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}{k \cdot i_D} \\ \dfrac{2 \cdot C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-) - 2 \cdot k \cdot i_D \cdot K_p}{k \cdot i_D \cdot T_s} > K_i > 0 \end{cases} \tag{21}$$

Consequently, K_p and K_i can be chosen properly.

VI. Experimental Verification

After the above analysis, the hardware is built in this section. As the pivotal part presented in the top right of Fig. 10, the adaptive impedance self-powered GD, which consists of gate driving part and power extracting part, is attached to the individual SiC MOSFET as a modular unit, and the parameters are listed in Table I. To assure the high voltage withstanding capability, a printed circuit board (PCB) transformer is designed in the power extracting part, as shown in the top left of Fig. 10. The copper trace is on the middle two layers of a four-layer FR4 PCB, which is adopted as the winding board. In this manner, the primary winding board and the secondary winding board are interleaved with three empty PCB boards, and thus the insulation requirement is satisfied. Further, based on the buck chopper circuit depicted in Fig. 7, the experimental platform is established as shown in the bottom of Fig. 10, and the experiments are conducted by using two 3.3kV/24A SiC MOSFETs (G2R120MT33J) to verify the effectiveness.

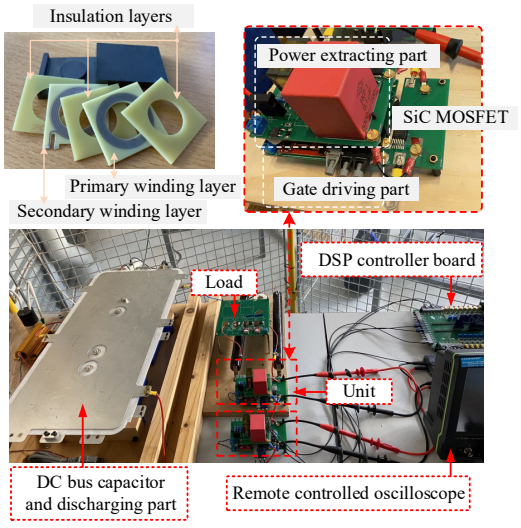

Fig. 10. Photograph of experimental platform with the modular unit

TABLE I
KEY PARAMETERS OF THE HARDWARE DESIGN

Name	Parameter
$C_1(C_2)$, C_X, R_X, k	100 nF, 680 pF, 5 MΩ, 0.1

A. Static VB performance

Firstly, the performance of the pulse generator is investigated to identify the relationship between $v_{C(i)}$ and $f_{(i)}$ (i = 1, 2) in (19). As given in Fig. 11(a), as $v_{C(i)}$ is increasing from 1 kV to 2 kV, T_{on} is kept 250 ns and $f_{(i)}$ is increased from 26.6 kHz to 47.0 kHz linearly, which proves the effectiveness of the pulse generator as analyzed. Hence, according to (4), the calculated r_V value curve versus $v_{C(i)}$ (i=1, 2) can be obtained as well, which performs the adaptive-impedance feature of the proposed self-powered GD. In this prototype, the expected operating range of GD is also 1 kV to 2 kV, and the calculated power loss curve of "snubber" versus $v_{C(i)}$ is depicted in Fig. 11(b). Also, the output power curve from power extracting part to gate driving unit versus $v_{C(i)}$ is included. Wherein a large power loss is for the VB purpose, and the low-efficiency is determined by the low input power requirement of the gate driving unit.

By changing the input connection of pulse generator in Fig. 5 to a fixed DC voltage source, the output will be a pulse with a fixed frequency and a fixed on time. In this manner, the self-

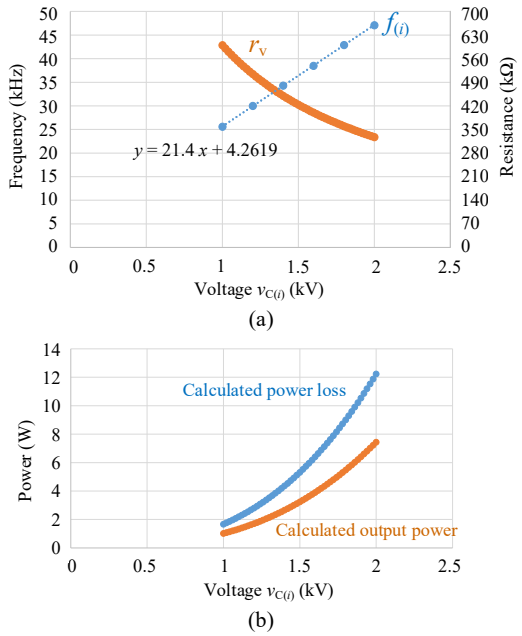

Fig. 11. (a) Relationship between $f_{(i)}$ (r_V) and $v_{C(i)}$, (b) calculated power loss and output power versus $v_{C(i)}$

This article has been accepted for publication in IEEE Transactions on Industrial Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TIE.2022.3231281

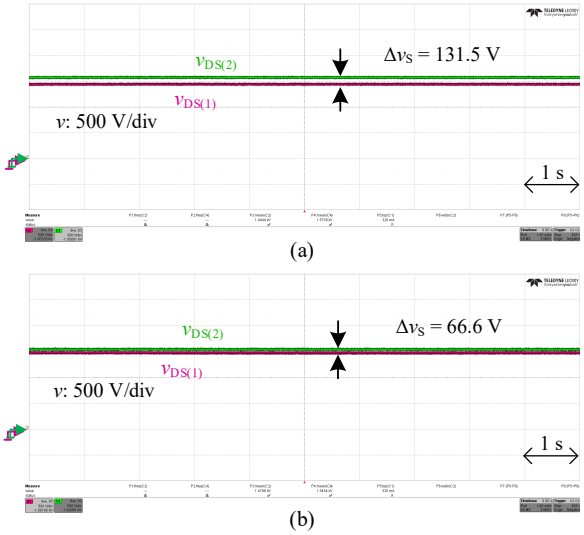

Fig. 12. Static VB performance with (a) conventional snubber (*case 1* & *case 2*), (b) adaptive-impedance "snubber" (*case 3*)

powered GD is working in the linear impedance mode (*case 2*) for static VB, which is equivalent to the conventional VB resistor strategy (*case 1*). In order to make the experimental comparison clear, an additional resistor branch is in parallel with S_1 to emulate the large discrepancy of leakage currents of S_1 and S_2. Considering the safety margin, $V_{DC(max)}$ is set as 3 kV, and then the frequency in *case 2* is set as 36.4 kHz to match with Fig. 11(a). Based on that, its static VB performance is shown in Fig. 12(a), and it is seen that the voltage unbalancing Δv_S is 131.5 V when V_{DC} is 3 kV. The calculated static power losses of S_1 and S_2 are 4.76 W and 6.12 W respectively, and their sum P_S in *case 2* is 10.88 W.

In contrast, with the adaptive-impedance self-powered GD (*case 3*), the static VB performance of series connection is shown in Fig. 12 (b). It is observed that Δv_S is reduced to 66.6V when V_{DC} is 3 kV. Both in *case 2 (case 1)* and *case 3*, the switching frequency of the flyback converter in the self-powered GD is nearly 36.4 kHz. Specifically, the calculated static power losses of S_1 and S_2 are 5.10 W and 5.79 W respectively, and thus P_S in *case 3* is 10.89 W. Therefore, P_S is nearly the same in both cases. In the meantime, Δv_S in *case 3* is reduced by 49.4% than that in *case 2* (*case 1*), which is considered consistent with the analyzed 50% in Section II. Correspondingly, when V_{DC} is the half of 3 kV, the loss P_S in *case 3* is 50% of that in *case 2* (*case 1*), while Δv_S is nearly the same. In conclusion, the proposed adaptive-impedance self-powered GD shows a better tradeoff between loss versus VB in static states.

B. Dynamic VB performance without closed-loop control

When S_1 and S_2 are continuously switching, the snubber circuits can help to reduce the dynamic VB caused by the mismatch of GDs, device characteristics, etc. Keeping the same parameter setting of GDs as the above, in *case 2* (*case 1*) as shown in Fig. 13(a), the conventional linear impedance mode of the "snubber" can reduce the voltage unbalancing Δv_D to 286.6V as measured under the specific condition: V_{DC}

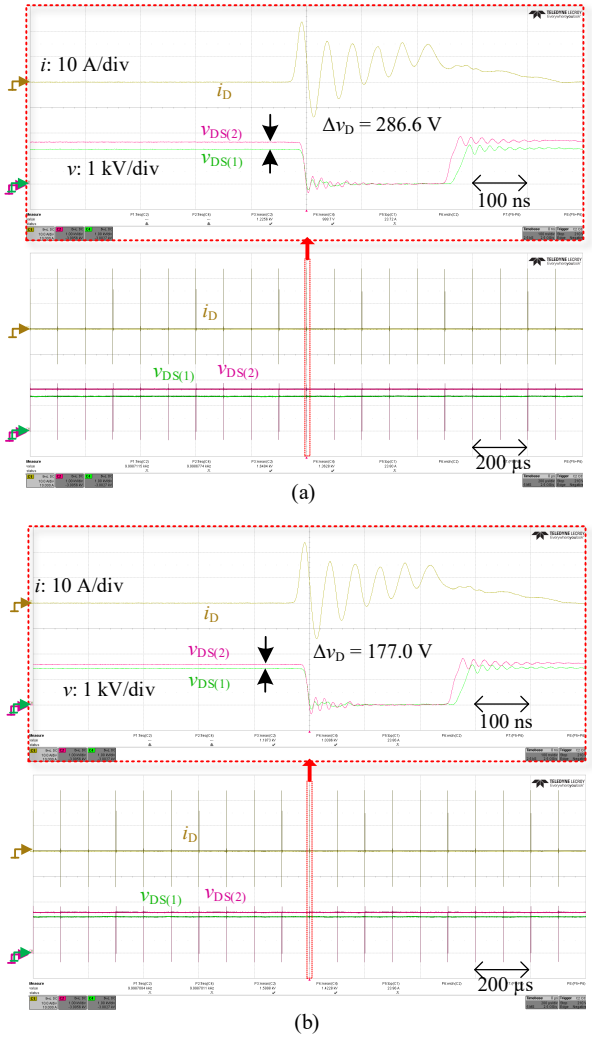

Fig. 13. Dynamic VB performance with (a) conventional snubber (*case 1* & *case 2*), (b) adaptive-impedance "snubber" (*case 3*)

= 3 kV, f_s = 10 kHz, i_D = 15 A. By contrast, in *case 3* as shown in Fig. 13(b), the proposed adaptive-impedance self-powered GD can reduce Δv_D to 177.0 V. Therefore, Δv_D in *case 3* is reduced by 38.2% of that in *case 2* (*case 1*) when V_{DC} is 3 kV, while the loss P_D is nearly the same as the calculated results in *case 2* and *case 3* are 11.02 W and 10.96 W respectively. It is a little larger than the analyzed 33.3% in Section II since some approximations are made in the theoretical analysis, and it also proves that a better tradeoff between loss versus VB is achieved in dynamic states. In the meantime, it manifests that, even with the optimization of the proposed adaptive-impedance "snubber", nearly 11 W power loss is required for reducing voltage unbalancing to 177 V in this prototype. If under the worse case that inconsistencies of GDs, devices characteristics, etc. are larger, the required power loss for VB could reach tens of watts or even higher, and that is the price that passive VB strategies need to take for less complexity and better robustness.

C. Dynamic VB performance of the hybrid VB strategy and its stability verification

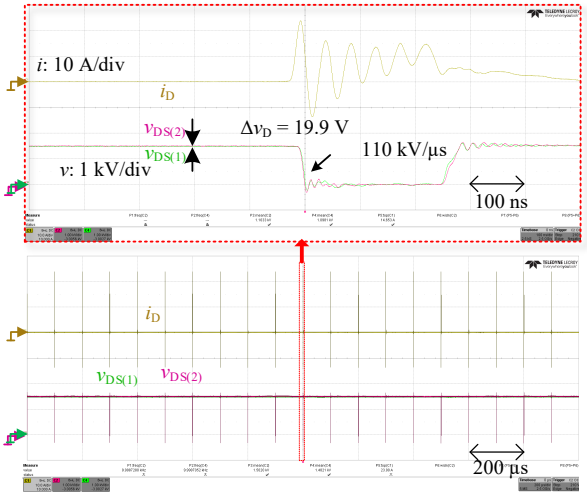

Fig. 14. Dynamic VB performance with hybrid VB strategy

Further, if a well balanced voltage distribution performance is desired while caring less on control complexity, the proposed passive "snubber" can be combined with active delay control strategy to accomplish this goal. By capturing $f_{(i)}$ (i = 1, 2) sent from the proposed GDs as feedbacks, the external DSP controller calculates and gives an accurate delay compensation to S_2 during the turn-off process as shown in Fig. 14, and thus an excellent VB performance of S_1 and S_2 is obtained as Δv_D measured to be 19.9V. Importantly, the proposed GD only absorbs the voltage overshoot once $v_{DS(i)}$ (i =1, 2) exceeds the clamping value and it does not influence the switching speed of SiC MOSFET. Also, the active delay control strategy does not slow down the device. Consequently, the proposed hybrid VB strategy contributes to maintaining the advantage of SiC device, resulting in a small switching loss. As measured, the dv/dt of S_i (i =1, 2) reaches 110 kV/μs during the turn-on process.

Since the closed-loop control is applied, the stability problem is introduced as well. As analyzed in Section IV, once the converter is built, the criterion for a stable system is obtained according to (21) and no experimental identification is required, which is superior than existing active delay control strategies. The hardware parameters have already been provided in Table I, and f_s = 10 kHz, i_D = 15 A, T_s = 0.2 s (with the diode-capacitor structure tolerating the voltage unbalancing temporarily, the controller calculation burden can be eased by choosing a relatively large T_s) are known in advance, hence, the appropriate range of K_p and K_i can be obtained. When K_p = 0, K_i is calculated to be smaller than $4.35 \cdot 10^{-7}$ and larger than 0. For the experimental verification, three following cases are respectively representing no closed-loop VB control, stable closed-loop VB control and unstable closed-loop VB control:

(1) K_i = 0 (beyond the parameter range): the experimental waveforms are performed in Fig. 13(b), and a visible voltage unbalancing is still observed.

(2) $K_i = 10^{-7}$ (within the parameter range): the experimental waveforms are shown in Fig. 15(a), and it is seen that, the voltage unbalancing of $v_{DS(1)}$ and $v_{DS(2)}$ only exists during the initial stage and VB is gradually achieved with the closed-loop

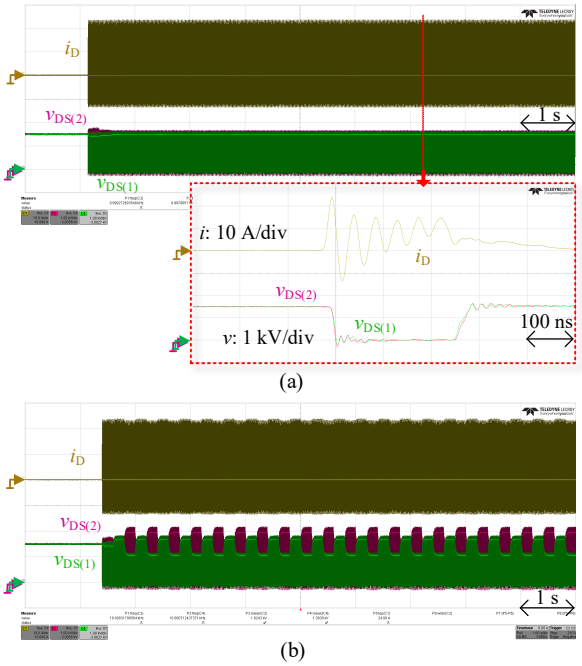

Fig. 15. Dynamic VB performance with (a) stable delay compensation, (b) unstable delay compensation

control. Then $v_{DS(1)}$ and $v_{DS(2)}$ keep the balanced state, as shown in the bottom of Fig. 15(a). Once the disturbance arrives such as the variation of i_D, the clamping capacitor as a buffer will tolerate the temporary voltage unbalancing until the DSP calculates and gives another appropriate delay compensation for dynamic VB.

(3) $K_i = 10^{-6}$ (beyond the parameter range): the experimental waveforms are shown in Fig. 15(b), and it is seen that an unstable phenomenon occurs when the parameter is not chosen properly. Since the maximum delay compensation is set in the software for the safety purpose, $v_{DS(1)}$ and $v_{DS(2)}$ alternately reach the maximum value 2.2 kV in a period of 0.4 s, which is determined by T_s. This unstable state will remain and it is not acceptable in series connection.

In summary, the experimental results verify the effectiveness of the proposed hybrid VB strategy, and also the correctness of the established small-signal system model which provides an intuitive guidance for parameters selection. In conclusion, the comparisons can also be made with the traditional GD delay control method with clamping RCD snubbers. In addition to the advantage of "self-powered design", from the perspective of loss, the proposed hybrid VB strategy exhibits the same switching loss of main transistors S_i and less snubber loss. While from the perspective of cost and size, the proposed strategy requires two additional main components: the low current rating transistor T_P (3300V/4A SiC MOSFET and its cost: $20.56/pcs), and the transformer (the designed PCB transformer and its size: 40.64mm*32.00mm*15.20mm in this prototype).

VII. Conclusion

In this article, a novel adaptive-impedance "snubber" concept is proposed for series connected power devices, so

that a better trade-off is achieved between loss and VB both in static and dynamic states compared to the conventional snubber. The corresponding analysis is given in detail, and the realization is by utilizing the designed converter-based self-powered GDs, which well satisfies the requirement of less control complexity in some applications. Specifically, static and dynamic voltage unbalancing is reduced by 50% and 33.3% respectively under the designed $V_{DC(max)}$, compared to the clamping RCD snubber.

Otherwise, if a better dynamic VB performance is pursued while caring less on the control complexity, the proposed passive "snubber" also provides an interface for the closed-loop control. Hence, it is further combined with active delay control strategy to form a hybrid VB strategy. Owing to the "snubber" design, the small-signal system model becomes easier to establish and the stability conditions are concluded accordingly.

Finally, the experimental results of two series connected 3.3kV SiC MOSFETs verify the VB performance of the adaptive-impedance self-powered GDs, which is consistent with the analysis. With the hybrid VB strategy, the voltage unbalancing is limited to 19.9V when DC bus voltage is 3 kV, and the fast switching speed of SiC MOSFET is not influenced.

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Rui Wang (S'18) received the B.S. degree in Electrical Engineering and Automation from Hunan University, Changsha, China, in 2017. He received the M.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2020. He is currently pursuing the Ph.D. degree in Aalborg University, Aalborg, Denmark.

His research interests include wide band-gap power semiconductor devices, their active gate drivers, series-connection technology and converter design.

Asger Bjørn Jørgensen received the M.Sc. and Ph.D. degrees in energy engineering from Aalborg University, Denmark, in 2016 and 2019, respectively.

He is currently working as an Assistant Professor at the Department of Energy Technology, Aalborg University. His research interests include power module packaging, wide bandgap power semiconductors and multi-physics finite element analysis within power electronic applications.

Wentao Liu (Graduate Student Member, IEEE) received the B.S. and M.S. degrees from Shandong University, Jinan, China, in 2018 and 2020, respectively. He is currently working toward a Ph.D. degree with AAU Energy, Aalborg University, Denmark.

His research interests include modeling and stability analysis of MMCs, as well as medium-voltage converter enabled by wide band-gap power devices.

Hongbo Zhao (S'16, M'21) received the Ph.D. degree in Power Electronics from Aalborg University, Denmark in 2021. Currently, he is a Postdoc Researcher with Aalborg University, Aalborg, Denmark.

His research interests include high-frequency modeling and analysis of high-power magnetics and filters, as well as medium-voltage converters enabled by wide band-gap power devices.

Zhixing Yan received the B.Eng. degree in electrical engineering and automation from Southwest Jiaotong University, Chengdu, China, in 2018, and M.Eng. degree in electrical engineering from South China University of Technology, Guangzhou, China, in 2021. He is currently working toward the Ph.D. degree in power electronics with Aalborg University, Aalborg, Denmark.

His current research interests include medium-voltage converters enabled by wide band-gap power devices.

Stig Munk-Nielsen (S'92–M'97) received the M.Sc. and Ph.D. degrees from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently a Professor at the Department of Energy Technology, Aalborg University. His research interests include LV and MV Si, SiC and GaN converters, packaging of power electronic devices, electrical monitoring apparatus for IGBTs, failure modes and device test systems. In the last ten years, he has been involved or has managed 10 research projects.

Published 242 international power electronic papers being co-author or author.