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A Hybrid-Bridge-Based Dual Active Bridge Converter With Reduced Device Count

JIAHUI WU [1] (Student Member, IEEE), DONG LIU [2] (Senior Member, IEEE), YANBO WANG [1] (Senior Member, IEEE), HONGBO ZHAO [1] (Member, IEEE), AND ZHE CHEN [1] (Fellow, IEEE)

[1]Department of Energy Technology, Aalborg Universitet, 9220 Aalborg, Denmark
[2]Group of Power Electronics, Lightyear, 5708 JZ Helmond, Netherlands

CORRESPONDING AUTHOR: DONG LIU (e-mail: liudong@ieee.org)

ABSTRACT In this paper, a hybrid-bridge-based dual-active-bridge (DAB) converter with a three-level (TL) half-bridge and a two-level full-bridge is proposed, which can be utilized to interface the medium voltage and low voltage DC. In the proposed converter, there are only eight power switches in total. Compared with the traditional hybrid-bridge-based DAB converter with a neutral-point-clamped (NPC) type TL half-bridge, a fewer power device count and higher efficiency can be realized in the proposed converter due to removing clamping diodes. Thus, a more compact circuit structure and a lower cost can be obtained. Moreover, zero-voltage-switching (ZVS) of all switches in primary-side and secondary-side can be achieved in the proposed converter. The operating principle, performances, and characteristics of the proposed converter are analyzed in detail. Also, a specification design case with a detailed key parameter design is given. Finally, a 1-kW experimental prototype is established to validate the proposed converter, and obtained experimental results are highly consistent with the theoretical analysis.

INDEX TERMS Dual-active-bridge (DAB) converter, hybrid-bridge, compact structure, zero-voltage-switching (ZVS).

I. INTRODUCTION

With the maturity of application technology and the reduction of cost, distributed renewable energy generation such as photovoltaics, wind turbine, and fuel cell accounts for more and more proportion in the future energy system [1], [2], [3]. Considering these power sources operate in DC before transmission, the use of DC grids becomes promising. Generally, these renewable energy sources are always fluctuant for maximum power point tracking (MPPT) performance and vary according to the changeable environmental conditions such as sunshine and wind [4]. In order to mitigate the power fluctuation caused by these new energy sources, the energy storage system (ESS) is usually equipped for DC grids.

Bidirectional converters are widely used to realize bidirectional power flowing and adjust voltage levels between low-voltage, medium-voltage, and high-voltage equipment in DC grid [5], [6], [7]. The dual-active-bridge (DAB) converter was first proposed in [8] and is becoming one of the most prevalent bidirectional converters due to its merits including wide range of zero-voltage switching (ZVS), compact structure, high power density, and galvanic isolation characteristics [9], [10].

Generally, the DAB converter is composed of two active bridges and one medium or high frequency transformer with a relatively large leakage inductance. The magnitude and flowing direction of power transmission are controlled by the shifting phases between the two active bridges. Therefore, there have been many studies about the modulation strategy based on the phase-shifting (PS) control for DAB converter. The simplest modulation strategy, i.e., single phase-shift (SPS) strategy was proposed in [11]. The voltage gain and power transmission direction can be controlled by adjusting the phase-shift delay between the switches of the primary side and secondary side. However, the SPS strategy lacks flexibility due to only one control variable, so there exists a large amount of circulating current, which would result in

excessive conduction losses of switch. Besides, it is easy to lose the ZVS characteristics under light loads in the DAB converter with the SPS control. Thus, the DAB converter with the SPS control maybe not suitable for applications such as electric vehicle charger and energy storage equipment, for which a wide voltage and load range are required. To decrease the circulating current and enlarge the ZVS range of the DAB converter, [12] propose the extended phase-shift (EPS) strategy, in which an extra phase shift between the leading and trailing bridge in the primary side or secondary side is adopted. Moreover, to further optimize the performance of the DAB converter, the double and triple phase-shift strategy were proposed in [13] and [14], respectively.

Apart from the phase-shift control with all the switches operating at 0.5 duty cycle, asymmetric control with part or all switches operating at a non 0.5 duty ratio obtains extra degrees of freedom for the DAB converter control. In [15], an asymmetric modulation method is proposed for the half-bridge-based DAB converter, in which six operation modes are applied by changing the duty cycle of primary-side and secondary-side switches. Based on [15], a three degree of freedom control combing with the asymmetric PWM control for all devices and PS control between the two active bridges is proposed in [16]. Similarly, a hybrid control including the primary asymmetric PWM control plus the secondary PS control is proposed for a hybrid-bridge based semidual-active-bridge (S-DAB) converter to improve the efficiency at light load in [17]. For the full-bridge based DAB converter, [18] and [19] propose an efficiency-oriented hybrid duty modulation scheme and an optimal asymmetric duty modulation, respectively. Multi-degree-of-freedom controls can be obtained because of the increasing amount of power devices with asymmetric duty. Besides, for the DAB resonant converter, one more degree-of-freedom introduced by switching frequency is utilized to achieve zero reactive power in [20]. With the increasing degrees of control freedom [16], [17], [18], [19], [20], [21], [22], [23], the performances of the DAB converter such as the ZVS range, conduction power losses and reflux power were significantly improved. However, the optimization performances of these strategies highly depend on the circuit parameters, various working mode classifications, and complex computation.

Besides, there are some studies on new topologies of the DAB converter, which can be mainly categorized into the two-level and the three-level (TL) DAB converter. Referring to the two-level DAB converter, [24] proposed a dual-transformer-based DAB converter, in which the ZVS range and voltage conversion gain are widely extended. A modified resonant DAB converter with a fixed frequency phase-shift control and an improved DAB converter with two blocking capacitors were proposed in [25] and [26], respectively, to achieve both wide voltage conversion gain and maintain the high efficiency. However, these topologies require additional components, and their two-level structure is not suitable for medium voltage applications due to the high voltage stress on main power switches. For the TL DAB converter, it is more applicable for medium or even high voltage application because of the reducing half of the voltage stress by the TL structure. To obtain wide ZVS range, a TL based series resonant DAB converter was proposed in [27]. In [28] and [29], a TL DAB converter with two TL half-bridges was proposed for high voltage applications. Besides, the TL DAB converter composed of two TL full bridges were proposed in [30] and [31], in which a double phase-shifted modulation strategy and a novel modulation strategy with five control degrees of freedom are utilized, respectively. However, traditional diode-clamped TL bridge with large main device count is adopted in these TL DAB converters. Fig. 1 shows the circuit topology of a traditional hybrid-based DAB DC/DC converter with a diode-clamped TL structure.

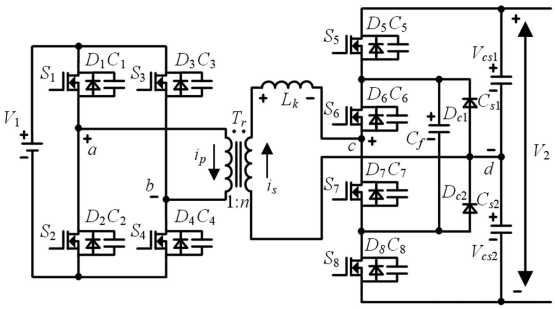


FIGURE 1. Conventional hybrid-bridge based DAB DC/DC converter with a diode-clamped TL structure.

Considering that more device count denotes more complex structure and higher cost, it is meaningful research on designing DAB converters with compact structures to enhance their industrial applicability for high voltage. Therefore, a hybrid-bridge-based DAB converter with a compact circuit structure is proposed in this paper as an extension of our previous work in [32]. The rest of this article is organized as follows. The proposed converter's structure and operating principle is introduced in Section II. A detailed analysis of the converter's performances and characteristics is presented in Section III. The design process of key parameters and a design case is presented in detail in Section IV. The results of verification experiments are demonstrated in Section V. Finally, conclusions are summarized in Section VI.

II. CIRCUIT STRUCTURE AND OPERATING PRINCIPLE

A. CIRCUIT STRUCTURE

The proposed hybrid-bridge based DAB convert with blocking capacitor is shown in Fig. 2. It consists of a primary two-level full-bridge, a secondary TL half-bridge, an intermediate frequency isolated transformer T_r with the turns ratio of 1: n, a blocking capacitor C_s in series with the secondary-side winds of T_r, and an auxiliary inductor if adding. In Fig. 2, V_1 is the primary voltage in the low-voltage dc port and maintains a constant voltage, V_2 is the secondary voltage in the high-voltage port. Between V_1 and V_2, the power flow is linked by the power link inductor L_k, the inductance of which is equals to the leakage inductance of T_r plus the auxiliary

TABLE 1. Comparison Results of Main Device Count

Items			Device count				
			Two-level resonant DAB converter [27]	TL half bridge DAB converter [29]	TL DAB converter [30]	Hybrid-bridge-based DAB converter with NPC type TL half-bridge (see Fig. 1)	Proposed converter (see Fig. 2)
Structure	Primary-side		Two-level full bridge	TL half bridge	TL full bridge	Two-level full bridge	Two-level full bridge
	Secondary-side		Two-level full bridge	TL half bridge	TL full bridge	TL half bridge	TL half bridge
Count of key component	Primary-side	V_1	**4**	**0**	**0**	**4**	**4**
		$V_1/2$	**0**	**4**	**8**	**0**	**0**
	Secondary-side	V_2	**4**	**0**	**0**	**0**	**0**
		$V_2/2$	**0**	**4**	**8**	**4**	**4**
	Resonant device		2	0	0	0	0
	Clamping capacitor		0	2	4	1	0
	Dividing Capacitor		0	4	4	2	2
	Blocking capacitor		0	0	0	0	1
	Clamping diode		**0**	**4**	**8**	**2**	**0**
	Total		**10**	**18**	**32**	**13**	**11**

Notes: the above comparison is based on the same specifications including the voltage level, power rating, and switching frequency. Besides, it is assumed that there have suitable power devices without the parallel and series connection for the compared converters based on the given specifications.

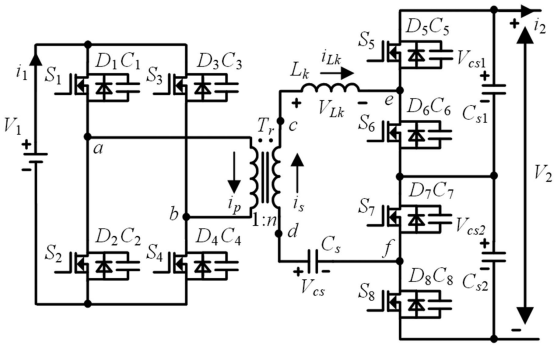


FIGURE 2. Circuit structure of proposed converter.

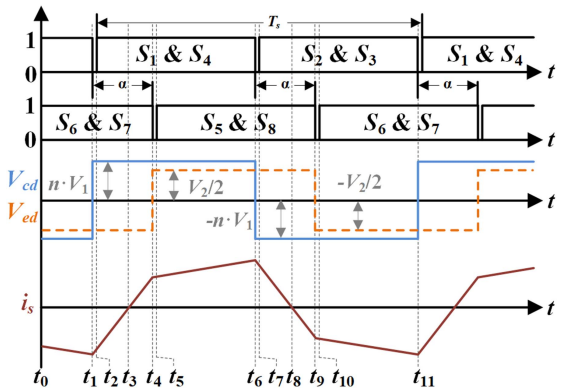


FIGURE 3. Typical operating waveforms when $2 \cdot n \cdot V_1/V_2 > 1$ in forward mode.

inductor. Besides, the secondary voltage V_2 is split into V_{cs1} and V_{cs2} halves by C_{s1} and C_{s2}.

The specific comparison results between the proposed converter and other DAB converters are presented in Table 1. According to Table 1, the following points can be observed. 1) Although the two-level DAB resonant converter has the lowest device count, power switches with high voltage stress are needed in secondary-side to withstand full of secondary-side voltage (V_2), for the proposed converter and other DAB converters with TL structure, power switches with only half of secondary-side voltage ($V_2/2$) stress are needed in TL side. 2) The proposed converter has fewer device count comparing with other TL half bridge-based and full-bridge based DAB converter by applying the hybrid-bridge structure. 3) More importantly, comparing with the traditional hybrid-bridge based DAB converter with NPC TL structure, two clamping diodes are removed in the proposed converter. Therefore, the proposed converter would be more applicable for interfacing the medium voltage and low voltage DC network and requiring a high-power density.

B. OPERATING PRINCIPLE

The SPS control is utilized in the proposed converter, the phase shift angle α between primary and secondary sides can be adjusted to control the voltage gain, and transferred power, and even working mode. Namely, the proposed converter works in forward and backward mode when α is positive and negative respectively. Take the forward mode for example to analyze the operating principle of the proposed converter in detail. With the same analysis method, the operating principle in backward mode can be also obtained.

Fig. 3 shows the typical operation waveforms of proposed converter in forward mode. Fig. 4 presents the equivalent operating circuits during $[t_0 - t_6]$ shown in Fig. 3.

Stage 1 $[t_0 - t_1]$ (see Fig. 4(a)) During this stage, switches S_2, S_3, S_6, and S_7 are on, switches S_1, S_4, S_5, and S_8 are off. Since the transformer's primary voltage V_{ab} is $-V_1$, the transformer's secondary voltage V_{cd} is $-n \cdot V_1$. Besides, the voltage V_{ef} is clamped to 0 V and the voltage of blocking capacitor V_{cs} is $V_2/2$. Considering the sum of the voltages on L_k is negative, L_k is discharged, and its current i_{Lk} reduces linearly. The following relationships can be obtained.

$$\begin{cases} i_s(t) = i_{Lk}(t) = i_{Lk}(t_0) + \frac{V_{cd}+V_{cs}-V_{ef}}{L_k} \cdot t \\ V_{ab} = -V_1, V_{cd} = -n \cdot V_1, V_{cs} = V_2/2, V_{ef} = 0 \end{cases} \quad (1)$$

where $i_{Lk}(t_0)$ is the current through L_k at t_0.

Stage 2 $[t_1 - t_2]$ (see Fig. 4(b)) At t_1, switches S_2 and S_3 are turned off. The junction capacitors C_1, C_4 and C_2, C_3 are charged and discharged respectively by the primary current of transformer i_p. During this period, i_p can be remained as constant because of the large enough power link inductor L_k, and C_2, C_3 will be charged from 0 V to V_1, while C_1, C_4 will

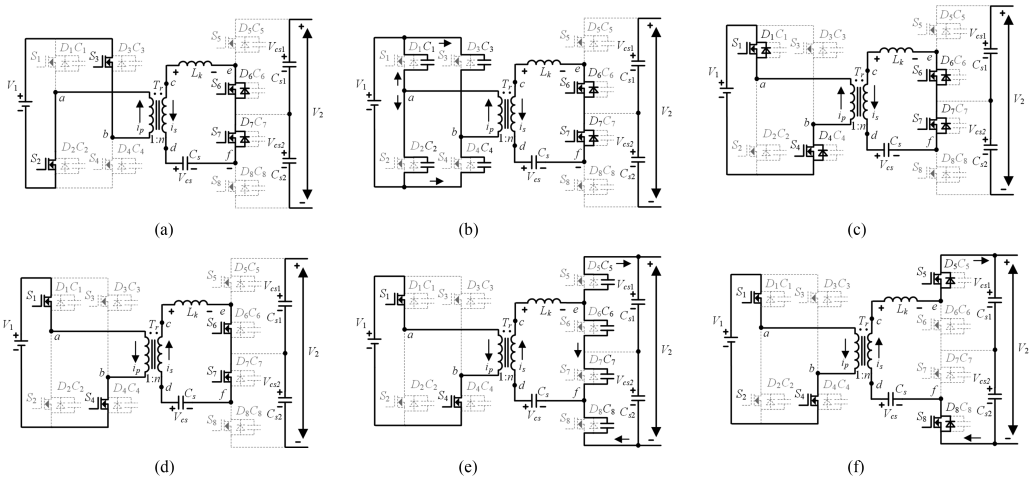


FIGURE 4. Equivalent operating circuits. (a) $[t_0 - t_1]$. (b) $[t_1 - t_2]$. (c) $[t_2 - t_3]$. (d) $[t_3 - t_4]$. (e) $[t_4 - t_5]$. (f) $[t_5 - t_6]$.

be discharged from V_1 to 0 V. After the process of charging and discharging complete, the body diode of S_1 and S_4 will conduct due to the negative current i_p. Thus, the ZVS of S_1 and S_4 would be achieved when they are turned on in the next stage. To ensure the ZVS of S_1 and S_4, the primary current of transformer i_p should be negative when the power switches S_2 and S_3 are turned off, and the energy E_1 stored in the power link inductor L_k should be large enough to complete discharging of C_1, C_4 and charging of C_2, C_3 before the power switches S_1 and S_4 are turned on in the next stage. Based on these principles, the ZVS conditions of S_1 and S_4 can be expressed as:

$$E_1 = \frac{1}{2}\frac{L_k}{n^2}\left(i_p\left(t_1\right)\right)^2 \geq \frac{1}{2}\left(C_1 + C_4 + C_2 + C_3\right)V_1^2 \quad (2)$$

where $i_p(t_1)$ is the instantaneous primary current of the transformer at the time point t_1, which can be expressed as:

$$i_p\left(t_1\right) = n \cdot i_s\left(t_1\right) = n \cdot i_{Lk}(t_1) \quad (3)$$

where $i_s(t_1)$ is the instantaneous secondary current of the transformer at the time point t_1.

Stage 3 $[t_2 - t_3]$ (see Fig. 4(c)) At t_2, switches S_1 and S_4 are turned on. During this period, V_{ab} is clamed to V_1, so V_{cd} changes to $n{\cdot}V_1$. Additionally, V_{cs} and V_{ef} are still $V_2/2$ and 0 V, respectively. Considering the sum of the voltages on L_k is positive, L_k is charged, and its current i_{Lk} increases linearly. The transformer's currents and voltages can be expressed as:

$$\begin{cases} i_s(t) = i_{Lk}\left(t\right) = i_{Lk}(t_2) + \frac{V_{cd}+V_{cs}-V_{ef}}{L_k} \cdot t \\ V_{ab} = V_1, V_{cd} = n \cdot V_1, V_{cs} = V_2/2, V_{ef} = 0 \end{cases} \quad (4)$$

Stage 4 $[t_3 - t_4]$ (see Fig. 4(d)) At t_3, i_{Lk} increases to 0 A, then it changes the flowing direction. During this period, i_{Lk} still increases linearly with the same slope rate during the last stage.

Stage 5 $[t_4 - t_5]$ (see Fig. 4(e)) At t_4, switches S_6 and S_7 are turned off. Then, the junction capacitors C_5, C_8 and C_6, C_7 are discharged and charged respectively by the secondary current of transformer i_s. During this period, C_6, C_7 will be charged from 0 V to $V_2/2$, while C_5, C_8 will be discharged from $V_2/2$ to 0 V. After the process of the charging and discharging complete, the body diode of S_5 and S_8 would conduct to realize ZVS for S_5 and S_8 in the next stage. To ensure the ZVS of S_5 and S_8, the secondary current of transformer i_s should be positive when the power switches S_6 and S_7 are turned off, and the energy E_2 stored in the power link inductor L_k should be large enough to complete the discharging of C_5, C_8 and charging of C_6, C_7 before the power switches S_5 and S_8 are turned on in the next stage. Based on these principles, the ZVS conditions of S_5 and S_8 can be expressed as:

$$E_2 = \frac{1}{2}L_k(i_s\left(t_4\right))^2 \geq \frac{1}{2}\left(C_5 + C_8 + C_6 + C_7\right)\left(\frac{V_2}{2}\right)^2 \quad (5)$$

Stage 6 $[t_5 - t_6]$ (see Fig. 4(f)) At t_5, switches S_5 and S_8 are turned on with zero voltage. During this stage, V_{ab} and V_{cd} are still V_1 and $n{\cdot}V_1$, respectively. Additionally, V_{cs} is still $V_2/2$, but V_{ef} becomes V_2. The transformer's currents and voltages can be given as (6).

$$\begin{cases} i_s(t) = i_{Lk}\left(t\right) = i_{Lk}(t_5) + \frac{V_{cd}+V_{cs}-V_{ef}}{L_k} \cdot t \\ V_{ab} = V_1, V_{cd} = n \cdot V_1, V_{cs} = V_2/2, V_{ef} = V_2 \end{cases} \quad (6)$$

At t_6, switches S_1 and S_4 are turned off, then the next half switching period $[t_6 - t_{11}]$ starts. The operating principle in the rest of the switching period is similar to that during $[t_1 - t_6]$.

III. PERFORMANCE AND CHARACTERISTICS

A. POWER CHARACTERISTIC

The expressions of the transformer's primary current i_p can be obtained as (7) according to the analysis of Fig. 4 in Section II.

$$\begin{cases} i_p(t) = i_p(t_1) + \frac{n{\cdot}V_1+V_2/2}{L_k} \cdot n \cdot tt_1 \leq t \leq t_4 \\ i_p(t) = i_p(t_4) + \frac{n{\cdot}V_1-V_2/2}{L_k} \cdot n \cdot tt_4 < t \leq t_6 \\ i_p(t_6) = -i_p(t_1) \end{cases} \quad (7)$$

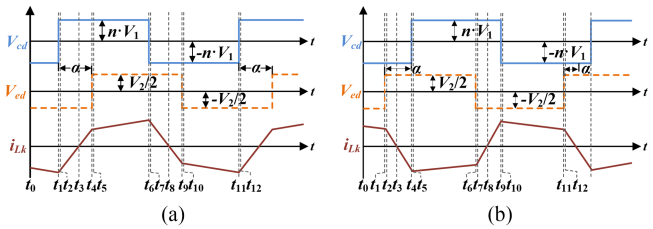


FIGURE 5. Typical waveforms when $2{\cdot}n{\cdot}V_1/V_2 > 1$. (a) Forward mode, i.e., $0 < \alpha < T_s/4$. (b) Backward mode, i.e., $-T_s/4 < \alpha < 0$.

Then, $i_p(t_1)$, $i_p(t_4)$, and $i_p(t_6)$ can be calculated as (8) if neglecting the dead-times $[t_1 - t_2]$ and $[t_4 - t_5]$.

$$\begin{cases} i_p(t_1) = -[\frac{n{\cdot}V_2{\cdot}(4{\cdot}\alpha - T_S) + 2{\cdot}n^2{\cdot}V_1{\cdot}T_S}{8{\cdot}L_k}] \\ i_p(t_4) = \frac{n{\cdot}V_2{\cdot}T_s + 2{\cdot}n^2{\cdot}V_1{\cdot}(4{\cdot}\alpha - T_S)}{8{\cdot}L_k} \\ i_p(t_6) = -i_p(t_1) \end{cases} \tag{8}$$

Based on (7) and (8), the average value of the transformer's secondary current i_{p_avg} in a half switching period can be calculated as:

$$i_{p\_\mathrm{avg}} = \frac{\int_{t_1}^{t_6} i_p(t)dt}{T_s/2} = \frac{n \cdot V_2 \cdot \alpha \cdot (T_s/2 - \alpha)}{L_k T_s} \tag{9}$$

Then, the primary transferred power of the proposed converter can be derived as:

$$P_1 = V_1 \cdot i_{p\_avg} = \frac{n \cdot V_1 \cdot V_2 \cdot \alpha \cdot (T_s/2 - \alpha)}{L_k T_s} \tag{10}$$

where P_1 is the primary transferred power.

B. VOLTAGE GAIN

In the proposed converter, the transferred power can be calculated as (11) if ignore the power losses on the transmission lines between the primary side and secondary side.

$$P_1 = i_1 \cdot V_{p\_\mathrm{avg}} = P_2 = \frac{V_2^2}{R_2} \tag{11}$$

where R_2 is the secondary output resistance. P_2 is the secondary transferred power.

From (10) and (11), the transformer's secondary side voltage V_2 can be derived as

$$V_2 = \frac{n \cdot V_1 \cdot R_2 \cdot \alpha \cdot (T_S/2 - \alpha)}{L_k T_S} \tag{12}$$

Then, the voltage gain can be further obtained as (13).

$$G = \frac{V_2}{n \cdot V_1} = \frac{R_2 \cdot \alpha \cdot (T_S/2 - \alpha)}{L_k \cdot T_S} \tag{13}$$

C. ZVS PERFORMANCE

Fig. 5 presents the main operation waveforms of these two modes if ignoring the dead-time. Fig. 5(a) and (b) show the typical waveforms when $0 < \alpha < T_s/4$ and $-T_s/4 < \alpha < 0$ respectively.

Considering that the voltage stress of the switches in the primary-side and secondary-side are different, two different kinds of switches with different parasitic capacitor are utilized here. Before analyzing the ZVS performance, the following assumptions of the parasitic capacitors of S_1- S_8 are made.

$$C_1 = C_2 = C_3 = C_4 = C_p \tag{14}$$

$$C_5 = C_6 = C_7 = C_8 = C_s \tag{15}$$

Based on (2), (5), (14), and (15), the ZVS constraints of S_1, S_4 and S_5, S_8 can be further derived as (16) and (17), respectively.

$$i_p(t_1) \le -2 \cdot n \cdot V_1 \cdot \sqrt{C_p/L_k} \tag{16}$$

$$i_s(t_4) \ge V_2 \cdot \sqrt{C_s/L_k} \tag{17}$$

With the similar analysis method, the ZVS constraints of all switches under both forward mode and backward model can be obtained and summarized in Table 2. Furthermore, the instantaneous currents in Table 2 can be further derived according to the voltage on L_k during each working stage. The corresponding calculation formulas of the transformer's primary currents in forward mode have been offered in Section II–B. With a similar derivation method, the transformer's secondary currents can be also derived. Table 3 summarizes the calculation formulas of the instantaneous currents shown in Table 2. According to Tables 2 and 3, the unified ZVS constraints can be further obtained as shown in Table 4.

Here, takes the forward mode as an example to further explain the ZVS performance. By substituting the formula (12) to the formulas in Table 4, the final expression of the ZVS constraints in the forward mode can be derived as shown in Table 5. From Table 5, it can be observed that the ZVS constraints are related to the secondary-side resistance R_2, phase shift time α, and power link inductor L_k. However, R_2 and α are normally determined by practical operating. Thus, the ZVS range can be optimized only through an optimal design of the power link inductor L_k.

The ZVS constraint of primary-side switches with the function of α namely $f_1(\alpha)$ is given as (18).

$$f_1(\alpha) = \frac{R_2 \cdot \alpha \cdot (T_s/2 - \alpha) \cdot (T_s - 4 \cdot \alpha)}{2 \cdot L_k \cdot T_s^2} + \frac{8 \cdot \sqrt{L_k \cdot C_p}}{n \cdot T_s} \le 1 \tag{18}$$

The maximum value of $f_1(\alpha)$ can be calculated as (19)

$$f_1(\alpha)_{\max} = f_1(\alpha)\Big|_{\alpha = \frac{3-\sqrt{3}}{12}T_s} = \frac{\sqrt{3} \cdot R_2 \cdot T_s}{576 \cdot L_k} + \frac{8 \cdot \sqrt{L_k \cdot C_p}}{n \cdot T} \tag{19}$$

Combining the formulas (18) and (19), (20) can be obtained.

$$\frac{\sqrt{3} \cdot R_2 \cdot T_s}{576 \cdot L_k} + \frac{8 \cdot \sqrt{L_k \cdot C_p}}{n \cdot T} \le 1 \tag{20}$$

The lower limit of the power link inductance L_k which is subject to the ZVS constraints of primary-side switches can be obtained based on (20).

TABLE 2. ZVS Constraints of All Power Switches

	S_1, S_4	S_2, S_3	S_5, S_8	S_6, S_7
Forward mode (See Fig. 5(a))	$i_p(t_1) \le -2\cdot n\cdot V_1\cdot\sqrt{C_p/L_k}$	$i_p(t_6) \ge 2\cdot n\cdot V_1\cdot\sqrt{C_p/L_k}$	$i_s(t_4) \ge V_2\cdot\sqrt{C_s/L_k}$	$i_s(t_9) \le -V_2\cdot\sqrt{C_s/L_k}$
Backward mode (See Fig. 5(b))	$i_p(t_4) \le -2\cdot n\cdot V_1\cdot\sqrt{C_p/L_k}$	$i_p(t_9) \ge 2\cdot n\cdot V_1\cdot\sqrt{C_p/L_k}$	$i_s(t_1) \ge V_2\cdot\sqrt{C_s/L_k}$	$i_s(t_6) \le -V_2\cdot\sqrt{C_s/L_k}$

TABLE 3. Instant Currents When Turning on Power Switches

	S_1, S_2, S_3, and S_4	S_5, S_6, S_7, and S_8
Forward mode (See Fig. 5(a))	$i_p(t_1) = -[\frac{n\cdot V_2\cdot(4\cdot\alpha - T_s) + 2\cdot n^2\cdot V_1\cdot T_s}{8\cdot L_k}] = -i_p(t_6)$	$i_s(t_4) = \frac{V_2\cdot T_s + 2\cdot n\cdot V_1\cdot(4\cdot\alpha - T_s)}{8\cdot L_k} = -i_s(t_9)$
Backward mode (See Fig. 5(b))	$i_p(t_4) = -[\frac{n\cdot V_2\cdot(-4\cdot\alpha - T_s) + 2\cdot n^2\cdot V_1\cdot T_s}{8\cdot L_k}] = -i_p(t_9)$	$i_s(t_1) = \frac{V_2\cdot T_s + 2\cdot n\cdot V_1\cdot(-4\cdot\alpha - T_s)}{8\cdot L_k} = -i_s(t_6)$

TABLE 4. The Unified Expression of the ZVS Constraints

	S_1, S_2, S_3, and S_4	S_5, S_6, S_7, and S_8
Forward mode Backward mode	$V_2\cdot(4\cdot\lvert\alpha\rvert - T_s) + 2\cdot n\cdot V_1\cdot T_s \ge 16\cdot\sqrt{C_p\cdot L_k}\cdot V_1$	$V_2\cdot T_s + 2\cdot n\cdot V_1\cdot(4\cdot\lvert\alpha\rvert - T_s) \ge 8\cdot\sqrt{L_k\cdot C_s}\cdot V_2$

TABLE 5. The Final Expression of the ZVS Constraints Under Forward Mode

	S_1, S_2, S_3, and S_4	S_5, S_6, S_7, and S_8
Forward mode	$\frac{R_2\cdot\alpha\cdot(T_s/2-\alpha)\cdot(T_s-4\cdot\alpha)}{2\cdot L_k\cdot T_s^2} \le 1 - \frac{8\cdot\sqrt{L_k\cdot C_p}}{n\cdot T_s}$	$\frac{2\cdot L_k\cdot(T_s-4\cdot\alpha)}{R_2\cdot\alpha\cdot(T_s/2-\alpha)} \le 1 - 8\cdot\sqrt{L_k\cdot C_s}/T_s$

TABLE 6. Specifications of the Design Case and Experiments

Rated secondary-side voltage V_{2_rated} (V)	400	Rated secondary-side power P_{2_rated} (kW)	1
Secondary-side voltage V_2 (V)	360~440	Rated secondary-side load resistor R_2 (Ω)	160
primary-side voltage V_1 (V)	128	Switch frequency f_s (kHz)	50
Parasitic capacitor of primary-side C_p (pF)	200	Parasitic capacitor of secondary-side C_s (pF)	40

The ZVS constraint of S_5, S_6, S_7, and S_8 with the function of α namely $f_2(\alpha)$ is given as (21).

$$f_2(\alpha) = \frac{R_2\cdot\alpha\cdot(T_s/2-\alpha)\cdot(1-8\cdot\sqrt{L_k\cdot C_s}/T_s)}{2\cdot L_k\cdot(T_s-4\cdot\alpha)} \ge 1 \tag{21}$$

According to (21), it can be observed that $f_2(\alpha)$ is a monotonically increasing function with the increase of α. It should be noted that (21) may not be always satisfied during $\alpha\in(0, T_s/4)$ with different L_k, which means the ZVS of secondary-side switches may not be achieved within the entire operating voltage range with different L_k. However, an optimal design of L_k can widen the ZVS range.

Fig. 6 shows the ZVS boundary of S_5, S_6, S_7, and S_8 with different L_k under forward mode, in which R_2 keeps at its rated value and other circuit parameters are shown in Table 6. In Fig. 6, when the proposed converter operates from the operating point A to C, the corresponding voltage gain is from 0.9 to 1.1. The operating point B represents the critical ZVS operating point when $f_2(\alpha)$ equals 1.

According to Fig. 6, it can be observed that the ZVS range of S_5, S_6, S_7, and S_8 is extended with the increase of L_k, and the ZVS can be achieved during the entire operating voltage range when L_k reaches 179 μH. Consequently, in order to achieve the ZVS for S_5, S_6, S_7, and S_8 during the entire operating voltage range, the critical ZVS condition at the lowest voltage gain should be satisfied with the minimum L_k. When $G = G_{min}$, it has

$$\begin{cases} f_2(\alpha) = \frac{R_2\cdot\alpha\cdot(T_s/2-\alpha)(1-8\cdot\sqrt{L_k\cdot C_s}/T_s)}{2\cdot L_k\cdot(T_s-4\cdot\alpha)} = 1 \\ G_{min} = \frac{R_2\cdot\alpha\cdot(T_s/2-\alpha)}{L_k\cdot T_s} \end{cases} \tag{22}$$

The minimum L_k which is subject to the ZVS constraints of secondary-side switches can be obtained based on (22).

IV. DESIGN OF KEY PARAMETERS

A. FLOWCHART OF DESIGN PROCESS

Fig. 7 shows a flowchart of the design process of key parameters in the proposed converter.

The transformer's turns ratio n, the power link inductor L_k, and the blocking capacitor C_s are designed step by step.

B. TURNS RATIO OF TRANSFORMER

Considering the voltage gain is equal to 1 at the rated output voltage V_{2_rated}, the transformer's turns ratio n can be obtained according to (23), it has

$$n = \frac{V_{2\_rated}}{V_1} \tag{23}$$

Thus, $n = 25{:}8$ can be obtained by (23) for the design case.

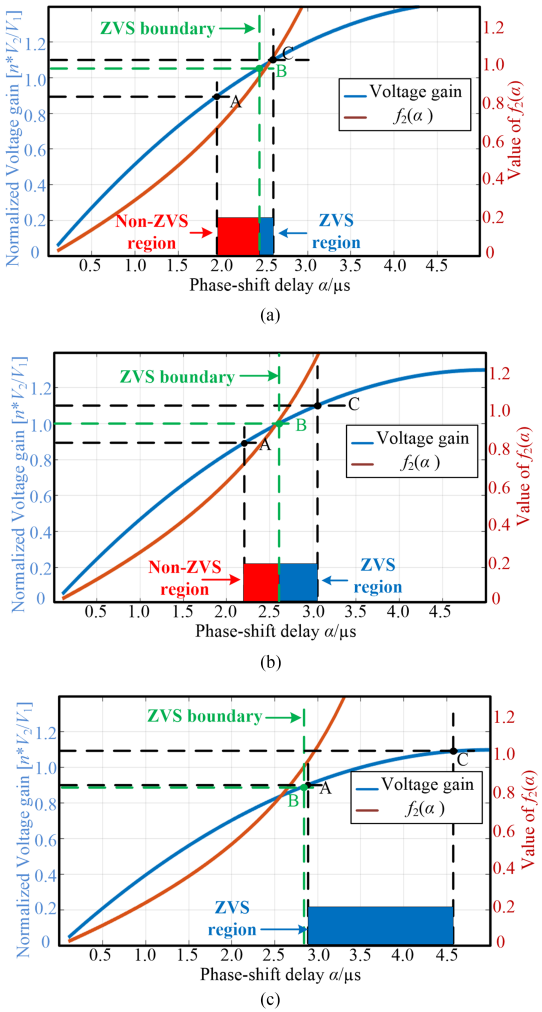


FIGURE 6. ZVS boundary of S_5, S_6, S_7, and S_8 with different L_k under forward mode. (a) $L_k = 140$ μH. (b) $L_k = 153$ μH. (c) $L_k = 179$ μH.

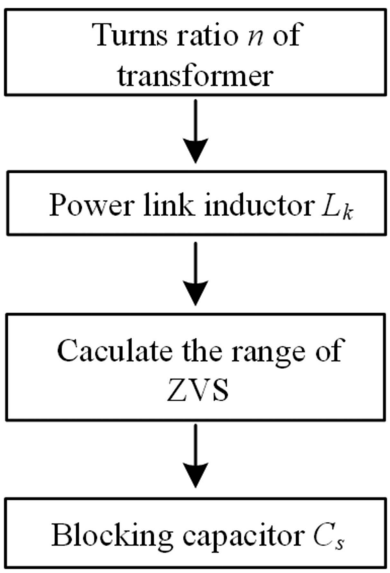


FIGURE 7. The design process of key parameters.

C. POWER LINK INDUCTOR

The range of the voltage gain is $G \in \left(\frac{V_{2\_\min}}{n \cdot V_1}, \frac{V_{2\_max}}{n \cdot V_1}\right)$ based on the given V_1, V_2, and selected n. Besides, the theoretically maximum voltage gain $G_{\max}$ can be obtained when the phase shift angle α is T_s / 4, which is shown in (24),

$$G_{\max} = G(\alpha)\Big|_{\alpha=\frac{T_S}{4}} = \frac{R_2 \cdot T_S}{16 L_k} \tag{24}$$

In order to meet the requirement of the operating voltage range, the formula (25) should be fulfilled.

$$G_{\max} \geq \frac{V_{2\_\max}}{n \cdot V_1} \tag{25}$$

Combining (24) and (25), the constraint for L_k due to the required operating voltage range can be obtained as (26)

$$L_k \leq \frac{n \cdot R_2 \cdot V_1 \cdot T_S}{16 \cdot V_{2\_\max}} \tag{26}$$

From (26), it can be observed that the inductance of the power link inductor L_k has an upper limit $L_{k\_\max}$ due to the requirement of the operating voltage range. For the given design case, it can be obtained that $L_{k\_\max} = 182$ μH based on (26).

Besides, the reflux power of the bidirectional converter should be considered when designing the power link inductor L_k since its increasing would increase the conduction losses of the converter. Here, the relation between reflux power P_r and L_k is analyzed in the forward mode as an example. During the stage 3 as shown in Fig. 4, the transformer's primary-side voltage V_{ab} and current i_p are positive and negative respectively, which would thus result in the reflux power flow from secondary-side to primary-side. The reflux power P_r can be calculated as [27], [33].

$$P_r = \frac{\alpha^2 \cdot V_1^2 \cdot T_s}{4 \cdot L_k} \tag{27}$$

According to (27), it can be seen that larger power link inductor L_k is of benefit to reduce the reflux power.

Moreover, based on the analysis in Section III–C, L_k is also subject to the ZVS constraints, which set a lower limit for L_k. According to (20) and (22), it is obtained that $L_k \geq 40.1$ μH and $L_k \geq 178.3$ μH, respectively, for the given design case. Thus, $L_k \geq 178.3$ μH should be satisfied.

Consequently, with the consideration of the constraints from the operating voltage range, reflux power, and ZVS, the power link inductance L_k should be less than 182 μH but larger than 178.3 μH. Here, $L_k = 179$ μH is chosen for the given design case.

D. BLOCKING CAPACITOR AND DIVIDING CAPACITORS

The blocking capacitor C_s is also an important component of the proposed converter. To select an appropriate blocking capacitor for the proposed converter, the following points have been considered.

1) The multilayer capacitor or film capacitor is recommended for the blocking capacitor. If utilizing the electrolytic capacitor, a significant loss would be occurred because of its high equivalent series resistance (ESR). Besides, the electrolytic capacitor may be destroyed by the negative voltage.
2) The voltage rating of the blocking capacitor should be higher than the steady-state operating voltage $0.5V_2$. Also, a voltage derating for the capacitor needs to be considered. Accordingly, the film or multilayer capacitors with a voltage rating of 0.75 V_2 or V_2 are suggested to be used for the blocking capacitor.
3) The capacitance of the blocking capacitor should be large enough to keep its operating voltage within a required range, such as 5% of V_2. Since the film capacitor or multilayer ceramic capacitor is utilized here and their ESR is low, the voltage ripple of the blocking capacitor is mainly decided by the charging and discharging of the capacitor. Thus, the voltage ripple on the blocking capacitor can be expressed as:

$$\Delta V_{Cs} = \frac{i_{p\_avg}}{n} \cdot \frac{T_S}{2 \cdot C_S} \tag{28}$$

Through substituting (9) into (28), (29), it can be obtained

$$C_S \geq \frac{\alpha \cdot (T_S/2 - \alpha)}{0.1 \cdot L_k} \tag{29}$$

According to (29), $C_s \geq 1.4\ \mu$F. It should be mentioned that in order to reduce the current stress, the blocking capacitor is normally composed of multiple groups with small value capacitors in parallel. In addition, the voltage ripple introduced by the ESR of pins and pads should be also considered. In this case, the voltage ripple on the blocking capacitor can be expressed as

$$\Delta V_{Cs} = \frac{i_{p\_avg}}{n} \cdot \frac{T_S}{2 \cdot C_S} + R_{\mathrm{ESR}} \cdot \Delta i_{L_k} \tag{30}$$

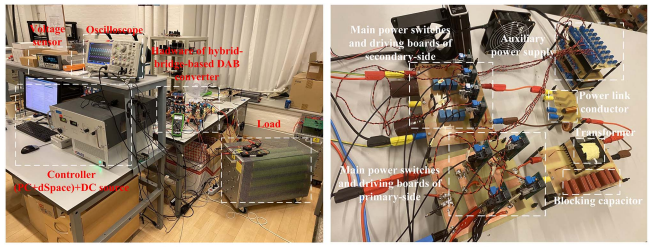
where R_{ESR} is the total ESR between the ends of the blocking capacitor; Δi_{Lk} is the current ripple of the power link inductor L_k and can be expressed as

$$\Delta i_{L_k} = \frac{nV_1 + \frac{1}{2}V_2}{L_k} \cdot \alpha + \frac{nV_1 - \frac{1}{2}V_2}{L_k}(T_s/2 - \alpha) \tag{31}$$

Generally, the electrolytic capacitor with a relatively large ESR is selected for the dividing capacitor and the voltage ripple on the dividing capacitor is mainly up to voltage ripple on ESR due to its high capacitance. In addition, the voltage ripple of secondary-side voltage should be limited within a required range, such as 5% of V_2. According to this requirement, it can be obtained as:

$$R_{DESR} \cdot \Delta i_{L_k} \leq 0.05 \cdot \frac{1}{2}V_2 \tag{32}$$

where R_{DESR} is the equivalent series resistor of the dividing capacitor.



(a) (b)

FIGURE 8. (a) Experimental setup. (b) Hardware of experimental prototype.

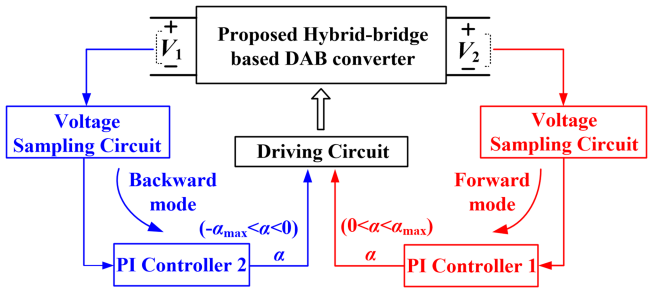


FIGURE 9. Control block diagram for proposed converter.

V. EXPERIMENTAL VERIFICATION

In order to verify the proposed converter, a 1-kW prototype is established, whose experiment setup and hardware are shown in Fig. 8(a) and (b), respectively. Here, the modulation and control are implemented by dSpace. When the proposed converter operates in forward mode, the DC source and resistive load are connected to the primary and secondary sides, respectively. The connection of the DC source and resistive load is just the opposite in backward mode.

In the built prototype, IRFI4229PbF and IPA50R380CE are used for power switches S_1-S_4 and S_5-S_8, respectively. The voltage dividing capacitors C_{s1}, C_{s2} are 470 μF, and the blocking capacitor C_S is 5.5 μF with 50 mΩ ESR.

Fig. 9 presents the control block diagram of the proposed converter, in which a simple digital proportional-integral (PI) controller is utilized to realize the voltage control by regulating the phase shift angle α. Besides, to avoid the conflict between the implementation of forward mode and backward mode, an upper limitation of phase-shift angle $\alpha_{\max}$ is set.

Fig. 10(a) and (b) show the steady-state operating waveforms of the proposed converter with the rated work conditions ($V_1 = 128$V, $V_2 = 400$V) in forward and backward mode respectively. In forward mode, the converter's primary side is used as an input port and powered by a DC source while the secondary side is used as an output port and connected to resistive load, which is just opposite in backward mode. In Fig. 10(a) and (b), V_1, V_2, i_1 and i_2 are the voltages and currents of the primary and secondary sides of converter respectively; V_{ab} is the transformer's primary-side voltage; V_{Cs} is the voltage on the blocking capacitor.

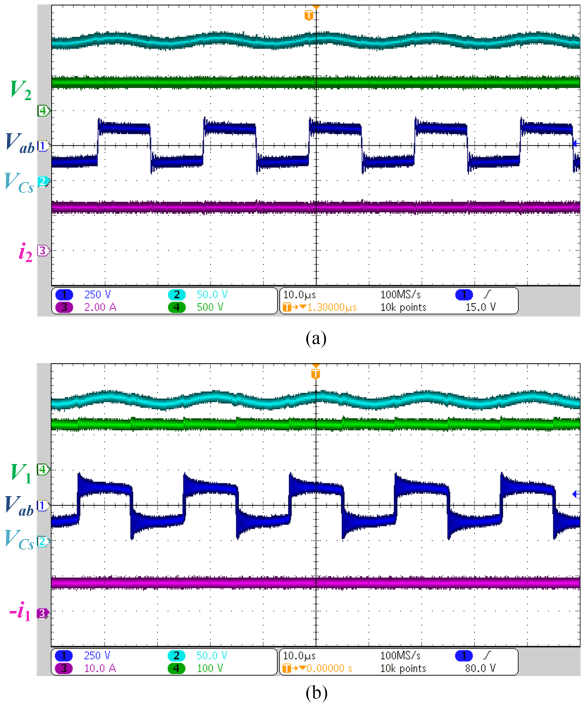


FIGURE 10. Steady state waveforms of the proposed converter under rated work conditions. (a) Forward mode ($P_2 = 1$ kW). (b) Backward mode ($P_1 = 1$ kW).

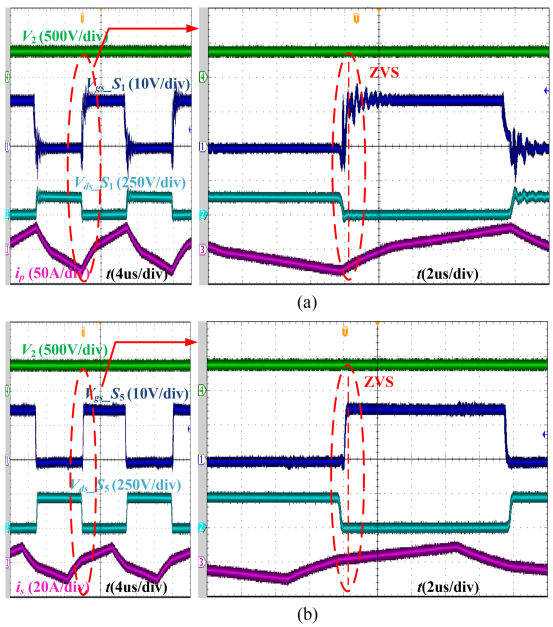


FIGURE 11. Driving signal and drain-source voltage of main switches when $V_2 = 400$ V, $R_2 = 160\Omega$, $P_2 = 1$ kW in forward mode. (a) S_1. (b) S_5.

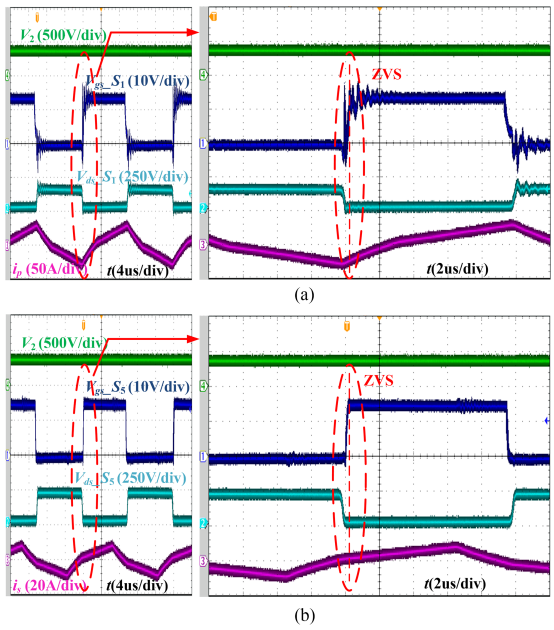


FIGURE 12. Driving signal and drain-source voltage of main switches when $V_2 = 360$ V. $R_2 = 160\Omega$, $P_2 = 810$ W in forward mode (a) S_1. (b) S_5.

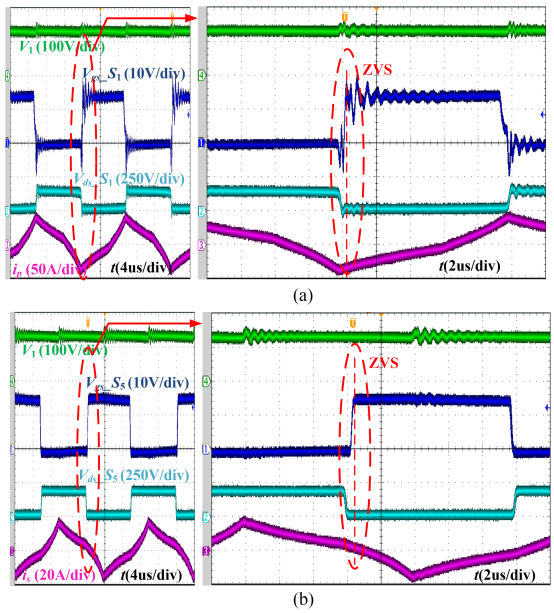


FIGURE 13. Driving signal and drain-source voltage of main switches when $V_1 = 128$ V, $V_2 = 400$ V, $P_1 = 1$ kW in backward mode. (a) S_1. (b) S_5.

Figs. 11–14 show the ZVS performances in forward and backward mode, which are measured under various work conditions. In Figs. 11–14, V_{gs}_S_1, V_{gs}_S_5 and V_{ds}_S_1, V_{ds}_S_5 are the driving signal and drain-source voltage of S_1 and S_5 respectively. i_p and i_s are the currents flowing through the transformer's primary side and secondary side.

From Fig. 10(a) and (b), it can be observed that V_{Cs} is about 200V, i.e., about $V_2/2$. The voltage ripple of V_{Cs} is 18.7 V and 19.5 V in forward and backward mode respectively, which are both less than $5\%*V_2$. The obtained results are also applicable to other work conditions and the related waveforms are not repeated here due to the page limitation.

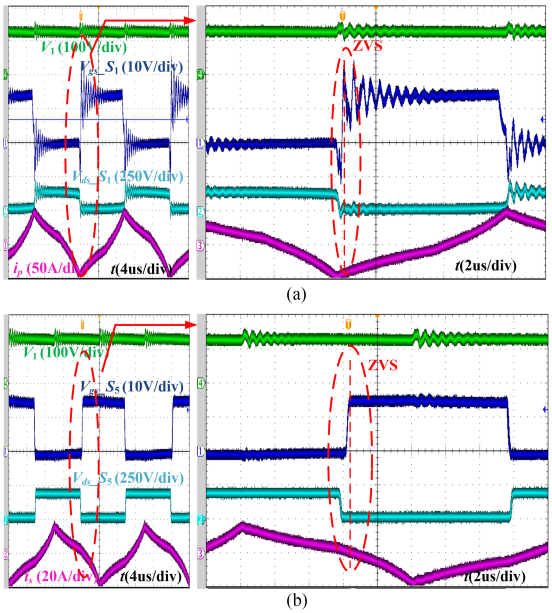


FIGURE 14. Driving signal and drain-source voltage of main switches when $V_1 = 128$ V, $V_2 = 360$ V, $P_1 = 1$ kW in backward mode. (a) S_1. (b) S_5.

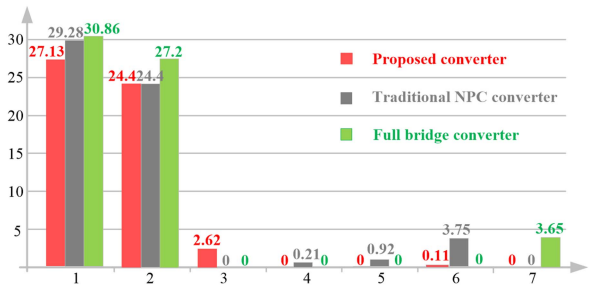


FIGURE 15. Comparison results about loss breakdown when $V_1 = 128$ V and $V_2 = 400$ V. Note: 1. Total loss of main devices in secondary-side 2. Power switches' loss; 3. Blocking capacitor's loss; 4. Clamping capacitor's loss; 5. Clamping diodes' loss; 6. Dividing capacitors' loss; 7. Output capacitor's loss.

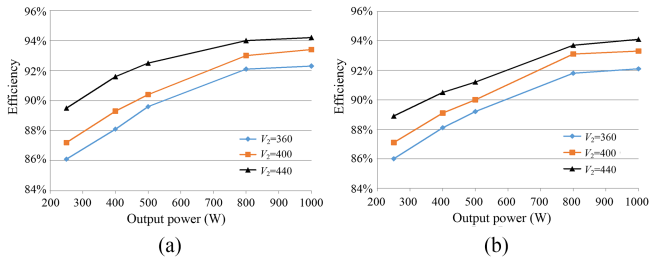


FIGURE 16. Efficiency results. (a) Forward mode. (b) Backward mode.

From Figs. 11–14, the following points can be observed. 1) The voltage stress on the power switch S_5 is about half of V_2, whose result is also applicable to switches S_6–S_8. 2) S_1 and S_5 can achieve ZVS within the entire operating voltage range of the secondary side, whose result is also applicable to S_2–S_4 and S_6–S_8. 3) The ZVS achievement of S_5 is more critical than that of S_1 because the transformer's secondary-side current i_s is close to 0 before S_5 is turned on. This means that the ZVS achievement of the high-voltage-side switches (i.e., S_5–S_8) would become deteriorate even lose under light load conditions.

Considering the same primary-side structure, transformer and power link inductor, the comparison of the loss breakdown only focuses on the secondary-side of the proposed converter, the traditional NPC converter, and the two-level full-bridge converter. The voltages of primary-side and secondary-side are 128 V and 400 V, the switching frequency is 50 kHz, and the delivering power is 1 kW for these three converters. Besides, the circuit parameters and corresponding modulation strategy of the traditional NPC converter are presented in Appendix. For the two-level full-bridge converter, IPN80R750P7 with a higher voltage rating and the single-phase-shift control strategy are applied. The selected power switches for the proposed and traditional NPC converter are the same, as mentioned above. Fig. 15 presents the calculated loss breakdown of main components in the secondary side. The related calculation methods are given in Appendix.

As a result, the total loss of the proposed converter is less than that of the traditional NPC converter and the two-level full-bridge converter. It should be mentioned that: 1) the AC current mainly passes through the blocking capacitor instead of the two dividing capacitors in the proposed converter, and the film capacitor with small capacity and low ESR is utilized for the blocking capacitor of the proposed converter; however; 2) the AC current only passes through the two dividing capacitors in the traditional NPC converter and the output capacitor in the two-level full-bridge converter, and the electrolytic capacitor with a large capacity and ESR is normally utilized for them. That is the reason why the total power loss of the blocking capacitor and dividing capacitors in the proposed converter is less than that of the clamping capacitor and dividing capacitors in the traditional NPC converter as well as that of the output capacitor in two-level full-bridge converter; 3) The entire secondary-side current would flow through the blocking capacitor in the proposed converter. As a result, it may be difficult to select the appropriate blocking capacitor for the proposed converter applied for high-power applications compared with the traditional NPC converter.

Fig. 16 presents the efficiency results of the proposed hybrid-bridge based DAB converter under forward mode and backward mode, in which the primary-side voltage V_1 maintains 128V.

From Fig. 16, it can be seen that the peak efficiency of the proposed converter in both forward and backward mode is over 94% under the rated work condition.

VI. CONCLUSION

This paper proposes a hybrid-bridge based DAB converter with a compact structure. Compared with other existing DAB converters and the traditional hybrid-bridge based NPC DAB converter, the following merits can be concluded for the proposed converter. 1) It would be more applicable for the

connection between the medium voltage and low voltage DC thanks to having the hybrid-bridge structure. 2) It has fewer main components and lower cost due to the removal of two clamping diodes. 3) It has higher efficiency and power density because of the replacement of the electrolytic clamping capacitor with a large capacity by the film blocking capacitor with a small capacity. Besides, with an optimal parameter design elaborated in this paper, ZVS of all the active switches on the primary-side and secondary-side can be achieved within the operating voltage range. Finally, the experimental results obtained from an established 1-kW prototype verify the correctness of the theoretical analysis and parameter design of the proposed converter.

APPENDIX

TABLE 7. Circuit Parameters for Conventional NPC Converter

Clamping capacitor C_f (μF)	100	Clamping diodes D_{C1}, and D_{C2}	IDP30E60
Dividing capacitors C_{S1}, and C_{S2} (μF)	470	ESR of diving capacitors (Ω)	0.15

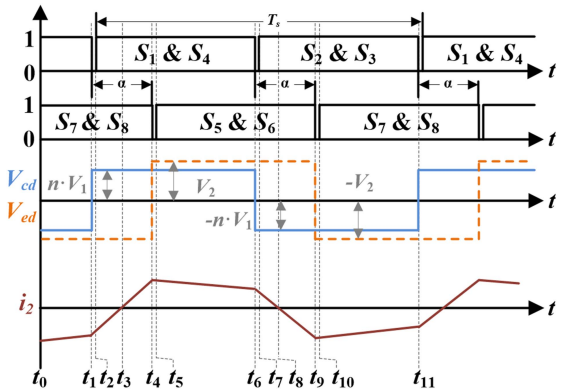


FIGURE 17. Typical operating waveforms of traditional NPC converter in forward mode.

The loss of power switches can be calculated as [34]:

$$\begin{cases} P_{total} = P_{on} + P_{turn\_off} \\ P_{on} = I_{s\_RMS}^2 \cdot R_{ds\_on}, P_{turn\_off} = \frac{V_{ds} \cdot I_{s\_RMS} \cdot t_f \cdot f_s}{2} \end{cases} \quad (33)$$

Where P_{total} is the total loss of power switches, which consists of conduction loss P_{on} and turn-off loss P_{turn_off}. The turn-on loss is eliminated because of the achievement of ZVS. I_{s_RMS} is the RMS current through the power switches, R_{ds_on} and t_f are the conduction resistor and turn-off delay time of power switches. $V_{\rm ds}$ is the voltage on the power switches, which is $V_2/2$ in the proposed converter and conventional NPC converter, and V_2 in the two-level full-bridge converter.

The loss of capacitor can be calculated as [35]:

$$P_c = I_C^2 \cdot R_{RSE} \quad (34)$$

Where P_c is loss of capacitor, I_c is the RMS current through the capacitor.

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JIAHUI WU (Student Member, IEEE) received the B.Eng. degree in electrical engineering from the Xi'an University of Technology, Xi'an, China, in 2015, and the M.Sc. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2018. He is currently the Ph.D. degree with Aalborg University, Aalborg, Denmark. His research interests include novel topology and advanced control strategy of the DC/DC converter for future energy system.

DONG LIU (Senior Member, IEEE) received the B.Eng. and M.Sc. degrees in electrical engineering from the South China University of Technology, Guangzhou, China, in 2008 and 2011, respectively, and the Ph.D. degree in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2018. From 2018 to 2021, he was a Postdoctoral Researcher with the Department of Energy Technology, Aalborg University. From June 2021 to December 2021, he was also a Research Associate with the Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield, U.K. He is currently a Power Electronics Engineer with Lightyear – Solar Electric Vehicle, The Netherlands. From 2011 to 2014, he was an R&D Engineer with Emerson Network Power Co., Ltd., Shenzhen, China. From May 2017 to November 2017, he was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA. His main research interests include the modeling and control of power electronics converters, high-efficiency power conversion systems, and power electronics applications in renewable energy power generation.

YANBO WANG (Senior Member, IEEE) received the Ph.D. degree with the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2017. He is currently with the Department of Energy Technology, Aalborg University, as an Assistant Professor. From June to October of 2016, he was a Visiting Scholar with Power System Research Group, Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, MB, Canada. His research interests include distributed power generation system, wind power system, microgrid, and operation and control technologies of power electronic-dominated power system. Dr.Wang's paper on Distributed Power System was the recipient of the First Prize Paper Award of the 6th International Conference of Smart Grid cosponsored by IEEE Industry Application Society in 2018, and the Best Session Paper Award at the annual conference of the IEEE Industrial Electronics Society in 2015 in Japan.

HONGBO ZHAO (Member, IEEE) received the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2021. He is currently a Postdoc Researcher with Aalborg University. His research interests include high-frequency modeling and analysis of high-power magnetics and filters, and medium-voltage converters enabled by wide band-gap power devices.

ZHE CHEN (Fellow, IEEE) received the B.Eng. and M.Sc. degrees in electrical engineering from the Northeast China Institute of Electric Power Engineering, Jilin, China, the M.Phil. in power electronic from Staffordshire University, Stoke-on-Trent, U.K., and the Ph.D. degree in power and control from the University of Durham, Durham, U.K.

Since 2002, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He is currently the Leader of Wind Power System Research Program with the Department of Energy Technology, Aalborg University. His main research interests include wind power, power electronics, power systems, and multi energy systems.

Chen is also an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, a Member of Editorial Boards of many international journals, a Fellow of the *Institution of Engineering and Technology* (IET, London, U.K.), and a Chartered Engineer in the U.K.