Isolation Forest Based Submodule Open-Circuit Fault Localization Method for Modular Multilevel Converters

Deng, Fujin; Chen, Yufei; Dou, Jingming; Liu, Chengkai; Chen, Zhe; Blaabjerg, Frede

Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2022.3167138

Publication date:
2023

Document Version
Accepted author manuscript, peer reviewed version

Isolation Forest Based Submodule Open-Circuit Fault Localization Method for Modular Multilevel Converters

Fujin Deng, *Senior Member, IEEE*, Yufei Chen, Jingming Dou, Chengkai Liu, Zhe Chen, *Fellow*, *IEEE* and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*- Fault localization is one of the most important issues for modular multilevel converters (MMCs) consisting of numerous switches. This paper proposes an Isolation Forest (IF) based SM switch open-circuit fault localization method for MMCs. Based on the continuous sampling SM capacitor voltages, a number of Isolation Trees (ITs) are produced to construct the IFs for MMCs. Through the comparison of continuous IFs' outputs, the faulty SM can be effectively localized. The proposed IF based fault localization method only requires SM capacitor voltages in the MMC to construct concise low-data-volume tree models, and uses sparsity and difference properties of outlier data to localize fault, and accordingly it simplifies calculation complexity. In addition, it does not require the MMC's mathematical models and manual setting of empirical thresholds. Simulation and experiment are conducted, and the results confirm the effectiveness of proposed method.**

***Index terms*- Isolation forest, isolation tree, modular multilevel converter, open-circuit fault, submodule.**

I. Introduction

Modular multilevel converters (MMCs) have gained increasingly applications in medium/high-voltage systems [1]. Compared with traditional multilevel converters, the MMC has a series of irreplaceable advantages such as modularity, flexibility, scalability, high efficiency, low switching frequency and superior harmonic performance, etc. [2].

Reliability is one of the important issues for MMCs. The MMC consists of numerous submodules (SMs) and each SM contains several power switches, where each switch could be a potential failure point and the switch open-circuit fault would affect the safe operation of MMCs [3], [4], and accordingly it is crucial to localize the faulty SM after the fault occurrence.

Recently, the SM fault localization methods for MMCs can be categorized into three categories. One category is hardware circuit-based method. Reference [5] presents the fault detection method based on the voltage across arm inductors using an additional winding. References [6] present the fault localization methods based on extra sensors and driver modules. The hardware circuit-based method requires extra circuits not only leads to increased cost but also new potential failure points.

One category is mathematical model-based method. References [7]-[11] adopt the Kalman Filter, sliding mode observers, single ring theorem, state observer for fault localization in MMCs. Reference [12] presents a fault localization method for MMCs under SM lower switch open-circuit fault. Reference [13] investigates the fault localization strategy based on the switching function. Mathematical model-based method requires the MMC's mathematical models, whose characteristics of high-order, nonlinear and strong coupling make it complicated. In addition, it needs to artificially set the threshold that varies with the operation conditions of the MMC, which also brings difficulties.

Artificial intelligence (AI)-based method is another category, which is attractive and competitive to be used for switch open-circuit fault localization in MMCs. Reference [14] presents an SM open-circuit fault localization strategy using sliding-time window based features extraction algorithm and two-dimensional convolutional neural networks (2D-CNNs). Reference [15] presents the one-dimensional convolutional neural networks (1D-CNNs) based fault localization method. Not only a large amount of voltage and current data, but also complex calculation is required for the method, which results in high calculation cost, and accordingly affect the efficiency of fault localization. Reference [16] presents an SM open-circuit fault localization method based on SM voltage similarity and time-domain feature extraction of capacitor voltages. Reference [17] presents the fault localization method based on two-dimensional trajectory pattern recognition of SM characteristic variables using clustering algorithm. However, the methods in [16], [17] still need to build detailed mathematical models of the MMC and set threshold artificially.

In this paper, an Isolation Forest (IF) based switch open-circuit fault localization method is proposed for MMCs. The IF composed of numerous Isolation Trees (ITs) is proposed to

This work was supported in part by the National Natural Science Foundation of China under Project 61873062. *(Corresponding author: Fujin Deng.)*

F. Deng is with the School of Electrical Engineering, Southeast University, and Jiangsu Key Laboratory of Smart Grid Technology and Equipment, Nanjing 210096, China (e-mail: fdeng@seu.edu.cn).

Y. Chen is with School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: 220192812@seu.edu.cn).

J. Dou is with China Electric Power Research Institute, Beijing 100192, China (e-mail: doujingming@epri.sgcc.com.cn).

C. Liu is with School of Electrical Engineering, Southeast University, Nanjing 210096, China and with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: lckisafish@163.com).

Z. Chen and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: zch@et.aau.dk; fbl@et.aau.dk).

be constructed based on continuous sampling SM capacitor voltages. Based on IFs' outputs, which are determined by SM average depth, the faulty SM can be effectively localized. The primary contributions of proposed method include: 1) it avoids constructing precise mathematical models and artificially setting empirical threshold in comparison with [16], [17]; 2) it directly utilizes the statistical characteristics of SM capacitor voltages instead of complicated feature extraction process in comparison with [14]-[17]; 3) it constructs concise low-data-volume tree models, uses sparsity and difference properties of outlier data to localize faulty SM, and accordingly it has low calculation complexity in comparison with [14], [15].

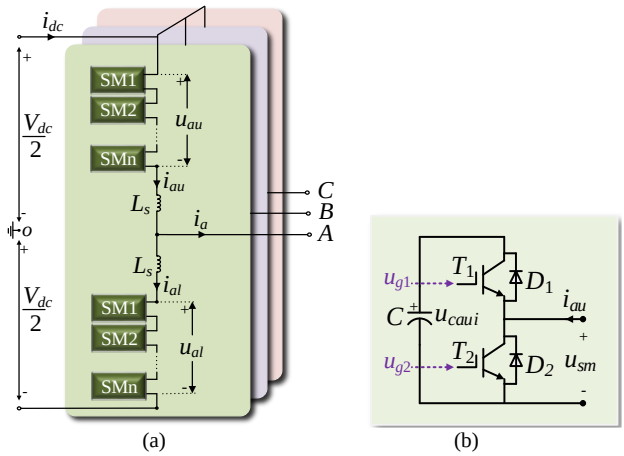
The rest of the paper is organized as follows. Section II describes the fault characteristics of MMCs. Section III proposes the IF based fault localization method for MMCs. Section IV discusses the proposed method. Sections V and VI present the simulation and experiment studies, respectively. Finally, the conclusion is presented in Section VII.

II. MMC Anomaly under Switch Open-Circuit Faults

A. Normal Operation of MMCs

A three-phase MMC consisting of six arms is shown in Fig. 1(a). Each arm consists of n identical SMs and an arm inductor L_s. Fig. 1(b) shows the i-th SM in upper arm of phase A, which consists of upper switch/diode T_1/D_1, lower switch/diode T_2/D_2 and a capacitor C [18]. Each SM is controlled by a switching function S_{aui} as

$$S_{aui}=\begin{cases}1, & T_1 \text{ is turned on \& } T_2 \text{ is turned off}\\ 0, & T_1 \text{ is turned off \& } T_2 \text{ is turned on}\end{cases} \tag{1}$$



(a) (b)

Fig. 1. MMC topology. (a) Three-phase MMC. (b) Submodule.

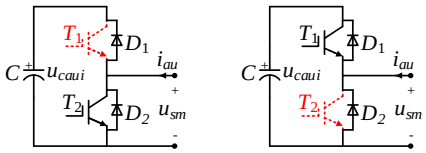
Table I shows four normal operation modes of the SM. In mode 1, the arm current i_{au} is positive and S_{aui}=1. Here, T_1 is switched on and T_2 is switched off. The SM output voltage u_{sm} is the capacitor voltage u_{caui}, the capacitor C is charged and u_{caui} is increased. In mode 2, i_{au} is positive and S_{aui}=0. Here, T_1 is switched off and T_2 is switched on. The u_{sm} is 0 and u_{caui} is unchanged. In mode 3, i_{au} is negative and S_{aui}=1. Here, T_1 is switched on and T_2 is switched off. The u_{sm} is u_{caui}, the capacitor is discharged, and the u_{caui} is decreased. In mode 4, i_{au} is negative and S_{aui}=0. Here, T_1 is switched off and T_2 is switched on. The u_{sm} is 0 and u_{caui} is unchanged [19].

TABLE I
Normal Operation Modes of SM in MMCs

Mode	i_{au}	S_{aui}	T_1	T_2	u_{sm}	u_{caui}
1	≥0	1	On	Off	u_{caui}	Increased
2		0	Off	On	0	Unchanged
3	<0	1	On	Off	u_{caui}	Decreased
4		0	Off	On	0	Unchanged

B. SM Switch Open-Circuit Faults Characteristics

Switch open-circuit fault can be categorized into two types of faults, as shown in Fig. 2.



(a) (b)

Fig. 2. SM open-circuit fault. (a) Type I. (b) Type II.

Type I: T_1 open-circuit fault, as shown in Fig. 2(a). T_1 fault has no impact on SM operation when i_{au} is positive. However, when i_{au} is negative, the i_{au} flows through D_2 and cannot flow through T_1. Therefore, the Mode 3 is affected, as shown in Table II. Here, u_{sm}=0 and u_{caui} is unchanged [20].

TABLE II
Fault Characteristics of T_1 Open-Circuit Fault

Mode	i_{au}	S_{aui}	T_1	T_2	u_{sm}	u_{caui}
3	<0	1	Open-circuit	Off	0	Unchanged

Type II: T_2 open-circuit fault, as shown in Fig. 2(b). T_2 fault has no impact on SM operation when i_{au} is negative. However, when i_{au} is positive, the i_{au} flows through D_1 and C while cannot flow through T_2. Therefore, the Mode 2 is affected, as shown in Table III. Here, u_{sm}=u_{caui} and u_{caui} is increased [20].

TABLE III
Fault Characteristics of T_2 Open-Circuit Fault

Mode	i_{au}	S_{aui}	T_1	T_2	u_{sm}	u_{caui}
2	≥0	0	Off	Open-circuit	u_{caui}	Increased

C. Anomaly of SM Capacitor Voltage under Faults

Based on (1) and Tables I~III, the absorbed power P_{sm_n}, P_{sm_T1}, P_{sm_T2} of the healthy SM, the SM under Type I fault, the SM under Type II fault, respectively, can be obtained as

$$P_{sm\_n}=S_{aui}\cdot u_{caui}\cdot i_{au} \tag{2}$$

$$P_{sm\_T1}=\begin{cases}S_{aui}\cdot u_{caui}\cdot i_{au}, & i_{au}\ge 0\\ 0, & i_{au}<0\end{cases} \tag{3}$$

$$P_{sm\_T2}=\begin{cases}u_{caui}\cdot i_{au}, & i_{au}\ge 0\\ S_{aui}\cdot u_{caui}\cdot i_{au}, & i_{au}<0\end{cases} \tag{4}$$

According to (2)-(4), the switch fault would obviously result in the anomaly of capacitor voltage in the faulty SM, as shown in Table IV. Under T_1 open-circuit fault, the SM operation loses the capacitor discharge period, and there would be P_{sm_T1}>P_{sm_n}, and it results in that the capacitor voltage in faulty SM would be larger than that in healthy SMs. Under T_2 open-circuit fault, the capacitor in faulty SM charges longer time than healthy SMs, there would be P_{sm_T2}>P_{sm_n},

and it results in that the capacitor voltage in faulty SM would be larger than that in healthy SMs.

TABLE IV
Anomaly of Faulty SM

Fault type	Anomaly of faulty SM capacitor voltage
I	Larger than healthy SM
II	Larger than healthy SM

III. Proposed IF Based Fault Localization Method

IF shows state-of-the-art performance in the data-mining field, and widely used in data anomaly detection in industry, network security and financial transactions due to its linear time complexity and excellent accuracy [21]-[23]. In this paper, the IF is adopted to identify the outlier data of capacitor voltages under SM open-circuit fault, and an IF based fault localization method is proposed for MMCs. Fig. 3 shows the IF based fault localization method for the upper arm of phase A, which can localize the fault based on the IF constructed by the capacitor voltages u_{cau1}~u_{caun} in the upper arm of phase A of the MMC.

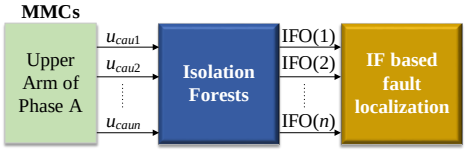


Fig. 3. Proposed IF based fault localization method for upper arm of phase A.

A. IT for MMCs

In the MMC, the n SM capacitor voltages u_{cau1}~u_{caun} in the upper arm of phase A are sampled, where the capacitor voltage sampling frequency is f_s and the sampling period is T_s=1/f_s. In each sampling period T_s, an IT is constructed by the sampled n SM capacitor voltages u_{cau1}~u_{caun}. Fig. 4 shows an IT example. The IT is a non-linear data structure, which contains a number of Levels. Each Level is composed of the Nodes, where the Node is separated into two Nodes in the next Level, as follows.

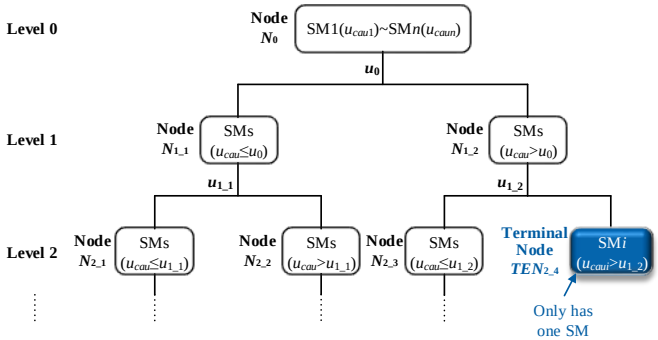


Fig. 4. An IT example for the upper arm of phase A.

Level 0: Root Node N_0, which contains n SMs as SM1~SMn.

Level 1: Randomly select a split value u_0, which is between the minimal SM capacitor voltages and the maximal SM capacitor voltages in Node N_0. Afterwards, the Node N_0 is separated into two Nodes N_{1_1} and N_{1_2}. The Node N_{1_1} contains the SMs in the N_0, whose capacitor voltage is less than or equal to u_0. The Node N_{1_2} contains the SMs in the N_0, whose capacitor voltage is more than u_0.

Level 2~Last Level: Referring to Level 1, the Nodes N_{1_1} and N_{1_2} are separated into more Nodes, respectively, until each Node only contains one SM.

Finally, the IT will have n terminal Nodes (TENs) localized at the terminals of these branches, where each TEN contains only one SM. Since the TEN only has one SM, it can no longer be separated. In the IT, the n SMs including SM1~SMn are finally distributed into the n TENs in the light of their corresponding capacitor voltages. In the IT, the TEN containing the SMi ($1\le i\le n$) can be expressed as TEN(SMi). The Level of TEN(SMi) in the IT can be expressed as IT[Level(TEN(SMi))].

B. SM Depth in IT

In the IT, the Depth $D(i)$ of the SMi ($1\le i\le n$) can be expressed with the Level of the TEN containing the SMi, as

$$D(i) = \mathrm{IT}[\mathrm{Level}(\mathrm{TEN}(\mathrm{SM}i))] \tag{5}$$

According to the IT principle [22], the smaller of the $D(i)$, there would be a high probability that the SMi would have a higher anomalous degree; the bigger of the $D(i)$, there would be a high probability that the SMi would have a lower anomalous degree, as shown in Table V.

TABLE V
IT Principle about SM Anomalous Degree and SM Depth

SM Depth	Anomalous degree
Small	High (High probability)
Big	Low (High probability)

In the MMC, the SM open-circuit fault would cause SM capacitor voltage anomaly, as shown in Table IV. According to IT principle [22] and Table V, suppose that the SM anomaly accounts for a small amount, the SM anomaly would result in a high probability that the depth D of faulty SM is small in comparison with that of healthy SM in the IT, as shown in Table VI.

C. IF for MMCs

An IF is composed of m_p (p=1, 2, 3 ...) continuous ITs including IT$_1$~IT$_{m_p}$, which is constructed based on n SM capacitor voltages u_{cau1}~u_{caun} sampled at m_p continuous sampling periods with the sampling interval as T_s.

Fig. 5(a) shows the IFs for the MMC with n=6 SMs per arm. In each IF, the j-th ($1\le j\le m_p$) IT has n TENs corresponding to the n SMs (SM1~SMn), respectively, where each SM corresponds with a depth. The $D(i, j)$ represents the Depth of the SMi ($1\le i\le n$) in the j-th IT of the IF. Fig. 5(a) also shows the anomalous degree for the TENs in the IF, where the Node with the color is TEN. Along with the darkening of the color, the anomalous degree of the TEN will have a high probability to be high, and the TEN would have a high probability to contain an anomalous SM.

D. SM Average Depth in IF

In each IF, the average depth $AD(i)$ of the SMi is

$$AD(i) = \frac{1}{m_p}\sum_{j=1}^{m_p} D(i, j) \tag{6}$$

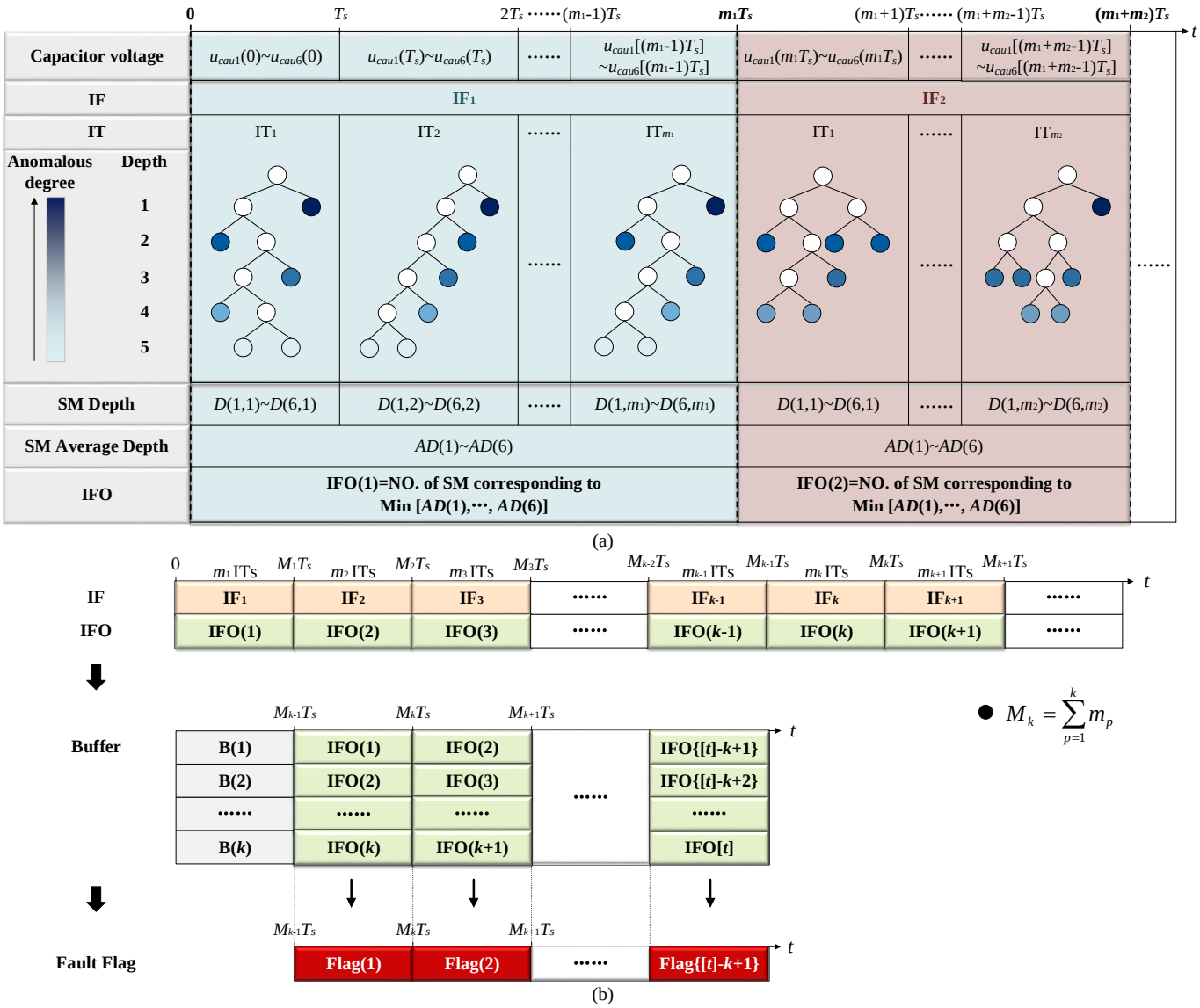


Fig. 5. IFs for the MMC. (a) IFs and IFOs. (b) Buffer and fault flag.

According to IF principle [22], the $AD(i)$ for the SMi depends on the capacitor voltage anomaly in the SMi, as shown in Table VI, as follows.

- If the SMi has no anomaly because its capacitor voltage has no anomaly, there is a high probability that the average depth $AD(i)$ of the SMi in the IF is big.
- If the SMi has anomaly because its capacitor voltage has anomaly, there is a high probability that the average depth $AD(i)$ of the SMi in the IF is small.

TABLE VI
IF for MMCs under Fault

SM state	SM Depth	SM's AD
Open-circuit fault	↓	↓
Health	↑	↑

E. IF Output

For each IF, its output IFO is defined as the number (e.g. 1, 2…n) of the SM corresponding to the minimal AD among $AD(1)$~$AD(n)$, as

$$\text{IFO} = \text{No. of SM corresponding to Min}[AD(1)\sim AD(n)] \quad (7)$$

Based on above analysis, it can be observed that the switch open-circuit fault in the SMi results in that the $AD(i)$ corresponding to the SMi has a high probability to be smallest. Consequently, the number i corresponding to the faulty SMi would be the output of the IF.

F. Fault Detection

With the IF principle, the IF_1, IF_2, IF_3…… for the MMC are produced over the time, which are not overlapped, as shown in Fig. 5(b). In order to achieve fault localization in the MMC, k number of continuous IFs are adopted, whose outputs are stored in the buffer, as shown in Fig. 5(b). The buffer can be expressed as

$$\text{Buffer}=\{B(1), B(2),\ldots, B(k)\} \quad (8)$$

with

$$\begin{cases} \mathrm{B}(1) = \mathrm{IFO}\{[t]-k+1\} \\ \quad\vdots \\ \mathrm{B}(k-1) = \mathrm{IFO}\{[t]-1\} \\ \mathrm{B}(k) = \mathrm{IFO}[t] \end{cases} \tag{9}$$

where B(1), …, B(k) represent k elements in the buffer. IFO[t] is defined as the latest IFO at time t, IFO{[t]-1} is defined as the sub-latest IFO at time t, and so on. The buffer is updated every m_pT_s, where the oldest IFO is popped and the newest IFO is inserted.

Based on the k number of values B(1), B(2),…, B(k) in the buffer, a fault flag is defined as

$$\mathrm{Flag}=\mathrm{TRUE}\{\mathrm{B}(1)=\mathrm{B}(2)=\ldots=\mathrm{B}(k)\} \tag{10}$$

The faulty SM in the MMC can be detected based on the Flag, as follows.

- When the k values in the buffers are all the same as B(1)=B(2)=…=B(k)=γ ($1\le\gamma\le n$), it means that the k numbers of continuous IFOs are the same, the Flag will be "1", and the γ-th SM is detected with the fault. And then, the γ-th SM is bypassed from the MMC. Afterwards, the fault localization still continues to work to detect the fault.
- When the k values in the buffers B(1), B(2),…, B(k) are not the same, it means that the k numbers of continuous IFOs are not the same, the Flag will be "0", the MMC works normally without faults. And then, the fault localization still continues to work to detect the fault.

IV. Analysis on Proposed Fault Localization Method

A. Selection of m_p

An IF contains m_p ITs. Taking the MMC with 6 SMs per arm as an example, as shown in Table VIII. Fig. 6(a) and Fig. 6(b) show the average depth $AD(1)$~$AD(6)$ of a constructed IF with various m_p, where the T_1 open-circuit fault and T_2 open-circuit fault occur in the SM1 of the MMC working in inverter mode, respectively. In the Fig. 6, the $AD(1)$ is the smallest among $AD(1)$~$AD(6)$ owing to the fault in SM1.

According to IF algorithm [21]-[23], along with the increase of m_p, the AD would be stable and nearly constant, as shown in Fig. 6. As a result, m_p can be selected when the AD becomes nearly constant. The selection of m_p can be implemented as follows. A number of latest $AD(i)$s are selected and their average value is calculated as $AD(i)_{avg}$. When these latest $AD(i)$s are in the range of $[(1-\varepsilon)\cdot AD(i)_{avg}$, $(1+\varepsilon)\cdot AD(i)_{avg}]$ and lasts for several periods, where ε is error, the $AD(i)$ can be regarded to be stable, and then the m_p can be selected. For example, the selection of m_p in Fig. 6 can be implemented, where the m_p can be obtained as 84 when ε=0.5%.

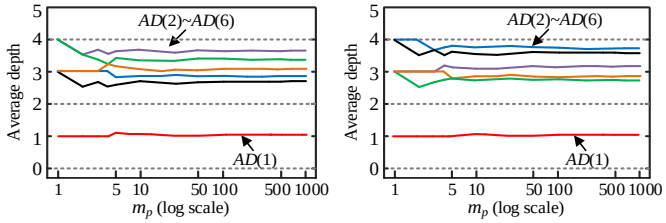


Fig. 6. AD of IT under various m_p. (a) T_1 fault. (b) T_2 fault.

B. Selection of k

The buffer has k IFOs. Obviously, the bigger of k, the longer of the fault localization time, and vice versa. In addition, the k is related to the fault localization accuracy, where the fault localization accuracy is increased when the k is increased, and vice versa. Fig. 7 shows the relationship between k and fault localization accuracy based on the system shown in Table VIII, where 250 samples under fault cases and 250 samples under fault-free case are considered. All samples are divided into two types as 0 (health) and 1 (fault) and the accuracy can be expressed as (11) based on confusion matrix theory [24].

$$Accuracy = \frac{TP+TN}{TP+FP+TN+FN} \tag{11}$$

where TP is true positive defined as the number of samples predicted as 1 and actually is 1. FP is false positive defined as the number of samples predicted as 1 but actually is 0. FN is false negative defined as the number of samples predicted as 0 but actually is 1. TN is true negative defined as the number of samples predicted as 0 and actually is 0.

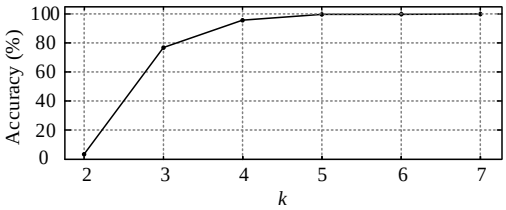


Fig. 7. Relationship between fault localization accuracy and k.

From Fig. 7, it can be observed that the accuracy is increased along with the increase of k, where the accuracy reaches 99.2% when k=5. Hence, to ensure the accuracy, the k can be selected as 5 for this MMC system.

C. Discussion of Fault Localization Time

The fault localization time is related to the arm current at the fault occurrence instant. Figs. 8 and 9 show the fault localization time of the MMC working in inverter mode and rectifier mode, respectively, which are derived from the simulation system in Section V. Here, T_1 open-circuit fault occurs in the SM1 of the MMC and T_2 open-circuit fault occurs in the SM1 of the MMC are considered, respectively. Figs. 8(a) and 9(a) show the arm current in one period. Figs. 8(b) and 9(b) show the fault localization time of the MMC corresponding to various arm current at fault occurrence instant. It can be observed that the arm current direction at fault occurrence instant affects the fault localization time. The proposed fault localization method can effectively localize the faulty SM within one fundamental period, 20 ms.

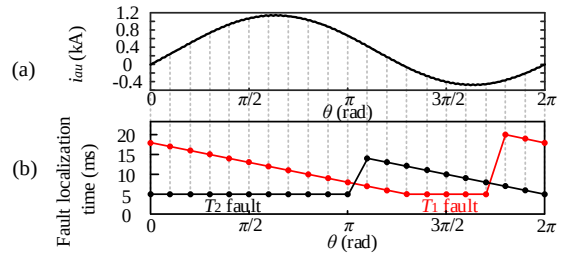


Fig. 8. Fault localization time for MMCs in inverter mode. (a) Arm current. (b) Fault localization time corresponding to various arm current at fault instant.

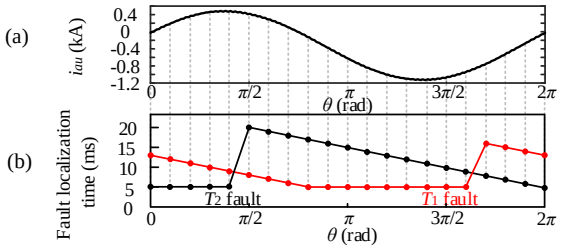


Fig. 9. Fault localization time for MMCs in rectifier mode. (a) Arm current. (b) Fault localization time corresponding to various arm current at fault instant.

Figs. 10(a) and (b) shows the fault localization time for the MMC with different numbers of SMs per arm, including 10, 20, 50, 100 and 200, where the MMC working in inverter mode and rectifier mode are considered, respectively. For the MMCs with different number of SMs per arm, their capacitor voltages are kept the same. Fig. 10(a) shows the fault localization time for the MMC when the fault occurs at θ=0 for arm current shown

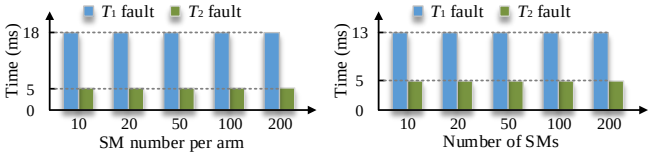


Fig. 10. Fault localization time for the MMC with different number of SMs per arm. (a) Inverter mode and θ=0. (b) Rectifier mode and θ=0.

in Fig. 8. Fig. 10(b) shows the fault localization time for the MMC when the fault occurs at θ=0 for arm current shown in Fig. 9. Here, the T_1 open-circuit fault of SM1 and T_2 open-circuit fault of SM1 in upper arm of phase A, respectively, are considered. It can be observed that different numbers of SMs per arm almost does not affect the fault localization time.

D. Implementation Time of Proposed Method

Fig. 11 shows the implementation time for one IT. It increases along with the increase of SM number n per arm, where the classic Pascal architecture (P40, P100) graphics-processing unit (GPU) is considered. The implementation time consists of two parts including calculation for depth and calculation for *AD*. It can be observed that the implementation time is less than 10 μs even n=200, which is quite short.

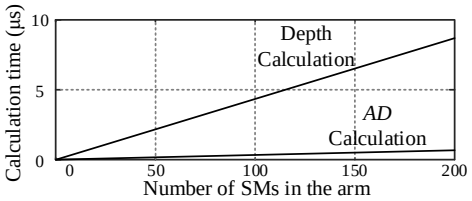


Fig. 11. Implementation time for one IT.

E. Comparison of Fault Localization Methods

Table VII compares the proposed method and other fault localization methods [5]-[10], [14]-[17], in view of mathematical models, extra hardware, data volume, calculation cost, and fault localization time.

TABLE VII
Comparison of Fault Localization Methods for MMCs

Method	Math Models	Extra Hardware	Data volume	Cal. cost	Localization time (ms)
[5]	No	Yes	/	/	About 100
[6]	No	Yes	/	/	About 40
[7]	Yes	No	/	/	About 100
[8]	Yes	No	/	/	About 40
[9]	Yes	No	/	/	About 40
[10]	Yes	No	/	/	40~100
[14]	No	No	Large	High	<20
[15]	No	No	Large	High	About 100
[16]	Yes	No	Large	High	<20
[17]	Yes	No	Large	High	About 40
Proposed	No	No	Small	Low	<20

The methods in [5], [6] require additional equipment, which would incur not only increased cost, but also new potential failure points. The methods in [7]-[10] rely on the MMC's detailed mathematical model, which would be complex along with the increase of the SM number. What is more, the methods in [7]-[10] require manual setting of complex empirical threshold. Both the AI-based methods [14]-[17] and the proposed method are data-driven. The methods in [14], [15] use numerous data in multiple dimensions including capacitor voltages, arm currents, circulating currents, etc., and it requires complex calculation. The methods in [16], [17] still need the MMC's mathematical models and set the complex threshold. However, the proposed method only depends on capacitor voltages, which reduces the data volume. Besides, the proposed method has low memory requirement and low calculation cost.

The proposed method can localize the fault within one fundamental period, 20 ms, with the advantage of concise low-data-volume tree models. The hardware circuit based methods [5], [6] require around 100 ms and 40 ms, respectively, to localize the fault. The mathematical model based methods [7]-[10] require around 40~100 ms. The method presented in [15] requires about 100 ms owing to the fact that inaccurate feature expression. Besides, the methods in [14], [16] can localize the fault within 20 ms and the method in [17] requires around 40 ms to localize the fault.

V. Simulation Studies

To verify proposed method, a three-phase MMC connected to the grid via a transformer is built with PSCAD/EMTDC. The system parameters are shown in Table VIII.

TABLE VIII
Simulation System Parameters

Parameter	Value
Rated power of the MMC	6 MW
DC-link voltage V_{dc}	6 kV
Number of SMs per arm	6
SM capacitance C	12.5 mF
Arm inductance L_s	3 mH
Filter inductance L_f	1 mH
Transformer voltage rating	3 kV/33 kV
Grid voltage	33k V
Grid frequency f_g	50 Hz
Sampling frequency f_s	100 kHz
ε	0.5%

A. Case 1: Normal Operation of MMCs in Inverter Mode

In this case, the MMC works normally without fault. Here, the MMC works in inverter mode. Fig. 12 shows the capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A. Fig. 13 shows the IFOs and fault flag of proposed method in a short time [1.2s, 1.2201s]. In Fig. 13, the Flag is always 0, and no false alarmed. It need be noted that the length of each square represents the time of an IF, which is nearly different from others.

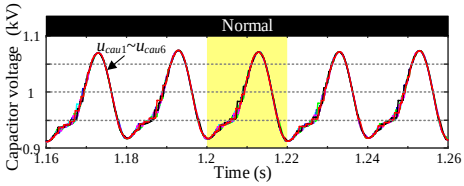


Fig. 12. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

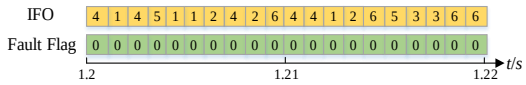


Fig. 13. IFO and fault flag.

B. Case 2: T_1 Open-Circuit Fault of MMCs in Inverter Mode

In this case, the T_1 open-circuit fault of SM1 occurs at 1.2 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 14 shows the capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A. Fig. 15 shows the IFOs and fault flag in a short time [1.2s, 1.2179s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau6} and the Flag is 0, while u_{cau1} becomes anomaly since 1.2128 s. The IFO becomes 1 at 1.2128 s and lasts for 5.1 ms. As a result, the Flag becomes 1 at 1.2179 s and the faulty SM1 is localized at a cost of 17.9 ms.

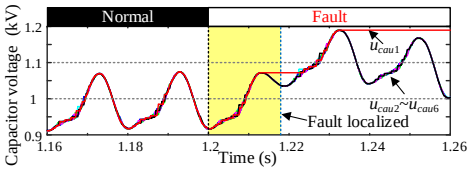


Fig. 14. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

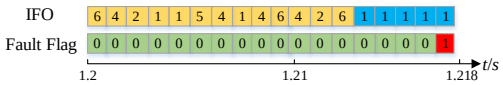


Fig. 15. IFO and fault flag.

C. Case 3: T_2 Open-Circuit Fault of MMCs in Inverter Mode

In this case, the T_2 open-circuit fault of SM1 occurs at 1.2 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 16 shows the capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A. Fig. 17 shows the IFOs and fault flag in a short time [1.185s, 1.2052s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau6} and the Flag is 0, while u_{cau1} becomes anomaly after fault. The IFO becomes 1 at 1.2004 s and lasts for 4.8 ms. As a result, the Flag becomes 1 at 1.2052 s and the faulty SM1 is localized at a cost of 5.2 ms.

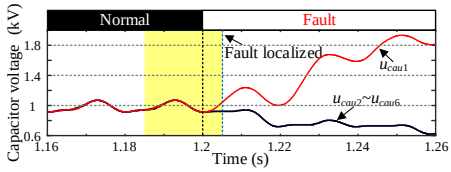


Fig. 16. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

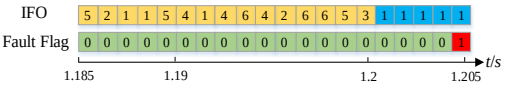


Fig. 17. IFO and fault flag.

D. Case 4: T_1 Open-Circuit Fault of MMCs in Rectifier Mode

In this case, the T_1 open-circuit fault of SM1 occurs at 1.21 s in upper arm of phase A, where the MMC works in rectifier mode. Fig. 18 shows the u_{cau1}~u_{cau6}. Fig. 19 shows the IFOs and fault flag in a short time [1.206s, 1.226s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau6}, and the Flag is 0. The u_{cau1} becomes anomaly since 1.221 s. The IFO becomes 1 at 1.2212 s and lasts for 4.8 ms. As a result, the Flag becomes 1 at 1.226 s and the faulty SM1 is localized at a cost of 16 ms.

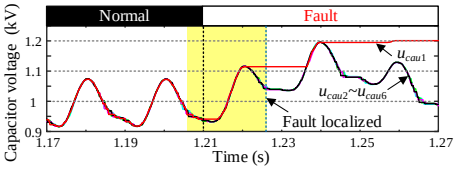


Fig. 18. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

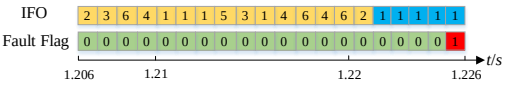


Fig. 19. IFO and fault flag.

E. Case 5: T_2 Open-Circuit Fault of MMCs in Rectifier Mode

In this case, the T_2 open-circuit fault of SM1 occurs at 1.21 s in upper arm of phase A, where the MMC works in rectifier mode. Fig. 20 shows the u_{cau1}~u_{cau6}. Fig. 21 shows the IFOs and fault flag in a short time [1.2s, 1.2181s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau6} and the Flag is 0, while u_{cau1} becomes anomaly since 1.213 s. The IFO becomes 1 at 1.2133 s and lasts for 4.8 ms. As a result, the Flag becomes 1 at 1.2181 s and the faulty SM1 is localized at a cost of 8.1 ms.

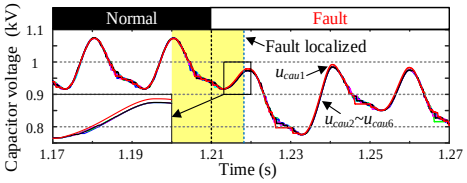


Fig. 20. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

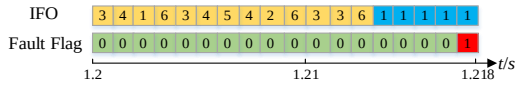


Fig. 21. IFO and fault flag.

F. Case 6: T_1 & T_2 Open-Circuit Faults of MMCs in Inverter Mode

In this case, both T_1 & T_2 open-circuit fault of SM1 occurs at 1.2 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 22 shows the capacitor voltages u_{cau1}~ u_{cau6} in the upper arm of phase A. Fig. 23 shows the IFOs and fault flag in a short time [1.185s, 1.2051s]. In the initial stage, the u_{cau1} is normal and close to u_{cau2}~ u_{cau6} and the Flag is 0, while u_{cau1} becomes anomaly since 1.2005 s. The IFO becomes 1 at 1.2005 s and lasts for 4.6 ms. As a result, the Flag becomes 1 at 1.2051 s and the faulty SM1 is localized at a cost of 5.1 ms.

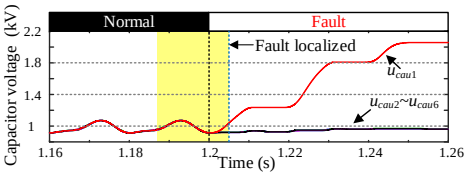


Fig. 22. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

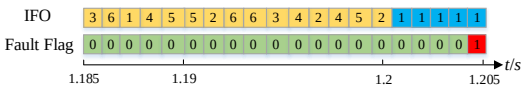


Fig. 23. IFO and fault flag.

G. Case 7: T_1 & T_1 Open-Circuit Faults in Two Different SMs of MMCs in Inverter Mode

In this case, the T_1 open-circuit fault of SM1 and T_1 open-circuit fault of SM2 occur at 1.213 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 24 shows the capacitor voltages u_{cau1}~u_{cau6} in upper arm of phase A. Fig. 25 shows the IFOs and fault flag in a short time [1.203s, 1.2227s]. In the initial stage, the u_{cau1}~ u_{cau2} are normal as u_{cau3}~ u_{cau6} and the Flag is 0, while u_{cau1}~ u_{cau2} become anomaly since 1.213 s. The IFO becomes 2 at 1.213 s and lasts for 4.9 ms. Then the IFO becomes 1 at 1.2179 s and lasts for 4.8 ms. As a result, the Flag becomes 1 at 1.2179 s and 1.2227 s, the faulty SM1 and SM2 are localized at a cost of 9.7 ms and 4.9 ms respectively.

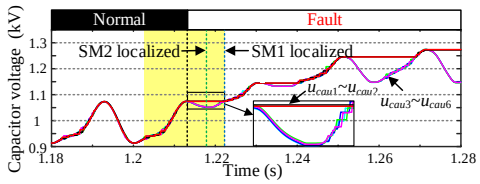


Fig. 24. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

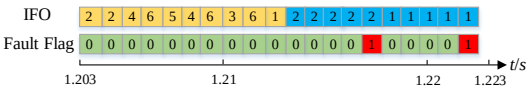


Fig. 25. IFO and fault flag.

H. Case 8: T_1 & T_2 Open-Circuit Faults in Two Different SMs of MMCs in Inverter Mode

In this case, the T_1 open-circuit fault of SM1 and T_2 open-circuit fault of SM2 occur at 1.21 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 26 shows the capacitor voltages u_{cau1}~ u_{cau6} in the upper arm of phase A. Fig. 27 shows the IFOs and fault flag in a short time [1.2s, 1.2195s]. In the initial stage, the u_{cau1}~ u_{cau2} are normal as u_{cau3}~ u_{cau6} and the Flag is 0, while u_{cau1}~ u_{cau2} become anomaly since 1.21 s. The IFO becomes 2 at 1.2101 s and lasts for 4.7 ms. Then the IFO becomes 1 at 1.2148 s and lasts for 4.7 ms. As a result, the Flag becomes 1 at 1.2148 s and 1.2195 s, the faulty SM1 and SM2 are localized at a cost of 9.5 ms and 4.8 ms respectively.

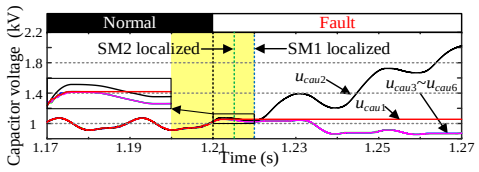


Fig. 26. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

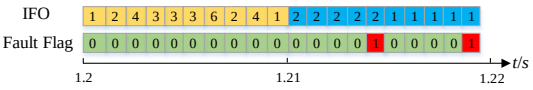


Fig. 27. IFO and fault flag.

I. Case 9: T_2 & T_2 Open-Circuit Faults in Two Different SMs of MMCs in Inverter Mode

In this case, the T_2 open-circuit fault of SM1 and T_2 open-circuit fault of SM2 occur at 1.2 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 28 shows the capacitor voltages u_{cau1}~ u_{cau6} in the upper arm of phase A. Fig. 29 shows the IFOs and fault flag in a short time [1.191s, 1.2106s]. In the initial stage, the u_{cau1}~ u_{cau2} are normal as u_{cau3}~ u_{cau6} and the Flag is 0, while u_{cau1}~ u_{cau2} become anomaly since 1.201 s. The IFO becomes 1 at 1.2012 s and lasts for 4.9 ms. Then the IFO becomes 2 at 1.2061 s and lasts for 4.5 ms. As a result, the Flag becomes 1 at 1.2061 s and 1.2106 s, the faulty SM1 and SM2 are localized at a cost of 6.1 ms and 10.6 ms, respectively.

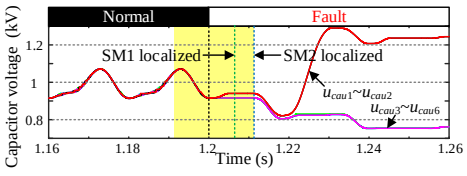


Fig. 28. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

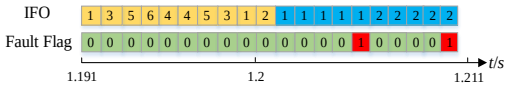


Fig. 29. IFO and fault flag.

J. Case 10: T_1 Open-Circuit Fault of MMCs in Inverter Mode under Capacitor Parameter Inaccuracy

In this case, the performance of the proposed method under capacitor parameter inaccuracy is considered, where C_{au2}=14 mF, C_{au3}=11 mF, the other capacitance are 12.5 mF. The T_1 open-circuit fault of SM1 occurs at 1.2 s in the upper arm of phase A, where the MMC works in inverter mode. Fig. 30 shows the capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A. Fig. 31 shows the IFOs and fault flag in a short time [1.2s, 1.2183s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau6} and the Flag is 0, while u_{cau1} becomes anomaly since 1.213 s. The IFO becomes 1 at 1.2134 s and lasts for 4.9 ms. As a result, the Flag becomes 1 at 1.2183 s and the faulty SM1 is localized at a cost of 18.3 ms. As can be seen, the inaccuracy of capacitor parameters almost has no effect on fault localization, which shows the robustness of the proposed method.

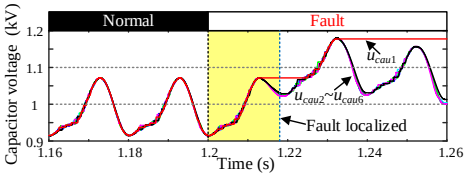


Fig. 30. Capacitor voltages u_{cau1}~u_{cau6} in the upper arm of phase A.

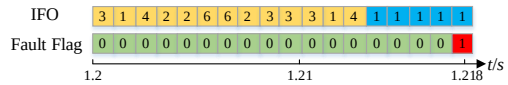


Fig. 31. IFO and fault flag.

VI. Experimental Studies

To verify the proposed method, a MMC prototype is built. The control is implemented in the digital signal processor (DSP), and the driver signal from the controller is transferred to each SM via optical fiber. The dc side of the MMC is connected to a dc source, and the ac side of the MMC is connected to the grid. The system parameters are shown in Table IX.

TABLE IX
Experimental System Parameters

Parameter	Value
Rated Power	1 kW
AC-side frequency f_g	50 Hz
DC-link voltage V_{dc}	200 V
Number of SMs per arm	4
SM capacitance C	2.35 mF
Arm inductance L_s	3 mH
Sampling frequency f_s	100 kHz

A. Case 1: Normal Operation of MMCs in Inverter Mode

In this case, the MMC works normally. Fig. 32 shows the capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A. Fig. 33 shows the IFO and fault flag of the proposed method in a short time period [1.5s, 1.52s]. In Fig. 33, the fault flag is always 0, and no SM would be false alarmed.

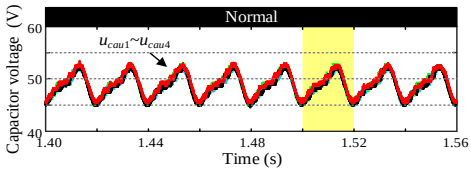


Fig. 32. Capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A.

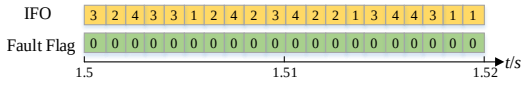


Fig. 33. IFO and fault flag.

B. Case 2: T_1 Open-Circuit Fault of MMCs in Inverter Mode

In this case, the T_1 open-circuit fault of SM1 occurs at 1.54 s in upper arm of phase A, where the MMC works in inverter mode. Fig. 34 shows the capacitor voltages u_{cau1}~u_{cau4}. Fig. 35 shows the IFOs and fault flag in the period [1.537s, 1.5564s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau4} and the Flag is 0, while u_{cau1} becomes anomaly after fault. The IFO becomes 1 at 1.5516 s and lasts for 4.8 ms. As a result, the Flag becomes 1 at 1.5564 s and the faulty SM1 is localized at a cost of 16.4 ms.

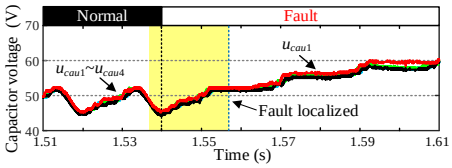


Fig. 34. Capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A.

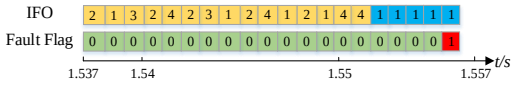


Fig. 35. IFO and fault flag.

C. Case 3: T_2 Open-Circuit Fault of MMCs in Inverter Mode

In this case, the T_2 open-circuit fault of SM1 occurs at 1.545 s in upper arm of phase A, where the MMC works in inverter mode. Fig. 36 shows the capacitor voltages u_{cau1}~u_{cau4}. Fig. 37 shows the IFOs and fault flag in the period [1.53s, 1.55s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau4} and the Flag is 0, while u_{cau1} becomes anomaly after fault. The IFO becomes 1 at 1.5452 s and lasts for 4.8 ms. As a result, the Flag becomes 1 at 1.55 s and the faulty SM1 is localized at a cost of 5 ms.

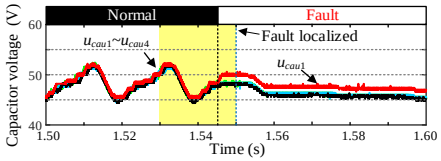


Fig. 36. Capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A.

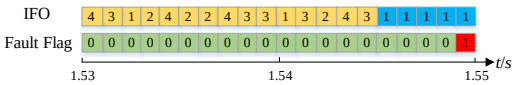


Fig. 37. IFO and fault flag.

D. Case 4: T_1 Open-Circuit Fault of MMCs in Rectifier Mode

In this case, the T_1 open-circuit fault of SM1 occurs at 1.53 s in upper arm of phase A, where the MMC works in rectifier mode. Fig. 38 shows the capacitor voltages u_{cau1}~u_{cau4}. Fig. 39

shows the IFOs and fault flag in the period [1.515s, 1.5348s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau4} and the Flag is 0, while u_{cau1} becomes anomaly after fault. The IFO becomes 1 at 1.5301 s and lasts for 4.7 ms. As a result, the Flag becomes 1 at 1.5348 s and the faulty SM1 is localized at a cost of 4.8 ms.

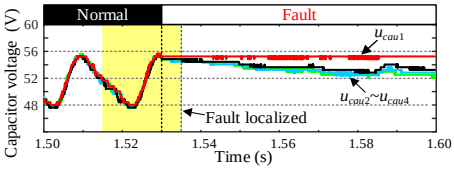


Fig. 38. Capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A.

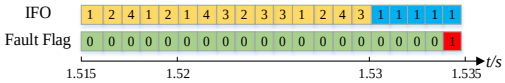


Fig. 39. IFO and fault flag.

E. Case 5: T_2 Open-Circuit Fault of MMCs in Rectifier Mode

In this case, the T_2 open-circuit fault of SM1 occurs at 1.54 s in upper arm of phase A, where the MMC works in rectifier mode. Fig. 40 shows the capacitor voltages u_{cau1}~u_{cau4}. Fig. 41 shows the IFOs and fault flag in the period [1.53s, 1.5478s]. In the initial stage, the u_{cau1} is normal as u_{cau2}~u_{cau4} and the Flag is 0, while u_{cau1} becomes anomaly after fault. The IFO becomes 1 at 1.5428 s and lasts for 5 ms. As a result, the Flag becomes 1 at 1.5478 s and the faulty SM1 is localized at a cost of 7.8 ms.

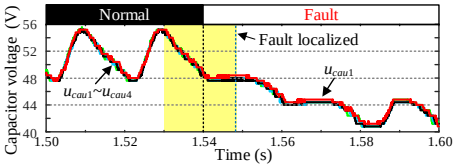


Fig. 40. Capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A.

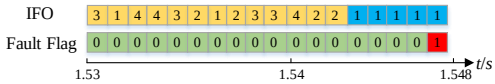


Fig. 41. IFO and fault flag.

F. Performance Evaluation under Various Power

Fig. 42(a) shows the fault localization time for the MMC in inverter mode, where the fault occurs at $\theta=\pi$ for arm current shown in Fig. 8. Fig. 42(b) shows the fault localization time for the MMC in rectifier mode, where the fault occurs at $\theta=0$ for arm current shown in Fig. 9. Here, the T_1 open-circuit fault of SM1 and T_2 open-circuit fault of SM1 in upper arm of phase A, respectively, are considered. In addition, various power of the MMC are considered including 1.0, 0.8, 0.6, 0.4 and 0.2 p.u. It shows that the power variation almost does not affect the fault localization time, where the T_1 fault can be localized at cost of 7 ms and T_2 fault can be localized at cost of 5 ms for the MMC in inverter mode; the T_1 fault can be localized at cost of 12 ms and T_2 fault can be localized at cost of 5 ms for the MMC in rectifier mode.

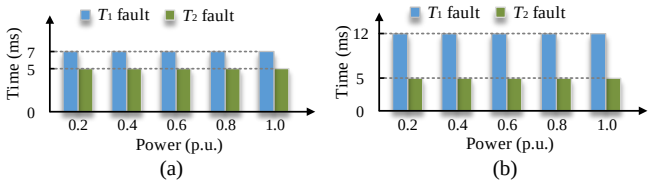


Fig. 42. Fault localization time under different power situations. (a) Inverter mode. (b) Rectifier mode.

G. Performance Evaluation of Proposed Method

For the MMC with four SMs per arm, the upper arm of phase A will have 8 kinds of fault situations and 1 fault-free situation, totally 9 situations. Moreover, 10 fault occurred positions with 2 ms as interval in a fundamental period and 3 different system power situations including 1.0, 0.6 and 0.2 p.u. are considered. Hence, 9×10×3=270 sets of experiment samples are obtained.

Based on the calculation of the proposed method with above samples, the 2×2 confusion matrix is obtained, as shown in Table X. Then, true positive rate (TPR) and false positive rate (FPR) can be calculated based on (12)-(13).

$$TPR = \frac{TP}{TP + FN} \tag{12}$$

$$FPR = \frac{FP}{FP + TN} \tag{13}$$

TABLE X
Confusion Matrix for MMCs in experiment

Actual / Predict	1	0
1	TP=240	FP=1
0	FN=0	TN=29

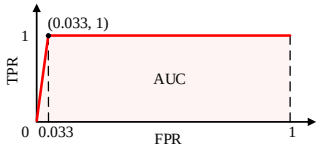


Fig. 43. ROC curve for the MMC in the experiment.

According to Table X and (12)-(13), TPR and FPR can be calculated as 1 and 0.033, respectively, and then the receiver operating characteristic (ROC) curve is obtained, as shown in Fig. 43. The area under curve (AUC) is an evaluation index for the ability of the proposed method to correctly classify 0 (health) and 1 (fault), where the closer of the AUC is to 1, the better the fault diagnosis effect. In Fig. 43, the AUC is calculated as 0.9835, which shows that the proposed method performances well for fault localization in MMCs.

VII. Conclusions

This paper proposes an IF based SM switch open-circuit fault localization method for MMCs. A number of ITs are produced to construct the IFs for MMCs based on SM capacitor voltages, and the faulty SM can be accurately localized through IFs' outputs. The proposed IF based fault localization method constructs concise low-data-volume tree models only depend on SM capacitor voltages, and uses sparsity and difference properties of outlier data to localize faulty SM. The proposed method has linear time complexity

with low calculation complexity. In addition, it does not require detailed mathematical models of MMCs and manual setting of empirical thresholds. The simulation studies and experimental studies are conducted to show the effectiveness of the proposed method.

REFERENCES

[1] C. Liu et al., "An Isolated Modular Multilevel Converter (I-M2C) Topology Based on High-Frequency Link (HFL) Concept," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1576-1588, Feb. 2020.

[2] C. Liu et al., "Crossing Thyristor Branches-Based Hybrid Modular Multilevel Converters for DC Line Faults," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9719-9730, Oct. 2021.

[3] F. Deng et al., "Capacitor ESR and C Monitoring in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4063-4075, April 2020.

[4] F. Deng, Y. Tian, R. Zhu and Z. Chen, "Fault-Tolerant Approach for Modular Multilevel Converters Under Submodule Faults," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7253-7263, Nov. 2016.

[5] J. Wang, H. Ma and Z. Bai, "A Submodule Fault Ride-Through Strategy for Modular Multilevel Converters With Nearest Level Modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1597-1608, Feb. 2018.

[6] R. Picas, J. Zaragoza, J. Pou and S. Ceballos, "Reliable Modular multilevel converter fault detection with redundant voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 39–51, Jan. 2017.

[7] F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault detection and localization method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721-2732, 2015.

[8] S. Shao, A. J. Watson, J. C. Clare and P. W. Wheeler, "Robustness Analysis and Experimental Validation of a Fault Detection and Isolation Method for the Modular Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3794-3805, May 2016.

[9] S. Shao, P. W. Wheeler, J. C. Clare and A. J. Watson, "Fault Detection for Modular Multilevel Converters Based on Sliding Mode Observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867-4872, Nov. 2013.

[10] W. Zhou, J. Sheng, H. Luo, W. Li and X. He, "Detection and Localization of Submodule Open-Circuit Failures for Modular Multilevel Converters With Single Ring Theorem," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3729-3739, April 2019.

[11] B. Li et al., "Fault Diagnosis and Tolerant Control of Single IGBT Open-Circuit Failure in Modular Multilevel Converters," *IEEE Trans. Power Electron*., vol. 31, no. 4, pp. 3165-3176, Apr. 2016.

[12] C. Liu et al., "Fault Localization Strategy for Modular Multilevel Converters Under Submodule Lower Switch Open-Circuit Fault," *IEEE Trans. Power Electron*., vol. 35, no. 5, pp. 5190-5204, May 2020.

[13] X. Chen et al., "A Diagnosis Strategy for Multiple IGBT Open-Circuit Faults of Modular Multilevel Converters," *IEEE Trans. Power Electron*., vol. 36, no. 1, pp. 191-203, Jan. 2021.

[14] F. Deng, M. Jin, C. Liu, M. Liserre and W. Chen, "Switch Open-Circuit Fault Localization Strategy for MMCs Using Sliding-Time Window Based Features Extraction Algorithm," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 10193-10206, Oct. 2021.

[15] S. Kiranyaz, A. Gastli, L. Ben-Brahim, N. Al-Emadi and M. Gabbouj, "Real-Time Fault Detection and Identification for MMC Using 1-D Convolutional Neural Networks," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8760-8771, Nov. 2019.

[16] D. Zhou, H. Qiu, S. Yang and Y. Tang, "Submodule Voltage Similarity-Based Open-Circuit Fault Diagnosis for Modular Multilevel Converters," *IEEE Trans Power Electron.*, vol. 34, no. 8, pp. 8008-8016, Aug. 2019.

[17] Q. Yang, J. Qin and M. Saeedifard, "Analysis, Detection, and Location of Open-Switch Submodule Failures in a Modular Multilevel Converter," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 155-164, Feb. 2016.

[18] F. Deng et al., "Power Losses Control for Modular Multilevel Converters Under Capacitor Deterioration," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4318-4332, Dec. 2020.

[19] F. Deng et al., "A Currentless Submodule Individual Voltage Balancing Control for Modular Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9370-9382, Nov. 2020.

[20] F. Deng, Y. Lü, C. Liu, Q. Heng, Q. Yu and J. Zhao, "Overview on submodule topologies, modeling, modulation, control schemes, fault diagnosis, and tolerant control strategies of modular multilevel converters," *Chin. J. Elect. Eng.*, vol. 6, no. 1, pp. 1-21, March 2020.

[21] F. T. Liu, K. M. Ting and Z. Zhou, "Isolation Forest," *2008 Eighth IEEE International Conference on Data Mining*, 2008, pp. 413-422.

[22] F. T. Liu et al., "Isolation-based anomaly detection,"*ACM Trans. Knowl. Discov. Data*, vol. 6, no. 1, pp. 3-1–3-39, Mar. 2012.

[23] C. C. Aggarwal, ''Isolation Forests,'' in *Outlier Analysis*, 2nd ed. New York, Ny, USA: Springer Nature, 2017, pp. 161–164.

[24] M. Ohsaki, P. Wang, K. Matsuda, S. Katagiri, H. Watanabe and A. Ralescu, "Confusion-Matrix-Based Kernel Logistic Regression for Imbalanced Data Classification," *IEEE Trans. Knowl. Data Eng*., vol. 29, no. 9, pp. 1806-1819, 1 Sept. 2017.

Fujin Deng (SM'19) received the B. Eng. degree in Electrical Engineering from China University of Mining and Technology, Jiangsu, China, in 2005, the M. Sc. Degree in Electrical Engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph. D. degree in Energy Technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012.

He joined the Southeast University in 2017 as a Professor in the School of Electrical Engineering, Southeast University, Nanjing, China. From 2013 to 2015 and from 2015 to 2017, he was a Postdoctoral Researcher and an Assistant Professor, respectively, in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His main research interests include wind power generation, multilevel converters, high-voltage direct-current technology, DC grid and offshore wind farm-power systems dynamics.

Yufei Chen was born in Zhejiang, China, in 1996. He received the B. Eng. degree in Electrical Engineering from Electrical Engineering College of Chongqing University, Chongqing, China, in 2019. And he is currently working toward the master degree in Electrical Engineering with Southeast University, Nanjing, China.

His main research interests include multilevel converters and artificial intelligence.

Jingming Dou was born in Hebei, China, in 1993. She received the B.Eng. and the M.Sc. degrees in electrical engineering from the Xi'an Jiaotong University, China, in 2014 and 2017, respectively. Currently, she is an engineer in China Electric Power Research Institute.

Her research interests include relay protection and power systems.

Chengkai Liu was born in Fujian, China, in 1996. He received the B. Eng. degree in Electrical Engineering from Chien-Shiung WU College of Southeast University, Nanjing, China, in 2018. Then, he works toward the Ph.D. degree with the School of Electrical Engineering, Southeast University. Currently, he is a Guest Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark.

His main research interests include multilevel converters and dc grids.

Zhe Chen (M'95-SM'98) received the B.Eng. and M.Sc. degrees all in Electrical Engineering from Northeast China Institute of Electric Power Engineering, Jilin City, China, MPhil in Power Electronic, from Staffordshire University, England and the Ph.D. degree in Power and Control, from University of Durham, England.

Dr Chen is a full Professor with the Department of Energy Technology, Aalborg University, Denmark. He is the leader of Wind Power System Research program at the Department of Energy Technology, Aalborg University and the Danish Principle Investigator for Wind Energy of Sino-Danish Centre for Education and Research.

His research areas are power systems, power electronics and electric machines; and his main current research interests are wind energy and modern power systems. He has led many research projects and has more than 400 technical publications with more than 10000 citations and h-index of 44 (Google Scholar).

Dr Chen is an Associate Editor of the IEEE Transactions on Power Electronics, a Fellow of the Institution of Engineering and Technology (London, U.K.), and a Chartered Engineer in the U.K.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.

He is nominated in 2014-2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.