Impact of Short-Circuit Events on the Remaining Useful Life of SiC MOSFETs and Mitigation Strategy

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BY
HE DU

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Impact of Short-Circuit Events on the Remaining Useful Life of SiC MOSFETs and Mitigation Strategy

By

He Du

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"Real generosity toward the future lies in giving all to the present."
Albert Camus

Preface

This Ph.D. thesis is a summary of the Ph.D. project "Impact of Short-Circuit Events on the Remaining Useful Life of SiC MOSFETs and Mitigation Strategy" conducted in Center of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Denmark.

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Abstract

Power semiconductor devices are critical components in power electronic systems. Thanks to the unprecedented performance compared with silicon-based devices, silicon carbide (SiC) devices are desirable for high-efficiency and high-power-density power converters. However, the proliferating demand for SiC MOSFETs raises concerns for long-term reliability and short circuit is one of the critical aspects as the devices withstand both high voltage and high current at the same time.

With the development of faster fault detection and short-circuit protection, the risk of catastrophic failure can be reduced, which allows the device to withstand many non-destructive short-circuit events during its life. Typically, the remaining useful life (RUL) of the devices can be estimated based on the condition monitoring parameters, i.e. the ageing indicators and it only considers the wear-out failures under normal operating conditions. Therefore, this Ph.D. thesis aims at investigating the impact of short-circuit events on the RUL of SiC MOSFETs.

The thesis starts with an analysis of the degradation indicators under short-circuit conditions to identify the one which can best reflect the short-circuit degradation process and two test approaches were performed. Then, static and dynamic characteristics measurements were performed during repetitive short-circuit tests, respectively and the purpose is to investigate the impact of short-circuit degradation on the normal operating performance of SiC MOSFETs. As the case temperature is subjected to real application conditions, its influence is also considered by performing the repetitive short-circuit tests at different case temperatures.

Thereafter, power cycling tests were used to evaluate the wear-out ageing and lifetime of the devices. Mixed power-cycling/short-circuit tests were performed to assess the impact of short-circuit degradation on the power-cycling conditions, and further on, the RUL by applying different short-circuit stress. To deeply analyse the degradation mechanisms, failure analysis tools (lock-in thermography, focused ion beam, and scanning electron microscope) were used on both failed and functional device. Besides, a transient thermo-mechanical simulation based on finite-element-analysis software was achieved to verify the degradation mechanisms. Finally, a mitigation strategy comprising a top-side thermal mass is studied.

The main contribution of this thesis is the strong implication of short-circuit events on the RUL of SiC MOSFETs. With a larger number of events, the higher gate leakage current results in higher junction temperature swing and less number of cycles to failure. The root cause of gate leakage current is the mismatch of coefficient of thermal expansion between Al and SiO_2, which forms the SiO_2 interlayer crack, and the molten Al flowing through the crack, which builds a conductive path between gate- and source terminals. Moreover, sintered Cu foil on the top side could be an effective approach to mitigate this short-circuit degradation.

Dansk Résumé

Effektelektronikke enheder er vigtige komponenter i kraftelektroniske systemer. På grund af den hidtil usete ydeevne sammenlignet med silicium-baserede enheder er siliciumcarbid (SiC) enheder højt ønsket til mere effektive og effekttæthed omformere. Imidlertid rejser den voksende demand efter SiC MOSFET bekymringer over langsigtet pålidelighed, og kortslutning er et af de kritiske aspekter, da enhederne samtidigt modstår både høj spænding og strøm.

Med udviklingen af hurtigere fejldetektion og kortslutningsbeskyttelse, kan risikoen for katastrofale fejl reduceres, hvilket gør det muligt for enheden at modstå mange ikke-destruktive kortslutningshændelser i sin levetid. Typisk kan den resterende livstid (remaining useful life, RUL) estimeres baseret på condition monitoring parametre, dvs. aldringsindikatorer, men denne inkluderer kun slitage under almindelig driftsforhold.

Denne ph.d. afhandling er målrettet mod at undersøge påvirkningen af kortslutningshændelser på RUL af SiC MOSFETs. Afhandlingen starter med en analyse af nedbrydnings indikatorer under kortslutnings forhold for at kunne identificere hvilke ene ud af alle, der bedst kan monitorere kortslutnings-nedbrydningsprocessen. Her er to test fremgangsmåder udført. Derefter blev der målinger udført af statiske og dynamiske egenskaber under gentagende kortslutningstest målrettet at undersøge påvirkningen af kortslutnings nedbrydnings processen på SiC MOSFETs normale driftsydeevne. Da skal udsættes for reelle applikationsbetingelser, er indflydelsen af temperaturen også overvejet ved at udføre gentagende kortslutnings tests ved forskellige temperature af enhedscase.

Derefter blev der udført power cycling tests, for at vurdere slitage og enhedernes resterende livtid. Blandet power-cycling- og kortslutningstests var udført også, for at anslå indvirkningen af kortslutningsnedbrydning på power cycling, og relateret RUL ved at give forskellige kortslutnings stress. For ordentligt at kunne analysere nedbrydnings mekanismer, er fejlanalyse værktøjer (lock-in-termografi, fokuseret ionstråle og scanning-elektronmikroskop) brugt på både nedbrudte- og virkende enheder. Derudover, blev der udført en forbigående termo-mekanisk simulation med finite-element software, for at validere nedbrydningsmekanismerne. Endeligt, er en afbødende strategi foreslået, der omfatter en termisk masse på chip toppen.

Hovedbidraget for denne afhandling er studien af de implikationer af kortslutningshændelser på RUL af SiC MOSFETs. Med stigende antal hændelser, vil den større og større lækstrøm fra gaten resultere i større og større temperatursvingninger og mindre og mindre antal cykler til fejl. Årsagen for gate lækstrøm er mismatchet af koefficienterne for termisk ekspansion mellem Al og SiO2. Dette former mellemlags revner i SiO2, hvor aluminum kan smeltes og flyde gennem revnerne og opbygge en ledende sti mellem gate- og source terminaler. Til sidst, der foreslås at en sinteret Cu-folie på chip toppen kan være en effektiv tilgang til at afbøde kortslutningsnedbrydning.

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Chapter 1

Introduction

This chapter presents the background and motivation of this thesis, followed by the scientific questions, thesis objectives, and limitations. The outline of the thesis is provided, along with a list of publications at the end.

1.1 Background

With the proliferation demand for electric vehicles and renewable energy systems, power electronic technology with the function of power conversion and energy process plays a more and more critical role [1]. The expected production of electric vehicles in Europe may grow to more than 4 million units in the next five years [2] and the total installed capacity of wind power in Europe will be more than 256 gigawatts by 2023 [3].

Modern power electronic systems mainly include three kinds of components: active components (i.e. the power semiconductor devices), passive components (e.g. transformers, capacitors, and inductors), and control units. Among these, power semiconductor devices are the key components to turn on or turn off the current flow. To meet the increasing requirements toward high efficiency, high power density, and highly-integrated systems, especially for the electric vehicle applications, power semiconductor devices need to have lower and lower power loss, higher switching speed, and blocking voltage capability [4].

Power electronic circuits mainly consist of active switches and diodes, where silicon (Si) is the dominant material. Typical active switches are metal-oxide-semiconductor field-effect transistors (MOSFET) and insulated gate bipolar transistor (IGBT). Among these, the former is a unipolar device, whereas the other one is a bipolar device, which uses majority as well as minority carriers (i.e. electrons and holes) at the same time.

Due to the absence of minority carriers, Si-based power MOSFETs have inherently fast switching capability and low switching losses. However, the blocking voltage capability is related to the thickness and doping concentration of the drift region. To enable a greater blocking voltage capability, its on-state resistance and conduction losses will increase. This factor results in a limited on-state current in high-voltage applications. Therefore, it is usually the choice for low operating voltage applications (below 600 V).

For bipolar devices, when the devices are in the on-state, minority carriers are injected into the high-resistance drift region, which causes a reduction in the resistivity. Thanks to this so-call conductivity modulation, they exhibit the advantages of high-current capability with low on-state resistance in high-voltage applications (from 600 V to 6.5 kV). Nevertheless, the switching frequency is limited.

Despite these advancements, the performance of Si-based power devices is now approaching the fundamental material limits for some high-power,

high-switching-frequency, and high-temperature applications. The maximum rating voltage of commercial Si-based IGBTs is 6.5 kV with a relatively slow switching speed and its practical operating temperature lower than 175 ºC, which doesn't meet the requirement for industrial and automotive applications [5]. The aforementioned factors also hinder the efficiency improvement of the power converters and result in bulky cooling systems at the same time. Although future development in Si-based power devices will not stop, the introduction of wide-bandgap materials brings a significant revolution to the power electronics technology and market. As a wide bandgap material, silicon carbide (SiC) has become a hot topic of interest and been the focus of many studies over the last two decades [6].

1.1.1 Silicon Carbide: From Material to Devices

SiC material exists in more than 250 different crystalline structures (i.e. polytypes) depending on the different stacking ways of identical two-dimensional layers, such as 3C-SiC, 4H-SiC, and 6H-SiC [7]. At present, 4H-SiC polytype is generally favoured by power device manufacturers for its wider bandgap, less ionization energy and higher carrier mobility [8] [9]. A comparison of physical properties between Si and 4H-SiC material with 10^{16} cm^{-3} doping density at room temperature is listed in Table 1.1[10] [11].

Since the critical electric field strength of 4H-SiC is significantly higher than that of Si, SiC devices can be made with much thinner drift layer and higher doping concentrations. Compared to Si, SiC devices such as MOSFETs can have very high blocking voltage capability and very low on-state resistance at the same time. In this case, the lower on-state resistance makes it possible to have a smaller chip size, resulting in lower parasitic capacitance and faster switching speed.

The switching speed of power devices is also related to the saturated drift velocity. With the influence of the high electric field, the drift velocity of carriers is no longer proportional to the electric field strength and it gradually becomes saturated due to the scattering phenomenon. During the turn-off transient, carriers are swept out of the

TABLE 1.1 - PHYSICAL PROPERTIES OF SI AND 4H-SIC [10] [11]

Material	Si	4H-SiC
Energy Bandgap (eV)	1.12	3.26
Electron Mobility ($cm^2/V{\cdot}s$)	1200	850
Hole Mobility ($cm^2/V{\cdot}s$)	420	115
Electron Saturated Drift Velocity (10^7 cm/s)	1	2.2
Critical Electric Field Strength (10^6 V/cm)	0.4	2.5
Relative Dielectric Constant	11.8	9.8
Thermal Conductivity (W/cm·K)	1.4 - 1.5	3.3 - 4.9
Melting Point (K)	1690	~3100
Young's Modulus (GPa)	160	390 - 690
Fracture Strength (GPa)	7	21

depletion region at the saturated drift velocity [12]. Since the saturated drift velocity of 4H-SiC is twice the value of Si, SiC devices reach higher switching speeds.

The much wider bandgap of 4H-SiC means that it can operate at extremely high temperatures beyond 600 ºC without suffering from intrinsic conduction effects. On the other hand, it has approximately three times higher thermal conductivity compared to Si material; this property enables to dissipate a larger amount of generated heat, which opens for applications requiring high cooling temperatures. Presently, the operating temperature of SiC devices remains from 150 ºC to 200 ºC due to the issues related to oxide quality [8] [13]. It is believed to operate at the temperature higher than 200 ºC with coming improvements [14].

All of the advantages mentioned above make SiC devices a most attractive candidate for high-power, fast-switching, and high-temperature power electronics applications. However, the cost still hinders their extensive diffusion into the market and a large proportion of the cost is from the 4H-SiC substrate. Nowadays, the physical vapor transport (PVT), also known as modified Lely method, is typically used for 4H-SiC crystal growth. The stability of different SiC polytypes is shown in Fig. 1.1 as a function of temperature and 4H-SiC growth only remains stable in the harsh temperature range, mainly from 1800 ºC to 2600 ºC [15]. Although the growth rate depends on many parameters (e.g. pressure and temperature), it is in the range of 0.2 – 2 mm/h, which is much lower than the value for Si crystal pulling [16]. Besides, a high-quality SiC crystal with a large diameter still faces challenges due to crystallographic defects such as stacking faults and threading dislocations.

With the improvement of SiC wafer quality and process technology, the SiC devices' market is booming. Some significant SiC development milestones have been reported in [17] and they are shown in Fig. 1.2 together with latest achievements.

Since Infineon launched the first commercial SiC Schottky diode in 2001, the SiC diodes have shown a continuous increase in the blocking voltage and conduction current rate. There are mainly three types of SiC diodes: Schottky barrier diode (SBD), junction barrier Schottky (JBS) diode, and PiN diode. With a combination of Schottky diode structure and SiC material, the SBDs show fast switching behaviour and no reverse recovery current thanks to the majority carrier conduction. However, as a result of

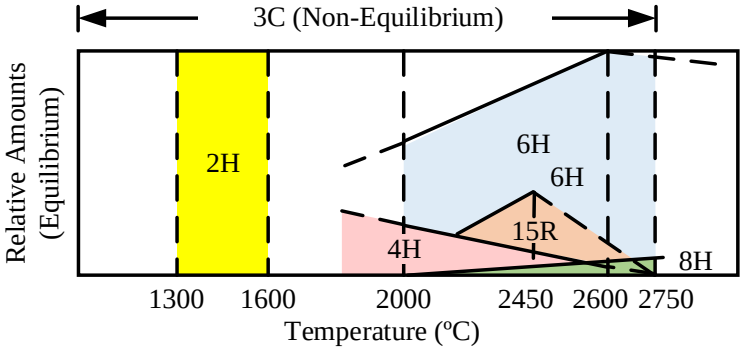


Fig. 1.1. Stability diagram of SiC polytypes [15].

Schottky barrier lowering effect, the leakage current of the SBDs increases fast at high temperatures, which limits its available blocking voltage. Benefiting from the effect of the P+ region, the JBS diodes keep lower leakage current even at high temperature. At present, most commercial SiC diodes in the market are JBS structures in the range from 600 V to 1.7 kV. Some 3.3 kV devices are also available in the market, but with lower current rating due to the thick drift layer. Besides, a 15 kV JBS diode has been designed for high-frequency application [18] and a trench structure has been proposed in [19]. As for the SiC PiN diode, it has much lower leakage current and its drift resistance is reduced with conductivity modulation, which makes it a possible candidate for high-temperature operations and ultra-high voltage ratings (such as 10 - 20 kV) [20]. On the other hand, the influence of minority carrier causes the disadvantage of a non-zero reverse recovery effect.

Regarding SiC active switches, the SiC junction field effect transistors (JFETs) became the focus at the early stage of development as can be seen in Fig. 1.2. Nevertheless, the JFET is inherently a normally-on device, which limits its usage in power electronic circuits. Normally-off trench JFETs have been proposed thanks to a higher built-in voltage of their P-N junctions, but the high channel resistance and low threshold voltage still needed to be improved [21]. Thanks to the double-side high-level injection and no channel region, the SiC BJT has the advantages of lower on-resistance, which enables high current ratings. However, it requires a large control current through the base-emitter junction, which causes a substantial power loss due to the built-in potential. Several high-voltage SiC IGBTs have also been developed over the past decade, showing much higher voltage ratings than their Si counterparts. Due to the much higher mobility of electrons than holes, the N-type SiC IGBTs have a faster switching speed than the

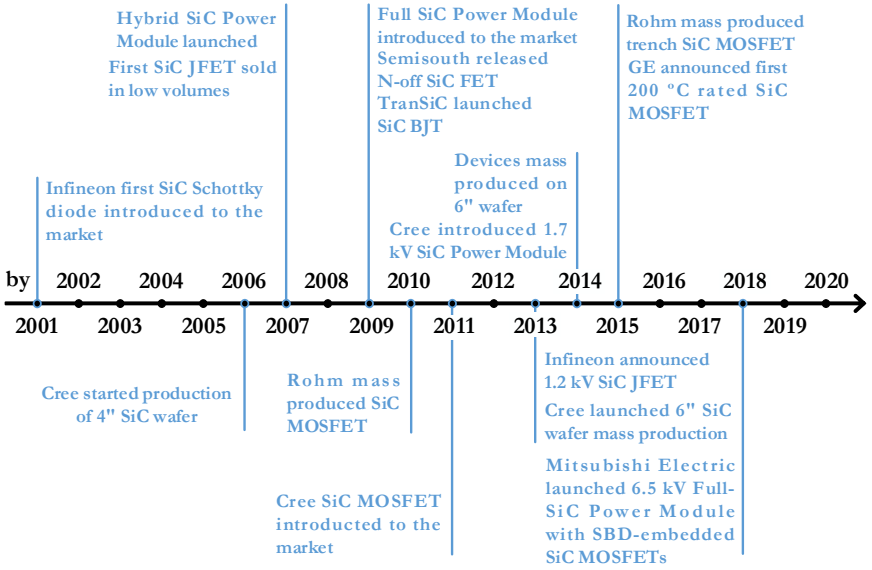


Fig. 1.2. SiC devices' development milestones [17].

P-type ones. However, the P+ substrate shows high resistivity and defect density, which impedes the development of the N-type IGBT until the free-standing technology proposed in 2010 [22] [23]. At present, the N-type and P-type SiC IGBT have reached 27 kV and 15 kV blocking voltage, respectively [24] [25]. In addition, the gate turn-off thyristor (GTO) and the emitter turn-off thyristor (ETO) based on SiC are also promising devices for high voltage applications [26] [27].

Among SiC switches, SiC power MOSFET is well suited for the voltage rating requirement from 600 V to 3.3 kV, especially the 1.2 kV – 1.7 kV range. Some high-voltage SiC MOSFETs have also been designed from 3.3 kV to 15 kV [28] [29] [30]. Compared to the Si IGBT, it has a lower switching loss because of majority carrier conduction mechanism. Besides, benefiting from SiC material, it shows a lower conduction loss than Si MOSFET. Apart from these, the body diode of SiC MOSFET is a P-N junction diode with short minority carrier lifetime and its recovery performance is similar to the one of SiC SBD, which enables an extremely low recovery loss [8]. However, bipolar degradation may occur when current flows through the body diode [31]. In this case, there remains a need to use external anti-parallel SiC SBD to suppress current flowing through the body diode. Since the chip size of an SBD could be larger for the higher blocking voltage, Mitsubishi Electric first launched the 6.5 kV full-SiC power module with SBD-embedded SiC MOSFETs in 2018 [32] [33].

Owing to the higher mobility of electrons in respect to holes, the SiC MOSFET is typically designed with N-channel. Nowadays, there are mainly two types of SiC MOSFET structures, named as planar and trench technology and Fig. 1.3 shows their typical cell structures.

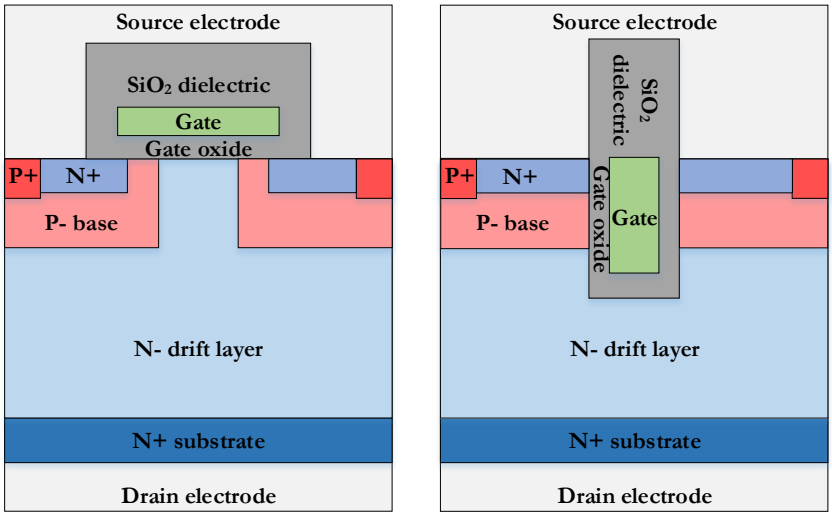


Fig. 1.3. Typical SiC MOSFET cell structures: (a) planar type; (b) trench type.

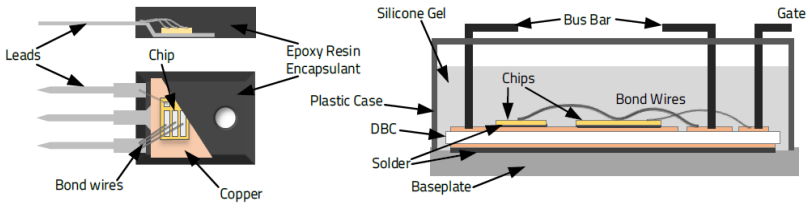
Rohm and Cree first launched the commercial SiC MOSFET in 2010 and 2011, respectively. General Electric (GE) released a SiC MOSFET with 200 °C junction temperature in 2014 [34]. In 2015, Rohm first mass-produced trench-type SiC MOSFET.

Based on the conduction current path, the on-state resistance of planar SiC MOSFET mainly consists of channel resistance, JFET region resistance, drift resistance and substrate resistance. In trench- MOSFETs, by eliminating the JFET region, the current density in the trench cell improves, which enables lower on-state resistance.

To ensure chip operation and meet application requirements, a suitable package is needed, which typically concerns three aspects: good thermal conductivity to dissipate the heat losses to an external cooling system; compact layout to achieve low parasitics (especially for high switching frequency applications); good protection against environmental influences (such as electrical insulations). In general, the package type depends on the power range of the chips. Nowadays, there are two conventional package types for SiC MOSFET chips, namely discrete devices and power modules, which mainly continue to use previous packaging technology for Si chips.

Discrete packages are generally used in the range of small power below 1.7 kV blocking voltage and 120 A rating current. A common through-hole design of this package in the market is transistor outline (TO) package. Fig. 1.4 (a) presents a single-chip discrete device with TO-247 (3-pin) package [35]. The drain of the SiC MOSFET chip is soldered on a lead frame, which is connected to the middle lead. The source and gate pads of the SiC MOSFET chip are connected to the other two leads through metal (such as Al and Cu) bond wires. For the purpose of protection and insulation, it is encapsulated with transfer mould compound such as epoxy resin. The backside of the device is normally metal and electrically-connected to the drain. The hole enables to mount the device on a heat sink, which allows dissipating more heat.

Power module, on the other hand, can provide a higher heat dissipation capability and make it possible multi-chip electrical connection internally, such as half-bridge and three-phase circuits, etc. Fig. 1.4 (b) exhibits a classical structure cross-section of the power module [35]. The drain of the SiC MOSFET chips is soldered on the direct bonded copper (DBC) substrate by means of a solder layer, which has an insulated ceramic substrate sandwiched with two copper layers and the multiple chips electrical connection are archived through the copper tracks and the bond wires. The backside of the DBC



(a) (b)

Fig. 1.4. Conventional SiC MOSFET package structures: (a) discrete device with TO-247-3 package; (b) power module [35].

substrate is also soldered on a base plate, which can be mounted on a cooling system with a thermal grease, such as a heat sink and provides mechanical support at the same time. To ensure the chips insulation and prevent environmental contamination/vibration, the silicone gel is poured into the module case and only the terminals, which connect to the copper tracks, are kept outside of it for power and control.

Apart from these, some advanced packaging structures for SiC MOSFET power modules have been investigated to meet the specific requirement for high switching frequency and high-temperature operations. Due to the influence of fast switching speed (dV/dt and di/dt), the parasitic properties need to be minimized and thereby, various wireless and novel structures have been proposed, such as flexible printed circuit board (PCB) with Ag sintering [36], press-pack structure [37] and chip-on-chip structure [38]. On the other hand, as SiC devices provide the potential to achieve operating temperature higher than 200 ºC, new packaging materials and techniques are drawing more and more attention [14] [39].

With the superior SiC material properties, improved chip design and packaging technology mentioned above, SiC devices are believed to play an important role for many specific power electronic applications. According to the report from Yole, the SiC devices market's value is expected to approach two billion USD by 2024 [40]. However, at the same time, the reliability and robustness challenges rise to the surface.

1.1.2 Reliability Challenges: Normal and Abnormal Conditions

To meet the long-term operation requirement and reduce the cost, the reliability prediction of Si-based power electronic system have been investigated extensively in the past, mainly from two aspects: the design for reliability and remaining useful life (RUL) prediction. However, due to the implementation of the SiC MOSFETs and its promising capability for high power density and harsh applications, the reliability and lifetime model of SiC MOSFETs itself needs to be investigated at first.

Failures can be divided into three categories: early failures, catastrophic failures, and ageing failures as listed in Table 1.2. Most early failures come from the defects and quality issues from the manufacturing process and supply chain. Catastrophic failures, in most case, are induced by abnormal events, which means that the SiC MOSFET exceeds its nominal conditions (i.e. safe operating area) for a short period and there are various types of abnormal events, such as overvoltage, overcurrent, short circuit, unclamped inductive switching (UIS), over-temperature. According to different root causes, catastrophic failures can also be divided into two subgroups, i.e. severe overstress and instabilities.

TABLE 1.2 - COMMON FAILURES AND ROOT CAUSES OF POWER DEVICES

Failures	Root Causes	
Early Failures	Manufacturing Defects	
Catastrophic Failures	Severe Overstress	(Abnormal Conditions)
	Instabilities	
Ageing Failures	Wear Out	(Normal Conditions)

The former is directly related to external conditions (e.g. system level) with higher stress than nominal value, whereas the latter is characterized by a loss of control internally (device level), leading to destruction. Despite instabilities can also be triggered by external conditions, they are strongly related to the chip technology, manufacturing process, and wire bonding quality [41]. As a result of wear-out under normal operating conditions, ageing failures typically take years to occur and a degradation process prior to failure can be observed.

From the perspective of device structures, failure modes of SiC MOSFETs can be classified into chip-level and package-level failure modes. Gate oxide and body diode are two common failure locations at the chip level. Due to increased scattering at the oxide/semiconductor interface, the electrons mobility in the inversion layer is lower than that in the bulk semiconductor. In SiC MOSFETs, the inversion layer mobility is only 5-10% of the bulk mobility, and this proportion is much lower than the one in Si MOSFETs, which is around 50% [10]. This factor results in larger channel resistance in SiC MOSFETs. In order to reduce channel resistance, a relatively low gate threshold voltage (V_{th}) is desired. However, as can be seen in Fig. 1.5, if the P-base doping concentration (N_A) is 1×10^{17} cm^{-3} and the gate oxide thickness is 0.1 μm, its V_{th} will reach as high as 11 V [42]. Thus, the gate oxide thickness tends to be thinner than Si MOSFETs and this raises reliability issues. Typically, the gate oxide thickness for SiC MOSFETs is designed only about 50 nm. Reducing the spacing between P-base regions of planar SiC MOSFETs can be an approach to shield the gate oxide region from the high electric field under forward blocking condition, but meanwhile, it results in an increased on-state resistance since the drain current flow is limited by the narrower JFET region. Therefore, a trade-off between on-state resistance and gate oxide reliability needs

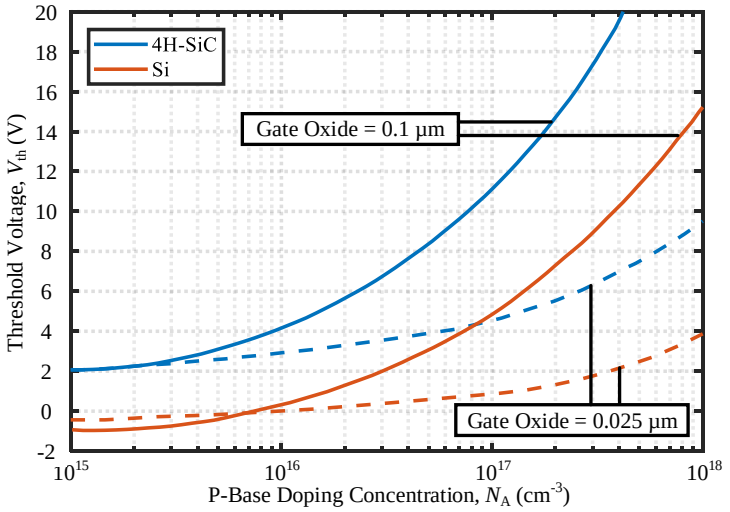


Fig. 1.5. Threshold voltage of SiC MOSFET compared to Si MOSFET (including the impact of N+ polysilicon gate and an oxide fixed charge of 2×10^{11} cm^{-2}) [42].

to be considered. In addition, locally-enhanced electric field provided by a relative thinner gate oxide, existing defects in gate oxide layer, and interface traps could cause time-dependent dielectric breakdown issues [43] [44] [45].

The body diode of the SiC MOSFETs is formed by the N- drift and P-base/P+ region and its reliability is also an important issue. When a surge stress is applied to the body diode, the overheating may cause the expansion of stacking faults from basal plane dislocation in the epitaxial layers, leading to a permanent forward voltage drop (V_F) increase [31] [46].

Since commercial SiC MOSFET devices are still packaged with a similar structure as Si-based devices and they show similar failure locations in the package level, i.e. bonding wire and solder layers. Fig. 1.6 shows package-level failure modes, including bond wire lift-off [47], bond wire fracture [48], solder layer fatigue [49] and Al metallization reconstruction [50].

Bonding wires mainly have two types of failure modes: bond wires fracture and bond wires lift-off. For power modules, the former occurs slowly at the interface with copper tracks of the DBC and this is caused by repetitive expansion and contraction due to alternative heat and cooling [51]. The latter generally happens at the interface with SiC die, induced by the mismatch of the coefficients of thermal expansion (CTE) between bond wires and SiC. Thermo-mechanical stress contributes to the metallization reconstruction and cracks near the interface, which gradually leads to a bond wire lift-off [52] and it is also observed in the discrete SiC MOSFETs after failure analysis [53].

Typically, solder layers in SiC power modules are used to attach the SiC die on the DBC substrate and connect the substrate with the baseplate. Also due to CTE mismatch between SiC and DBC, shear stress could gradually cause the cracks and voids in the

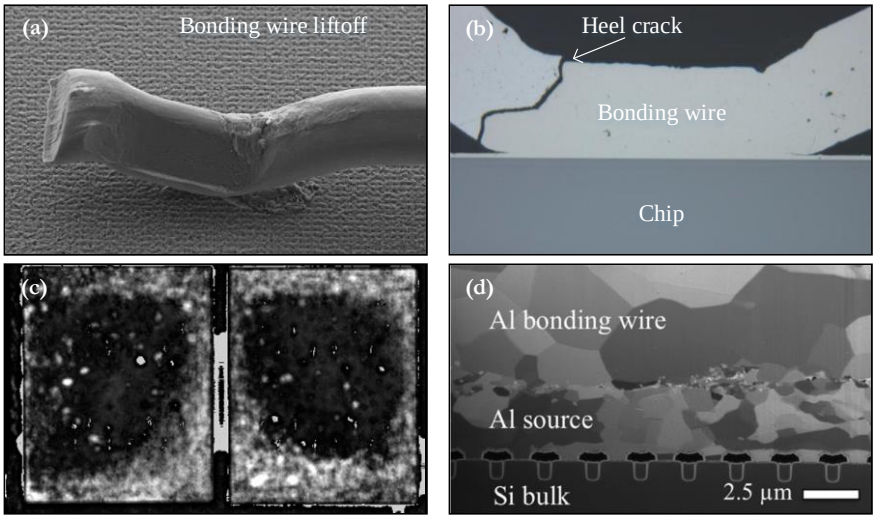


Fig. 1.6. Package-level failure modes in power module: (a) bonding wire lift-off [47]; (b) bonding wire fracture [48]; (c) chip solder edge delamination [49]; (d) Al metallization reconstruction [50].

solder layer, which increases the thermal resistance, resulting in temperature rise and further solder delamination [54].

Compared with Si devices, the package-level reliability of SiC MOSFETs is still facing some new challenges. The higher current density of the SiC chips may lead to more voids inside bond wires and solder layers under the influence of electromigration, which induces a more severe degradation [52] [55]. Since the SiC material has much larger Young's modulus than Si, as listed in Table 1.1, the interface between SiC die attached solder and the DBC substrate need to endure higher stress and accumulated creep strain [56]. Another factor is the thermal conductivity. Although the higher thermal conductivity of SiC material makes it possible for dissipating more heat, at the same time, it may cause a larger temperature variation in SiC devices than in Si, increasing the thermo-mechanical stress at the interfaces [57]. To summarize, the common failure locations of SiC MOSFETs and their main causes are listed in Table 1.3.

To ensure the reliable operation within expected service life and enable a reliability prediction under field stress conditions, many laboratory accelerated life tests (ALTs) have been developed and Table 1.4 lists the main ALTs for SiC MOSFETs.

Among these ALTs, the power cycling (PC) tests are designed to detect ageing failures induced by long-term wear-out under normal operating conditions (e.g. bond wires lift-off) since SiC MOSFET chips are actively heated by their generated losses and

TABLE 1.3 - FAILURE LOCATIONS AND CAUSES OF SIC MOSFETS

Level	Failure Location	Main Cause
Chip	Gate Oxide	High Electric Field/High Temperature
	Body Diode	Surge Current
Package	Bond Wires	High Current Density
	Solder Layers	High Temperature Swing and High Young's Modulus

TABLE 1.4 - ACCELERATED LIFE TESTS FOR SIC MOSFETS

Test	Brief Description	Test Condition
HTGB	High Temperature Gate Bias Test	Maximum V_{GS} and T_j Stress
HTRB	High Temperature Reverse Bias Test	Maximum V_{DS} and T_j stress
PC	Power Cycling Test	Internal Heating by Losses
TC	Temperature Cycling Test	Low External Heating Rate
TS	Thermal Shock Test	High External Heating Rate

this test approach is often used for reliability prediction and lifetime estimation. At present, a power cycling test protocol for SiC MOSFETs at high temperature has been proposed [58]. Different measurement and power cycling methods have been evaluated and the method of measuring the voltage drop of the body diode with negative gate voltage is found most suitable for SiC MOSFETs [59] [60]. In [61], a modified estimation model for the bond wire resistance increase is proposed based on chip degradation. In addition, several electrical parameters can be compared before and after the power-cycling tests showing that the threshold voltage, output characteristic and transfer characteristic are affected significantly [62].

Apart from these ALTs aiming at normal operating conditions, catastrophic failures of SiC MOSFETs, induced by abnormal conditions, also attracted extensive attention. To meet the requirements for power electronic applications, the SiC MOSFETs are expected to withstand short circuits and a short-circuit event can occur in different ways. For instance, Fig. 1.7 presents a conventional three-phase voltage source converter mainly used for motor drive applications, together with two possible short-circuit cases. 1) When the devices S_1 and S_4 start to work in the on-state, the short-circuit case 1 is caused by the unexpected conduction of the device S_2. In this case, the devices S_1 and S_2 withstand short-circuit stress. 2) Due to the degradation of phase-to-phase insulation, the short-circuit case 2 could occur and it leads to the short-circuit condition on the devices S_1 and S_4.

In fact, short circuit conditions can also be classified into different types [63]: 1) Type I (hard switching fault): A short circuit that already exists when the device is turned on. 2) Type II (fault under load): Short circuit occurs when the device is in the conducting state. 3) Type III: Short circuit occurs across the load during the conducting mode of the body diode. Recently, the SiC MOSFETs have been evaluated under various types of short circuits as well as stresses [64] [65] [66]. A short-circuit safe operation area (SCSOA) has been proposed for SiC MOSFET power devices [67].

Based on the experimental data obtained from ALTs, the lifetime model of SiC MOSFETs can be built and the approaches for lifetime estimation can be mainly divided

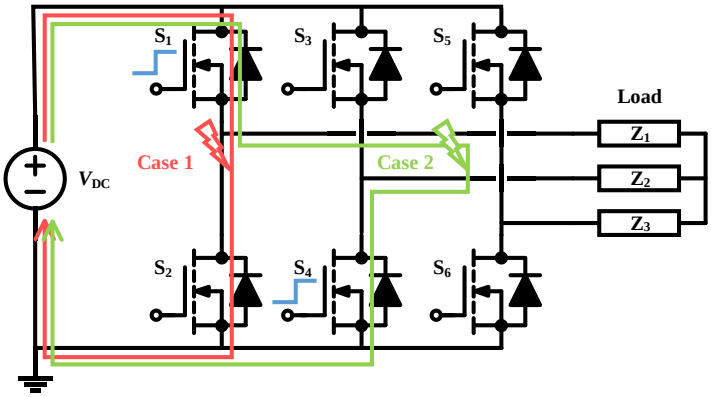


Fig. 1.7. Short-circuit cases in a three-phase voltage source converter.

into two groups: empirical lifetime models and physics-based lifetime models. The empirical models are statistical and cannot distinguish between different failure mechanisms. The latter, in contrast, is time-consuming but considers the physical interactions of the observed failure mechanisms taking into account the packaging geometric structure and materials [68]. In other words, the lifetime can be estimated based on the failure mechanism root cause. Besides, the RUL estimation also needs matched lifetime model and suitable ageing indicators. Therefore, it is critical to fully understand the ageing and failure mechanisms of SiC MOSFETs by taking into account various operating conditions.

1.2 Research Motivation

At present, many efforts have been devoted to investigate the reliability and robustness of SiC MOSFETs by performing either ALTs or short circuit tests, separately. As mentioned above, through different stresses of ALTs (especially power cycling tests), an accurate lifetime model of SiC MOSFETs can be worked out. Thereafter, when the SiC MOSFETs is used in a power electronic system, the remaining useful life (RUL) of SiC MOSFETs can be estimated based on the condition monitoring parameters, i.e. the ageing indicators. Notably, this approach only considers the ageing failures, in other words, the wear-out issues under normal operating conditions. On the other hand, the catastrophic failures of SiC MOSFETs, coming from abnormal operating conditions are investigated by performing UIS tests or short-circuit tests, which aim to evaluate its robustness (e.g. short-circuit capability) and failure mechanisms.

With the development of faster short circuit protection and desaturation fault detection for SiC MOSFETs, the device destruction can be avoided to some extents, allowing the SiC MOSFETs to withstand many non-destructive short-circuit events within its expected service lifetime. Since the impact of short-circuit events was used to be neglected before, this situation brings a new scientific question for the lifetime estimation of SiC MOSFETs. Therefore, the motivation of this thesis is to investigate the reliability of SiC MOSFETs by taking into account the short-circuit events.

1.3 Scientific Questions

Based on the background and research motivations regarding the above reliability issues of SiC MOSFETs, the overall question of this Ph.D. thesis is listed here:

What is the impact of short-circuit events on the Remaining Useful Life of SiC MOSFETs?

To be more specific, more detailed scientific questions are to be explored:

- How can the short-circuit conditions affect the electrical parameters of SiC MOSFETs? How to identify a suitable degradation indicator?
- How do the short-circuit conditions affect the normal operation of SiC MOSFETs? Assuming the device is utilized in applications at different temperatures, how to consider the influence of case temperature?
- How can short-circuit events affect the accelerated ageing tests and, further, the Remaining Useful Life of SiC MOSFETs?

- What is the short-circuit degradation mechanism? How can the impact of short circuit events be mitigated at the package-level?

1.4 Thesis Objectives

This Ph.D. thesis aims to investigate the impact of short-circuit conditions on the remaining useful life (RUL) of SiC MOSFETs. In order to answer the aforementioned scientific questions, the main objectives are described in this section as following:

- Study of degradation indicators under short-circuit conditions
  A suitable degradation indicator should be able to reflect the key degradation process under short-circuit conditions. Degradation indicators will be explored with two experimental approaches.
- Investigation on the impact of short-circuit degradation on the normal operation
  To meet the repeatability requirement, the short-circuit condition will be evaluated for a specific type of SiC MOSFET. By means of curve tracer and double pulse tests, the variation of static and dynamic characteristics will be explored extensively. The influence of case temperature will also be considered.
- Investigation on the impact of short-circuit degradation on the RUL
  Based on the mixed power-cycling/repetitive short-circuit tests, the quantitative impact of short-circuit events on the power-cycling conditions and further RUL will be explored. A deeper analysis of the failed and still functional device will be performed to better understand the degradation mechanisms.
- Simulation of the short-circuit degradation and mitigation strategy
  This study aims to simulate the thermal and mechanical behaviour of SiC MOSFETs under short-circuit conditions to explain the degradation observed in experimental test and failure analysis. Based on the degradation mechanisms, a package-level strategy will be explored to mitigate the impact of short-circuit events.

1.5 Limitations

With the improvement of higher quality SiC process technology and design evolution, many power semiconductor manufacturers are introducing new commercial SiC devices into the PE market. The various chip- and package level designs of SiC MOSFETs from 650 V to 1.7 kV may bring a deviation for reliability analysis. This thesis focuses on the planar-type SiC MOSFETs with the blocking voltage in the range of 1.0 kV – 1.2 kV, which is now to be regarded as mature, and is gradually replacing its Si counterparts in many applications.

Furthermore, the short-circuit tests done in this thesis have been performed with a low-inductance laboratory non-destructive tester. Since the short-circuit performance is affected by the stray inductances, the short-circuit events in the real case may result in a higher voltage overshoot, exceeding the maximum rated voltage. This factor is not taken into account in this thesis either.

Finally, the mixed power-cycling/short-circuit tests have been carried out with a restricted number of samples. Although the SiC MOSFET samples were well-selected

with matched electrical characteristics to mitigate the influence of characteristic variation, there has been a non-negligible dispersion in some cases.

1.6 Thesis Outline

The Ph.D. dissertation takes the form of a collection of papers and sums up the outcomes from a number of publications which are listed in Section 1.7. This thesis consists of two main parts: 1) a Report, which is organized with six chapters and 2) Selected Publications.

Chapter 1 has given an introduction to this thesis, mainly the research background and motivation. Following the scientific questions, the thesis objectives have been discussed as well as the limitations. Chapter 2 shows the short-circuit performance in SiC MOSFETs and the degradation indicators were analysed based on two experimental approaches. As the affecting main factors for the SiC MOSFETs operation, the variation of static and dynamic characteristics induced by the short circuits were assessed in Chapter 3. Since case temperature strongly depends on the field application, temperature-dependent degradation was also considered. Chapter 4 describes the investigation on the impact of short-circuit events on the power-cycling conditions, and furthermore, the RUL by applying different degrees of short-circuit stress. A revised lifetime model taking into account the short-circuit events is proposed. Chapter 5 gives a further insight into the short-circuit degradation by the achievement of thermo-mechanical simulation and failure analysis. Based on the degradation mechanisms, a package-level strategy is proposed to mitigate the impact of short-circuit conditions on the RUL. Finally, the conclusions are drawn in Chapter 6 together with the prospect of future research on this topic.

1.7 List of Publications

The publications related to this Ph.D. thesis are shown below and their relevant contribution to each chapter are listed in Table 1.5.

Journal Articles

[J1] **H. Du**, P. D. Reigosa, F. Iannuzzo, and L. Ceccarelli, "Investigation on the degradation indicators of short-circuit tests in 1.2 kV SiC MOSFET power modules," *Microelectronics Reliability*, vol. 88-90, pp. 661-665, 2018.

[J2] **H. Du**, L. Ceccarelli, F. Iannuzzo, and P. D. Reigosa, "Implications of short-circuit events on power cycling of 1.2-kV/20-A SiC MOSFET power modules," *Microelectronics Reliability*, vol. 100-101, pp. 113373, 2019.

[J3] **H. Du**, P. D. Reigosa, L. Ceccarelli, and F. Iannuzzo, "Impact of repetitive short-circuit tests on the normal operation of SiC MOSFETs considering case temperature influence," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 195-205, 2020.

[J4] **H. Du**, S. Letz, N. Baker, T. Goetz, F. Iannuzzo, and A. Schletz, "Effect of short-circuit degradation on the remaining useful lifetime of SiC MOSFETs and its failure analysis," *Microelectronics Reliability*, pp. 113784, 2020.

Publications in Conference Proceedings

[C1] **H. Du**, P. D. Reigosa, F. Iannuzzo, and L. Ceccarelli, "Impact of the case temperature on the reliability of SiC MOSFETs under repetitive short circuit tests," in *Proc. of 2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 332-337.

[C2] **H. Du**, N. Baker, and F. Iannuzzo, "Implications of short-circuit degradation on the aging process in accelerated cycling tests of SiC MOSFETs," in *Proc. of the 32nd IEEE International Symposium on Power Semi-conductor Devices and ICs (ISPSD)*, 2020, pp. 202-205.

[C3] **H. Du** and F. Iannuzzo, "A mitigation strategy for the short-circuit degradation in SiC MOSFETs," in *Proc. of IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia 2020 (WiPDA-Asia)*, 2020 (*in press*).

TABLE 1.5 - RELATED PUBLICATIONS TO THE CHAPTERS

Chapter No.	Relevant Publications
2	J1 and J3
3	J3 and C1
4	J2, J4, and C2
5	J4 and C3

Chapter 2

Degradation Indicators under Short-Circuit Conditions

In this chapter, the short-circuit performance in SiC MOSFETs considering several key factors is presented and two common failure modes under short-circuit conditions are introduced. Then an experimental short-circuit test bench is described in detail and the degradation indicators in terms of short-circuit tests are investigated with two experimental approaches. This chapter is mainly contributed by [J1] and [J3].

2.1 Short-Circuit Performance and Failure Modes

As mentioned above in Section 1.1.2, there are mainly three types of short-circuit conditions, and this thesis focuses on the type I, also termed hard switch fault. Fig. 2.1 shows a typical short-circuit behaviour of SiC MOSFETs including drain-source voltage (V_{DS}), gate-source voltage (V_{GS}), and drain current (I_D). Before turning on the SiC MOSFETs, a negative voltage is applied to V_{GS} and the V_{DS} keeps at rated high voltage with the value of V_{DC}. When the device turns on with short-circuit condition, the I_D starts to increase and settles at saturation current (I_{SC_max}) corresponding to specific V_{GS}. At the same time, the V_{DS} decreases for a short time due to the I_D gradient, i.e. di/dt. Then the device is subjected to both high voltage and high current simultaneously for several or up to 10 – 20 microseconds, and the I_{SC} decreases with time due to the

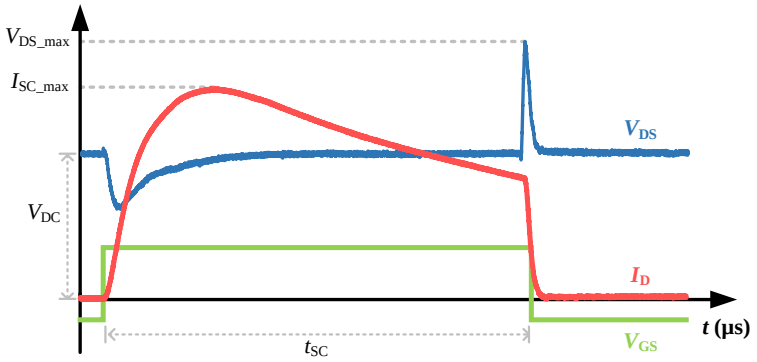


Fig. 2.1. Typical short-circuit (type I) behaviour in SiC MOSFETs.

self-heating. Thereafter, the short-circuit protection triggers and the device turns off with a negative V_{GS} to avoid catastrophic failures. During the turn-off period, an inductive voltage peak (V_{DS_max}) appears, which is also caused by the di/dt, similarly to turn-on transient. To ensure a lower V_{DS_max} than the rated blocking voltage of the device, the stray inductance in the power loop needs to be minimized and the di/dt must be limited by a higher gate resistance.

Meanwhile, the dissipated energy during short-circuit pulse (E_{SC}) can be calculated by integration and the critical value without any degradation or failure is regarded as the critical energy (E_C).

$$E_{SC} = \int_0^{tsc} V_{DS}(t) \cdot I_D(t) dt \tag{2.1}$$

Therefore, the short-circuit capability for a specific SiC MOSFET can be evaluated by increasing the drain bias voltage (V_{DC}) or short-circuit pulse duration (t_{SC}), and the maximum value of t_{SC} is typically known as the maximum short-circuit withstanding time (SCWT). Apart from these, the short-circuit energy is also determined by many other parameters, such as gate driver voltage (V_{GS}) [69], gate resistance (R_G) [70] and case temperature (T_C) [71]. Among these, the V_{GS} is a key factor to the E_{SC}. When the applied positive V_{GS} decreases, the MOS channel might not be fully turned on and this can lead to a lower saturation current (I_{SC}), which reduces the E_{SC} and enables a larger short-circuit capability.

It is worth noting that the short-circuit capability of SiC MOSFETs is much worse than Si IGBTs. Fig. 2.2 shows an example of the short-circuit I_D comparison between SiC MOSFET and Si IGBT with the same rated current and same test settings (except the V_{GS} is set based on the rating values) [72]. The 1.2 kV/40 A SiC MOSFET (C2M0040120D) has only 8 µs SCWT and the I_{SC_max} of 375 A (which is typically more than 6 times the rated current). In contrast, the Si IGBT (IKW40T120) has the SCWT of 38 µs and it only shows around 200 A I_{SC_max}.

One main reason for weaker short-circuit capability in SiC MOSFETs is the much smaller chip size, which leads to a higher power density in short-circuit condition. The

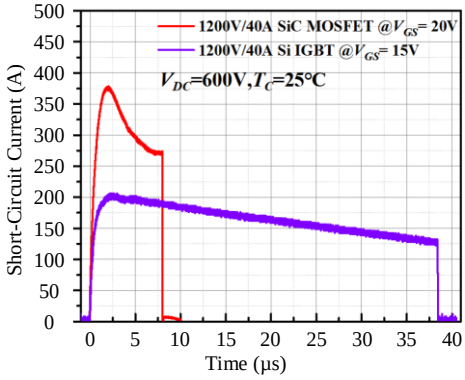


Fig. 2.2. Short-circuit current comparison of the 1.2 kV/40 A SiC MOSFET and Si IGBT (V_{DC} = 600 V, T_C = 25 °C) [72].

short-circuit energy dissipates in a relatively short time and the internal temperature rises significantly. Although SiC material has a much lower intrinsic carrier concentration than Si at the same temperature, thermal instability issue remains in SiC MOSFET similar to Si IGBT. When the junction temperature exceeds a critical limit, the intrinsic carrier concentration at the drift layer is not negligible anymore compared to its doping concentration. Therefore, the drain leakage current, induced by the drift of the thermally-generated intrinsic carriers, can trigger a so-called thermal runaway [73]. Besides, the large leakage current may flow horizontally the P-base region and activate the parasitic BJT, which can lead to the fast I_D increase and device failure [71]. This failure mode caused by the drain leakage current occurs several microseconds after short-circuit turn-off. Fig. 2.3 shows the short-circuit waveforms of a 1000 V/22 A SiC MOSFET (V_{DC} = 600 V, t_{SC} = 3 µs, and T_C = 100 °C). During turn-off transient, the device exhibits a drain current tail, which indicates the leakage current, and the thermal runaway failure occurs ~1 µs after turn-off [J3].

Another common failure mode, which has not been observed in Si devices during short-circuit conditions, is the shorted gate with source terminals. Due to the immature process technology of SiC MOSFET, the weakness of gate oxide may cause failures. Recent studies show that the intrinsic weakness of gate oxide grown on SiC have been improved and commercial SiC MOSFETs have an acceptable lifetime at normal operating gate voltage [72]. However, the gate oxides grown on SiC have a higher density of detects compared to Si and this weakness induced by the substrate and oxide defects still needs to be considered. In addition, as mentioned in Section 1.1.1, the gate oxide tends to be thinner than Si devices to ensure the gate threshold voltage at a reasonable

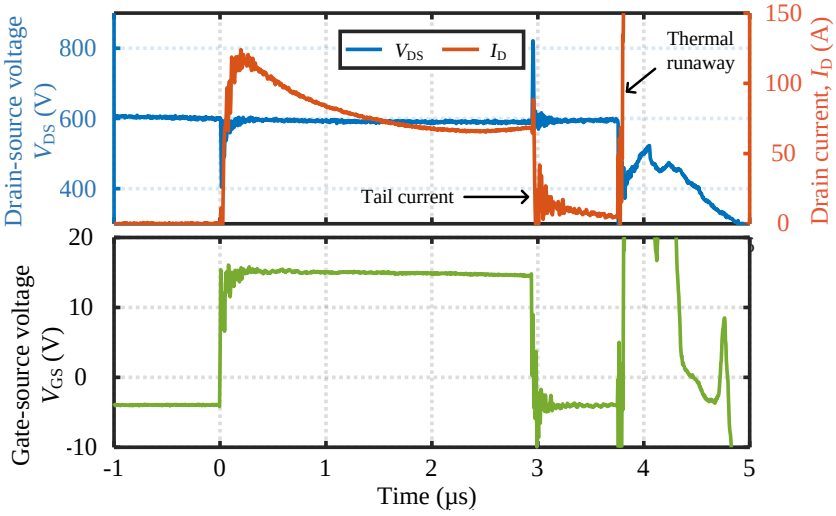


Fig. 2.3. Short-circuit waveforms of a 1000 V/22 A SiC MOSFET exhibiting thermal runaway failure mode [J3].

value, and SiC MOSFETs are typically designed to withstand much higher electric field stress than Si devices thanks to the superior critical electric field strength of SiC material (see Table 1.1, Page 2). According to Gauss' Law in (2.2), where ε_{SiC} and ε_{SiO2} are the dielectric constants of the SiC and SiO_2 material, respectively, the electric field strength in the gate oxide layer near the SiO_2/SiC interface can be very high. Therefore, the gate oxide breakdown is prone to occur [64].

$$E_{SiO2} = \frac{\varepsilon_{SiC}}{\varepsilon_{SiO2}} E_{SiC} \cong 3E_{SiC} \tag{2.2}$$

On the one hand, to avoid the short-circuit failures like thermal runaway and gate-source short-circuit, faster protection circuits and more reliable gate oxide layer have been developed recently. On the other hand, the slow degradation of SiC MOSFETs caused by short-circuit stress has become critical from a reliability standpoint.

2.2 Short-Circuit Test Bench

For the purpose of degradation study, the test bench needs to have the capability to perform short-circuit tests within the maximum SCWT, V_{GS} and blocking voltage of the device. The short-circuit tests of SiC MOSFETs in this thesis are performed thanks to the non-destructive tester (NDT) available at the Center of Reliable Power Electronics (CORPE), Aalborg University, Denmark [74].

The schematic of the 2.4 kV/10 kA NDT is shown in Fig. 2.4 [J1]. A high-voltage DC power supply is used to provide the DC-link voltage (V_{DC}) and charge up the large capacitor bank (C_{DC}). When the short circuit occurs, these can provide the required energy. The series protection is composed of four IGBT power modules in parallel to increase the total current capability during short-circuit condition, and it is used to prevent destructive explosions and make possible further analysis on the degraded samples. To ensure that the overshoot voltage during short-circuit turn-off does not exceed the maximum blocking voltage of the device, a custom-designed round laminated busbar with 10 nH stray inductance (L_{stray}) enables homogeneous short-circuit current distribution [74]. Both discrete SiC MOSFETs and power modules can be used as the

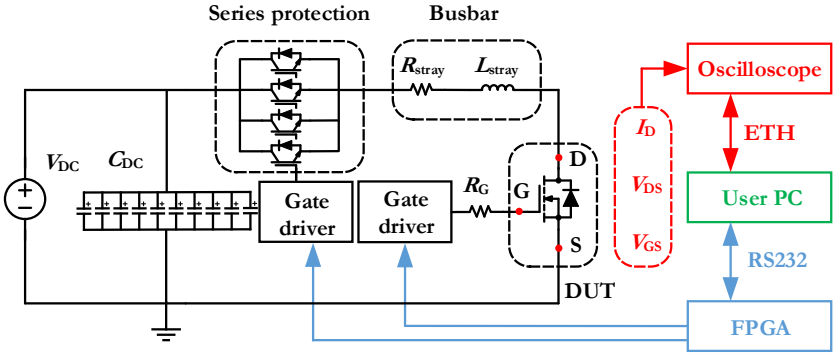


Fig. 2.4. Schematic of the non-destructive tester [J1].

device under test (DUT) employing matched adaptors connected to the busbar and a commercial gate driver is selected depending on the requirement of the DUT.

The control signals to the gate drivers of the series protection as well as the DUT are given by a 100-MHz field-programmable gate array (FPGA) board with a time accuracy of 10 ns. Fig. 2.5 shows the typical timings to achieve type-I short circuit and the adjustable pulse time is marked here as t_{SC}.

During short-circuit tests, V_{DS}, I_D, and V_{GS} waveforms are measured by an oscilloscope with a high-voltage probe, a current probe (extremely thin Rogowski coil), and a passive voltage probe, respectively. A personal computer (User PC) is the user interface, which connects the oscilloscope and FPGA board via the Ethernet and RS-232. Besides, repeated tests can be performed through a MATLAB graphical user interface (GUI) [75], which provides the capability to adjust the number of tests and the time interval between consecutive tests. Fig. 2.6 presents the appearance of the NDT setup. For the sake of clarity, main testing and measurement equipment are summarized in Table 2.1.

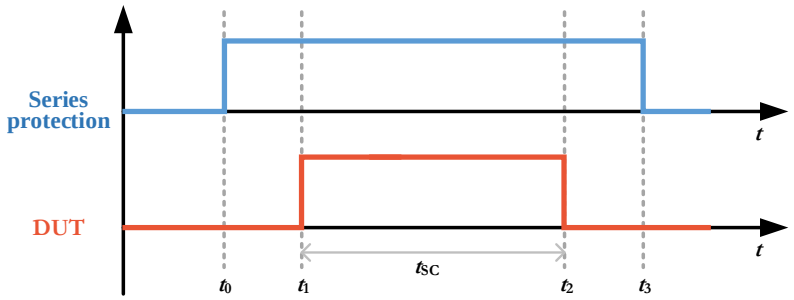


Fig. 2.5. Control signals for the gate drivers of series protection and DUT.

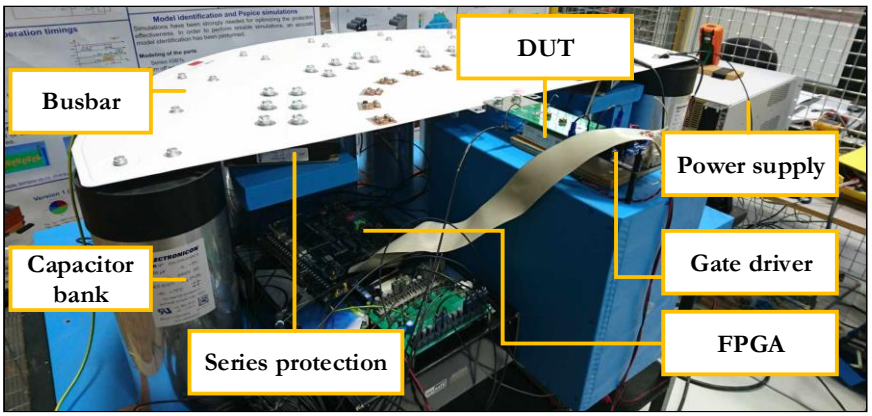


Fig. 2.6. Appearance of the non-destructive tester in the laboratory [J1].

TABLE 2.1 - MAIN TESTING AND MEASUREMENT EQUIPMENT (ACCESSORIES)

Name	Description
DC Power Supply	Magna – Power Electronics TS 6U
Capacitor Bank	10 × 1100 μF, 2400 V
Series Protection	4 × Dynex DIM1500ESM33-TS000 (3 kA/3.3 kV)
FPGA Board	Terasic DE2 – 115
Oscilloscope	Teledyne LeCroy HDO 6054-MS
HV Passive Probe	Teledyne LeCroy PPE 2 kV (Bandwidth 400 MHz)
Current Probe	PEM CWT 6 & 30 Ultra-mini (Bandwidth 30 MHz)
Passive Probe	Teledyne LeCroy PP018 (Bandwidth 500 MHz)

2.3 Short-Circuit Degradation Indicators

Many works have been carried out to investigate the degradation mechanisms of SiC MOSFETs under short-circuit conditions [76]. The dissipated heat induced by the short-circuit energy may lead to a thermally-generated current in the drift layer, which is shown as A in Fig. 2.7 (a), and this may cause the tail current during turn-off transient. On the other hand, according to simulation results in [71], the surface temperature can exceed 900 K and melt the Aluminium metallization, whose degradation location is represented as B in Fig. 2.7 (a). For instance, there would be voids in the Al/SiC interface

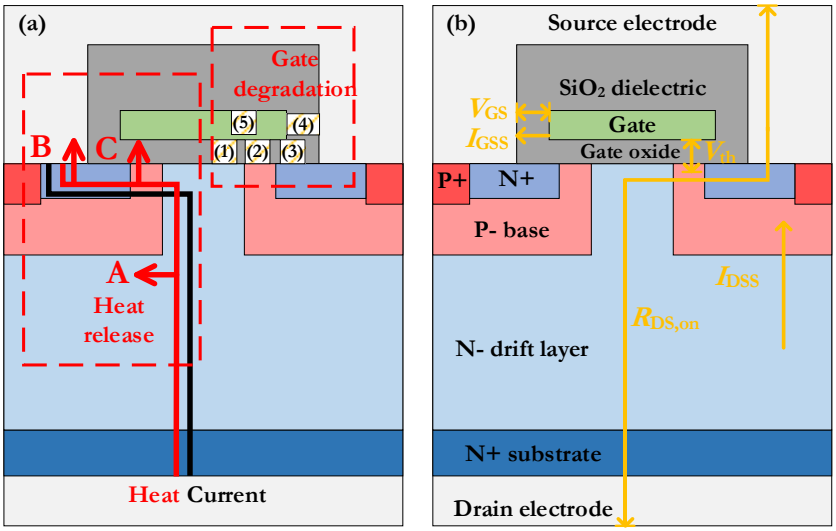


Fig. 2.7. (a) Degradation mechanisms and (b) degradation indicators under short-circuit conditions (different gate damages marked as type (1) - (5)).

because of current crowding and local heating [77], and the voids typically increase the contact resistance and contribute to the temperature increase. In addition, the released heat during short circuit could also lead to the ageing of the gate structure, which is shown as C in Fig. 2.7 (a). In [78], the degraded cells which are closer to the source bonding have been observed after a relatively low energy SC test. Among these three parts, the gate degradation attracts extensive attention and there are mainly four types of gate-source damages [79] and they are shown as type 1 to type 4 in Fig. 2.7 (a). Besides, damage inside the gate (type 5) also appear after repetitive short-circuit tests [80].

Based on the degradation mechanisms, several indicators have been proposed as can be seen in Fig. 2.7 (b), including on-state resistance ($R_{DS,on}$) [64], drain leakage current (I_{DSS}) [76], gate leakage current (I_{GSS}) [81], threshold voltage (V_{th}) [82], etc. However, most of the previous studies focused on discrete SiC MOSFETs, and a suitable degradation indicator, reflecting the short-circuit degradation process of SiC MOSFETs still needs to be considered. Therefore, in the following part of this section, the degradation indicators of short-circuit tests are investigated in SiC MOSFET power modules.

A flowchart and a sketch of the experimental approaches are shown in Fig. 2.8 and Fig. 2.9, mainly consisting of two parts: (a) static characterizations and (b) short-circuit

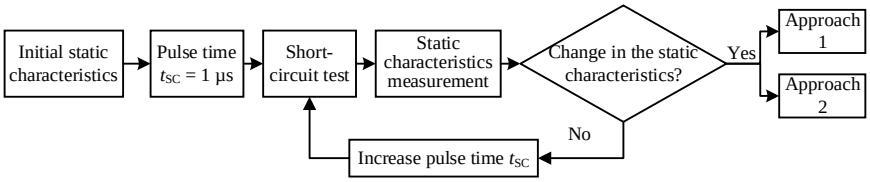


Fig. 2.8. Flowchart of two short-circuit test approaches for the degradation indicators [J1].

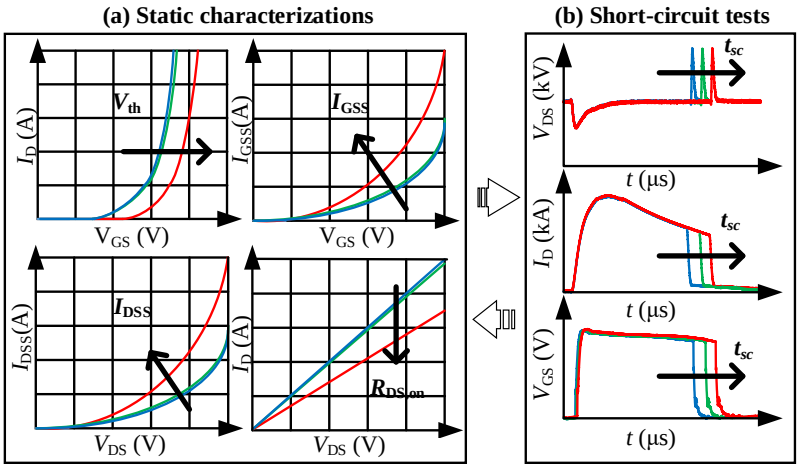


Fig. 2.9. Sketch of (a) appreciable changes in the static characteristics with (b) the short-circuit pulse time increase [J1].

tests [J1]. To begin with, the static characteristics, including V_{th}, I_{GSS}, I_{DSS}, and $R_{DS,on}$ are measured at the pristine condition. Then, a short-circuit test is performed with 1 µs pulse time and the short-circuit waveforms (V_{DS}, I_D, and V_{GS}) are obtained. After each short-circuit test, the static characteristics of the DUT are measured. If no appreciable changes, t_{SC} is increased step by step while the other settings are kept the same. When an appreciable change in the static characteristics is observed, this procedure stops. As shown in Fig. 2.9, there is no clear change in the static characteristics when t_{SC} is increased from the blue to the green line. If t_{SC} is further increased from the green to the red line, an obvious change appears. At this point, two different approaches are used on two different sets of samples as shown in Fig. 2.8. The first approach (i.e. approach 1) is to remain the last t_{SC} and perform multiple short-circuit tests with the same value. The other one named as 'approach 2', is to keep increasing t_{SC} [J1].

The DUT is 1.2 kV/500 A SiC MOSFET power module with 2nd-generation planar technology from Semikron (SKM350MB120SCH15), having a half-bridge configuration. A commercial gate driver (CGD15HB62P, Cree) is used for short-circuit tests with a +20 V/-5 V output voltage and a R_G equal to 10 Ω. The DC-link voltage is fixed at 500 V to avoid a high overshoot voltage. Another voltage probe placed at the other end of R_G is used to obtain the voltage drop across R_G. The static characteristics are measured with a power device analyser (B1506A, Keysight). All the experimental tests are performed at 25 °C [J1].

Regarding the test approach 1, at first, t_{SC} started from 1 µs and then it was increased in steps of 1 µs until it reached 10 µs; there was no obvious variation of the static characteristics. Since little change appeared for the first time at t_{SC} = 11 µs, t_{SC} was increased to 11.2 µs and at this point, a more obvious change was observed. Thus, the t_{SC} was no longer increased and short-circuit tests were repeated at the same conditions for five times.

The short-circuit waveforms (V_{DS}, I_D, and V_{GS}) when t_{SC} was set to 11 µs and multiple tests at 11.2 µs are shown in Fig. 2.10 [J1]. The on-state V_{GS} amplitude decreases evidently from the 3rd to the 4th repetition and a reduction of I_D can be observed at the same time. The degradation hypothesis is that a gradual increase in I_{GSS} resulted in the reduction of V_{GS}. Such a current could have been originated from conductive paths

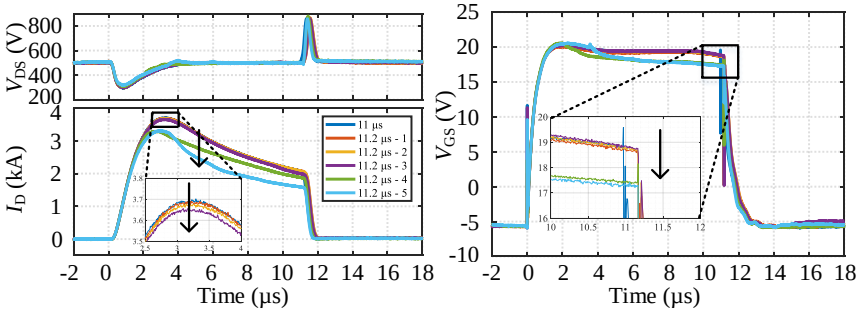


Fig. 2.10. Short-circuit waveforms (V_{DS}, I_D, and V_{GS}) of multiple tests at t_{SC} equal to 11.2 µs (approach 1) [J1].

which were formed between gate- and source terminals. In addition, the variation of V_{GS} and I_D observed in Fig. 2.10 [J1] are consistent with the results observed for discrete SiC MOSFETs in [81] and [83].

To verify this hypothesis, the gate current during short-circuit tests (I_G) was monitored by means of the voltage drop across R_G and the waveforms are presented in Fig. 2.11. The maximum I_{GSS} increased from 68 mA (1st repetition, 11.2 µs) up to 160 mA (5th repetition, 11.2 µs). After each short-circuit test, the static characteristics (i.e. V_{th}, I_{GSS}, I_{DSS}, and $R_{DS,on}$) were measured, and the results are shown in Fig. 2.12 from (a) to (d), respectively [J1].

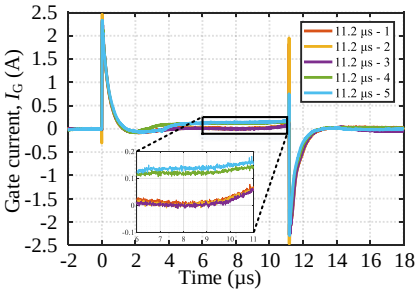


Fig. 2.11. Gate current waveforms of multiple 11.2 µs short-circuit tests (1st - 5th repetition) [J1].

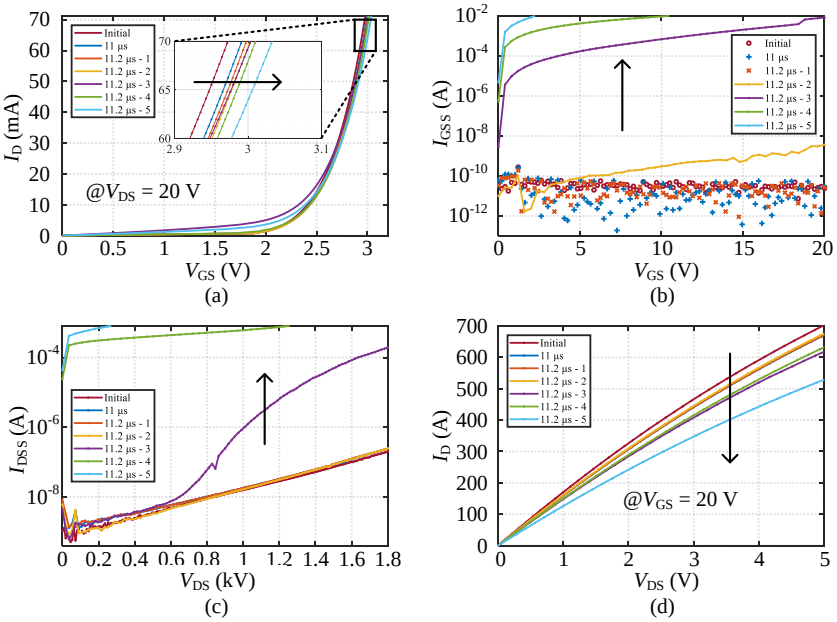


Fig. 2.12. Static characteristics variation after repetitive short-circuit tests at t_{SC} = 11.2 µs: (a) V_{th}, (b) I_{GSS}, (c) I_{DSS}, and (d) $R_{DS,on}$ [J1].

a) As can be seen in Fig. 2.12 (a), the V_{th} shifts positively after each short-circuit test at t_{SC} = 11.2 µs. b) Due to the increased conductivity between the gate and source terminal, the effective V_{GS} on the device decreases slightly, ending up in a further equivalent V_{th} shift. Fig. 2.12 (b) confirms the gradual increase in I_{GSS}; a non-negligible I_{GSS} could be observed after the 2nd short-circuit repetition and it continues to increase after each repetition. The maximum I_{GSS} reaches 0.1 A after the fifth short-circuit repetition at 11.2 µs. c) Likewise, the I_{DSS} and d) $R_{DS,on}$ increase are found after the third short-circuit repetition as presented in Fig. 2.12 (c) and (d). When the I_D-V_{DS} characteristic ($R_{DS,on}$) is measured, the non-negligible gate leakage current can lead to a lower V_{GS} than the applied value (20 V) and this could be one of the reasons for the $R_{DS,on}$ increase.

What follows is the experimental results from approach 2, consisting of increasing the t_{SC} regardless of the variation of the static characteristics. Fig. 2.13 presents the short-circuit waveforms from t_{SC} = 10 µs up to t_{SC} = 12.4 µs and these waveforms, together with the static characteristics, show similar trends as the approach 1. Also, the reduction of I_D caused by the V_{GS} reduction can be verified by a brief calculation according to (2.3) in the case of much larger V_{DS} than (V_{GS}-V_{th}) [J1].

$$I_D = \frac{1}{2} \cdot \kappa \cdot (V_{GS} - V_{th})^2 \tag{2.3}$$

Based on the short-circuit waveform at t_{SC} =12 µs in Fig. 2.13 (a) and (b), the constant parameter κ can be calculated. When I_D reaches the peak (i.e. I_{D_Exp} is 3.695 kA), the V_{GS} shows 19.480 V at this point. After this short-circuit test, the V_{th} obtained with static characterization is 3.08 V. Thus, the calculated value of κ is 27.48 and it can be used to verify the I_D peak in the following short-circuit tests at t_{SC} = 12.2 µs and 12.4 µs with the measured V_{GS} and V_{th}.

With respect to the short-circuit waveforms at t_{SC} = 12.2 µs, V_{GS} is 18.154 V and the measured V_{th} after this test is 3.093 V. The calculated I_D peak (I_{D_Cal}) is 3.115 kA, which is in agreement with the test results (i.e. I_{D_Exp} = 3.117 kA). Likewise, I_{D_Cal} in terms of the test at t_{SC} = 12.4 µs is 2.586 kA, keeping consistent with the experimental results, i.e. 2.6030 kA. Calculation verification is listed in Table 2.2 for the sake of clarity.

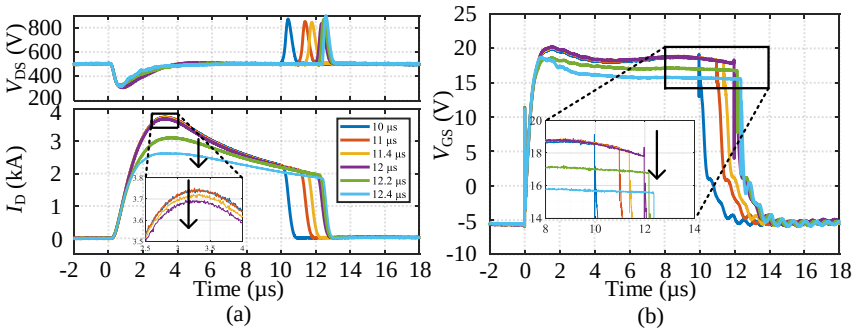


Fig. 2.13. Short-circuit tests with the pulse time increase: (a) V_{DS}, I_D, and (b) V_{GS} (approach 2) [J1].

TABLE 2.2 - CALCULATION OF THE PEAK DRAIN CURRENT REDUCTION

Case Study	A - 12 µs	B - 12.2 µs	C – 12.4 µs
V_{GS} (V)	19.480	18.154	16.820
V_{th} (V)	3.080	3.093	3.099
κ	27.48	27.48	27.48
I_{D_Exp} (kA)	3.695	3.117	2.630
I_{D_Cal} (kA)	-	3.116	2.586

As pointed out above, the V_{GS} drop caused by the increasing I_{GSS}, leads to the reduction of peak I_D, which affects the generated short-circuit energy. Although all four parameters (V_{th}, I_{GSS}, I_{DSS}, and $R_{DS,on}$) show evident variations after short-circuit tests, the formation of conductivity path between gate- and source terminal is the root cause of the short-circuit degradation, directly proven by an increase in I_{GSS}.

Furthermore, as can be seen in Fig. 2.11 and Fig. 2.12 (b), the I_{GSS} increase measured with static characterization can be reflected in the I_G waveforms as well as the measured on-state V_{GS} drop during short-circuit tests in Fig. 2.10. By observing Fig. 2.13, the on-state V_{GS} decreases first at the end of the pulse only, i.e. close to the turn-off time, then it starts decreasing uniformly. Therefore, gate leakage current (I_{GSS}) can be considered as a suitable short-circuit degradation indicator of SiC MOSFETs and the variation of the on-state V_{GS} during short-circuit test, especially at the end of the pulse can be used as a reference indicator, which is strongly related to the I_{GSS}.

2.4 Summary

In this chapter, the electrical performance of SiC MOSFETs under type-1 short-circuit conditions has been briefly described, considering the testing parameters, which affect the electrical behaviour, namely, drain-bias voltage, loop inductance, gate resistance, gate voltage, and case temperature. Thereafter, the failure modes under short-circuit conditions, i.e. thermal runaway and gate-to-source short path have been discussed, and they are mainly caused by high temperature and high electric field during short-circuit tests. Introduced by a description of the short-circuit test bench, the degradation mechanisms have been presented. To investigate the degradation mechanisms, four key electrical parameters (i.e. on-state resistance, drain leakage current, gate threshold voltage, and gate leakage current) have been measured with static characterization. To identify the indicator which can best reflect short-circuit degradation process, two test approaches have been performed: the first one is to maintain the same pulse time once an appreciable change in the static characteristics is detected and the second one is to keep increasing the pulse time regardless of the static characteristics change. The positive shift of gate threshold voltage, the increase of gate leakage current, drain leakage current and on-state resistance have been observed through experimental results, and indicated that a conducting path formed between the gate and source leads to the increase in gate leakage current. Meanwhile, it also results in the on-state

gate-source voltage decrease and the reduction of drain current peak. Therefore, the gate leakage current could be regarded as a promising degradation indicator and the on-state gate-source voltage during short-circuit test, especially at the end of the pulse can be used as a reference indicator.

Chapter 3

Impact of Short-Circuit Degradation on the Normal Operation

After introducing the short-circuit degradation and selecting effective degradation indicators in Chapter 2, this chapter focuses on the impact of short-circuit degradation on the normal operating performance of SiC MOSFETs, mainly consisting of [J3] and [C1]. Apart from static characteristics, the variation of the dynamic characteristics induced by short-circuit degradation is analysed. Since the case temperature is subjected to real application conditions, its influence is also considered.

3.1 Selected Conditions for Repetitive Short-Circuit Tests

To ensure that the short-circuit tests are performed without destructive failure at different case temperatures, appropriate testing conditions which allow for short-circuit repetitive tests need to be selected. Therefore, the maximum short-circuit withstanding time (SCWT) at different initial case temperatures (T_C) is investigated at first to identify the critical energy.

The short-circuit tests were performed with the NDT test bench as mentioned in Section 2.2. The DUT is a 1.0 kV/22 A, discrete-, planar-, 3rd-generation-, SiC MOSFET from Cree (C3M0120100K), having a separate Kelvin source pin (i.e. TO-247-4 package) to minimize the inductance in the gate loop. The case temperature is adjusted by an electrical heater together with a temperature controller and an isolated thermal interface material (TIM) is placed between the DUT and the heater. The commercial gate driver (CRD-001, Cree) is used and it gives a +15 V/-4 V output voltage to the V_{GS}. The gate resistance (R_G) is set to 20 Ω to dampen the possible oscillation.

The samples with matched static characteristics, especially $R_{DS,on}$ and V_{th}, were selected as the DUTs in order to mitigate the deviation caused by the samples themselves. The V_{DS} is clamped to the DC-link voltage (V_{DC} = 600 V) and the T_C is set to 25 ºC, 100 ºC, and 150 ºC, respectively for three fresh DUTs. In each case, the t_{SC} is increased from 1.5 μs and the experimental results are presented in Fig. 3.1 [C1] [J3].

At 25 ºC case temperature, the DUT can withstand 4 μs pulse duration. In spite of a clear V_{GS} reduction (which is marked in green dotted box), the DUT does not show destructive failure at this point. On the other hand, the tail current during turn-off transient can be observed in each case and is highlighted in blue dotted boxes. This phenomenon is caused by the leakage current increase as mentioned in Section 2.1. When the leakage current exceeds the limit value, the thermal runaway failure mode would

happen as marked in the red dotted boxes in Fig. 3.1 (b) and (c). Taken together, these results show that the SCWT decreases when the initial T_C increases from 25 ºC to 150 ºC. Also, the short-circuit energy (E_{SC}) at last time test was calculated to give a further insight into temperature-dependent short-circuit capability and it is summarized in Table 3.1 [J3]. At 150 ºC case temperature, the DUT shows the lowest maximum SCWT (2.7 µs) and critical energy (i.e. E_C = 0.12 J).

To achieve the short-circuit degradation, rather than destructive failure in the whole range of 25 ºC – 150 ºC case temperatures, E_{SC} needs to be lower than the minimum E_C (i.e. 0.12 J) and the t_{SC} needs to be shorter than 2.7 µs. According to this, the chosen

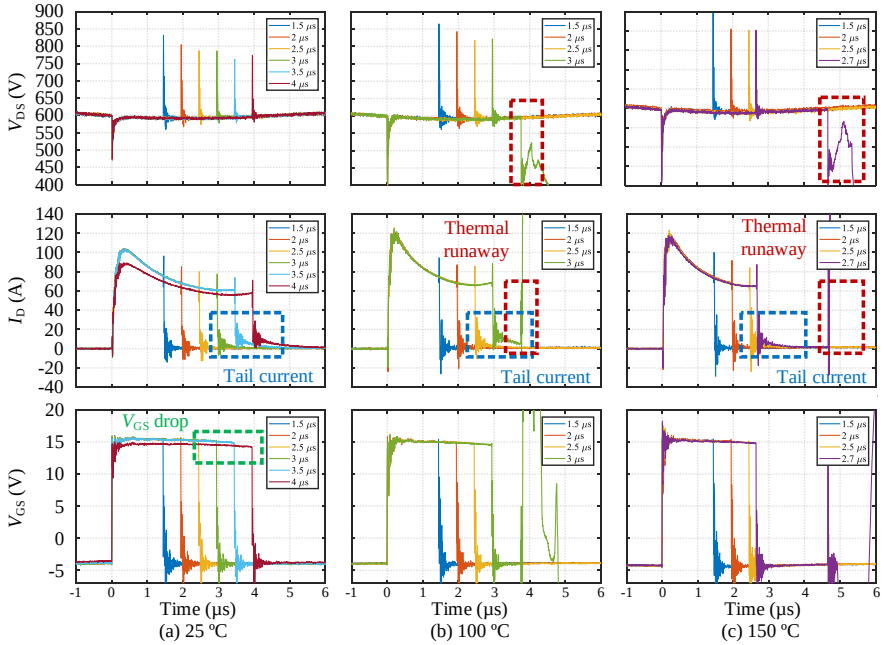


Fig. 3.1 Short-circuit tests (V_{DS}, I_D, and V_{GS} waveforms) with increasing t_{SC} at different initial case temperature (a) 25 ºC, (b) 100 ºC, and (c) 150 ºC [C1] [J3].

TABLE 3.1 - SUMMARY OF SHORT-CIRCUIT CAPABILITY WITH DIFFERENT CASE TEMPERATURES [J3]

Case Temperature (ºC)	Maximum SCWT (µs)	Critical Energy (J)
25	> 4	> 0.15
100	3	0.13
150	2.7	0.12

testing conditions have been: V_{DC} = 600 V, t_{SC} = 2.2 µs, V_{GS} = +15 V/-4 V, and R_G = 20 Ω.

3.2 Impact on the Static and Dynamic Characteristics

In order to evaluate the impact of short-circuit degradation on the normal operating performance of the DUTs, the variation of static and dynamic characteristics under repetitive short-circuit tests have been analysed, respectively.

The static characteristics of the DUT, including V_{th}, I_{GSS}, I_{DSS}, and $R_{DS,on}$, were measured with the power device analyser (B1506A, Keysight), which has been mentioned in Section 2.2. The static characterization was performed on the fresh DUT initially. Then after every 10 short-circuit repetitions, the static characteristics were measured again.

Fig. 3.2 presents the short-circuit waveforms (I_D and V_{GS}) every 20 repetitions and the test stops at 140 [J3]. Similarly to Fig. 2.10, the peak I_D and on-state V_{GS} decrease with the number of short-circuit repetitions, indicating the same degradation mechanism. The non-negligible I_{GSS} created a voltage drop across the R_G, thereby reducing the gate-source effective voltage (V_{GS_E}). This was shown as a decrease in the on-state V_{GS} during short-circuit test, which ended up in an I_D decrease. In other words, considering the influence of I_{GSS}, the V_{GS_E} on the device can be expressed by the output voltage of the gate driver (V_{driver}) as follows:

$$V_{GS\_e} = V_{driver} - R_G \times I_{GSS} \tag{3.1}$$

The measured I_{GSS} with the power device analyser verifies this degradation phenomenon and its variation relative to the number of short-circuit repetitions is shown in Fig. 3.3 [J3]. When the V_{GS} is set to 15 V, the I_{GSS} increases from 4.87 pA to 6.33 mA between the 20th and the 30th repetition. It continues to increase after 40 repetitions but decreases a bit after 50 repetitions. Thereafter, the I_{GSS} increases rapidly and the value at V_{GS} = 15 V reaches 100 mA after 140 repetitions.

Every 10 short-circuit repetitions, the I_D-V_{GS} curve, i.e. threshold voltage (V_{th}) was also measured and its variation is shown in Fig. 3.4 (a), which mainly consists of three stages. The V_{th} shifts positively from the initial state to the state after 20 repetitions. A possible explanation for this phenomenon could be the electrons trapping. To be specific,

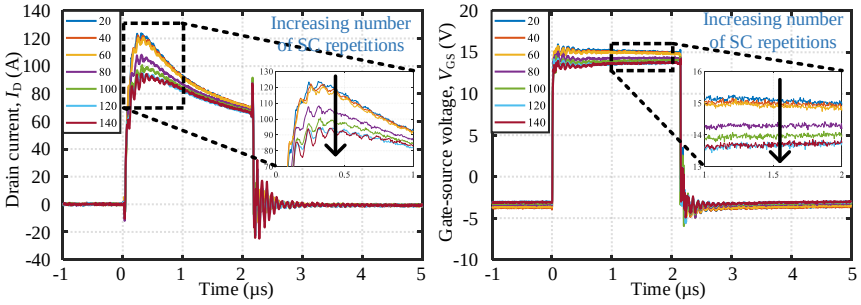


Fig. 3.2. Drain-source voltage (V_{DS}) and drain current (I_D) waveforms during repetitive short-circuit tests (20th - 140th repetition at 25 °C) [J3].

the thermally-grown gate oxide (i.e. the SiO_2 layer between substrate and polysilicon) contains four types of positive charges: trapped oxide charge (Q_T), mobile charge (Q_m), interface state charge (Q_I), and fixed oxide charge (Q_F) as shown in Fig. 3.4 (b) [13]. Due to the reduced thickness of the gate oxide, the electric field across it could be very high when a positive V_{GS} is applied and thereby, the electrons could tunnel into or through the gate oxide. This so-called Fowler-Nordheim tunnelling mechanism could be used to explain the V_{th} shift under short-circuit conditions [64] [84]. The increase in the net negative charge, such as electron trapping, can lead to V_{th} shift positively and it can be expressed as (3.2) where V_{thi} is the initial threshold voltage, Q_{ox} is the total charges in gate oxide layer (i.e. the sum of Q_T, Q_m, Q_I, and Q_F), and C_{ox} is the corresponding capacitance of gate oxide layer [13].

$$V_{\mathrm{th}} = V_{\mathrm{thi}} - \frac{Q_{\mathrm{ox}}}{C_{\mathrm{ox}}} \tag{3.2}$$

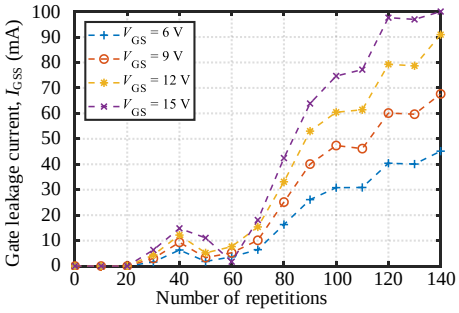
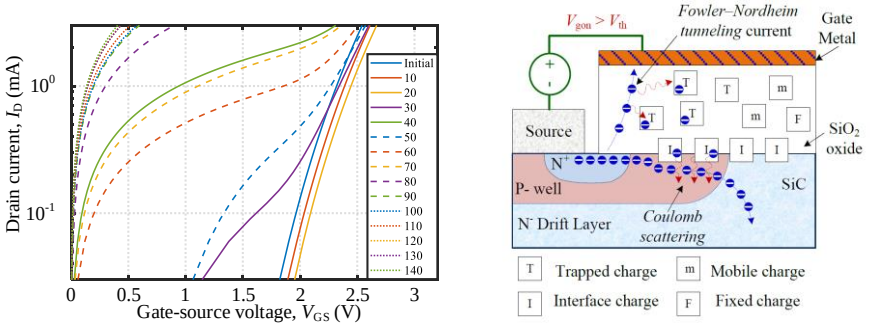


Fig. 3.3. Gate leakage current (from static characteristics measurement) versus the number of short-circuit repetitions [J3].



(a) (b)

Fig. 3.4. (a) I_D-V_{GS} curves variation from the initial state to the state after 140 short-circuit repetitions [J3]; (b) Multiple types of charges in the gate oxide layer and the schematic of Fowler-Nordheim tunnelling [13].

In the second phase of Fig. 3.4 (a), i.e. after 30 repetitions, the V_{GS} gradually decreases in the case of the same I_D. Since the drain and gate terminals are internally short-connected during the measurement, a possible cause of this may be that a conductive path between gate and source is built; this leakage current contributes a part of the I_D and the curves cannot be regarded as I_D-V_{GS} anymore. The last phase is the short-circuit repetitions from the 80th one to the 140th one, in which the conductivity between gate and source terminal increases further with the number of repetitions.

Another key parameter of static characteristics is the I_D-V_{DS} curve (output characteristics). According to the datasheet of the DUT, when the V_{GS} is set to 15 V and the I_D is equal to 15 A, its on-state resistance ($R_{DS,on}$) can be calculated. Fig. 3.5 (a) presents the impact of repetitive short-circuit tests on the $R_{DS,on}$ (in red) and its value increases with the number of repetitions [J3]. It might come from two parts; one is the positive shift of V_{th} and the other one is the reduction of gate-source effective voltage (V_{GS_E}), which is measured at the same time with power device analyser. As can be seen in Fig. 3.5 (a), although the V_{GS_E} keeps 15 V from initial state to the state after 20 repetitions, the $R_{DS,on}$ still increases a bit due to the V_{th} positive shift as mentioned above. From the point after 30 repetitions, the measured V_{GS_E} on the DUT starts to be lower than the setting value 15 V (i.e. $V_{GS\_E} < V_{GS\_SET}$ = 15 V) and this causes the further increase of $R_{DS,on}$. Apart from these reasons, another possible explanation might be the reduced mobility from increased oxide charge scattering, which still needs to be verified.

As pointed out previously in Section 2.3, the I_{GSS} can be considered as a suitable short-circuit degradation indicator and it affects the on-state V_{GS} during short-circuit test, especially at the end of the pulse. Since the on-state V_{GS} could be monitored directly during repetitive short-circuit tests, the correlation between the on-state V_{GS} and I_{GSS} is investigated. The I_{GSS} measured with the power device analyser (V_{GS_SET} = 15 V) increases with the number of repetitions as shown in Fig. 3.5 (b) and the short-circuit V_{GS} at t = 2 µs decreases at the same time. When the I_{GSS} reaches 100 mA after 140 repetitions, the V_{GS} decreases by 9.3% to 13.6 V (compared to the initial value 15 V).

To further verify the short-circuit degradation process and this correlation between I_{GSS} and V_{GS}, another fresh DUT was used to perform the repetitive short-circuit tests

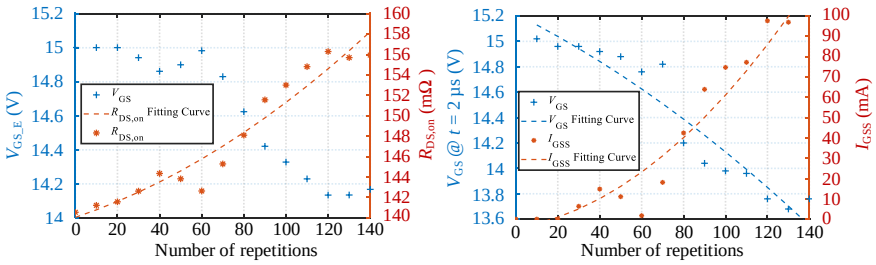


Fig. 3.5. (a) Increased $R_{DS,on}$ with the number of short-circuit repetitions; (b) correlation between the V_{GS} at t = 2 µs during short-circuit tests and the I_{GSS} measured with power device analyser [J3].

with the same settings. Considering the I_{GSS} measured with the power device analyser might be slightly different from the I_{GSS} during short-circuit tests, another probe is put before R_G to obtain the gate current I_G, similarly to Fig. 2.11. Therefore, the average gate leakage current from t = 1 µs to 2 µs (I_{GSS_AVG}) can be calculated and the correlation between I_{GSS_AVG} and on-state V_{GS} at t = 2 µs is provided in Fig. 3.6 [J3]. When the V_{GS} at t = 2 µs decreases to the same value (13.6 V) as the previous DUT, the number of short-circuit repetitions (N_{SC}) is equal to 124, which indicates similar degradation process. During the last short-circuit test (N_{SC} = 124), the I_{GSS_AVG} reaches 73.35 mA while the I_{GSS} measured by static characterization is 100 mA. Therefore, the on-state V_{GS} close to the end of the pulse can be used as the parameter to monitor the degradation process during repetitive short-circuit tests.

To evaluate the impact of short-circuit degradation on the dynamic characteristics, double pulse tests (DPTs) were combined together with repetitive short-circuit tests for another pristine device. Specifically, the repetitive short-circuit tests were performed with the same selected condition as before (V_{DC} = 600 V, t_{SC} = 2.2 µs, and T_C = 25 °C). Every 20 short-circuit repetitions, the dynamic characteristics were measured with DPT and its schematic is provided in Fig. 3.7 [J3]. The freewheeling diode (D_1) is a 1.2 kV/20 A SiC

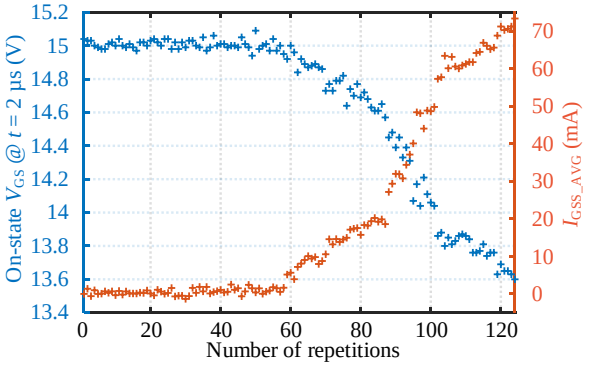


Fig. 3.6. Correlation between the V_{GS} at t = 2 µs and the I_{GSS_AVG} during repetitive short-circuit tests [J3].

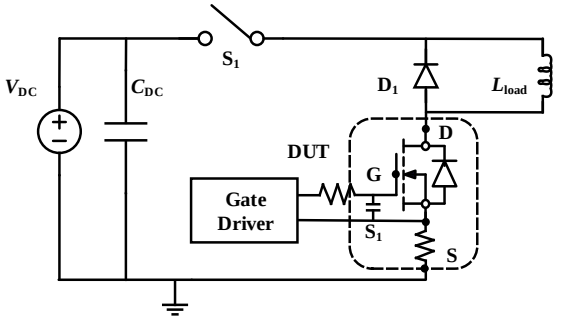


Fig. 3.7. Schematic of double pulse test [J3].

Schottky diode (APT20SCD120, Microsemi) and the load inductance (L_{load}) is 620 µH. The same gate driver (CRD-001, Cree) is used to drive the DUT with +15 V/-4 V output voltage. With the intent to avoid the oscillation during switching transient, a 4.7 nF gate capacitance is connected in parallel to compensate the parasitic inductance in the gate loop and the used gate resistance is 20 **Ω** to slow down the switching. The experimental DTP waveforms, including V_{DS}, I_D and V_{GS} are shown in Fig. 3.8 [J3]. After the first pulse time (t_1 = 18 µs), the I_D increases to the rated value of DUT (i.e. 22 A). Then the DUT is turned off for a period of 6 µs (t_2 = 6 µs), followed by the second narrow pulse (t_3 = 6 µs). The last DPT was performed after 110 short-circuit repetitions since the on-state V_{GS} at t = 2 µs during short-circuit test decreased to 13.6 V, and after that, the short-circuit tests were stopped.

The waveforms of DPT during turn-on and turn-off transient before and after 110 short-circuit repetitions are presented in Fig. 3.9 and Fig. 3.10, respectively. It can be observed that the DUT turns on slower and turns off faster than before [J3]. A possible explanation for this finding might be the reduction in effective V_{GS_E}. Before the turn-on

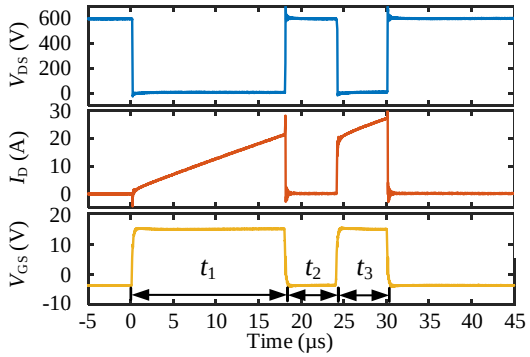


Fig. 3.8. Experimental waveforms of double pulse test (V_{DS}, I_D, and V_{GS}) [J3].

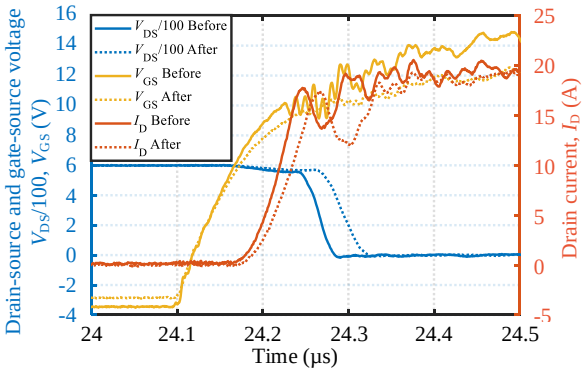


Fig. 3.9. Drain-source voltage, drain current and gate-source voltage waveforms during turn-on transient before and after 110 repetitions [J3].

transient, no I_D can flow through the DUT until the V_{GS} on the DUT exceeds its V_{th}. Since the effective V_{GS_E} on the DUT becomes lower after short-circuit tests, the V_{GS_E} needs a longer time to increases from 0 to V_{th} and this results in the increasing delay of I_D. Thereafter, when the V_{GS_E} exceeds the V_{th}, the I_D can be expressed as (3.3) where μ_{ni} is the inversion layer mobility, C_{ox} is the gate oxide capacitance, Z is the channel width, and L_{CH} is the channel length. In the case of the same t (e.g. $t = t_f = 24.2$ μs), the lower $V_{GS\_E}(t_f)$ after short-circuit tests leads to the lower $I_D(t_f)$ and this result agrees with the I_D curve shown in Fig. 3.9 [J3].

$$I_D(t) = \frac{\mu_{ni} C_{ox} Z}{2L_{CH}} [V_{GS}(t) - V_{th}]^2 \tag{3.3}$$

Apart from this, the reduction in transconductance, which comes from the increased scattering trapped charges and the decreased mobility, might also reduce the I_D and it needs to be further investigated. Similarly to the turn-on transient, the V_{GS_E} needs shorter time to decrease to V_{th} and thereby, after short-circuit degradation, the I_D decreases earlier than before as provided in Fig. 3.10 [J3]. At last, Fig. 3.11 presents the changes in switching loss with the number of short-circuit repetitions and the reduction

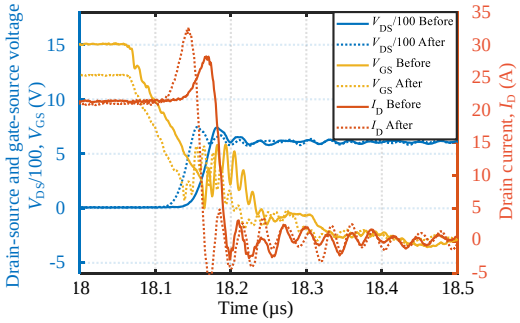


Fig. 3.10. Drain-source voltage, drain current and gate-source voltage waveforms during turn-off transient before and after 110 repetitions [J3].

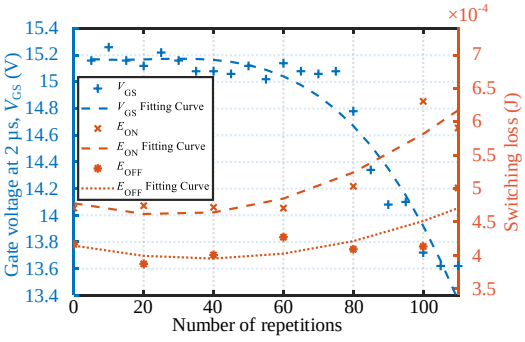


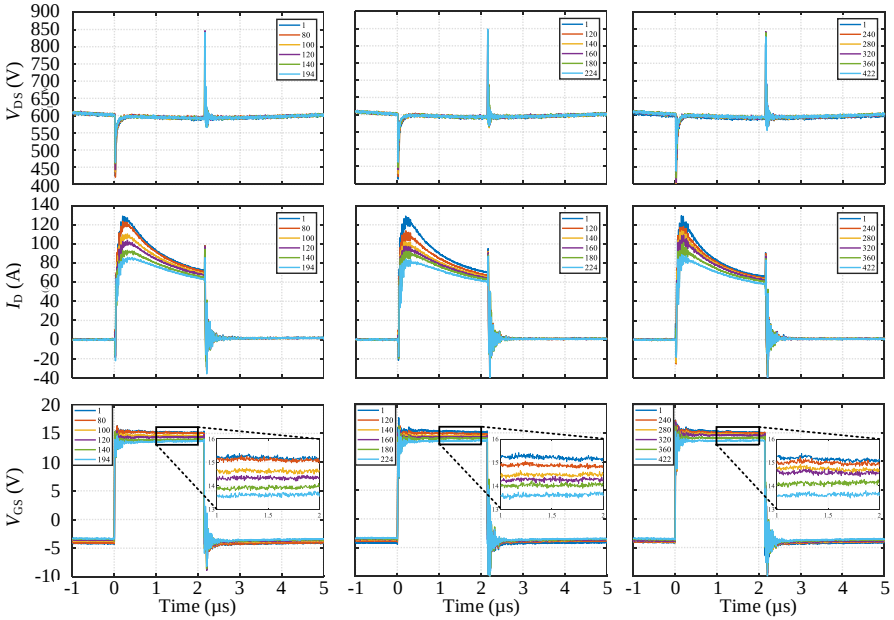
Fig. 3.11. Variation of switching loss and gate-source voltage reduction with the number of repetitions [J3].

of on-state V_{GS} at t = 2 µs is also included at the same time to show the degradation process. After 80 short-circuit repetitions, the turn-on loss (E_{on}) increases clearly while the on-state V_{GS} has an obvious decrease. In contrast, the turn-off loss (E_{off}) does not change significantly with short-circuit degradation and the E_{off} only increases slightly after 110 repetitions since the I_D spike becomes higher during turn-off transient [J3].

3.3 Case Temperature Influence Consideration

When the device works in the field application, its case temperature might vary and the case temperature influence on the short-circuit degradation needs to be considered. The repetitive short-circuit tests were performed for three pristine DUTs with the same selected conditions as before (V_{DC} = 600 V, V_{GS_SET} = +15 V/-4 V, and t_{SC} = 2.2 µs) except different T_C (i.e. 25 ºC, 100 ºC, and 150 ºC). The V_{DS}, I_D, and V_{GS} waveforms during short-circuit tests at T_C = 25 ºC, 100 ºC, and 150 ºC are displayed in Fig. 3.12, respectively [J3].

Similarly, the reduction in I_D and on-state V_{GS} increase is found in each case. When the on-state V_{GS} at t = 2 µs decreases from 15 V to 13.6 V, the tests are stopped. It is worth mentioning that the number of short-circuit repetitions (N_{SC}) increases from 194 to 224, and then 422 when the initial T_C increases from 25 ºC to 100 ºC, and then 150 ºC. Fig. 3.13 (a) shows V_{GS} (at t = 2 µs) reduction with the number of short-circuit repetitions



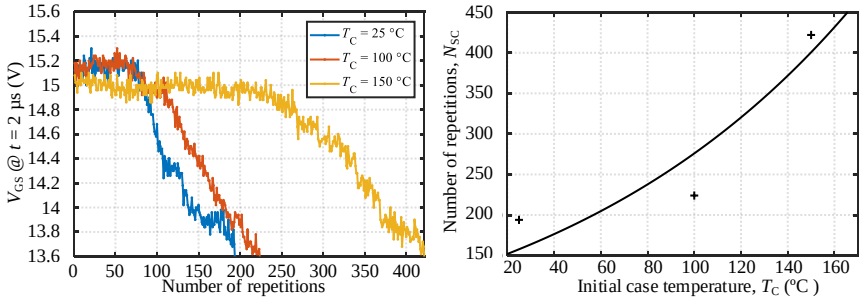
(a) 25 ºC (b) 100 ºC (c) 150 ºC

Fig. 3.12. V_{DS}, I_D, and V_{GS} waveforms of repetitive 2.2 µs short-circuit tests at different initial case temperatures: (a) 25 ºC, (b) 100 ºC, and (c) 150 ºC [C1] [J3].

at different T_C. Furthermore, the relationship between N_{SC} and T_C can be initially fitted with (3.4) and it is plotted in Fig. 3.13 (b) [J3].

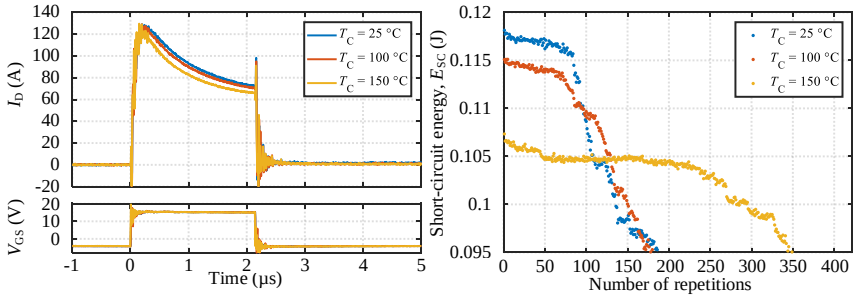
$$N_{SC} = f(T_c) = 130.9 \times \exp(0.007457 \times T_c) \tag{3.4}$$

Generally, it might be guessed that the increase in T_C could result in an earlier failure (i.e. smaller N_{SC}). However, it is not as expected in SiC MOSFETs; because of its negative temperature coefficient, when the T_C increases, the reduced I_D leads to the lower short-circuit energy (E_{SC}). So as to compare intuitively, the experimental waveforms (I_D and V_{GS}) during the first short-circuit test at different T_C are presented in Fig. 3.14 (a) together. All three cases have the same V_{GS}, but the different I_D. When T_C is equal to 150 ºC, the I_D is the lowest one. Similarly, the I_D at 100 ºC is lower than the one at 25 ºC. Furthermore, the short-circuit energy (E_{SC}) is calculated for each repetition (from t = 0 µs to 2.2 µs) in terms of different T_C as can be seen in Fig. 3.14 (b). At the very beginning, i.e. the N_{SC} is less than 100 repetitions, the E_{SC} is subjected to the T_C; the DUT at 25 ºC has the highest energy and the E_{SC} at 100 ºC is higher than the one at 25 ºC. When the



(a) (b)

Fig. 3.13. (a) V_{GS} reduction with the number of repetitions at T_C = 25 ºC, 100 ºC, and 150 ºC; (b) the relationship between the number of repetitions and T_C [C1] [J3].



(a) (b)

Fig. 3.14. (a) I_D and V_{GS} waveforms of the first short-circuit repetition at different T_C; (b) short-circuit energy reduction with the number of short-circuit repetitions at different T_C [C1] [J3].

N_{SC} is larger than 100 repetitions, the E_{SC} depends on the short-circuit degradation process. The reduction in V_{GS} causes the lower I_D and E_{SC} [J3].

Although as pointed out above that the higher T_C leads to lower E_{SC} and larger N_{SC}, it is not clear how the E_{SC} affects the N_{SC}. Therefore, in the following part, the thermal behaviour during short-circuit tests is analysed at different initial T_C. Since it is not easy to measure the very fast temperature transient during short-circuit tests (several microseconds), a 1-D thermal model was used to estimate the transient temperature at T_C = 25 ºC, 100 ºC, and 150 ºC, respectively [J3].

Fig. 3.15 shows a sketch of the 1-D thermal model. The junction depth is equal to 0.6 µm (i.e. x_j = 105.6 µm) and the depletion width of P- well region (x_p) is omitted here. The N- drift layer width (x_n) is calculated with (3.5) where ε_s is the SiC dielectric constant, which is equal to $9.66\times8.85\times10^{-12}$ F/m, q is the electron charge, and N_d is the doping concentration in the N- drift region, which is estimated as 1×10^{16} cm^{-3} [85].

$$x_n \approx \sqrt{\frac{2\varepsilon_s}{qN_d} V_{DS}} \tag{3.5}$$

During short-circuit condition, the V_{DS} is applied and the distribution of the electric field across the depletion width ($x_j \le x \le x_n$) can be calculated with (3.6). Meanwhile, the on-state I_D can flow through the DUT and this time-dependent value is derived from the experimental waveform provided above in Fig. 3.14 (a) so as to obtain accurate results. Considering the active chip area A (3.478 cm^2), the heat generation rate $Q(x, t)$ could be calculated with (3.7), in which the V_{DS} is assumed to be constant with time.

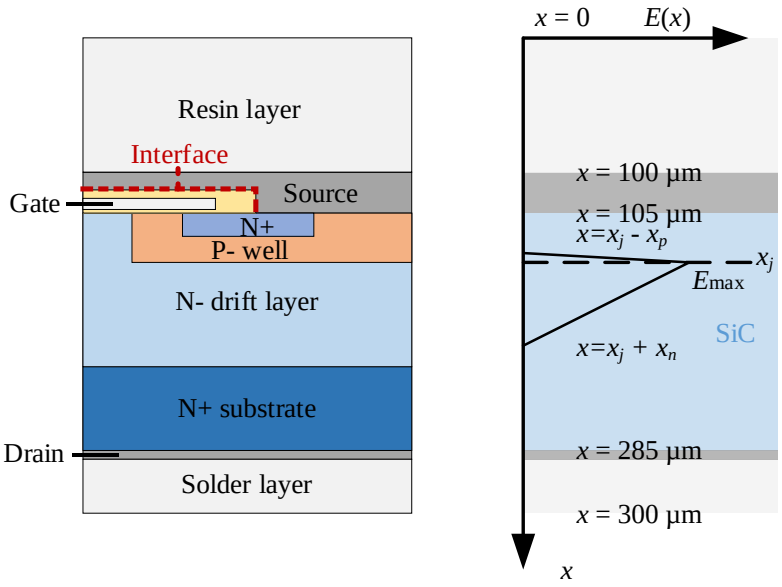


Fig. 3.15. 1-D heat propagation thermal model of the SiC MOSFET [J3].

$$E(x) = \frac{qN_d}{\varepsilon_s}\left(x_n + x_j - x\right) \tag{3.6}$$

$$Q(x,t) = E(x) \cdot \frac{I_D(t)}{A} \tag{3.7}$$

Then the typical heat equation can be used to simulate the transient temperature distribution as (3.8) where λ is thermal conductivity, ϱ is the physical density, and the c is the specific heat of the materials. Their values in SiC material are set according to the equations from (3.9) to (3.11) and the ones in other materials are listed in Table 3.2 [86] [J3].

$$\frac{\partial}{\partial x}\left(\lambda(T) \cdot \frac{\partial T}{\partial x}\right) + Q(x,t) = \rho \cdot c(T) \cdot \frac{\partial T}{\partial t} \tag{3.8}$$

$$\lambda(T)_{SiC} = (0.0003 + 1.05 \times 10^{-5} T)^{-1} \quad (W/m \cdot K) \tag{3.9}$$

$$\rho_{SiC} = 3.211 \ \ (g/cm^3) \tag{3.10}$$

$$c(T)_{SiC} = 925.65 + 0.3772T - 7.929 \times 10^{-5} T^2 - \frac{3.1946 \times 10^7}{T^2} (J/kg \cdot K) \tag{3.11}$$

To ensure that the simulation settings are matched with the actual experimental condition, the V_{DS} is 600 V and the t is set to increase from 0 to 2.2 µs in steps of 4 ns. Thanks to the very short pulse time, the top and the bottom point (x = 0 µm and 300 µm) of the model are kept the same value corresponding to its T_C (i.e. 25 °C, 100 °C, and 150 °C).

The simulation results are plotted in Fig. 3.16 and the maximum junction temperature rise ($\Delta T_j = T_j - T_C$) reduces from 554.1 °C to 534.8 °C and then 506.7 °C when the T_C increases from 25 °C to 150 °C. This also in agreement with the experimental results that the short-circuit energy (E_{SC}) reduces with the T_C increase [J3]. Considering the

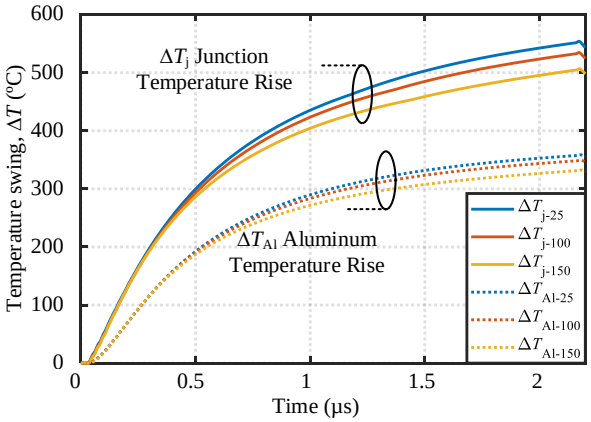


Fig. 3.16. Junction temperature and aluminium temperature rise at initial T_C = 25 °C, 100 °C, and 150 °C [J3].

TABLE 3.2 - THERMAL SIMULATION SETTINGS [J3]

Material	λ (W/m·K)	ϱ (g/cm3)	c (J/kg·K)
Resin	0.2	1.8	1000
Aluminum	167	2.7	900
Solder	50	7.4	190

short-circuit degradation process (i.e. N_{SC}) is more related to the ΔT_j, a likely cause of this may be the different CTE between Aluminium and SiO_2 dielectric, which induces a mismatch in the Al/SiC interface as marked in the red dotted line in Fig. 3.15. This hypothesis will be discussed and validated in Chapter 5.

Typically, the Coffin-Manson-Arrhenius law is used to estimate the number of cycles to failure (N_f) of bonding wires and solder layers under temperature cycling conditions and it can be expressed as (3.12) where A and α are parameters ($\alpha < 0$), E_a is the activation energy, K_B is the Boltzmann's constant, and T_{jmean} is the mean temperature. If this equation is used to the short-circuit degradation, the expected number of repetitions (N_{SC}) decreases with the larger temperature gradient ΔT_j, which is induced by a lower initial T_C.

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot \exp\left(\frac{E_a}{K_B \cdot T_{jm}}\right) \tag{3.12}$$

3.4 Summary

This chapter has described the investigation on the impact of short-circuit degradation on the normal operating performance of SiC MOSFETs and the initial case temperature influence on the degradation process has been included. At first, the critical short-circuit energy at three different case temperatures (25 ºC, 100 ºC, and 150 ºC) was confirmed through increasing the t_{SC} step by step and the short-circuit condition for repetitive tests below critical value was selected. Both static and dynamic characteristics measurements were combined with repetitive short-circuit tests at 25 ºC case temperature, separately. As the number of short-circuit repetitions increased, the threshold voltage shift and the increase in gate leakage current and on-state resistance were observed and they can be explained by the electron trapping mechanism and formed conductive path between gate and source terminal. Besides, the on-state gate-source voltage during short-circuit test could be used to monitor the degradation process. When the value was reduced by 9.3%, the short-circuit tests were stopped. Then the dynamic characteristics have been compared before and after the short-circuit degradation by performing double pulse tests. The turn-on and turn-off transient waveform showed a delay and advance respectively as the number of short-circuit repetitions increased, which might come from the reduction in the gate-source effective voltage and the turn-on loss increases correspondingly. Concerning the case temperature influence, the experimental results show that the DUT can withstand a larger number of short-circuit repetitions when the case temperature is higher. This finding gives the opposite trend compared to

the temperature-dependent short-circuit capability. When the case temperature increases, the reduced drain current leads to a lower short-circuit energy. To investigate how the short circuit energy affects the degradation, a 1-D thermal model was used to roughly estimate the chip temperature evolution during the first repetitive short-circuit tests. At higher case temperature, the maximum junction temperature rise was reduced and the mismatch of the coefficients of thermal expansion between Al and SiO_2 might be the cause of degradation, which would be further discussed in the following chapters.

Chapter 4

Impact of Short-Circuit Degradation on the Remaining Useful Life

As a conventional approach among accelerated life tests (ALTs), power cycling (PC) tests are typically used to evaluate the wear-out ageing mechanism and estimate the lifetime of power devices. In this chapter, first, a brief introduction about power-cycling test and its setup in the laboratory is given. Then, the impact of short-circuit degradation on the power-cycling conditions is analysed utilizing the mixed PC tests with repetitive short-circuit tests. Thereafter, with a different number of short-circuit repetitions, its impact on the remaining useful life (RUL) is presented. The relevant publications included in this chapter are [J2], [J4], and [C2].

4.1 Introduction of Power Cycling Test

Power semiconductor devices are subjected to a combination of influences under specific applications during service life, and this so-called mission profile has an effect on the reliability and lifetime, which involve both performance parameters (e.g. voltage and current) and environmental factors (e.g. temperature). Bonding wires lift-off and solder joints degradation are two common failure locations, which are generally attributed to the temperature swing together with large difference CTE of different materials inside the devices. Fig. 4.1 presents an example of the junction temperature mission profile

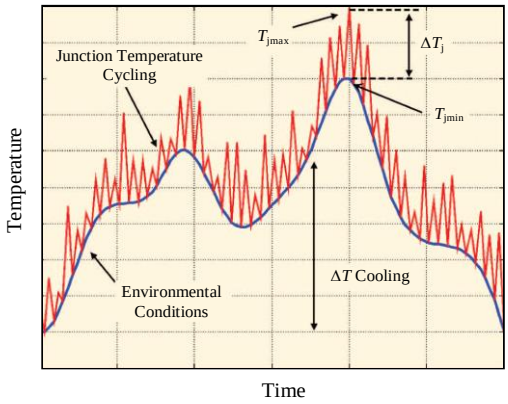


Fig. 4.1. Example of junction temperature mission profile [87].

taking into account the environmental conditions [87]. To achieve a junction temperature swing and accelerate the wear-out degradation, DC-based PC test can be an effective approach and adopted in the industry. Fig. 4.2 shows a typical chip junction temperature evolution of DC-based PC test. In this case, the DUT is heated up by the conduction loss (P_{cond}) and then cooled down by the external cooling. The maximum, minimum, and mean junction temperature are represented as T_{jmax}, T_{jmin}, and T_{jmean}, separately and shown in Fig. 4.2. As mentioned in Section 3.3, the T_{jmean} and junction temperature swing (ΔT_j) are typically used as the Coffin-Manson-Arrhenius law to estimate the lifetime of devices.

Depending on the heating method, the P_{cond} can come from the inverse body diode conduction, inverse or forward MOSFET conduction. To reflect the real operating condition, the forward MOSFET conduction is used; when the device turns on, the load current flows through the channel, which causes the conduction loss and heat generation. On the other hand, junction temperature (T_j) needs to be measured or estimated during the test to obtain initial test condition and monitor device degradation.

If it is available to direct access to the chip through optical or physical contact, such as openable power modules with transparent gel encapsulation, T_j could be measured directly. One way is to use the optical fibre thermal sensor in direct contact to the surface of the chip; it allows to retain the insulating gel and obtain the complete periodical T_j waveforms. Nevertheless, the temperature distribution on a single chip might be slightly different and the measured result may deviate from the average T_j of the whole chip depending on the fibre location. Besides, the temperature sensor can be fabricated on the chip surface [88], such as a temperature-dependent diode, which provides accurate measurements and can be used for moulded devices. However, it decreases the active area of the chip and increases the complexity of the device since additional contact pads and terminals are needed. Another way is to use infrared (IR) cameras to measure T_j. This method obtains the temperature distribution map and enables a better understanding of the temperature flow. The drawbacks are the need to remove the insulating gel material

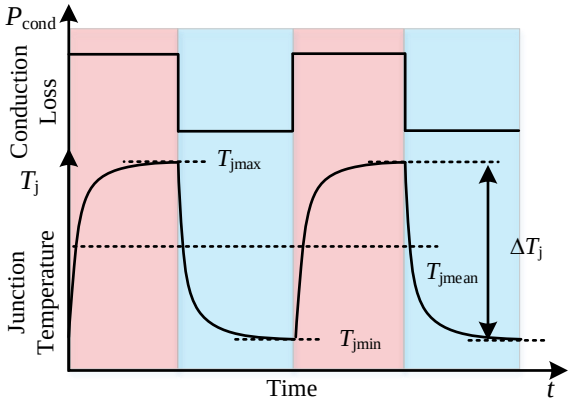


Fig. 4.2. Typical junction temperature evolution of the power-cycling test.

and spray thermographic paint to ensure uniform emissivity of the surface. Moreover, the paint thickness needs to be kept uniform to avoid its impact on the measurement.

For the devices which cannot be opened or directly accessed, the T_j estimation or indirect measurement are needed. Through the measured case temperature (T_C) and thermal network model, the T_j can be estimated. Since the solder layer degradation may lead to an increase in thermal resistance from the junction to the case, a periodical re-calibration is necessary during the PC test [89]. In addition, the temperature-sensitive electrical parameters (TSEPs) of the devices can be used to measure the T_j indirectly. Among these, the most common parameter is the on-state drain-source voltage drop ($V_{DS,on}$) or on-state resistance ($R_{DS,on}$). Since it consists of both chip-related and package-related voltage drop, the package-related degradation such as bonding wire lift-off can increase the $V_{DS,on}$ and the relationship between $V_{DS,on}$ and T_j needs to be re-calibrated periodically, which makes the test procedure complex. To mitigate this issue, a low-current injection is used in IGBTs (such as thousandth of the device rated current). However, such a method is not suitable for SiC MOSFETs due to the very small $V_{DS,on}$ and the sensitive gate oxide (e.g. V_{th} shift). Benefiting from the body diode in the MOSFET, the body diode voltage drop (V_{SD}) at low current injection could be a promising method for SiC MOSFETs, which has been used in [59] and [60]. Notably, when the gate is zero bias, the MOS-channel might also conduct current and cause a variation in the relationship between the T_j and the V_{SD}. Thus, a reasonable negative V_{GS} to completely turn off the channel is needed, ensuring accurate T_j estimation.

In conclusion, the optical fibre method was chosen for the modules, which allow the access to the chips through the gel, and the body-diode voltage drop method was chosen for the discrete devices. Fig. 4.3 and Fig. 4.4 show the schematic of the power-cycling test utilizing corresponding T_j measurement approaches.

As can be seen in Fig. 4.3, a DC power supply (SM 45-140, Delta) gives a constant current I_{load} to the system and two DUTs operate in a complementary mode with 1 ms overlap to maintain a stable I_{load} during switching transient. Their control signals are generated by an FPGA board and each DUT has an independent gate driver (CRD-001, Cree), which can adjust both negative and positive output voltage in order to meet

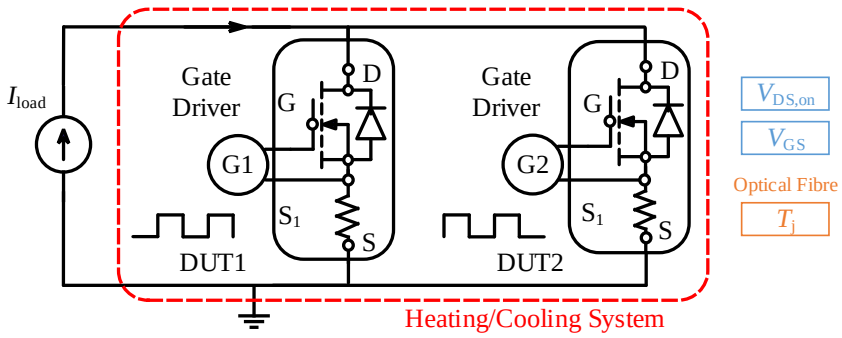


Fig. 4.3. DC-based power-cycling test with the optical fibre T_j measurement [J2].

different V_{GS} requirement. By changing the on-state and off-state time duration (t_{on}/t_{off}) of each period and the I_{load}, the needed ΔT_j can be achieved.

A heat/cooling system, consisting of an external heater and forced-air cooling fan, can adjust the T_{jmean} and maintain stable case temperature (T_C). During the test, the V_{DS} and V_{GS} are monitored with an oscilloscope (HDO6054-MS, Teledyne LeCroy) and a signal conditioner unit (CoreSens, Opsens) together with two optical fibre thermal sensors (OTG-F-10, Opsens) are used to monitor the T_j waveforms. Fig. 4.5 showcases the way we measured T_j with optical fibre thermal sensor.

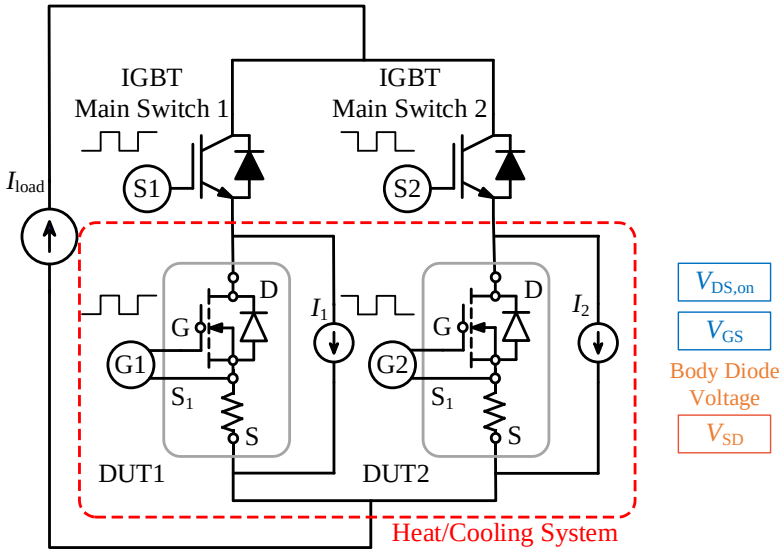


Fig. 4.4. DC-based power-cycling test with T_j measurement through body diode voltage drop (V_{SD}) [J4].

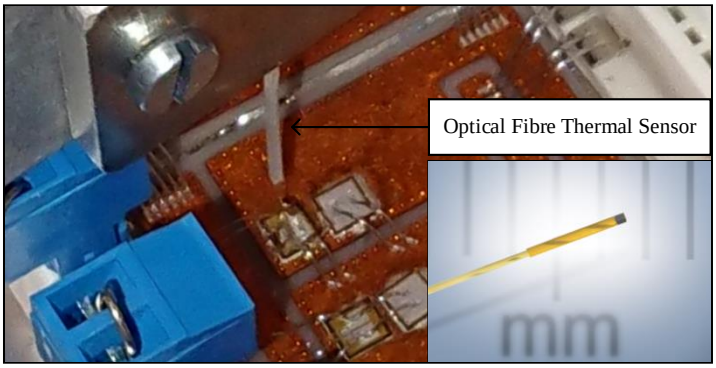


Fig. 4.5. An example of junction temperature measurement using optical fibre thermal sensor.

For the PC test with T_j measurement through V_{SD}, two main switches are included in the power loop, separately, which enable the low-current measurement by opening the power circuit as shown in Fig. 4.4. Two 1200 V/85 A IGBTs in a power module from IXYS are selected as the main switches and their corresponding independent gate drivers (CRD-001, Cree) receive the same complementary control signals as the two DUTs. The microcontroller board (Mbed LPC1768, ARM) provides the control signals as well as streams the measured real-time data to the MATLAB interface. The $V_{DS,on}$ are measured primarily using operational amplifiers and 14-bit analogue-to-digital converters (AD7367, Analog Devices) [90] and the measurement circuit is similar to [91]. As shown in that paper, a diode is used in the measurement circuit to protect high voltage when the DUT is in the off-state, and at the same time, a small current injects through the body diode to measure the V_{SD} and obtain the T_j. Similarly to the first PC test bench, the I_{load} and t_{on}/t_{off} are used to achieve the required initial ΔT_j and the T_{jmean} is mainly adjusted by the external heat/cooling system.

The following experimental tests in this chapter involve two types of DUTs. In Section 4.2, the DUT is a 1.2 kV/20 A three-phase SiC power module (CCS020M12CM2, Cree) with 2nd-generation planar gate and the T_j is measured through optical fibres. The layout of the module is shown in Fig. 4.6; six SiC MOSFET are named from S_1 to S_6, and the diodes are named from D_1 to D_6 [J2]. In Section 4.3, the DUT is a 1.0 kV/22 A SiC MOSFET (C3M0120100K, Cree) with the 3rd-generation planar gate and it has TO-247-4 discrete package with separate Kelvin source pin. The T_j is measured through the body diode voltage drop.

4.2 Mixed Power-Cycling/Repetitive Short-Circuit Test

Mixed power cycling test with repetitive short circuits can be performed to investigate the impact of short-circuit degradation on the power-cycling condition and further remaining useful life. Prior to this, the PC and SC test conditions are selected for this specific DUT. Table 4.1 summarises the test conditions for the PC test [J2].

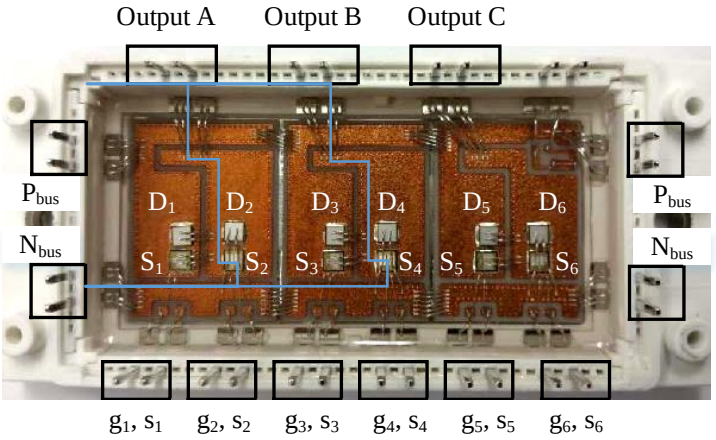


Fig. 4.6. Layout of the three-phase SiC module (1.2 kV/20 A) [J2].

The constant current (20 A) flows through each of two DUTs, alternatively and the on-state period of each DUT is set to 2 s. To achieve the needed temperature condition, the external heat/cooling system is set to 98 °C. Considering inevitable characteristics deviation of DUTs, the applied V_{GS} on two DUTs can be different to ensure that they have the same $V_{DS,on}$ and withstand the same thermal stress (i.e. ΔT_j). As for the conditions for repetitive short-circuit tests, first, the short-circuit capability of this DUT (S_5) is evaluated with increasing t_{SC} in steps of 0.2 µs (T_C = 25 °C, V_{DC} = 600 V, and V_{GS} = +20 V/-5 V). Fig. 4.7 presents the short-circuit waveforms, and the on-state V_{GS} (at the end of the pulse) begins to decrease when t_{SC} increases to 3.6 µs [J2]. Thereafter, the on-state V_{GS} reduces from 20 V to 18.5 V at t_{SC} = 4.4 µs. Similar to the approach in Section 3.1, the repetitive short-circuit test conditions for the DUTs were selected and they are listed in Table 4.2. To figure out the degradation process under this short-circuit

TABLE 4.1 - TEST CONDITION FOR THE POWER CYCLING TEST [J2]

Parameters	Value	Unit
Load Current (I_{load})	20	A
On-State and Off-State Time (t_{on}, t_{off})	2, 2	s
Initial Maximum Junction Temp. (T_{jmax})	162	°C
Initial Minimum Junction Temp. (T_{jmin})	104	°C
Initial Junction Temp. Swing (ΔT_j)	58	°C

TABLE 4.2 - TEST CONDITION FOR THE REPETITIVE SHORT CIRCUIT TEST

Parameters	Value	Unit
DC-Link Voltage (V_{DC})	600	V
Gate-Source Voltage (V_{GS})	+20/-5	V
Pulse Time (t_{SC})	3	µs
Initial Case Temperature (T_C)	25	°C

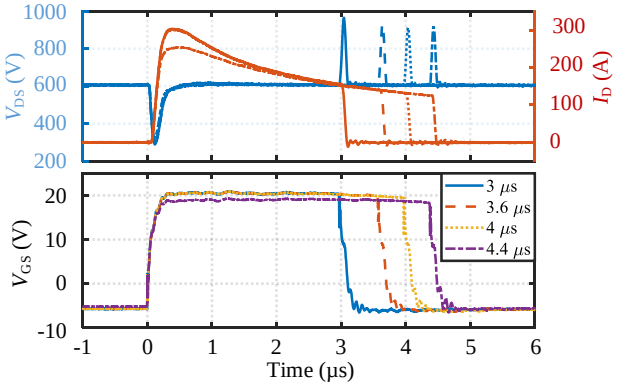


Fig. 4.7. Short-circuit waveforms of DUT S_5 with increasing t_{SC} [J2].

condition, another fresh DUT (S_6) was used to perform repetitive short-circuit tests with the selected condition listed in Table 4.2. At an increasing number of repetitions, the degradation indicator (i.e. V_{GS} at t = 2.8 µs, which is close to the end of the pulse time) decreases gradually as shown in Fig. 4.8 [J2]. After 143 repetitions, its value reduces from 20 V to 18 V and this strong relationship has been explained in previous chapters.

Thereafter, two fresh DUTs (S_2 and S_4) were adopted to perform the mixed power-cycling/short-circuit test and the test approach is presented in Fig. 4.9 [J2]. Initially, the static characteristics were measured with power device analyser. Due to the slightly different $R_{DS,on}$, the applied V_{GS} on DUT S_2 and S_4 was set to 18 V and 20 V, respectively to reach the same initial ΔT_j. Prior to the power-cycling test, 1 k cycles were spent to keep a stable temperature condition. Then power cycling tests were performed for both DUTs and the initial temperature conditions have been described in Table 4.1. After 15 k number of cycles, the power cycling test was stopped and, in agreement with the previous results in [61], the DUTs had not significantly been degraded yet. At this point, 50 times repetitive short-circuit tests were performed on DUT S_2 with the selected condition mentioned in Table 4.2. After this, both DUTs were power-cycled until failure happened on one of the DUTs. In other words, DUT S_4 was only stressed with power cycling for comparison purposes only.

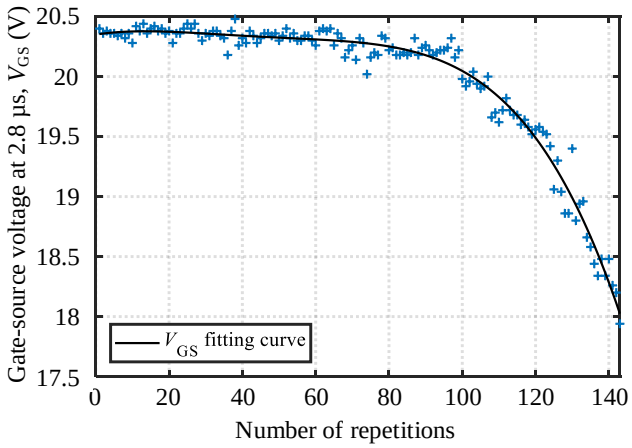


Fig. 4.8. Reduction of gate-source voltage at t = 2.8 µs (DUT S_6) with the number of repetitions increase [J2].

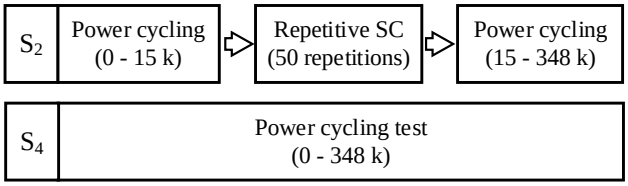
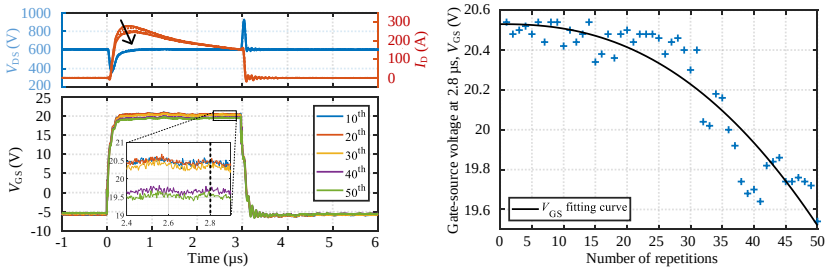


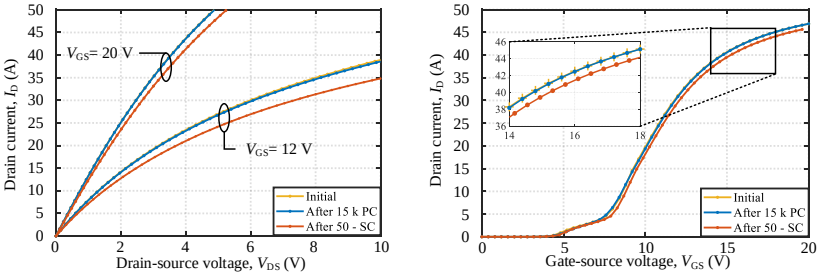
Fig. 4.9. The approach of mixed power-cycling/repetitive short-circuit test [J2].

The experimental waveforms of short-circuit tests with the 10th - 50th (in steps of 10) repetition are displayed in Fig. 4.10 (a) and a clear V_{GS} reduction appears at the 40th repetition [J2]. Similarly, the on-state V_{GS} at t = 2.8 µs decreases with the number of short-circuit repetitions as shown in Fig. 4.10 (b) and it reduces to 19.5 V after 50 repetitions. Fig. 4.11 and Fig. 4.12 show the static characteristics measured before starting



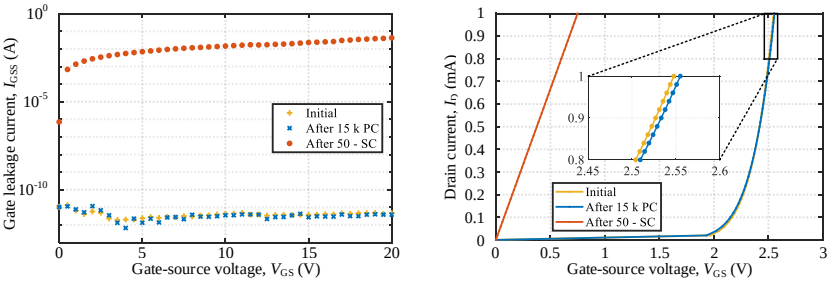
(a) (b)

Fig. 4.10. (a) Short-circuit waveforms of DUT S_2 from the 10th to the 50th repetition; (b) gate-source voltage at t = 2.8 µs versus the number of repetitions [J2].



(a) (b)

Fig. 4.11. (a) I_D-V_{DS} and (b) I_D-V_{GS} curves of DUT S_2 before the test, after 15 k power cycles, and after 50 short-circuit repetitions [J2].



(a) (b)

Fig. 4.12. (a) Gate leakage current and (b) threshold voltage of DUT S_2 before the test, after 15 k power cycles, and after 50 short-circuit repetitions [J2].

the power cycling test, after 15 k power cycles, and after 50 short-circuit repetitions (only for DUT S_2) [J2]. Both I_D-V_{DS} and I_D-V_{GS} curves show that the $R_{DS,on}$ increases slightly after short-circuit repetitions. Also, a significant increase in the I_{GSS} of DUT S_2 is observed after short-circuit tests and its value at V_{GS} = 20 V increases from 3.84 pA to 42.62 mA. For the threshold voltage, it shifts positively from 2.547 V to 2.555 V after 15 k cycles, which might be caused by the trapping mechanisms at the SiC/SiO_2 interface as explained in Section 3.2. Due to the non-negligible I_{GSS} induced by the short-circuit stress, the curve becomes linear, as a pure resistance between gate and source [J2].

Fig. 4.13 shows the $V_{DS,on}$ evolution of DUT S_2 and S_4 during the power-cycling test [J2]. Both DUTs have the same $V_{DS,on}$ from 0 to 15 k cycles. After 15 k cycles, the DUT S_2 is subjected to 50 short-circuit repetitions, then power cycling tests are started over for both DUTs. Although the settings of power-cycling test are kept the same as before, the measured $V_{DS,on}$ on DUT S_2 increases from 3.12 V to 3.34 V. Then its $V_{DS,on}$ increases faster than DUT S_4 until failure (N_f = 348 k).

The T_j waveforms at several number of cycles are selected and shown in Fig. 4.14. The figure clearly shows an increase in the T_{jmax} and ΔT_j of DUT S_2 after 50 short-circuit repetitions. Then it continues to increase with the number of cycles and at 334 k cycles, the T_{jmax} exceeds 175 °C. In contrast, the T_{jmax} and ΔT_j of DUT S_4 keep constant during

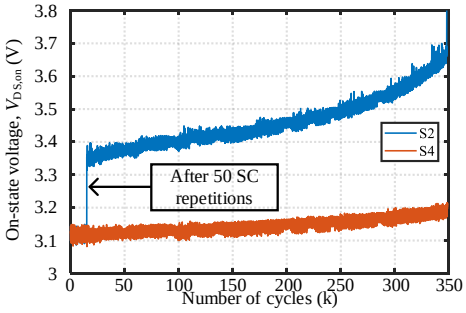
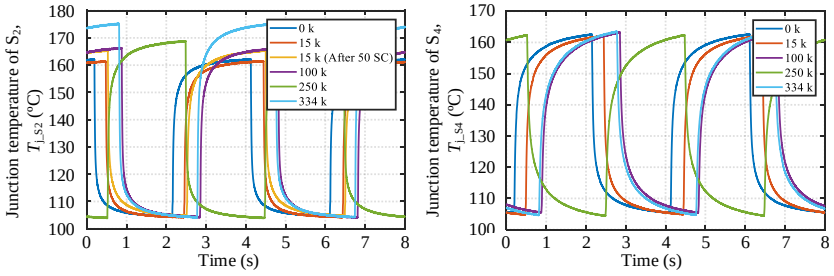


Fig. 4.13. Evolution of $V_{DS,on}$ throughout the mixed power-cycling test with/without 50 short-circuit repetitions performed at 15 k cycles [J2].



(a) (b)

Fig. 4.14. T_j waveforms of power-cycling test at 0 k, 15 k, 100 k, 250 k, and 334 k: (a) DUT S_2 and (b) DUT S_4 [J2].

the whole test. The T_j variation of both DUTs is compared in Fig. 4.15 and it confirms the effect of short-circuit degradation on T_j [J2].

It is now clear that the degradation caused by short-circuit stress has a strong effect on both $V_{DS,on}$ and ΔT_j. This might come from the significant increase in the I_{GSS}, which causes a lower V_{GS} on the DUT, and thereby a higher $V_{DS,on}$ during power cycling test. Apart from this, Al metallization reconstruction induced by short-circuit stress may also lead to a $V_{DS,on}$ increase. The increased $V_{DS,on}$ results in higher conduction losses (P_{cond}) and, in turn, higher ΔT_j as depicted in Fig. 4.16 [J2]. At the same time, the higher ΔT_j and T_{Jmean} accelerate the ageing process and result in positive feedback to $V_{DS,on}$ as well as earlier wear-out failure.

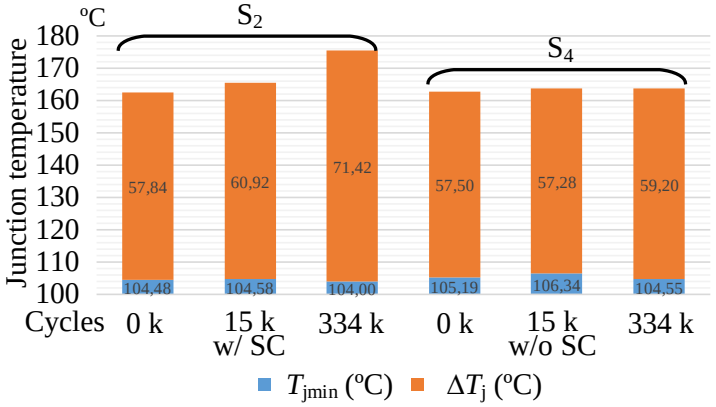


Fig. 4.15. Comparison of junction temperature (T_{jmax}, T_{jmin}, and ΔT_j) variation between DUT S_2 and S_4 (with/without 50 short-circuit repetitions) [J2].

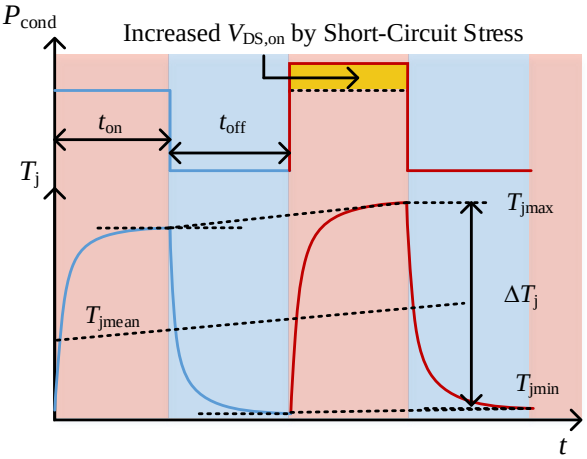


Fig. 4.16. Effect of short-circuit degradation on the power-cycling conditions [J2].

4.3 Impact of Short Circuit on the RUL

It has been demonstrated in the previous section that the short-circuit degradation can exacerbate the junction temperature conditions during a power cycling test, which may aggravate the ageing process. As of the time of writing of this thesis, and to our best knowledge, there is no evidence in the literature of studies about the effects of short-circuit events on the remaining useful life (RUL) of SiC MOSFETs.

In this thesis work, power cycling tests were adopted to implement accelerated ageing condition and $V_{DS,on}$ was taken as the ageing indicator. A different number of short-circuit repetitions were performed during the power cycling tests to assess their impact on the number of cycles to failure (N_f). The discrete DUT used for the tests has been described in Section 4.1. The samples were selected with matched static characteristics (especially $R_{DS,on}$ and V_{th}) and they were named from S_1 to S_8. Fig. 4.17 presents the flow chart of the test approach [J4].

At first, DUT S_1 and S_2 are used to perform a power cycling test without any short-circuit stress in order to estimate the expected life. When one of the DUTs is open-circuit or shows very high $V_{DS,on}$, its number of cycles is regarded as N_{f1}. Then, three sets of power-cycling tests are performed and $10\% \cdot N_{f1}$ is adopted as the time point of short-circuit stress. This way, the DUTs can maintain consistent electrical characteristics at the beginning of the test, and the impact of power-cycling ageing on the short-circuit performance can be neglected [92]. At this point, a different number of short-circuit repetitions (40, 80, and 120) are performed on DUT S_3, S_5, and S_7, respectively. The other three DUTs (S_4, S_6, and S_8) are tested for the sake of a reference without short-circuit stress and they are used to ensure that the settings are kept the same (e.g. I_{load}) when the power cycling tests continue after $10\% \cdot N_{f1}$.

The power cycling tests and selected repetitive short-circuit conditions for this type of DUT are listed in Table 4.3 and Table 4.4, respectively. For the power cycling, the on-state and off-state times are 2 s with 0.5 ms overlap and the V_{GS} is set to +15 V/-4 V.

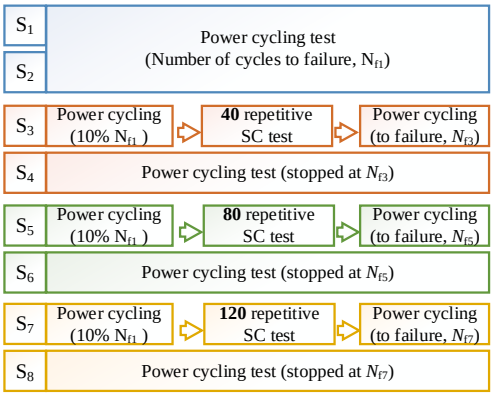


Fig. 4.17. Test approach of mixed power-cycling/repetitive short-circuit test with a different number of short-circuit repetitions (the devices paired with the same colours have been tested until the same number of cycles) [J4].

When the DUT turns off, a small current (20 mA) is injected into the body diode (V_{SD}) and the T_j can be measured in this way. Besides, the relationship between V_{SD} and T_j is calibrated before the power-cycling test and after short-circuit stress.

The power-cycling test results of DUT S_1 and S_2 are shown in Fig. 4.18 [J4]. Both DUTs exhibit a similar trend in the $V_{DS,on}$ and T_{jmax} until 25 k cycles. Then, the $V_{DS,on}$ of DUT S_2 starts increasing and brings to failure at 30.4 k cycles – this condition corresponds to open-circuit failure and its number of cycles is regarded as N_{fl}. Thus, the time point of short-circuit stress was chosen to be 3 k cycles (10%· N_{fl}).

Then, in the following three sets of tests, 40, 80, and 120 short-circuit repetitions were applied after 3 k cycles on DUT S_3, S_5, and S_7, respectively. The reduction of the on-state V_{GS} and peak I_D were observed on all three DUTs after short-circuit stress.

TABLE 4.3 - TEST CONDITIONS FOR THE POWER CYCLING TEST

Parameters	Value	Unit
On-State and Off-State Time (t_{on}, t_{off})	2, 2	s
Gate-source Voltage (V_{GS})	+15/-4	V
Initial Maximum Junction Temp. (T_{jmax})	130	°C
Initial Minimum Junction Temp. (T_{jmin})	70	°C
Initial Junction Temp. Swing (ΔT_j)	60	°C

TABLE 4.4 - TEST CONDITIONS FOR THE REPETITIVE SHORT CIRCUIT TEST

Parameters	Value	Unit
DC-Link Voltage (V_{DC})	600	V
Gate-source Voltage (V_{GS})	+15/-4	V
Pulse Time (t_{SC})	2.2	µs
Initial Case Temperature (T_C)	25	°C

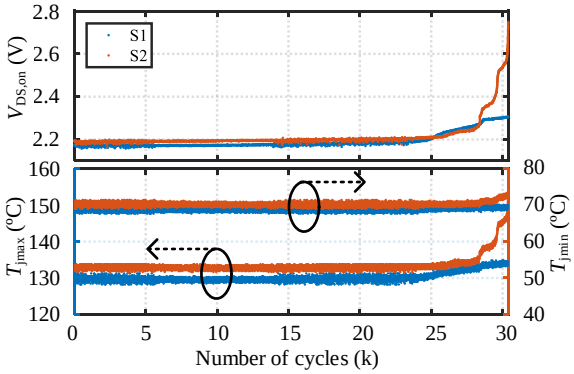


Fig. 4.18. Power cycling test results ($V_{DS,on}$, T_{jmax}, and T_{jmin}) of DUT S_1 and S_2 without any short-circuit stress [J4].

Among these, DUT S_7, which was subjected to 120 repetitions, showed the lowest V_{GS} (13.5 V) during the last repetition, indicating the most serious degradation. The first- and the last-repetition waveforms of DUT S_3, S_5 and S_7 are plotted in Fig. 4.19 [J4].

The on-state V_{GS} at the end of the pulse duration (t = 2 µs) was used as a short-circuit degradation indicator and the I_{GSS} at the same time could be calculated by the voltage drop across R_G, which is equal to 20 Ω. The short-circuit energy (E_{SC}) of every repetition was also calculated. As can be seen from Fig. 4.20 (a), regardless of the number of repetitions, the energy decreases with I_{GSS}. On the other hand, all three DUTs have the same initial E_{SC}, which is equal to 0.114 J and this value is below the critical energy (E_{SC}/E_C = 0.76). It is notable that the degree of degradation is largely depending on the number of repetitions as shown in Fig. 4.20 (b) [J4].

To obtain accurate T_j measurement, the relationship between the V_{SD} and T_j (V_{GS} = -4 V) was recalibrated again after short-circuit repetitions and an obvious variation was observed in DUT S_3, S_5, and S_7 as presented in Fig. 4.21 (a). For the DUTs without short-circuit stress, it can be seen in Fig. 4.21 (b) that their V_{SD}-T_j curves keep the same

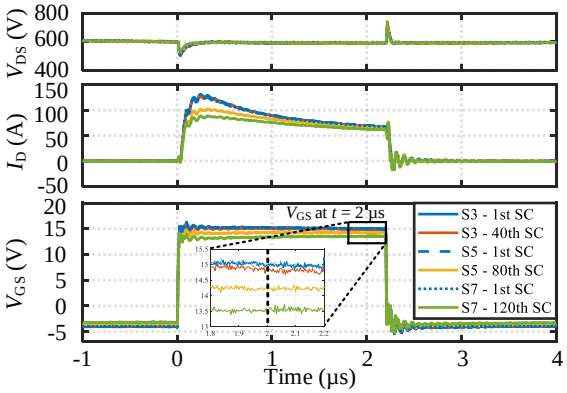
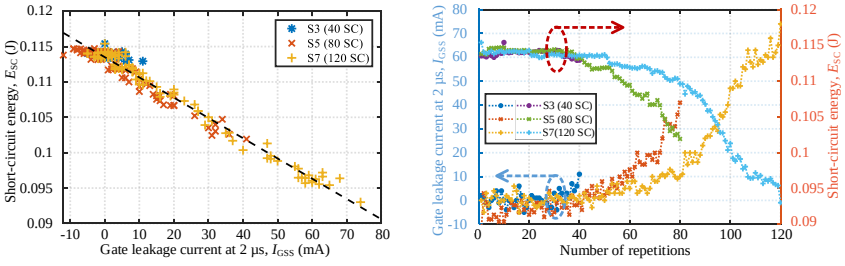


Fig. 4.19. Repetitive short-circuit test results of DUT S_3, S_5, and S_7 (only the first and last repetition) [J4].



(a) (b)

Fig. 4.20. (a) Relationship between short-circuit energy (E_{SC}) and gate leakage current at 2 µs I_{GSS}; (b) I_{GSS} and E_{SC} versus number of repetitions [J4].

as the initial one when the power-cycling tests stop [C2]. It is worth to point out that the behaviour depicted in Fig. 4.21 (a) is not clear as of the time of writing. A reasonable hypothesis is that the leakage through the gate oxide prevents the channel from being fully off, altering the measurement, which is performed at 20 mA. However, the calibration procedure of Fig. 4.21 still holds as there is a clear relationship between V_{SD} and T_j.

After this, power cycling tests continued to run. Although the positive output voltage from the gate driver was still 15 V, the effective measured V_{GS_E} of DUT S_3, S_5, and S_7 decreased from 15 V to 14.2 V, 11.8 V, and 11.1 V, respectively. At the same time, the $V_{DS,on}$ became much higher than before. As shown in Fig. 4.22, the DUT S_7, which has withstood the largest N_{SC}, exhibits the highest $V_{DS,on}$ (or $R_{DS,on}$) [J4]. This effect has been explained in Section 4.2 in the case of a power module. In the same test, higher $V_{DS,on}$ and ΔT_j led to earlier wear-out failure, and the number of cycles to failure (N_f) for DUT S_3, S_5, and S_7 was 6.3 k, 5.25 k, and 4.88 k, respectively. On the other hand, DUT S_4, S_6, and S_8 maintained the stable $V_{DS,on}$ till the power-cycling tests stopped.

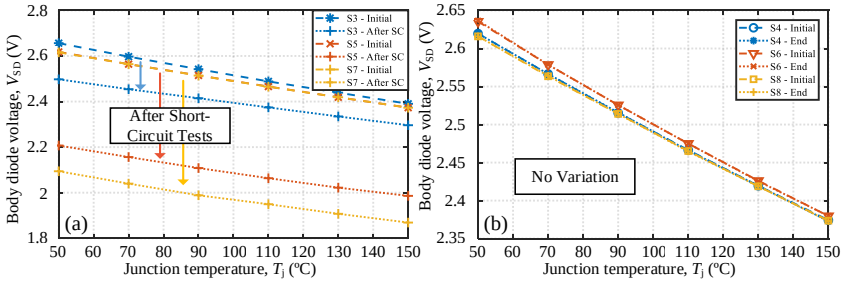


Fig. 4.21. (a) V_{SD}-T_j curve of DUT S_3, S_5, and S_7 before test and after short-circuit repetitions; (b) V_{SD}-T_j curve of DUT S_4, S_6, and S_8 before and after power-cycling test [C2].

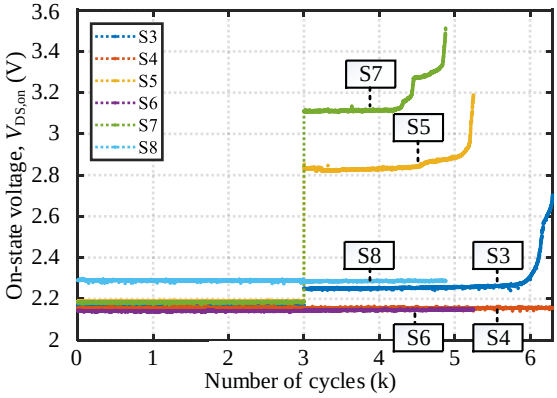


Fig. 4.22. $V_{DS,on}$ evolution of DUT S_3 - S_8 with the number of power cycles [J4].

The calculated T_j in Fig. 4.23 proves the higher ΔT_j caused by the short-circuit stress and the one of DUT S_7 increases the most, reaching 90 ºC after the short-circuit stress [J4]. Therefore, as a preliminary approach, the effect of short-circuit degradation on the RUL estimation could be transferred to the equivalent increased ΔT_j.

For this specific DUT, the relationship between N_f and the number of short-circuit events (N_{SC}) is built as shown in Fig. 4.24. This figure represents a suitable candidate to enhance lifetime model taking into account the short-circuit events. The number of cycles to failure considering short-circuit stress (N_{f_SC}) can be expressed by N_{f1} with a parameter B, as in (4.1) and (4.2), where N_{f1} is the number of cycles to failure without any short-circuit stress (i.e. N_{f1} = 30.4 k), and B is a parameter that is initially fitted based on the experimental results in Fig. 4.24.

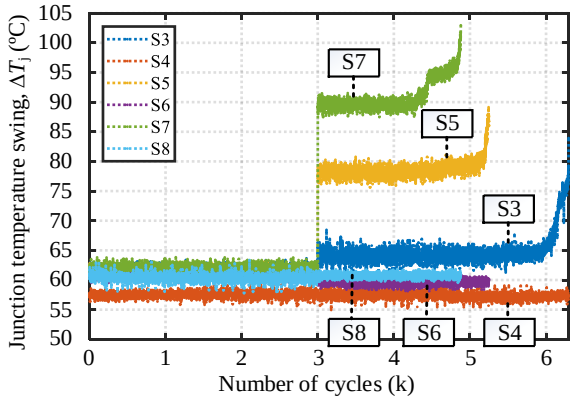


Fig. 4.23. Evolution of the junction temperature swing (ΔT_j) with the number of power cycles on DUT S_3 - S_8 [J4].

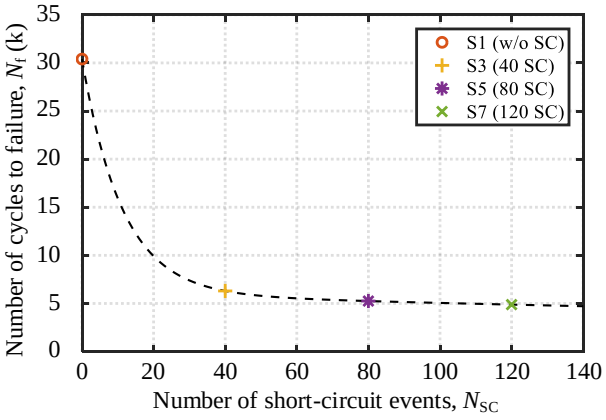


Fig. 4.24. The number of power cycles to failure (N_f) versus the number of short-circuit repetitions (N_{SC}).

$$N_{\mathrm{f\_SC}} = N_{\mathrm{f1}} \cdot B \tag{4.1}$$

$$B = 0.8023 \times \exp(-0.089 \times N_{\mathrm{SC}}) + 0.1977 \times \exp(-0.00174 \times N_{\mathrm{SC}}) \tag{4.2}$$

When the Coffin-Manson-Arrhenius law is used to estimate the number of cycles to failure of a device, a revised lifetime model taking into account of short-circuit events can be expressed as (4.3).

$$N_{\mathrm{f\_SC}} = A \cdot \Delta T_{\mathrm{j}}^{\alpha} \cdot \exp\left(\frac{E_{\mathrm{a}}}{K_{\mathrm{B}} \cdot T_{\mathrm{jm}}}\right) \cdot B(N_{\mathrm{SC}}) \tag{4.3}$$

Then, for a given V_{DC} and a protection time (i.e. t_{SC}), both depending on the application, mixed power-cycling/repetitive short-circuit tests need to be performed to work out a relationship between N_{f} and N_{SC} as Fig. 4.24. Thereafter, the parameter B in (4.2), which is a function of N_{SC} can be calibrated in this way.

4.4 Summary

In this chapter, a detailed study of the short-circuit degradation effect on the RUL of SiC MOSFET has been provided. Firstly, the power cycling test bench and junction temperature measurement approach have been introduced. Depending on the packaging type of the DUT, the optical fibre and body diode voltage method have been selected for power modules and discrete devices, respectively. Secondly, the power cycling tests have been performed with and without short-circuit stress to assess the degradation effects on the power cycling. It could be found that the increased gate leakage current induced by the short-circuit stress mainly leads to a higher on-state resistance and conduction loss during the power cycling test. In this case, the junction temperature swing becomes higher than before and this factor aggravates the ageing process, resulting in earlier failure.

For the purpose of further study on the short-circuit degradation effect on the RUL, three different number of short-circuit repetitions (40, 80, and 120) have been applied. The experimental results show that the larger number of repetitions could cause a higher on-state voltage and less number of cycles to failure. A relationship between the number of cycles to failure and the number of short-circuit events has been built and a more accurate RUL estimation could be achieved based on the revised lifetime model proposed in Section 4.3.

Chapter 5

Short-Circuit Degradation Analysis and Mitigation Strategy

This chapter, consisting of [J4] and [C3], presents failure analysis on the degraded device through lock-in thermography, scanning electron microscopy, and focused ion beam. The outcome of these results is important to understand the short-circuit degradation mechanisms. Based on the experimental results, a thermo-mechanical simulation of short-circuit condition is made with COMSOL Multiphysics and a mitigation strategy is proposed based on it, which founds on the enhancement of the top-side thermal mass of the chip.

5.1 Failure Analysis

In order to further understand the impact of short-circuit degradation, more in-depth failure analysis was carried out on DUT S_5 and S_6 that had been tested in Section 4.3, Page 53. Firstly, the DUTs were de-capsulated by laser ablation (Laser Micro Machine GL compact, GFH) and etching with high-temperature sulphuric acid. The residue was removed by an ultrasonic cleaner. On DUT S_5, bonding wires were swept away during the process, which obviously indicates a heavy bonding weakness or a complete lift-off after the stress test. In contrast, DUT S_6, which was not failed and exhibited a stable $V_{DS,on}$ until the end of the power-cycling test, kept Al wires bonded on the top surface of the chip. Also, these results indicate the negligible influence of de-capsulation and cleaning process on the bonding wires. Unfortunately, the only clear pictures taken of both DUTs are the ones of lock-in thermography (see Fig. 5.1 and Fig. 5.2).

Subsequently, the damaged areas of DUT S_5 were localized by performing lock-in thermography (LIT) measurement. LIT is a well-established investigation technique based on active thermography for non-destructive failure analysis of samples. Typically, a heat generation (or other excitation) is stimulated periodically at a certain lock-in frequency and the temperature response is analysed over time. Compared to steady-state thermography, this approach allows detecting very-low-power spots such as leakage current without suffering from spatial resolution issue caused by the fast heat diffusion. To achieve an improved sensitivity of the measurement, a large number of pulses are used and results are averaged. Typically, the applied frequency is an important degree of freedom, as a lower one is useful to investigate high temperature swings, whereas a higher one reduces the thermal diffusion and helps to improve the spatial resolution [93].

The used lock-in thermal imaging system (CG Systems) has a high-performance and high-resolution InSb 320 M thermal imaging camera. During the measurement, the drain terminal and source pad are both connected to the ground through two probes and another probe on the gate pad is used to apply a periodical pulse voltage (i.e. V_{GS}). The gate leakage current is used as the periodical heat source and a compliance value can be set in this system so as to avoid artificial damages. The amplitude image exhibits total temperature rise within the DUT and the phase image display the time delay after the pulse is applied. Therefore, the value close to 0° indicates a very short delay of the heat diffusion and this typically occurs in the damaged region.

Fig. 5.1 and Fig. 5.2 show both amplitude and phase images of lock-in thermography for DUT S_5 and S_6, respectively [J4]. Concerning DUT S_5, its I_{GSS} increases to 1 mA when the V_{GS} pulse is set to 0.84 V. As marked in the red boxes in Fig. 5.1 (a) and (b), two damaged regions can be observed; their bright colour in the amplitude image demonstrates the hotspot placement (higher temperature rise) and the grey colour in the phase image indicates that the heat generation is very close to the surface in the direction normal to the chip surface. However, it is still not clear why the locations are in the periphery, nearby the border between the active region and the termination. The interpretation of this phenomenon is difficult and involves the position of bond wires during the thermal transient, along with corner effects and the distance from the gate runner. However, similar results have been presented recently by the other research

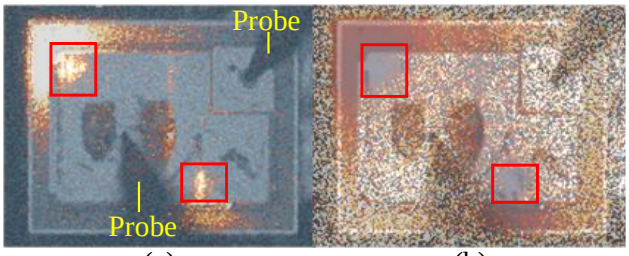


Fig. 5.1. Lock-in thermography results of DUT S_5: (a) amplitude image; (b) phase image [J4].

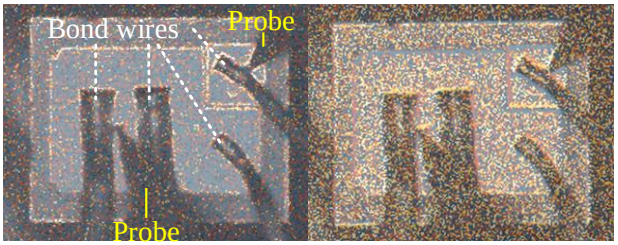
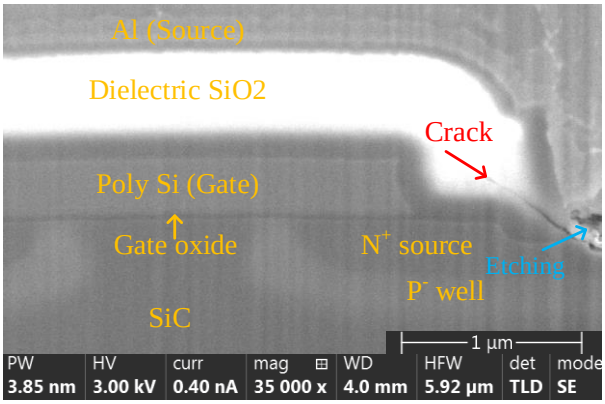


Fig. 5.2. Lock-in thermography results of DUT S_6: (a) amplitude image; (b) phase image [J4].

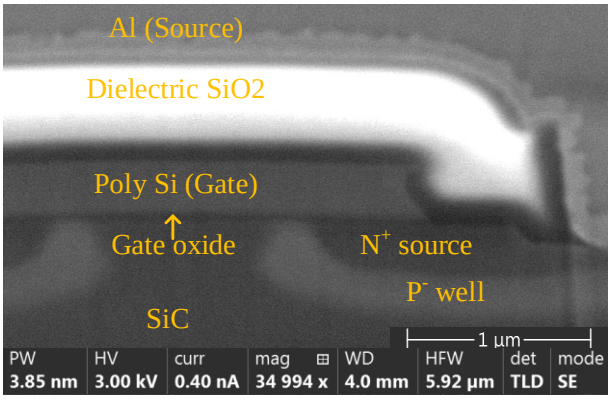
groups [94]. A possible contribution might be the formation of current filament during the short-circuit test. On the contrary, even though the V_{GS} pulse is set to 15 V on DUT S_6, its I_{GSS} keeps negligible, i.e. equal to 0.17 nA. Fig. 5.2 (a) and (b) show its amplitude and phase image, respectively and the results indicate no gate damage on this DUT.

After this, a Helios G4 PFIB UX3 system from Thermo Fisher Scientific was used to perform the focused ion beam (FIB) analysis on the damaged location of DUT S_5 as well as an arbitrary location of the still functional DUT S_6 for comparison. Then the vertical cross-section of the DUT could be obtained through scanning electron microscopy (SEM). For DUT S_5, a crack in the dielectric SiO_2 interlayer was found in one of the cells as presented in Fig. 5.3 (a) [J4]. In contrast, the cells of DUT S_6 are undamaged with no cracks and the SEM image of one cell is shown in Fig. 5.3 (b).

Because the thickness of the gate oxide layer between the SiC and the polysilicon is only 50 nm, the SEM resolution limits further observation on this thin layer. However, a



(a)

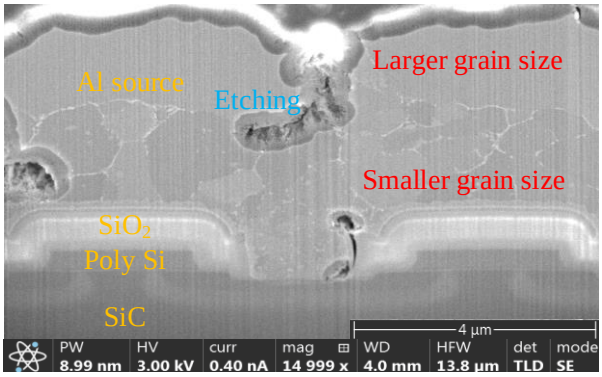


(b)

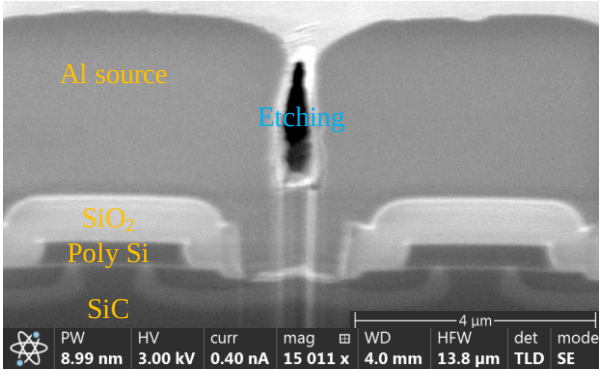
Fig. 5.3. Cross-sectional SEM images: (a) DUT S_5 (the damaged cell and the SiO_2 crack marked with the red arrow); (b) DUT S_6 (the intact cell) [J4].

more likely cause of this crack is the mechanical stress on the Al/SiO_2 interface due to the CTE mismatch between the Al and SiO_2 material; the crack as shown in Fig. 5.3 (a) may cross the SiO_2 interlayer to the gate terminal in the direction normal to the figure and this type of SiO_2 dielectric crack has also been found in [79] and [95] after short-circuit test. Furthermore, the energy dispersive spectrometer (EDS) results in [96] confirm a significant amount of Al migrating into the crack. Since the maximum temperature in the Al layer can reach more than 1000 K based on TCAD simulation results [97], it reveals that the molten Al can flow through the crack. Then the formation of a conductive path between the gate and source leads to the I_{GSS} increase.

On the other hand, as displayed in Fig. 5.4 (a), the grain sizes in the top and bottom locations of the Al layer in DUT S_5 are remarkably different, which could make think of a phenomenon similar to the Al metallization reconstruction discussed in [98]. Manifested as the reduction of grain size, this kind of Al layer degradation can be illustrated by the dislocation-based plasticity [99]. The vertical temperature gradient might



(a)



(b)

Fig. 5.4. Cross-sectional SEM images: (a) DUT S_5 (different grain sizes in the Al metallization layer); (b) DUT S_6 (no observable grain boundaries) [J4].

lead to the microstructural evolution, further resulting in inhomogeneity of Al grain size along with the temperature gradient. For the sake of comparison, the SEM image of DUT S_6 in Fig. 5.4 (b) shows no recrystallization and grain boundaries of the Al layer. This finding indicates that the Al recrystallization might be a contribution of short-circuit stress itself and the followed more severe power-cycling conditions. Due to the multiplication of grain boundaries and the formation of intergranular cracks, the Al layer resistance could increase [99].

5.2 Thermo-Mechanical Simulation of Short-Circuit Condition

As the thermal measurement cannot be performed during short-circuit tests owing to the very fast temperature transient, simulation is a reasonable approach to analyse the thermal behaviour of the device. Technology computer-aided design (TCAD) tools from Synopsys and Silvaco are typically used to perform an electro-thermal modelling of single-cell SiC MOSFETs under given conditions, such as short-circuit conditions [97]. These tools allow gaining a reasonable insight of the current density, electric field, and lattice temperature distribution, and their transient evolution. However, as mentioned in Section 5.1, gate degradation is mainly related to thermo-mechanical stress. Therefore, a finite-element-method (FEM) simulation tool (COMSOL Multiphysics) was selected to obtain temperature and mechanical stress distribution under short-circuit condition and the main goal was to gain a deeper insight into the short-circuit damage process.

The commercial 1.0 kV/22 A discrete SiC MOSFET with TO-247-4 package, which has been tested above, is adopted as the case study. A 2-D single-cell FEM model is built and the planar-gate structure is matched with the SEM image in Fig. 5.3 and Fig. 5.4. To be specific, a sketch of the simulation model is shown in Fig. 5.5 and the chip is encapsulated with epoxy resin [C3].

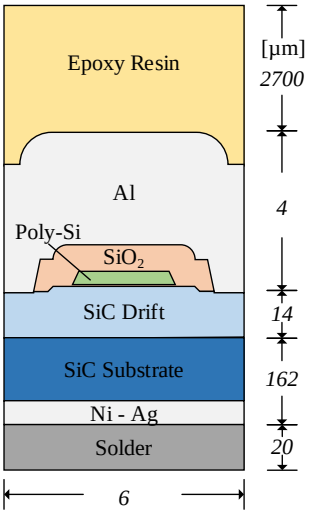


Fig. 5.5. Sketch of the simulation model (not to scale) [C3].

To ensure accurate simulation, the thermal conductivity (λ_{SiC}) and specific heat of SiC material (C_{SiC}) are dependent with temperature, expressed as (3.8) and (3.9) in Section 3.3, and its physical density is equal to 3211 kg/m^3 [100]. Table 5.1 provides the thermal properties of the other materials and the mechanical properties are listed in Table 5.2 [101] [102].

Regarding the boundary settings, the whole SiC drift region is set as the heat source and its value is derived from the experimental results. Fig. 5.6 shows the short-circuit test

TABLE 5.1 - THERMAL PROPERTIES OF THE MATERIALS [C3]

Materials	**Density** ***kg/m³***	**Thermal Conductivity** ***W/(m·K)***	**Specific Heat** ***J/(kg·K)***
Epoxy Resin	1250	0.3	900
Aluminum	2700	239×f(T) [101]	910
SiO_2	2200	1.4	730
Polysilicon	2320	$(-2.2\times10^{-11}\times T^3 + 9\times10^{-8}\times T^2 - 1\times10^{-5}\times T + 0.014)^{-1}$	678
Solder	7400	60	160

TABLE 5.2 - MECHANICAL PROPERTIES OF THE MATERIALS [C3]

Materials	**CTE** ***×10⁻⁶ 1/K***	**Young's Modulus** ***GPa***	**Poisson's Ratio** ***1***
Epoxy Resin	24	17	0.3
Aluminum	23.2	70.3	0.346
SiO_2	0.5	75	0.17
Polysilicon	2.8	169	0.22
SiC	4.3	500	0.157
Solder	28.7	13.79	0.35

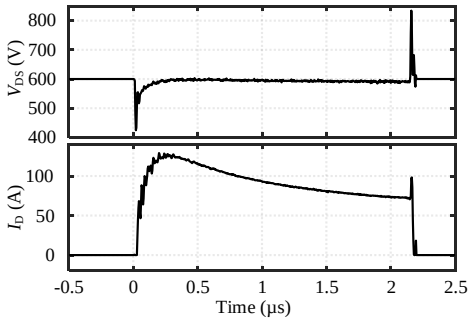


Fig. 5.6. Short-circuit waveforms derived from experimental test (V_{DC} = 600 V, t_{SC} = 2.2 μs, and T_C = 25 ºC) [C3].

waveforms of this DUT with the same conditions (V_{DC} = 600 V, t_{SC} = 2.2 μs, T_C = 25 ºC). Specifically, the heat source of the total chip could be obtained by the product of V_{DS} (t) and I_D (t) waveforms. For the single cell, active area factor of the chip (A) needs to be considered first by (5.1), where S_T represents the total active area of the chip, W means the width of a single cell (i.e. 6 μm), and the depth of the model D has a default value 1 μm. Then the heat source applied in this single-cell model (Q) can be calculated as (5.2), where S_H represents the size of the heat source region in the 2-D model [C3].

$$A = \frac{S_T}{W \times D} \quad [1] \tag{5.1}$$

$$Q = \frac{V_{DS}(t) \times I_D(t)}{A \times S_H \times D} \quad [\mathrm{W/m^3}] \tag{5.2}$$

Apart from this, a constant room temperature (25 ºC) is set to the top side and bottom side of the model. A fixed constraint is applied to the bottom side only since the DUT is fixed through the hole during the experimental test. The left and right side of the model are symmetry boundary in the physics of both heat transfer in solids and solid mechanics. Thereafter, the transient thermo-mechanical simulation is performed with 2.2 μs short-circuit pulse and the time is from 0 μs to 5 μs in steps of 0.004 μs. During the simulation, the heat spreads from the SiC drift region upwards and downwards.

The transient temperature distribution at different time points (such as t = 1.0 μs) are presented in Fig. 5.7 from (a) to (f). Due to the very low thermal conductivity of epoxy

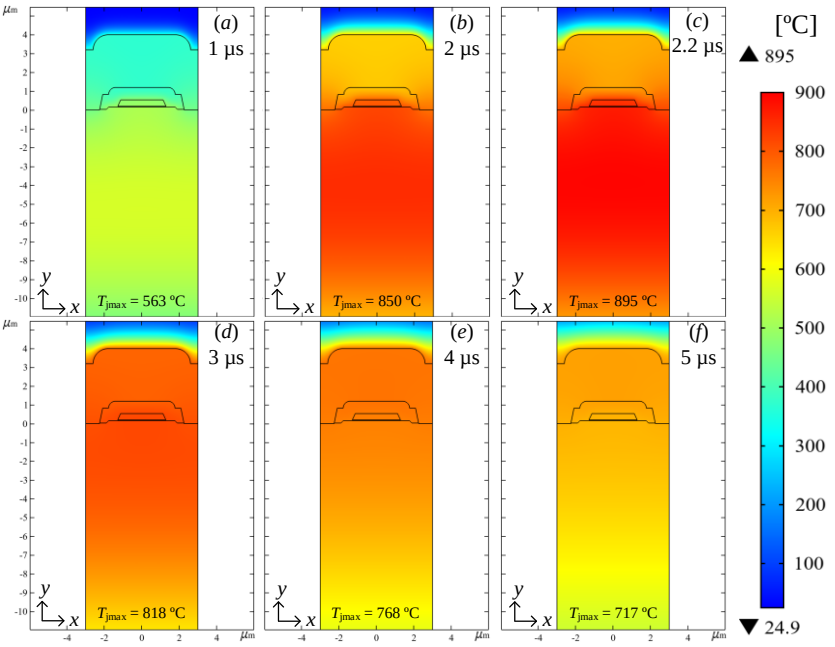


Fig. 5.7. Transient temperature distribution under short-circuit condition at different time point: (a) 1 μs; (b) 2 μs; (c) 2.2 μs; (d) 3 μs; (e) 4 μs; (f) 5 μs.

resin, the temperate increase caused by the short-circuit energy concentrates on the SiC drift region, SiO_2 interlayer and Al metallization layer. The maximum temperature within the model increases to 895 ºC when the time is equal to 2.2 µs (i.e. at the end of pulse time). The temperature variation in the SiC drift region agrees with the TCAD simulation results in [97].

It is worth noting that the maximum temperature in the Al layer reaches 829 ºC. Since the melting point of Al is equal to 660 ºC, the presence of molten Al is very likely, which is one of the two preconditions to form the conductive path. Besides, the temperature distribution along with the vertical direction Y (X = 0 µm) is plotted in Fig. 5.8 when the time is equal to 2.2 µs [C3].

Fig. 5.9 from (a) to (f) presents the von Mises stress distribution in the SiO_2 interlayer against time [C3]. It is worth to note that 1.4 GPa is the strength limit for the SiO_2

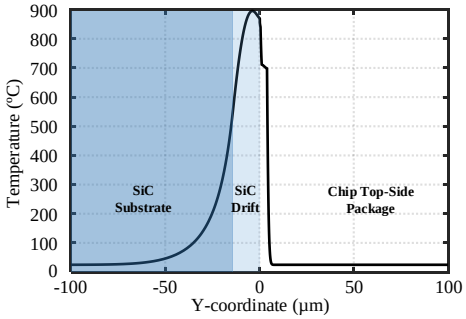


Fig. 5.8. Temperature distribution along the Y-coordinate (X = 0 µm) at the end of pulse time (t = 2.2 µs) [C3].

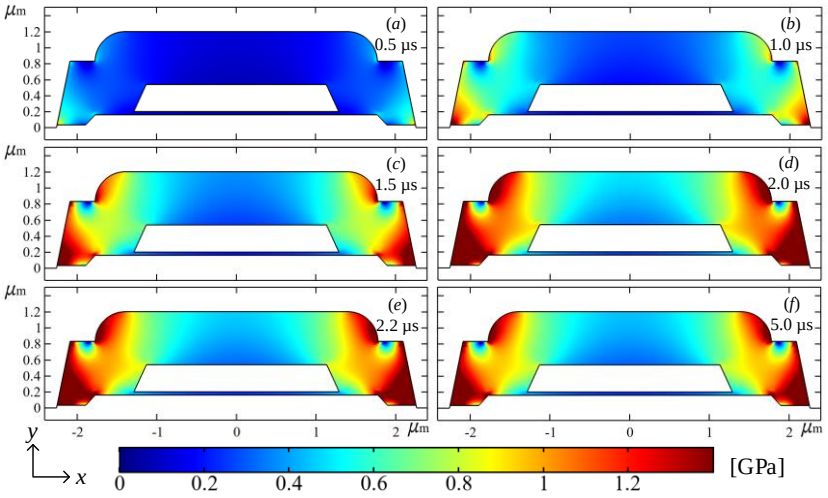


Fig. 5.9. Von Mises stress distribution under short-circuit condition at different time point: (a) 0.5 µs; (b) 1.0 µs; (c) 1.5 µs; (d) 2.0 µs; (e) 2.2 µs; (f) 5 µs.

material [103]. At t = 1.0 μs, the mechanical stress larger than the limits appears at the lower left and right corners of the Al/SiO_2 interface as shown in Fig. 5.9 (b). This location is consistent with the crack location observed from the SEM image in Fig. 5.3 and it is caused by the CTE mismatch between the Al and SiO_2 material. Then the area with the stress higher than the critical value gradually becomes larger with the time and it spreads towards the polysilicon gate. These results justify the formation of crack, which is the second preconditions for gate degradation. Therefore, the simulation results indicate that SiO_2 dielectric crack is formed first due to thermal expansion and then the molten Al caused by the high temperature flows through the crack, resulting in the gate-source conductive path and I_{GSS} increase. On the other hand, the high temperature in the Al region may lead to the smaller grains, intergranular cracks, and even voids, which can further increase the $R_{DS,on}$ resistance.

5.3 Mitigation Strategy: Top-Side Thermal Mass

The impact of short-circuit degradation on the normal operating condition and the RUL has been discussed in previous chapters. After understanding the underlying degradation mechanism, the question turns into how to mitigate this degradation. Typically, the reduction of short-circuit energy can decrease the heat generated, thereby alleviating the degradation process and it can be achieved by changing many factors during the tests, such as the reduction of DC-link voltage (V_{DC}), gate-source voltage (V_{GS}), pulse time (t_{SC}), and the increase of the gate resistance (R_G), case temperature (T_C). However, these parameters may not be changed in the field applications.

If the device itself is considered, the mitigation approach could be either at chip-level or packaging-level. At chip-level, the short-circuit energy can be improved by reducing the saturated short-circuit current. Nevertheless, the on-state resistance increases at the same time and there is a trade-off between the short-circuit capability (E_{SC}) and $R_{DS,on}$, which has been pointed out in [104]. On the other hand, pushing the location of the heat source further away from the gate structure could be another possible solution. Fig. 5.10 shows the simulated temperature distribution of two trench-gate SiC MOSFET designs during short-circuit condition at 0.2 μs [105]. The semi-super junction (SJ) type has a

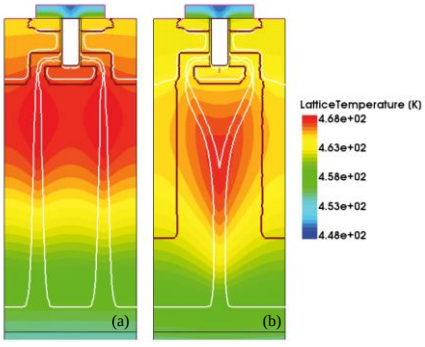


Fig. 5.10. Lattice temperature distribution during the short-circuit condition at 0.2 μs: (a) conventional MOSFET; (b) semi-SJ MOSFET [105].

deeper hotspot than the conventional one. It is realized by changing the electric field distribution since the differential form of the generated heat can be expressed as (5.3), where Q represents the joule heat density, J is the current density, and E is the electric field. This simulation work is also verified by the experimental test and the Semi-SJ device shows more than 13% short-circuit capability increase [105].

$$Q = J \cdot E \tag{5.3}$$

The optimization of gate structure might be another mitigation approach. By increasing the Al thickness and decreasing the SiO_2 thickness appropriately, the stress on the Al/SiO_2 interface could be reduced slightly [96]. Furthermore, replacing as the better CTE-matched interlayer material and higher melting point metallization layer might be a promising approach, but this may face manufacturing process challenges.

As for the packaging-level approach, since the heat flux generated by short-circuit test diffuses for a limited distance towards the substrate, which can be seen in Fig. 5.8, the short-circuit degradation could be independent of the bottom-side layer and external cooling system. Despite the top-side package design like thick copper metallization has been used to increase the short-circuit robustness of Si IGBT, it is still not clear how much effect on the degradation of SiC MOSFET it can produce. Considering the Al layer surface is close to the heat source, an additional metal foil on the top of the surface can be used to spread the heat.

Based on the previous case study in Section 5.2, another model is built in COMSOL Multiphysics and Fig. 5.11 presents a sketch of the new model. Compared to Fig. 5.5, a 50 µm copper foil is silver-sintered on the top surface of the Al metallization layer and the thickness of the sintered layer is equal to 20 µm. Other than that, everything else remains the same size [C3]. This approach is similar to the Danfoss Bond Buffer technology [106], which has practical feasibility. Similarly, a transient thermo-mechanical

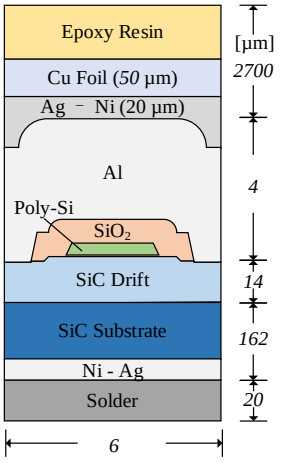


Fig. 5.11. Sketch of the simulation model with Cu foil sintered on the top surface of the Al metallization layer (not to scale) [C3].

simulation is computed from 0 μs to 5 μs and the time step is equal to 0.004 μs. The boundary conditions and material properties are kept the same as the settings in Section 5.2. The physical properties of Cu foil and sintered Ag are listed in Table 5.3 [C3].

When the same experimental short-circuit waveforms are used as the heat source for both two models, their results can be compared. For the sake of clarity, the conventional package model is regarded as the model without Cu foil and the new one is referred to the model with Cu foil.

The temperature distribution of two models at the end of the pulse time (i.e. t = 2.2 μs) is selected for comparison as shown in Fig. 5.12 [C3]. The upper one shows the results without Cu foil and the maximum temperature of the model is equal to 895 ºC. In contrast, the lower one presents the results with Cu foil and the maximum temperature

TABLE 5.3 - PHYSICAL PROPERTIES OF THE OTHER MATERIALS [C3]

	Cu Foil	**Sintered Ag**	**Unit**
Density	8700	9500	kg/m^3
Thermal Conductivity	400	170	W/(m·K)
Specific Heat	385	200	J/(kg·K)
CTE	17	19.75	×10^{-6} 1/K
Young's Modulus	110	12~32	GPa
Poisson's Ratio	0.35	0.3	1

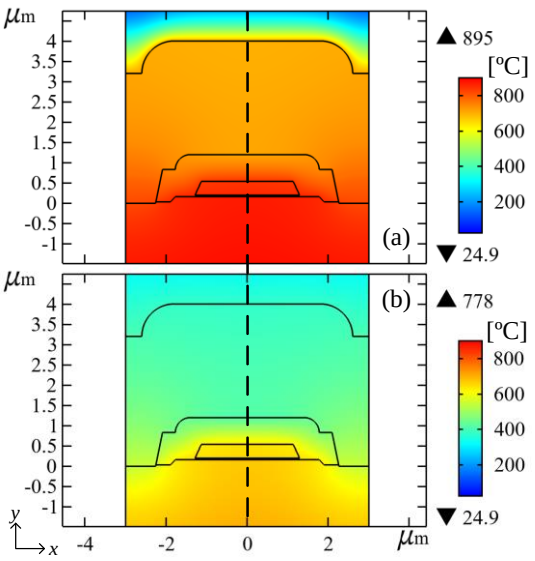


Fig. 5.12. Temperature distribution comparison of two models at t = 2.2 μs (a) the model without Cu foil (b) the model with Cu foil [C3].

is 778ºC. Similarly, the temperature distribution along with the vertical direction Y-coordinate at X = 0 (i.e. the dotted line) is selected to better understand the contribution of Cu foil. As can be seen in Fig. 5.13, both the maximum temperature and temperature gradient are reduced due to the Cu foil [C3].

The maximum temperature within three different regions, including the Al layer, SiO_2 interlayer, and SiC drift region are selected, respectively and their temperature variations with the time can be plotted. In Fig. 5.14, the maximum temperature in the Al layer region shows a significant decrease from 820 ºC to 569 ºC with Cu foil [C3]. These results indicate that the top-side Cu foil can benefit the mitigation of short-circuit degradation from two aspects. With the lower temperature rise, the Al metallization reconstruction can be alleviated. At the same time, melting can be avoided. Because the maximum

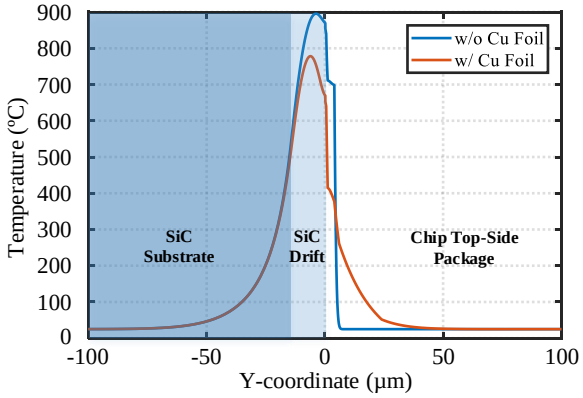


Fig. 5.13. Temperature distribution along with the vertical direction Y-coordinate (X = 0) at t = 2.2 μs in the model without and with Cu foil [C3].

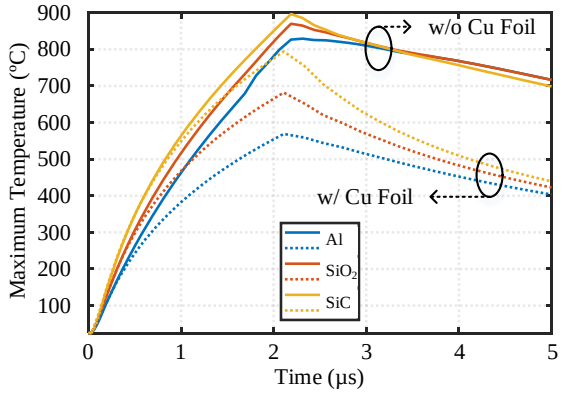


Fig. 5.14. Evolution of maximum temperature with the time inside the Al, SiO_2, and SiC drift region in the model without and with Cu foil [C3].

temperature variation of the Al layer region in the model with Cu foil is still below the melting point (660 ºC), the pulse time can be increased. As shown in Fig. 5.15, when the short-circuit waveforms of 2.2 µs are replaced with the ones of 2.8 µs, the maximum temperature of the Al layer reaches the melting point. Apart from the Al layer region, the temperature rise inside the SiO_2 and SiC region is also reduced due to the Cu foil [C3].

Fig. 5.16 shows the comparison of von Mises stress distribution in the SiO_2 interlayer region for both models [C3]. In the model with Cu foil, because of the lower temperature increase in the Al layer and SiO_2 interlayer region, the mechanical stress caused by the thermal expansion mismatch is reduced significantly, compared to the model without Cu foil. These results suggest that the SiO_2 crack risk could be mitigated in this way.

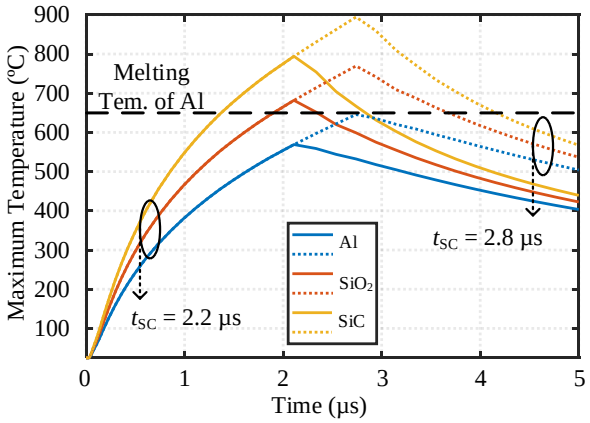


Fig. 5.15. Evolution of maximum temperature inside the Al, SiO_2, and SiC drift region in the model with Cu foil (increased pulse time from 2.2 µs to 2.8 µs) [C3].

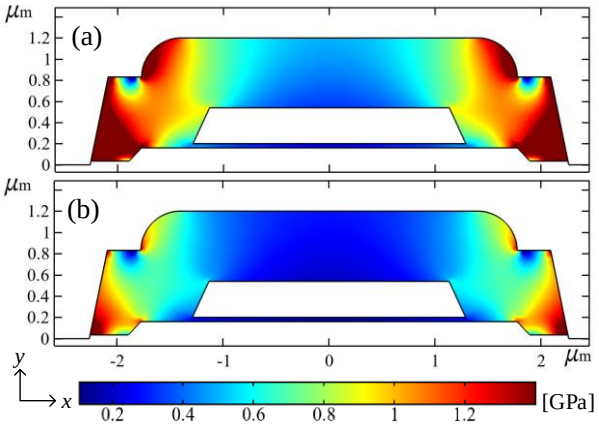


Fig. 5.16. Comparison of mechanical stress distribution in the SiO_2 interlayer region in the model (a) without Cu foil; (b) with Cu foil [C3].

5.4 Summary

This chapter has aimed at providing an interpretation of the short-circuit damage-formation mechanisms and a related mitigation approach. At first, a more in-depth analysis has been carried out on both the failed device as well as the still functional device. Lock-in thermography results show a gate leakage current increase and the damaged region has been identified. The SEM image of the failed device exhibits a SiO_2 interlayer crack and this phenomenon can be related to the gate leakage current increase. At the same time, the inhomogeneity of Al grains size has also been observed and it might be caused by the high temperature reached, together with dislocation-based plasticity. With a higher temperature, the multiplication of grain boundaries and intergranular cracks could further increase the on-state resistance. In contrast, the other device shows undamaged active region and no observable grain boundaries.

Then a 2-D single-cell model of this specific planar-gate device has been built as a case study. A transient thermo-mechanical FEM simulation under short-circuit condition has been carried out. Regarding the gate degradation, the root cause could be the molten Al flowing through the crack. To be specific, the mechanical stress on the Al/SiO_2 interface caused by the CTE mismatch exceeds the strength limitation, which forms the SiO_2 crack. On the other hand, the Al temperature becomes larger than the melting point, which leads to the presence of molten Al. These two factors make the conductive path between gate and source, resulting in the gate leakage current increase.

Finally, the possible approaches to mitigate this short-circuit degradation have been investigated. Top-side package with sintered Cu foil can be an effective approach, mainly for two aspects. The Al metallization reconstruction can be alleviated due to the lower Al temperature rise. The gate leakage current issue can be mitigated by reducing the stress on the SiO_2 interlayer to decrease the crack risk, as well as by avoiding the molten Al to flow into the crack. These end up in a reduced increase in the on-state resistance after short-circuit stress.

Chapter 6

Conclusions and Future Work

The purpose of this chapter is to summarize the research outcomes achieved in this thesis and highlight the main contributions. Moreover, some proposals for future work are discussed.

6.1 Summary

The main research objective of this thesis is to investigate the impact of short-circuit events on the remaining useful life of SiC MOSFETs and a possible mitigation approach. To achieve this goal, a combination of short-circuit tests and power-cycling tests have been performed for the first time on both discrete SiC MOSFETs and power modules. Meanwhile, static and dynamic characteristics measurements have been performed during the test to obtain the parameters variation and the effect of short-circuit degradation. Further failure analysis and thermo-mechanical simulation have been carried out to reveal the short-circuit degradation mechanisms. Finally, a mitigation approach consisting in an additional top-side thermal mass has been proposed and verified by simulation.

In Chapter 1, an introduction to the background and research motivation in the SiC MOSFET together with reliability challenges has been provided. The scientific questions, thesis objectives and limitations have been discussed.

In Chapter 2, the short-circuit performance and failure modes of SiC MOSFETs have been presented. Thanks to the laboratory non-destructive short-circuit test bench and static characteristics measurement, the electrical parameters variation caused by the short-circuit events have been investigated. Results from two different test approaches corroborate the threshold voltage shift theory and the increase in the gate leakage current, drain leakage current and on-state resistance. During short-circuit test, the non-negligible gate leakage current builds a voltage drop across the gate resistance, which leads to the reduction of the on-state gate-source voltage and drain current peak. Since the gate leakage current can reflect the short-circuit degradation process, it has been selected as a suitable indicator and the on-state gate-source voltage drop can be regarded as a directly affected parameters in the short-circuit test.

In Chapter 3, the impact of short-circuit events on the normal operating condition has been investigated. The repetitive short-circuit tests have been carried out to set a deeper focus on the gate-leakage current and on-state resistance evolution with the number of repetitions. By performing double-pulse tests, the dynamic characteristics variation with the number of short-circuit repetitions have also been evaluated. As the number increases, the turn-on and turn-off transient waveforms exhibit a delay and anticipation, respectively and the turn-on loss increases correspondingly. In addition,

with the higher initial case temperature, the lower drain current results in a lower short-circuit energy, which makes possible for the device to withstand much more number of repetitions. The simulation results from a 1-D heat propagation model shows the lower junction temperature rise at higher case temperature, which implies that degradation process is thermally-related.

In Chapter 4, a thorough study of the short-circuit degradation effect on the remaining useful life has been presented. Mixed power-cycling/short-circuit tests have been performed for both SiC MOSFET power modules and discrete devices. By the comparison of the device with and without short-circuit stress, it can be concluded that the increased gate leakage current caused by the short-circuit stress results in the increased on-state resistance and conduction loss during power-cycling condition. With a higher junction temperature swing, the ageing process can be aggravated, leading to an earlier failure. Furthermore, different number of short-circuit repetitions have been performed to assess its effect on the RUL quantitatively. The larger number of repetitions leads to a much higher on-state resistance, junction temperature swing, and less number of cycles to failure. According to the relationship between the number of cycles to failure and the number of short-circuit events, a revised lifetime model taking into account the short-circuit events has been proposed to enable a more accurate RUL estimation.

In Chapter 5, a deeper analysis of the devices after mixed power-cycling/short-circuit test has been given. For the device that had been subjected to short-circuit stress, the gate leakage current increase and damaged region have been confirmed with lock-in thermography. A SiO_2 interlayer crack and the inhomogeneity of Al grain sizes have been observed. In contrast, the device without short-circuit stress was still functional after the test and the gate leakage current was negligible. The SEM image show undamaged cell and no Al grain boundaries. Then a 2-D single-cell FEM model has been built as the case study for this device and the transient thermo-mechanical simulation of short-circuit event has been performed. The simulation results agree with failure analysis and reveal the gate degradation mechanisms: a) the mechanical stress on the Al/SiO_2 interface caused by the CTE mismatch exceeds the strength limitation and forms the SiO_2 crack; b) the Al temperature becomes larger than the melting point, resulting in the molten Al; c) the molten Al flowing through the crack forms the conductive path and leads to the gate leakage current increase. At last, the effect of short-circuit degradation can be mitigated by a top-side thermal mass. With the sintered Cu foil on top of the chip, the Al metallization reconstruction can be alleviated. The probability of SiO_2 crack risk and molten Al can be reduced, which mitigates the gate leakage current issue.

6.2 Research Highlights

The main contributions of this thesis are summarized as follow:

1. **Gate leakage current can be regarded as a promising short-circuit degradation indicator.**

   By performing both static characteristics measurement and short-circuit tests alternately, the variation of threshold voltage, gate leakage current, drain leakage current, and on-state resistance have been evaluated. Among these, the increase in the gate leakage current is strongly related to the increasing number of

short-circuit repetitions. On the other hand, the gate leakage current builds a voltage drop across the gate resistance, which results in the reduction of on-state gate-source voltage during short-circuit tests.

2. **At higher case temperature, the device can withstands larger number of short-circuit repetitions due to the lower energy.**
   Repetitive short-circuit tests have been carried out at three different case temperatures (i.e. 25ºC, 100 ºC, and 150 ºC) and experimental results demonstrate that the device can withstand more number of repetitions at higher case temperature. This effect is caused by the reduced drain current at higher case temperature, which leads to the lower generated energy.
3. **Short-circuit events lead to a higher on-state voltage and lesser power cycles to failure, affecting the RUL.**
   Mixed power-cycling/short-circuit tests have been performed to investigate the impact of short-circuit events on the power cycling and the RUL. With a larger number of short-circuit events, the higher gate leakage current results in the higher on-state voltage. The increased conduction loss leads to a higher junction temperature swing and less number of cycles to failure. Based on the relationship between the number of cycles to failure and the number of short-circuit events, the revised model considering short-circuit events can be a suitable candidate to achieve a more accurate RUL estimation.
4. **The molten Al flowing through the formed SiO_2 crack is the cause of gate degradation.**
   Failure analysis and thermo-mechanical simulation results reveal the gate degradation mechanisms. Due to the CTE mismatch between Al and SiO_2, the mechanical stress exceeds the limitation and the crack is formed. Then the Al temperature reaches the meting point and the molten Al flows through the crack. The conductive path between gate- and source terminal leads to the gate leakage current increase.
5. **Sintered Cu foil on the top side could be an effective approach to mitigate this short-circuit degradation.**
   Based on the degradation mechanisms, a mitigation approach has been proposed. Transient thermo-mechanical simulation results show that the Al temperature increase and the mechanical stress in the SiO_2 layer can be reduced when the sintered Cu foil is applied on the top side of the chip. This can avoid Al metallization reconstruction and mitigate the gate leakage current issue.

6.3 Proposals for Future Work

The possible future work is listed below:

1. **Validation of revised lifetime model for single short-circuit event**
   The gate leakage current increases gradually with the number of short-circuit repetitions, which aggravates the ageing process and leads to the less number of cycles to failure. Considering the cumulative effect of short-circuit degradation, mixed power-cycling test with a single short-circuit event needs to be performed to validate the proposed lifetime model in Section 4.3.

2. **Introducing short-circuit events at different number of cycles**
   Different number of short-circuit events were introduced into the power-cycling test at the same number of cycles (e.g. 10% N_f). The purpose of this approach is to keep the short-circuit energy same at each repetition. Since the short-circuit robustness may be decreased with the number of cycles, the number of cycles when short circuit happens might have different effects on its remaining useful life.
3. **Experimental verification of the device with sintered Cu foil**
   When the Cu foil is Ag sintered on the top-side chip, the simulation result show that short-circuit degradation can be mitigated. Further work can be done on performing experimental test of both the conventional discrete SiC MOSFET and the one with sintered Cu foil. The actual mitigation effect can be evaluated quantitatively.
4. **Body diode voltage measurement after short-circuit stress**
   As presented in Fig. 4.21 (a), Page 56, the relationship between body diode voltage and junction temperature has been changed after short-circuit events. A possible explanation is that the leakage through the gate oxide prevents the channel from being fully off, which alters the measurement. This hypothesis needs to be verified in the future work.

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