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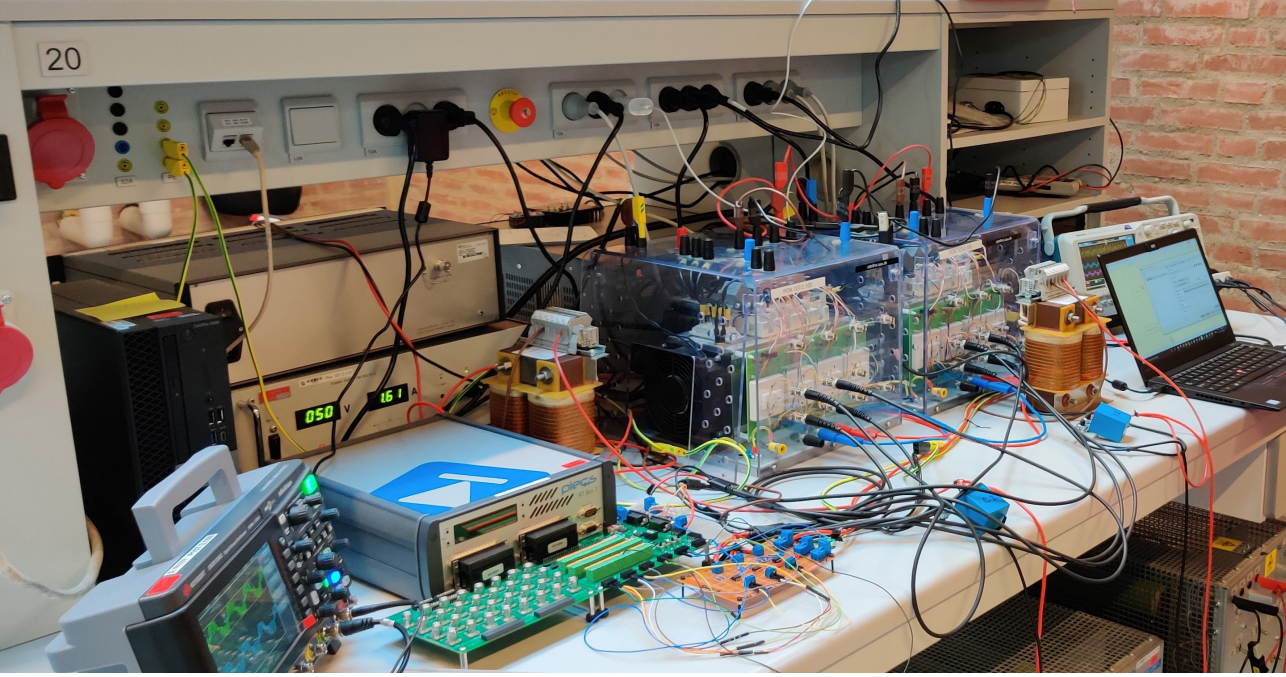

DC-LINK HARMONIC CURRENT MITIGATION STRATEGIES FOR IMPROVEMENT OF DC-LINK CAPACITOR LIFETIME IN A MULTIDRIVE SYSTEM

BY
SILPA BABURAJAN

DISSERTATION SUBMITTED 2022

AALBORG UNIVERSITY
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DC-link Harmonic Current Mitigation Strategies for Improvement of DC-link Capacitor Lifetime in a Multidrive System

Ph.D. Dissertation

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Curriculum Vitae

Silpa Baburajan

Silpa Baburajan (S'18) received a B.Sc. degree in Electrical Engineering from the American University of Sharjah, United Arab Emirates, in 2015, and M.Sc. degree in Electrical Engineering from the Rochester Institute of Technology, U.S.A, in 2017. Currently, she is pursuing a Ph.D. degree in Power Electronics Engineering in collaboration with Danfoss Drives A/S, Gråsten, from the Aalborg University, Denmark. From 2015 to 2016, she served as a Graduate Teaching Assistant, and then as Assistant Lecturer (January 2018-June 2018) at the Rochester Institute of Technology, U.S.A.

Her current research interests include harmonic analysis and mitigation techniques in multidrive system, and DC-link capacitor lifetime in power electronics. Furthermore, she was one of the 16 students, who were selected from different study backgrounds to work with a start-up in the Scandinavian Growth Creators Program, Denmark, 2020. She worked closely with an Aalborg University Startup "Cryer" for 7 sessions and was a part of their development, where she gained knowledge about tools and methods within the field of business development.

Abstract

It is now a common practice to connect multiple drives to a common AC supply system at the point of common coupling. In this kind of conventional parallel-connected system, each inverter shares the common AC-link. This means that the total number of rectifiers for each of these inverters needed in the whole system increases with the increasing number of converters connected in parallel [**J1**]. This causes, an increase in the overall size and reducing the reliability of the overall multidrive system. To overcome this challenge, in this Ph.D. research, a multidrive system having a common DC-link (using a centralized rectifier), is utilized [**J2**]. Notably, the centralized rectifier is sized according to the total load power demand and is connected to the AC-supply. In such cases, the common DC-bus provides power to the drive modules. Each drive module has its individual inverter, which then converts the DC-power to AC-power and then transfers it to the associated motor. Moreover, in case if the centralized rectifier fails, the common DC-bus can be powered by battery or generation from other renewable sources that can provide sufficient power to continue the load system at the same operating conditions (in the meantime could be possible to correct the rectifier system).

However, in such parallel systems, the DC-link current harmonics may increase, causing unstable operation, and possible failure of the fragile components such as DC-link capacitors and consequently multiple system downtime and extra maintenance requirement [**J1**]. Given this background, it can be inferred that in a DC-bus-connected multidrive system, there is a need for research in the analysis of DC-link harmonics mitigation methods, and the design of DC-link capacitors to reduce the overall effect of DC-harmonics and increase the lifespan of DC-link capacitor.

The main focus of this Ph.D. project is to mitigate the DC-link harmonics in a multidrive based drivetrain system. Then to also improve the lifetime of DC-link capacitor. First, an analytical model is developed to find the DC-link capacitor-current [**J1,J2**]. Next, using developed DC-current harmonics mitigation techniques, the DC-link current harmonics will be reduced. This will significantly reduce the DC-link capacitor current,

which will reduce the power-losses within the DC-link capacitor and reduce the hotspot temperature, due to which the overall reliability will increase. Also, using this achieved proposed minimum DC-link capacitor current, a capacitor sizing/design [**J1,J2**] is proposed which could reduce the volume as well as cost of DC-capacitor bank up to 50%, and increase the lifetime, considering the worst-case scenarios in motor drive system.

The results from this Ph.D. research can serve as a guideline for minimizing the DC-link harmonics in multidrive system and for practically designing the DC-link capacitor in multidrive applications using the proposed minimum DC-capacitor-current operation in a low-cost manner [**C1,J1,J2**].

Resumé

For at forbedre kapaciteten, fleksibiliteten og pålideligheden af industrielle motorstyringer, er det blevet almindelig praksis at tilslutte flere drev (multidrevsystem) til et fælles AC-forsyningssystem. Denne form for konventionelle parallelforbundne motorstyringer har hver sin inverter til at styre sin elektromotor med sit eget individuelle ensrettersystem og deler dermed det fælles AC-forsyningssystem. Det betyder, at det samlede antal ensrettere, der er nødvendige i hele systemet, stiger proportionalt med øgede antal parallelkoblede omformere, hvilket i sidste ende vil forøge den samlede størrelse på systemet og endda kunne reducere pålideligheden af det samlede multidrevsystem. For at løse denne udfordring omhandler denne PhD afhandling et multidrevsystem med et fælles DC-link (ved hjælp af kun en centraliseret ensretter). Den centraliserede ensretter er dimensioneret i overensstemmelse med det samlede belastningseffektbehov og er alene forbundet til AC-forsyningen. I sådanne tilfælde leverer den en fælles DC-bus strøm til drevmodulerne (inverter og kondensator). Hvert drevmodul har sin individuelle inverter, som konverterer DC-effekten til AC-effekt som via dette overfører effekten til den tilhørende elektromotor. Parallelforbindelsen af omformere med fælles DC-bus har af flere årsager fået øget opmærksomhed i de seneste år; løsningen har øget pålidelighed gennem et reduceret antal konverteringstrin, modularitet, nem vedligeholdelse gennem drift af identiske enheder, et skalerbart design, samt en reduceret størrelse af det overordnede system. Derudover kan den fælles DC-bus forsynes af et batteri eller andre vedvarende kilder, hvis den centraliserede ensretter svigter og dermed levere tilstrækkelig strøm til at fortsætte driften af motordrevene (i mellemtiden kunne det i nogle tilfælde være muligt at oprette ensrettersystemet igen).

I sådanne parallelle systemer med flere invertere tilsluttet samme DC-bus, kan der genereres en større strømrippel (harmoniske) i DC-linket på grund af de harmoniske vekselvirkninger mellem inverterne, som eksisterer ud over de harmoniske fra puls- breddemodulations metoderne, der skal til for at drive motorerne. Denne harmoniske interaktion i DC-linket kan resultere i øgede DC-link strømharmoniske, give ustabil drift og

mulig fejl i de mest sårbare komponenter, såsom kondensatorerne og med risiko for flere nedetider og ekstra vedligeholdelseskrav.

På denne baggrund er det projektets hypotese, at der i et DC-bus-forbundet multidrevsystem er behov for studier af metoder til reduktion af de DC-link strømharmoniske, og dermed også muliggøre et design af DC-link kondensatorerne for at øge deres levetid. Der udfærdiges en analytisk model til at kunne bestemme DC-link kondensatorstrømmen i et sådant multidrevsystem, som vil hjælpe hardware designere med at beregne DC-kondensatorstrømmen i systemer med flere drev. Dernæst, ved hjælp af den udviklede analytiske model, er det muligt at reducere de harmoniske strømme via en optimal interleaving-teknik (overlappende drift) af inverternes udgangsstrømme ved at faseforskyde modulations-bærebølgerne af de parallelforbundne invertere. Dette vil kunne reducere DC-link-kondensatorstrømmen betydeligt, og dermed også reducere effekttabene i DC-link-kondensatoren, samt hotspot-temperaturen i disse. En følgeeffekt vil være at den samlede pålidelighed vil stige. Ved at bruge den foreslåede minimale DC-link-kondensatorstrøms metode foreslås en ny design-metode, der kan bestemme levetid, effekttab, pris og volumen på kondensatorerne. Den foreslåede metode kan reducere volumen og omkostningerne ved DC-kondensatorbanken med op til 50

Contents

Thesis Details

Thesis Title:	DC-link Harmonic Current Mitigation Strategies for Improvement of DC-link Capacitor Lifetime in a Multidrive System
Ph.D. Student:	Silpa Baburajan
Supervisors:	Prof. Frede Blaabjerg, Aalborg University
Co-Supervisors:	Assistant Prof. Haoran Wang, Aalborg University Senior R & D Engineer Dr. Dinesh Kumar, Danfoss

The main body of this thesis consist of the following papers:

Publications in Peer-Reviewed Journals and Conferences

[**J2**] **S. Baburajan**, H. Wang, F. Mandrile, B. Yao, Q. Wang, D. Kumar, and F. Blaabjerg, "Design of Common DC-Link Capacitor in Multiple-Drive System Based on Reduced DC-Link Current Harmonics Modulation," *IEEE Transactions on Power Electronics*, Status: Accepted (Early Access).

[**J1**] **S. Baburajan**, H. Wang, D. Kumar, Q. Wang, and F. Blaabjerg, "DC-link Current Harmonic Mitigation via Phase-shifting of Carrier-waves in Paralleled Inverter Systems," *Energies*, vol. 14, no. 14, pp. 1–16, 2021.

[**C1**] **S. Baburajan**, S. Peyghami, D. Kumar, F. Blaabjerg, and P. Davari, "Effect of Unipolar and Bipolar SPWM on the Lifetime of DC-link Capacitors in Single-Phase Voltage Source Inverters," *European Conference on Power Electronics and Application*, pp.1–10, 2020.

The submitted thesis for assessment is in partial fulfillment of the PhD degree. It is based on the submitted or published scientific papers which are listed above, and parts of the published papers are used directly or indirectly in the thesis. Co-author statements have been made available to the assessment committee and are also available at the Faculty. The thesis is not in its present form acceptable for open publication but only in limited and closed circulation as copyright may not be ensured.

Preface

The work presented in this dissertation is a summary of the outcome from the Ph.D. project "DC-link Harmonic Current Mitigation Strategies for Improvement of DC-link Capacitor Lifetime in a Multidrive System", which was carried out at the Department of AAU Energy, Aalborg University, Denmark.

I am grateful for all experiences - a lot of harsh downs and little ups at Aalborg University, which made me stronger and helped me realize what I want to achieve in the long run in my life. I would like to thank the main supervisor Professor Frede Blaabjerg, the co-supervisors Dr. Haoran Wang and Senior R & D Engineer Dr. Dinesh Kumar, and all co-authors.

Last but not the least, and most importantly, I would like to express my gratitude to my family for having faith in me even during the difficult days when I did not believe in myself and supporting me. If not for them, I would not have been able to complete my Ph.D. thesis.

Being a self-funded student, there were lots of hard times for me, and a special thank you to my family for financially supporting my PhD studies throughout.No amount of words is enough to describe the strength my family have been providing me all my life.

Silpa Baburajan
Aalborg University, June 15, 2022

Part I

Report

Chapter 1

Introduction

"The way I measure my life is –
Am I better than I was last year?"

Satya Nadella

1.1 Background

Overwhelming advancements in the power electronics technologies have been seen in the past few decades, owing to the growing energy demands, increasing trend of utilizing renewable energy resources, in addition to the important role played by power electronics in improving for energy efficiency, in electric vehicles, as well as strong growing industrial automation. That also means, power electronic systems are major consumers of electricity. Looking at Fig. 1.1, it can be observed that electric-drive systems consume more than 40% of the electricity in the world. Hence, to improve the overall efficiency of the electric-motor-driven systems, the use of multidrive systems have been increased in the past few years.

1.2 Common Parallel Connected Multidrive System

Commonly, multiple adjustable-speed-drive (ASD) systems are connected to a common point of coupling (PCC) in the AC utility system, [2–5]. In this kind of (conventional) parallel-connected system [2, 6, 7], each inverter has its own individual rectifier system and shares a common AC-link, as shown in Fig. 1.2. This means that the total number of

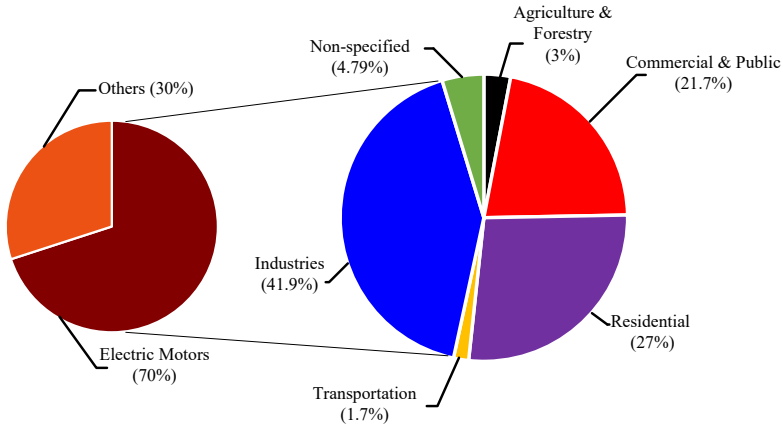


Fig. 1.1: Estimation of electricity consumption by electric-motor-driven systems [1]

rectifiers connected to the AC-supply in the whole system increases with the increasing number of converters connected in parallel, eventually increasing the overall size and cost of the overall multidrive system. Here, there is a potential to save cost by using a common Dc-link and also utilize the energy better. If one unit breaks, the other unit can consume it. This can not be done using a common AC-link system.

To overcome this challenge, in this Ph.D. research, a common DC-link (having a centralized rectifier sized according to the total load power demand, and it is connected to the AC-supply), is utilized as shown in Fig. 1.3.

There are several benefits of employing DC-bus-connected multidrive system. Firstly, this lowers the total system cost [**J2**], [8]. Secondly, because of the reduced component count, the space savings are improved, and the reliability is increased as now a centralized rectifier is used instead of each inverter having its rectifier [**C1**], [**J1**], [9]. This kind of common connection also helps to breaching energy from one unit to feed another unit. Moreover, in case the centralized rectifier fails, the common DC-bus can be powered by battery connected to the DC-link system which can provide sufficient power to continue the load system at the same operating conditions (in the meantime it is possible to do maintenance of the rectifier system). Additionally, it is possible to connect renewable energy resources such as PV inverters due to their DC nature with ease at the common DC-bus of the multidrive system [10,11] and [7,12], [**J2**] shown in Fig. 1.3.

Despite the above stated benefits, one of the main challenges of the multidrive system is the presence high DC-link current harmonics content in the system [13–15] which may

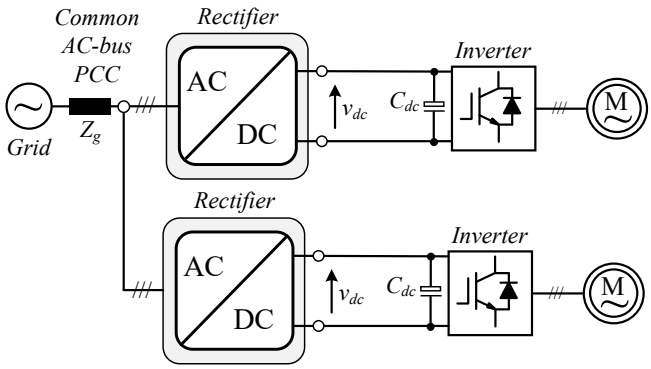


Fig. 1.2: Schematic of a conventional parallel-connected system.

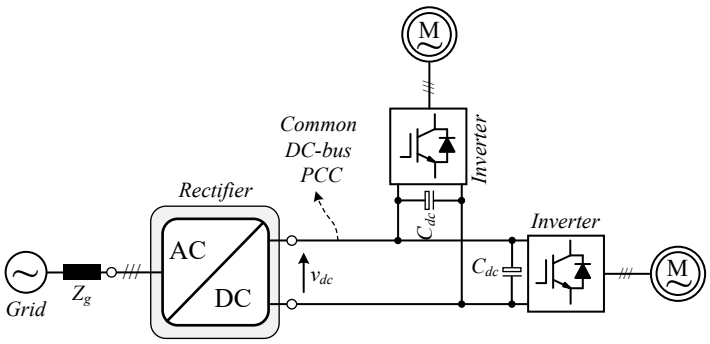


Fig. 1.3: A simple block diagram of DC-bus-connected multidrive systems.

cause failure of fragile components such as DC-link capacitors [2,16].

1.3 DC-link Capacitor in Multidrive System

DC-link capacitor, is important in power conversion stages for several industrial applications. “Often, aluminum-electrolytic-capacitors (El-caps) are used as DC-link capacitors, due to their advantage of providing a high capacitance per unit volume at low costs compared to other types of capacitors ”[**J1**]

The lifetime of DC-link capacitors depend on the power losses with in the capacitor, which in turn depend on the DC-link current. In a proposed multidrive system where a number of drives sharing a common DC-bus, the lifetime of DC-link capacitors, becomes more challenging due to the presence of high DC-link current harmonics, which increases DC-link capacitor current. This decreases DC-capacitor lifetime due to an increase in the internal temperature [**J1**]. To extend the lifetime of the DC-link capacitor, in this thesis, the current stresses of the DC-link capacitor is actively reduced in a low-cost manner.

1.4 Literature Review of Multidrive System

A few researchers have focused on reliability of DC-capacitors [17–19]. A lifetime estimation comparison between El-caps and slim capacitors under grid voltage unbalanced conditions are detailed in [17]. A review of reliability of DC-capacitors are presented in [18]. A time equivalent model for obtaining the electro-thermal stress of [**J2**] individual capacitors under grid voltage unbalance is proposed by [19] [**J2**]. The available literature has not so far addressed a cost-effective harmonic mitigation techniques in multidrive systems with a centralized rectifier".

"A plethora of research has also been conducted on DC-link harmonic mitigation techniques, like interleaving the carrier-waves of parallel-connected PWM inverters to reduce the DC-link current harmonics [3, 5, 20–22]. Lowering the DC-link harmonics reduces the power-losses within the capacitors [20]. In a parallel-connected system, the phase-shifted switching-cycles of the carrier-waves can effectively reduce the current ripple; as a result [5], the size and weight of passive components, such as the DC-link capacitors and harmonic filters, can be reduced. A detailed study of a harmonic reduction technique using synchronized phase-shifted PWM voltage source inverter (VSI) units having an individual DC-source has been provided in [2]. Alternatively, article [3] presents the effect of an optimal phase-shift angle on reducing DC-current ripples under unequal DC-link voltage scenarios in two parallel three-phase grid-connected VSI units ” [**J1**]. Discussion on connecting multiple converters in parallel, and how an interleaving scheme has reduced the harmonics at the common point of connection, is presented in [22]. However, multiple standard drives systems are connected to a common AC

source in these aforementioned articles using their own individual rectifier resulting in an increased number of converters in the system [**J2**]. There have been studies on DC-link ripple current reduction for paralleled three-phase voltage source converters with interleaving in [23, 24]." However, for single phase systems, not much literature is available.

Given this background, it can be stated that in a DC-bus-connected multidrive single-phase system, there is a research gap in the analysis of DC-link harmonics mitigation methods to reduce the overall effect of DC-link harmonics and increase the lifespan of DC-link capacitor in a low-cost manner.

1.5 Project Motivation

Knowing that some power-losses in multidrive systems are unavoidable in reality, to address the aforementioned research gaps, it is necessary to find methods to mitigate the DC-link current harmonics and to improve the lifetime of DC-capacitor in multidrive systems.

1.6 Project Objectives and Limitations

1.6.1 Research questions and objective

The main goal of this Ph.D. study to find whether it is possible to increase the drive system reliability of multidrive systems, and it can be formulated by the following overall research questions:

1. *"How to mitigate the DC-link harmonics in a multidrive based drivetrain system?"*
2. *"How to maintain or increase DC-link capacitors lifetime?"*

Based on the overall research questions, multiple sub-objectives are formulated in order to solve the problems:

1. **Find which sinusoidal pulse-width modulation (SPWM) strategies produces least DC-link capacitor-current harmonics in a multidrive system**

   The multidrive system will be modulated using unipolar and bipolar SPWM [**C1**] to find which SPWM produces the least amount of the DC-link capacitor current harmonics. After that, the lifetime of DC-link capacitor in the multidrive will be modelled to see whether unipolar and bipolar SPWM results in a higher DC-capacitor lifetime. The following will be the case scenarios: DC-link capacitor lifetime versus different loading conditions, and DC-link capacitor lifetime versus different values of the modulation-amplitude-index (M_A). This evaluation will

help to understand better, which SPWM modulation produces the minimum DC-link harmonics (produces least electro-thermal stress on the DC-link capacitor) and has a better DC-link capacitor lifetime in a DC-bus-connected multidrive system.

2. **Propose two different configurations of common DC-connected multidrive systems**

   Two common DC-link structures will be proposed [**J1**]: one multidrive system with an individual DC-bank and another multidrive system with a common DC-bank. In the proposed systems, a centralized rectifier is to be implemented to reduce the overall cost and reduce the number of power electronic components (rectifiers) and thereby increasing the overall system reliability.

3. **Propose a new modulation method to reduce the DC-link capacitor requirement for the above proposed topologies**

   A carrier phase-shifting strategy will be implemented for the above two proposed multidrive systems. This method does not need to change any hardware in the system, while the DC-link ripple and capacitance are expected to be reduced, which benefits the cost, volume, and weight of the overall system [**J1**]. The effectiveness of this mitigation strategy will be analyzed even in cases where the inverters do not have the same output power.

4. **Design the common DC-link capacitor in a multidrive system based on the analytically modelled and reduced DC-link capacitor-current**

   After reducing DC-link current analytical, "a new capacitor sizing/design will be proposed considering the lifetime, power-loss, cost, and volume of the DC-capacitor bank based on the reduced new DC-link capacitor current " [**J2**].

The overall research activities in this Ph.D. project are summarized in Fig. 1.4.

1.6.2 Project limitations

The discussions in this project are limited to parallel-connected single-phase motor systems in a multidrive system. Due to the time restrictions, proposed solutions have not been extended to three-phase systems. Also, in this Ph.D. thesis, the switching frequency is considered to be 20 kHz.

1.7 Thesis Outline

The research outcomes of the Ph.D. project are submitted as a collection of papers published during the Ph.D. study. First part of this thesis is the **Report** and second part is the **Publications.** The thesis structure is illustrated in Fig. 1.5.

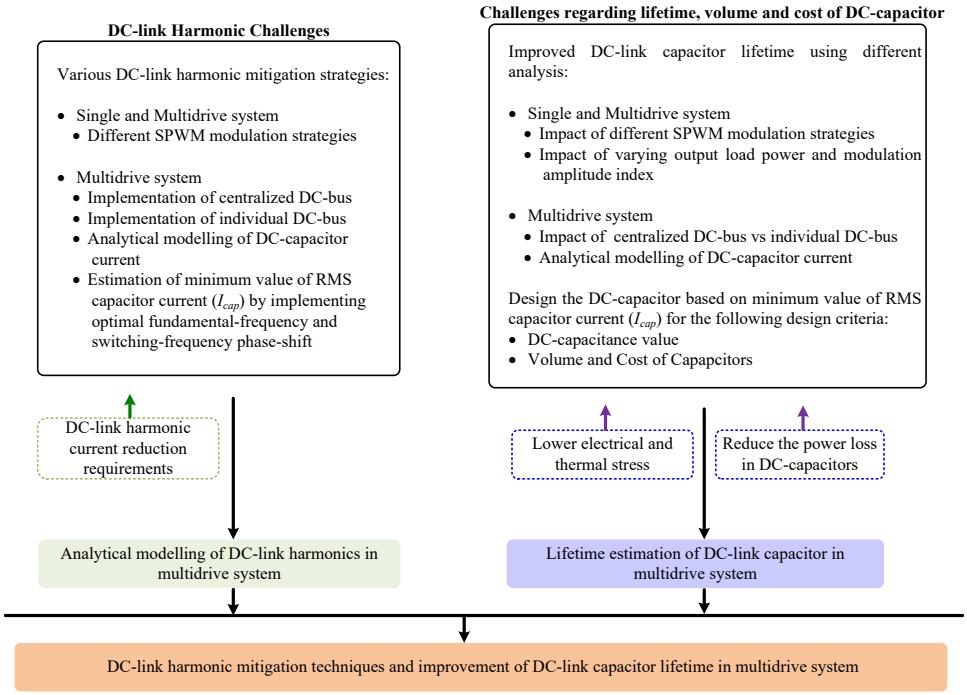


Fig. 1.4: Research activities in the Ph.D. project: DC-link Harmonic Mitigation Strategies and Improvement of DC-link Capacitor Lifetime in Multidrive System.

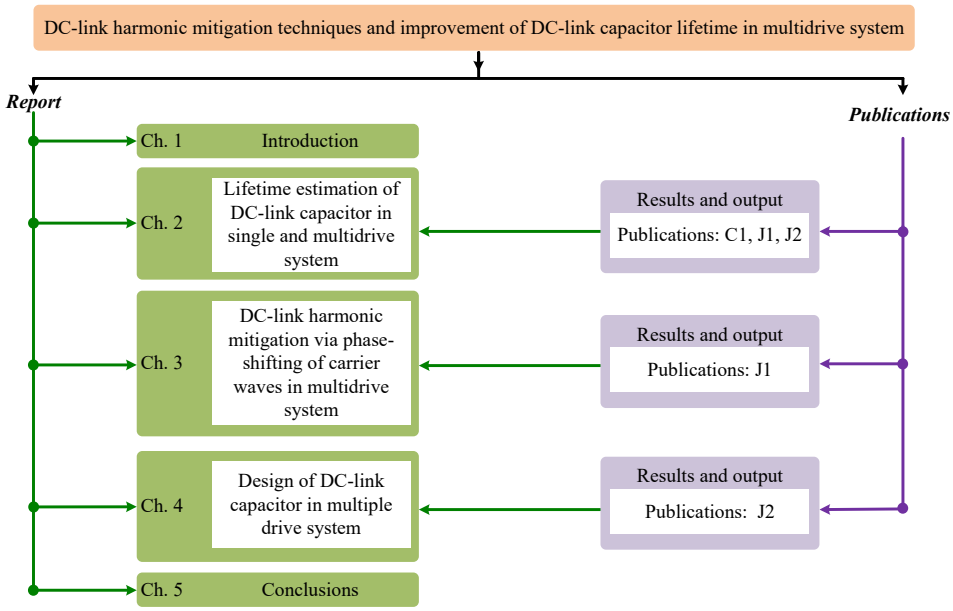


Fig. 1.5: Thesis structure and key articles of each chapter.

The **Report** has five chapters, where the main results are based on the **Publications**. Chapter 1 gives the introduction of the Ph.D. thesis [**C1, J1, J2**] where the background of the research topic, project motivation, and research questions are discussed in detail. The following Chapter 2 focuses on the impact of different SPWM techniques on the lifetime of DC-link capacitors in DC-bus-connected multidrive systems [**C1**]. The DC-link harmonics are modelled in PLECS and the lifetime of DC-link capacitors are modelled in MATLAB. The following two chapters focus on the DC-link harmonic mitigation techniques and design the of the DC-capacitor based on proposed minimum DC-capacitor-current [**C1**]. In Chapter 3, a carrier-based phase-shifting scheme is presented to minimize the DC-link current harmonics in the two proposed configurations of a common DC-bus connected multidrive systems that have a centralized rectifier [**C1, J1**]. The proposed DC-link harmonic mitigation strategy is also experimentally validated. The analytical modelling of the DC-link current harmonics in a multidrive system is developed in Chapter 4 [**J2**]. Also, in this chapter, a a low cost-effective design method for the DC-link capacitor is explained. Finally, the summary of this Ph.D. thesis along with the future research is in Chapter 5.

1.8 List of publications

The research outcomes during the Ph.D. study have been published as listed in the following. Parts of these publications are used in the Ph.D. thesis, providing reference.

Publications in Peer-Reviewed Journals and Conferences

[**J2**] **S. Baburajan**, H. Wang, F. Mandrile, B. Yao, Q. Wang, D. Kumar, and F. Blaabjerg, "Design of Common DC-Link Capacitor in Multiple-Drive System Based on Reduced DC-Link Current Harmonics Modulation," *IEEE Transactions on Power Electronics*, Status: *Accepted (Early Access)*.

[**J1**] **S. Baburajan**, H. Wang, D. Kumar, Q. Wang, and F. Blaabjerg, "DC-link Current Harmonic Mitigation via Phase-shifting of Carrier-waves in Paralleled Inverter Systems," *Energies*, vol. 14, no. 14, pp. 1–16, 2021.

[**C1**] **S. Baburajan**, S. Peyghami, D. Kumar, F. Blaabjerg, and P. Davari, "Effect of Unipolar and Bipolar SPWM on the Lifetime of DC-link Capacitors in Single-Phase Voltage Source Inverters," *Proc. of European Conference on Power Electronics and Application*, pp.1–10, 2020.

Chapter 2

Lifetime Estimation of DC-Link Capacitor in a Multidrive System

2.1 Background

Studies [25, 26] have shown that for different PWM techniques, DC-link capacitor-current as well as its harmonic spectrum changes, [7] which affects the DC-link capacitor's lifetime. So, in this chapter, the first DC-link current harmonic mitigation method in this thesis is analyzed with different modulation schemes. The lifetime of DC-link capacitors in a multidrive system sharing a common DC-bus is analyzed for unipolar and bipolar SPWM to find which of the modulation techniques produce the least capacitor-ripple current at different output power levels and different values of the M_A [**C1**].

2.2 System Description

An H-bridge VSI like shown in Fig. 2.1 and a multidrive system with centralized DC-capacitor-bank shown in Fig. 2.2 are used in this chapter. To keep it simple, this chapter uses only a resistor as a load, and also assumes that the rated RMS load voltage as well as load frequency remains constant [**C1**].

A large DC-link capacitor-bank ($C_{dc-bank}$) having El-caps, are used in both topologies. The total DC-link capacitor-ripple current is represented by ($I_{capbank}$).(I_{cap}) de-

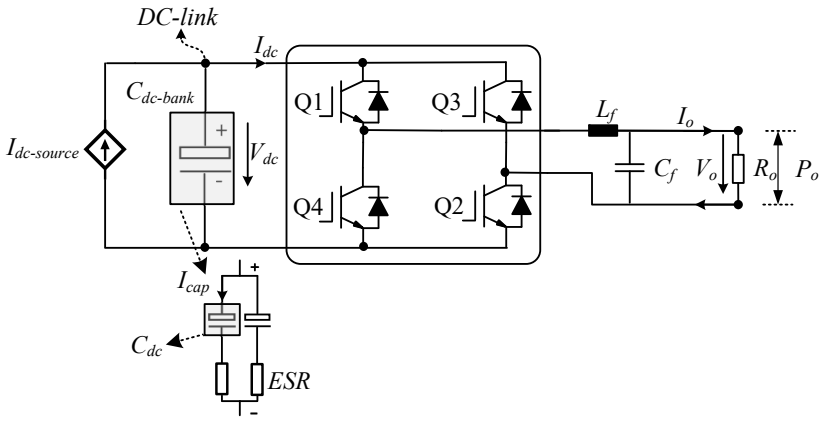


Fig. 2.1: Schematic of single-phase voltage source inverter [**C1**].

notes the single capacitor current. $I_{dc-source}$ denotes the DC source current, I_{dc} is the current drawn by the total load. The specifications of the VSI units are given in Table 2.1 and that of the inverter output filter (L_f and C_f), designed according to [27] is given in Table 2.2 [**C1**]. The DC-capacitor is designed according to [28, 29] and the chosen capacitor(s) data [30] is shown in Table 2.3 and Table 2.4 respectively [**J2**].

2.3 SPWM Modulation Schemes

The topologies use both unipolar SPWM and bipolar SPWM, which are detailed in [31] to control the four switches Q_{x1}, Q_{x2}, Q_{x3}, Q_{x4} (where x= U or L), in the VSI units [**C1**]. The switching technique for unipolar and bipolar SPWM is shown in Fig. 2.3. In unipolar SPWM, when the sine wave is greater in amplitude than the triangular wave, then the switch Q_{x1} is turned on and the output of the 1st leg is $+V_{dc-ref}/2$. Otherwise, when sine wave is less than triangular wave, then the switch Q_{x4} is turned on and the output of the 1st leg is -$V_{dc-ref}/2$. Comparing the negative sine wave with the triangular wave, when the negative sine wave is greater than the triangular wave, then the switch Q_{x3} is turned on and the output of the 2nd leg is $+V_{dc-ref}/2$ [**C1**]. On the other hand, when the negative sine wave is less than the triangular wave, the switch Q_{x2} is turned on and the output of the 2nd leg is -$V_{dc-ref}/2$. The difference of both leg output in case of unipolar SPWM varies between 0 to $+V_{dc-ref}$ and 0 to -V_{dc-ref}. Now for the bipolar SPWM, when the sine wave is greater in amplitude than the triangular wave, then the switches Q_{x1} and Q_{x2} are turned on, producing an output $+V_{dc-ref}/2$

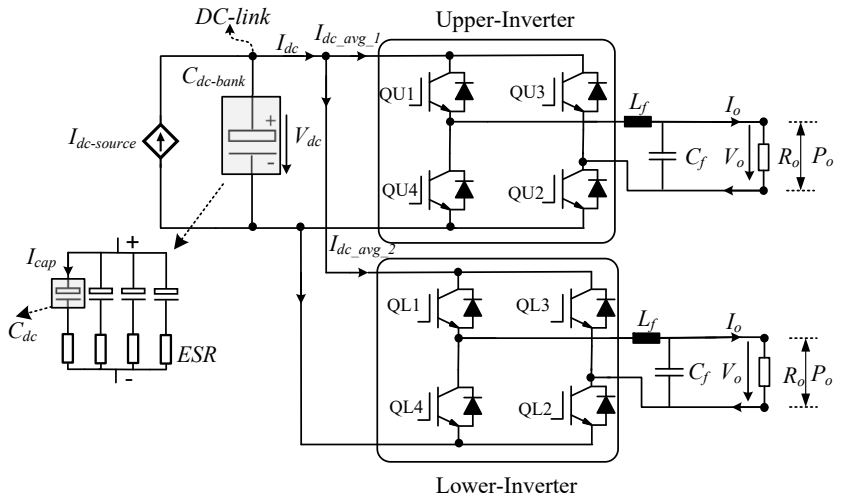


Fig. 2.2: Schematic of a multidrive system with two parallel voltage source inverter units connected to a common DC-bus with paralleled capacitors [**C1**].

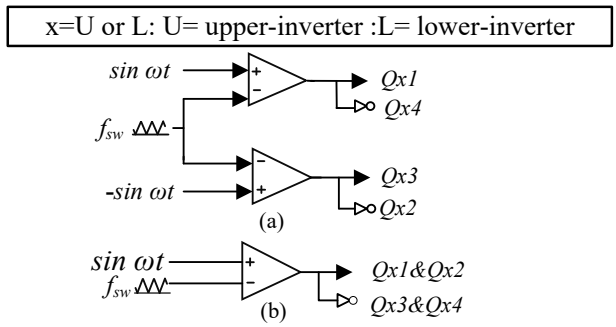


Fig. 2.3: Control algorithm for (**a**) unipolar SPWM, (**b**) bipolar SPWM.

Table 2.1: Specifications of the VSI units shown in Figs. 2.1 and 2.2 [**C1**].

Parameter	Symbol	Value
Rated power (kW)	P_o	2.5
Load (Ω)	R_o	20
Rated RMS load voltage (V)	$V_{sine-ref}$	230
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	400
Switching-frequency (kHz)	f_{sw}	20
Modulation-amplitude-index	M_A	0.8

Table 2.2: Specifications of the inverter output filter [**C1**].

Parameter	Symbol	Value
Inductor-filter ripple current limit	I_{f_ripple}	20%
Inductor (mH)	L_f	2
Filter cutoff frequency (kHz)	f_{cutoff} (f_{cutoff}<$f_{sw}/10$)	2
Filter capacitor (μF)	C_f	6

Table 2.3: Design criteria for DC-link capacitor [**C1**].

Parameter	Symbol	Value
Ripple DC-link voltage peak to peak (p−p) value (V)	V_{p-p}	20
Hold-up time (ms)	$t_{hold}(=1/f_o)$	20
Minimum required capacitor value (mF)	C_{min}	3.3

Table 2.4: Datasheet of the chosen DC-capacitor (BDK4345) [30]

Parameter	Symbol	Value
Single capacitance (μF)	C_{dc}	460
Equivalent series resistance ($m\Omega$)	ESR	0.18 (at 100 Hz)
Thermal resistance (°C/W)	R_{th}	5.74
Rated lifetime (hours)	L_o	5000 (at T_{rated} & I_{rated})
Rated upper category temperature (°C)	T_{rated}	105
Rated ripple current (A)	I_{rated}	2.54 (at 100 Hz),
Rated voltage (V)	V_{rated}	500
Operating temperature (°C)	T_a	55

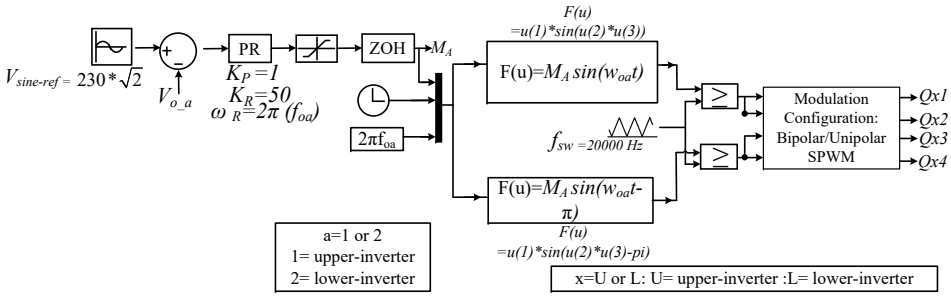


Fig. 2.4: Control algorithm for inverter unit output voltage (K_P−proportional parameter, K_R− resonant coefficient, ω_R−angular resonant frequency, ω_{oa}−angular output load frequency and ω_{oa}=2πf$_{oa}$) [**C1**][**J1**].

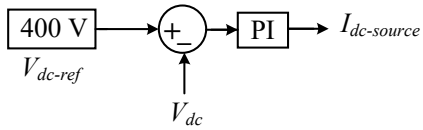


Fig. 2.5: Control algorithm for input DC-link voltage (V_{dc}: K_P-proportional parameter= 2, K_I-integrator parameter = 100 [**C1**].

in the 1st leg and -V_{dc-ref}/2 in the 2nd leg. Furthermore, when the sine wave is lesser in amplitude than the triangular wave, then the switches Q_{x3} and Q_{x4} are turned on, producing an output -V_{dc-ref}/2 in the 1st leg and +V_{dc-ref}/2 in the 2nd leg. Thereby, the output of the inverter when using a bipolar SPWM is +V_{dc-ref} to -V_{dc-ref} [**C1**].

"A Proportional-Resonant (PR) controller (designed according to [27, 32]) is used to maintain a rated output voltage of 230 V (RMS value) for each inverter unit. The control algorithm for the inverter unit output voltage is shown in Fig. 2.4. As both VSI units are synchronized for multidrive system, and have the same system ratings, the parameters for the controller of each inverter unit have the same value. A Proportional – Integral (PI) controller is employed to regulate the DC-link voltage (V_{dc}) at a rated value of 400 V using a current source as depicted in Fig. 2.5 " [**C1, J2**]. In this chapter, a constant source of DC power is assumed for simplicity in the analysis.

2.4 Lifetime Estimation of DC-link Capacitor

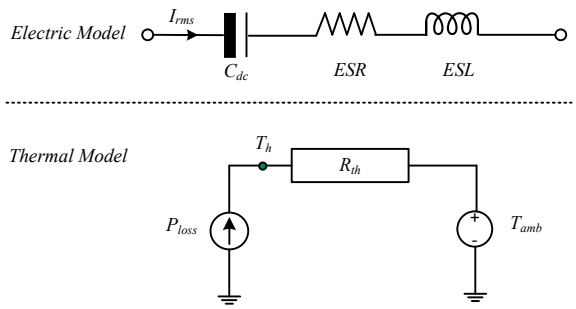


Fig. 2.6: Equivalent electrical and thermal model of the DC-link capacitor [**C1**].

2.4.1 Electrical and Thermal Stress Analysis

The equivalent circuit model for a DC-link capacitor used in this paper is illustrated in Fig. 2.6.

An increase in the electrical stress and thermal stress may increase the overall hot-spot temperature and power-losses with the capacitor, thereby, lowering DC-capacitor lifetime. With lesser DC-capacitor-current harmonics, the overall electrical and thermal stress in the capacitor decreases, which results in an improved DC-link capacitor lifetime, denoted by L_x [**C1**]. The electro-thermal stress of the DC-link capacitor can be found using the following equations :

$$T_h = T_a + (P_{loss} \times R_{th}) \tag{2.1}$$

$$P_{loss} = \sum_{i=1}^{n} (I_{rms(f_i)})^2 \times ESR(f_i), \tag{2.2}$$

where $I_{rms(f_i)}$ denotes the total DC-link capacitor current RMS value [**C1**] at the frequency f_i. The ESR at the i^{th} frequency f_i is depicted by $ESR(f_i)$. The total number of DC-link capacitor current harmonics is depicted by n. T_h is the hot-spot temperature of the DC-capacitor, estimated by (2.1). The power-loss P_{loss} of the capacitor is calculated using (2.2) [**C1**]. From the above two equations, it can be understood that decreasing the capacitor-current decreases the power-losses and decreases the capacitor core temperature (T_h). This means that lifetime of the DC-link capacitor will be increased.

2.4.2 Lifetime Estimation Equation

Finally, the lifetime of the El-caps can be estimated by using,

Table 2.5: Specifications of the VSI units shown in Figs. 2.1 and 2.2 [**C1**].

Case	No. of units	Unipolar SPWM	Bipolar SPWM
1.1	1	✓ $f_{sw} = 20$ kHz	✗
1.2	1	✗	$f_{sw} = 20$ kHz
1.3	1	✗	$f_{sw} = 40$ kHz
2.1	2	✓ $f_{sw} = 20$ kHz	✗
2.2	2	✗	✓ $f_{sw} = 20$ kHz
2.3	2	✓ $f_{sw} = 20$ kHz	✓ $f_{sw} = 20$ kHz
2.4	2	✓ $f_{sw} = 20$ kHz	✓ $f_{sw} = 40$ kHz

$$L_x = L_o \times (\frac{V_{dc-ref}}{V_{rated}})^{-p} \times 2^{\frac{T_{rated}-T_h}{10}} \tag{2.3}$$

where, for El-caps, p is between 3 and 5 [20]. The rated values are given previously in Table 2.4 and T_h can be calculated as explained in the above section using (2.1)-(2.2). This method of estimating the lifetime of DC-link capacitor is used throughout this Ph.D. thesis.

2.5 Case Studies for Lifetime Estimation of DC-capacitor

For simplicity, both inverter units in the multidrive system (shown in Fig. 2.2), are assumed to have same operating conditions. This helps to identify which SPWM technique produces the least amount of DC-link capacitor ripple and gives the longest lifetime. Two scenarios are analyzed in this chapter. In the first scenario, the two topologies shown in Figs. 2.1 and 2.2 are studied under varying output power conditions, and then in varying modulation indices [**C1**]. Simulations are carried out under four cases 2.1, 2.2, 2.3, and 2.4 using the specifications as explained in Table 2.5) [**C1**]. The results from the simulations can be summarized below.

2.5.1 Results of Scenario-1: Lifetime estimation for Different Output Power Conditions

The results from graphs in Figs. 2.7(a)-(b), indicate that the DC-link capacitor current increases with the increase in output power, thereby decreasing the lifetime of C_{dc} [**C1**]. The output power is varied by varying the resistor load value. From the three cases studies shown in Figs. 2.7(a), the DC-link capacitor lifetime is the highest in case 1.1 when the single unit VSI is using unipolar SPWM, compared to when using bipolar

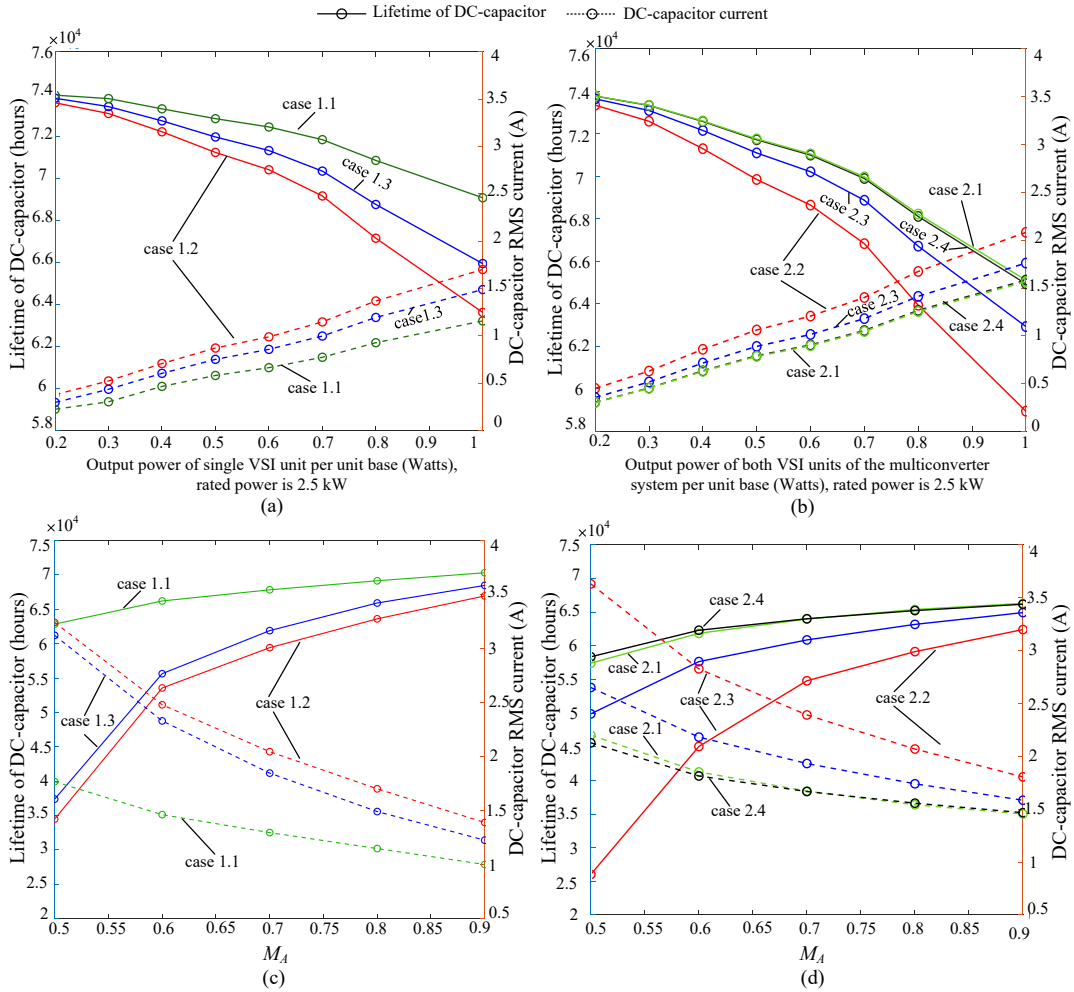


Fig. 2.7: Effect of SPWM techniques on the lifetime, *under different output power conditions in*: (**a**) single VSI unit (Fig. 2.1), (**b**) multidrive system having a common DC-bus (Fig. 2.2), and *under varying values of modulation index M_A in*: (**c**) single VSI unit (Fig. 2.1), (**d**) multidrive system having a common DC-bus and both inverters having same M_A (Fig. 2.2) [**C1**]. Note that single inverter has two parallel DC-link capacitors and multidrive system has four parallel DC-link capacitors

modulation. This is because, for unipolar modulation, the switching frequency harmonics appears at two times the switching frequency, which is far from the fundamental frequency compared to the bipolar SPWM where the switching frequency harmonics appears at the switching frequency itself. This results in unipolar modulation generating a lower harmonic content in the DC-link capacitor current, than bipolar SPWM. Also from Fig. 2.8, it can be seen that the DC-current ripples are lower when using unipolar SPWM (green wave) compared to the bipolar SPWM (red wave). Eventually, the RMS value of current flowing through the DC-link capacitor is reduced [**C1**]. From the right y-axis of Fig. 2.7(a), it can be observed that I_{cap} is less for unipolar SPWM compared to bipolar SPWM. This means that using unipolar SPWM results in lower electro-thermal stress on the capacitor compared to when using bipolar SPWM [**C1**]. It is visible from Fig. 2.7(a) that the L_x of case 1.3 (having $f_{sw} = 40$ kHz) is higher than in case 1.2 (having $f_{sw} = 20$ kHz). The is because the switching frequency harmonics will be further away from the fundamental frequency in case 1.3 and have lesser effect on DC-link capacitor fundamental current waveform [**C1**].

As expected from the single-unit topology results, in the multidrive system, when both inverters used unipolar SPWM, the DC-link current harmonics were lowest, thereby, resulting in a longer lifetime, compared to when using bipolar SPWM for both lower and upper VSI units. The Fig. 2.7(b), shows that simulation results match the expectations, where case 2.2 resulted in the lowest L_x and case 2.1 resulted in the highest L_x for the DC-link capacitor [**C1**].

From Fig. 2.7 (b) and (d) it can be seed that, case 2.1 and case 2.4 results in almost the same C_{dc} lifetime. This is because in both cases, the switching frequency harmonics appear at 40 kHz) . However, comparing case 2.1 and case 2.4, it is better to use case 2.1 because of the lower switching-frequency capacitor-current ripple as shown in Fig. 2.9 [**C1**]. The low switching ripple occurs as in the unipolar SPWM, the output is switched from 0 to $+V_{dc}$ in the first half-time period and then from 0 to -V_{dc} in the second half-time period compared to bipolar SPWM which has the output switched from $+V_{dc}$ to -V_{dc}. The lower switching ripples means that less heat is generated within the capacitor, which will increase the lifetime of DC-link capacitor. It can also be noted that for the DC-link capacitor, current when using two inverters is not double compared to when using a single inverter [**C1**]. This is because when using two inverters, the DC-capacitor bank has four parallel capacitors, compared to having two parallel capacitors in a single unit.

2.5.2 Results of Scenario-2: Lifetime estimation for Varying Modulation Amplitude Index

From the results shown in Fig. 2.7(c)-(d), it can be observed that DC-link capacitor current increases with the decrease in the modulation amplitude index [**C1**]. When the DC-link voltage is constant, and the M_A value decreases, the output voltage decreases

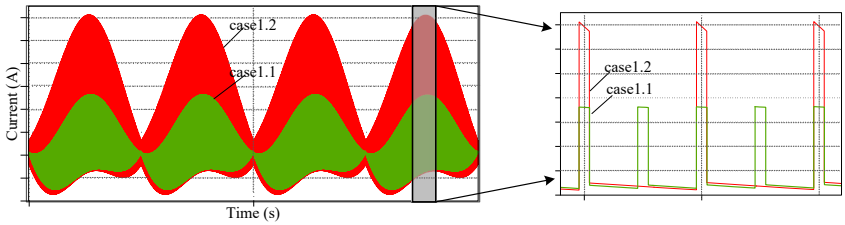


Fig. 2.8: At rated P_o = 2.5 kW and M_A= 0.8: time-domain waveforms DC-current for case 1.1 and case 1.2 in a single unit VSI (shown in Fig. 2.1) [**C1**].

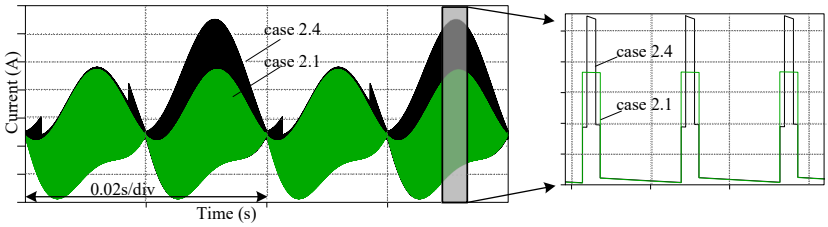


Fig. 2.9: At rated P_o = 2.5 kW and M_A= 0.8: time-domain waveforms of DC-current for case 2.1 and case 2.2 in a multidrive system (shown in Fig. 2.2) [**C1**].

[**C1**]. Thereby, to maintain a constant output power (by changing output load values), the output current increases, which causes a decrease in the lifetime of C_{dc}. It can be seen from the result in Fig. 2.7(c) that for this scenario also, the unipolar SPWM gives the highest lifetime for DC-link capacitors in a single unit VSI whereas bipolar SPWM produces the lowest L_x [**C1**]. Likewise, for the two VSI unit's topology, the highest lifetime for the C_{dc} as shown in Fig. 2.7(d) is observed when both units have unipolar SPWM. This is because of the lower DC-capacitor-current ripple produced when using unipolar SPWM as illustrated in Fig. 2.9, which results in the least thermal stress on the capacitor and consequently giving the highest lifetime [**C1**].

2.6 Summary

This chapter investigated the effect of different SPWM techniques [**C1**] on the lifetime of the DC-link capacitor in a multidrive topology having a common DC-bus. Two scenarios were analyzed in this study. The obtained results indicate that when using a unipolar SPWM, it produces a lower harmonic current in the I_{cap}, consequently a longer DC-link capacitor lifetime. This is because, for unipolar modulation, the switching frequency harmonics appears at two times the switching frequency, which is far

from the fundamental frequency compared to the bipolar SPWM where the switching frequency harmonics appear at the switching frequency itself. This results in unipolar modulation generating a lower harmonic content in the DC-link capacitor current, than bipolar SPWM. The lower the value of I_{cap} is, the longer is the lifespan of the capacitor due to a decrease in the power-losses, which will decrease the core-temperature.

Publication in Peer-Reviewed Conference

[**C1**] **S. Baburajan**, S. Peyghami, D. Kumar, F. Blaabjerg, and P. Davari, "Effect of Unipolar and Bipolar SPWM on the Lifetime of DC-link Capacitors in Single-Phase Voltage Source Inverters," *European Conference on Power Electronics and Application*, pp. 1–10, 2020.

Chapter 3

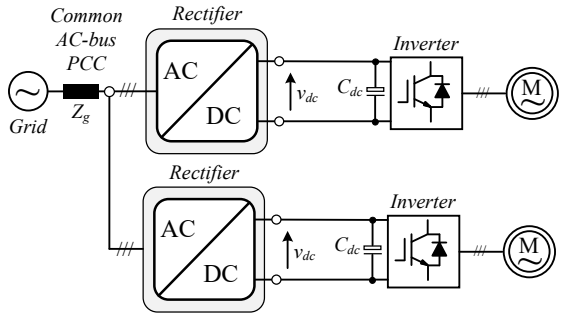
DC-bus Harmonic Mitigation in a Multidrive System

In the previous chapter, it is given that using a unipolar SPWM produces a lower DC-link harmonic content and thereby a longer lifetime of the capacitors [**J1**]. With this knowledge, in this chapter we are trying to further minimize the DC-link current harmonics using a carrier-based phase-shifting scheme in multidrive systems that have a centralized rectifier [**J1**].

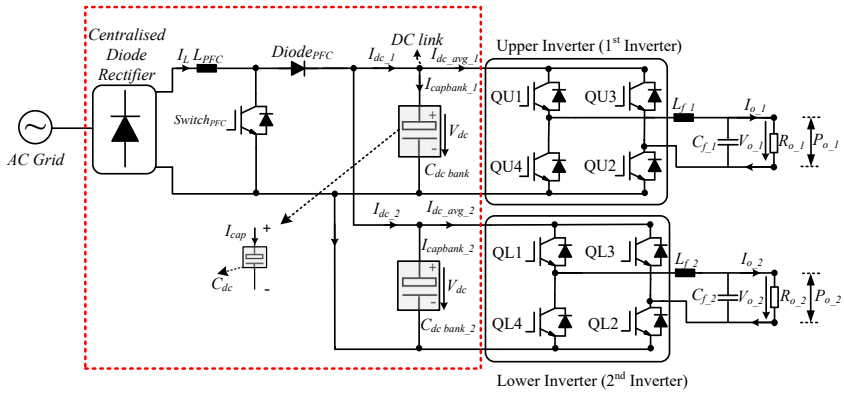
3.1 Background

The following are the key contributions [**J1**] of this chapter:

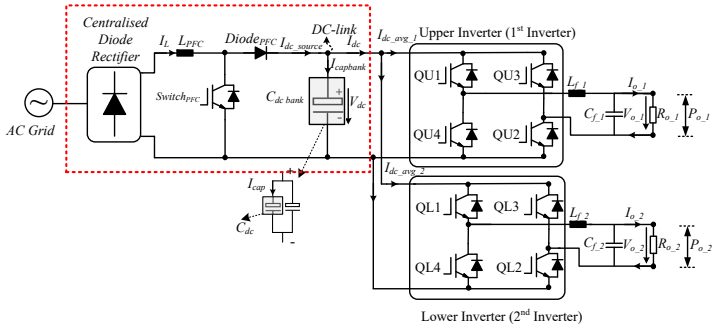
1. Two common DC-link multidrive system structures are proposed: one has an individual DC-bank (shown in Fig. 3.1b), and the other has a common DC-bank (shown in Fig. 3.1c) [**J1**]. In a traditional system, as seen in Fig. 3.1(a), each inverter has its own individual rectifier system and shares the common AC link at PCC [**J1**]. Compared to this kind of system, the proposed systems in Fig. 3.1(b-c) have the following advantages. In the proposed multidrive system, the overall system cost would be less: in the traditional system each inverter has its own rectifier, and the cost for two rectifiers has to be considered, which will increase the overall cost. However, in the proposed systems, due to the implementation of a centralized rectifier, the cost would be less. Secondly, due to the reduced number of power electronic components (rectifiers) in the proposed system, the reliability will be higher.



(a)



(b)



(c)

Fig. 3.1: Schematic of: (**a**) the conventional parallel-connected drive system, (**b**) a multidrive system with individual DC-bank having a centralized rectifier, (**c**) a multidrive system with common DC-bank having one centralized rectifier [**J1, C1**].

Table 3.1: Specifications of the boost PFC [**J1**].

Parameter	Symbol	Value
Power rating (kW)	P_{PFC}	2.5
RMS AC−input voltage (V)	V_S	230
PFC switching frequency (kHz)	f_{PFC}	20
PFC inductor current ripple	I_{PFC_ripple}	30%
PFC inductor current maximum (A)	I_{PFC}	16
PFC inductor minimum (H)	L_{PFC}	3×10^{-3}
Ripple output peak to peak (p−p) voltage (V)	V_{PFC_p-p}	20
Hold-up time (s)	$t_{hold}(= 1/f_o)$	$20{\times}10^{-3}$
PFC capacitor minimum (F)	C_{PFC}	$3.3{\times}10^{-3}$

2. Besides, a new DC-link harmonic mitigation method via phase-shifting of the carrier-waves is introduced in this chapter, which also reduces the DC-link capacitor current [**J1**].

3.2 Proposed System Topology

The multidrive system with individual DC-bank is shown in Fig. 3.2 and Fig. 3.3 shows the multidrive system with a common DC-bank [**C1**] [**J1**]. The two inverters in the proposed system have the same phase and have the same output waveforms. The two topologies also use a boost power-factor-corrector (PFC) followed by a DC-choke and a large El-cap. In the proposed multidrive system with individual DC-banks, individual capacitor-bank to limit the DC-link voltage fluctuation. Whereas, a common capacitor-bank with parallel individual capacitors are used in the proposed multidrive system with a common DC-bank. ($I_{capbank}$) represents the total DC-link capacitor current, and current through a single capacitor by is shown using (I_{cap}) [**J1**].

" The four switches Q_{x1}, Q_{x2}, Q_{x3}, Q_{x4} of the VSI units, shown in both Figs. 3.2 and 3.3, are controlled using the unipolar sinusoidal PWM (SPWM) technique, like explained in Chapter 2. The specifications of the inverter system and output filter (designed according to [33]) are given in Tables 2.1 and 2.2. Both the topologies (in Figs. 3.2 and 3.3) have the same parameters and loading conditions. The rated output voltage of 230 V (RMS value) for each inverter unit is maintained by its own specific Proportional–Resonant (PR) controller, which is designed according to [27, 32]. The control algorithm for the inverter is shown in Fig. 2.4 and for the boost PFC, it is shown in Fig. 3.4 [**J1**]". The boost PFC parameters are shown in Table 3.1 and Table 3.2 has the DC-link capacitor specifications in [34].

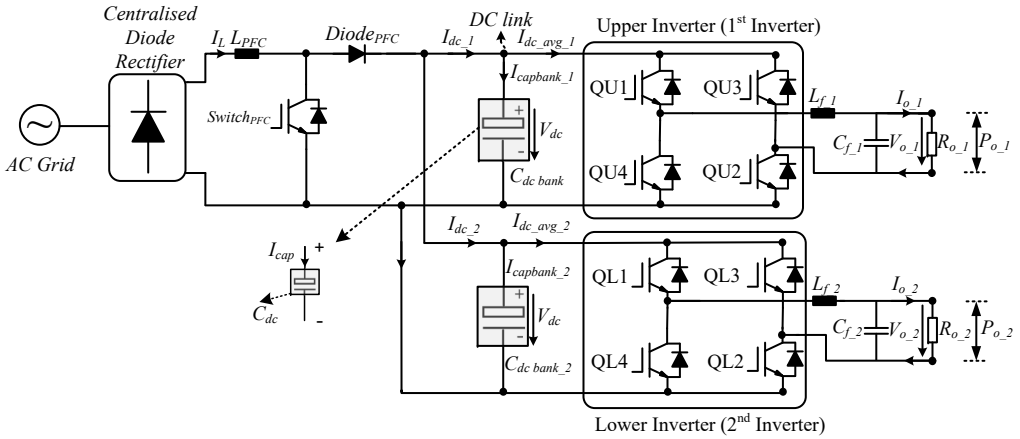


Fig. 3.2: Schematic of the multidrive system with individual DC-banks [**J1**].

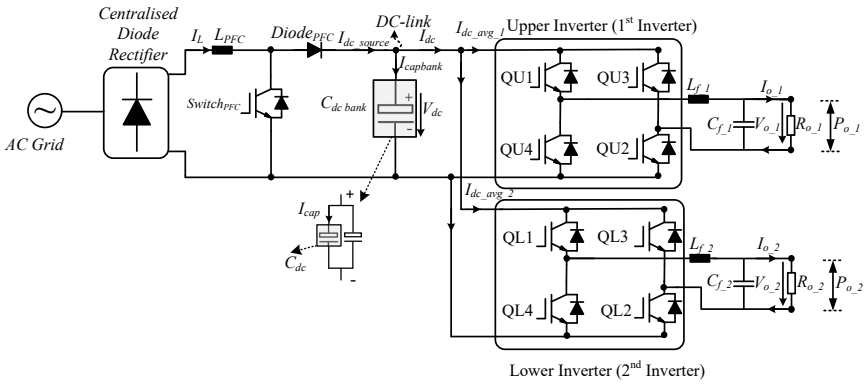


Fig. 3.3: Schematic of the multidrive system with a common DC-bank [**J1**].

Table 3.2: Specifications of the DC-capacitor (KEMET−AlS8(1)(2)392NF500) [**J1**].

Parameter	Symbol	Value
Single capacitance (μF)	C_{dc}	3900
Equivalent series resistance ($m\Omega$)	ESR	61 (100 Hz), 46 (10 kHz)
Thermal resistance (°C/W)	R_{th}	3.8
Rated lifetime (hours)	L_o	9000 (at T_{rated} & I_{rated})
Rated upper category temperature (°C)	T_{rated}	105
Rated ripple current (A)	I_{rated}	12.2 (100 Hz), 19.0 (10 kHz)
Rated voltage (V)	V_{rated}	500
Operating temperature (°C)	T_a	45

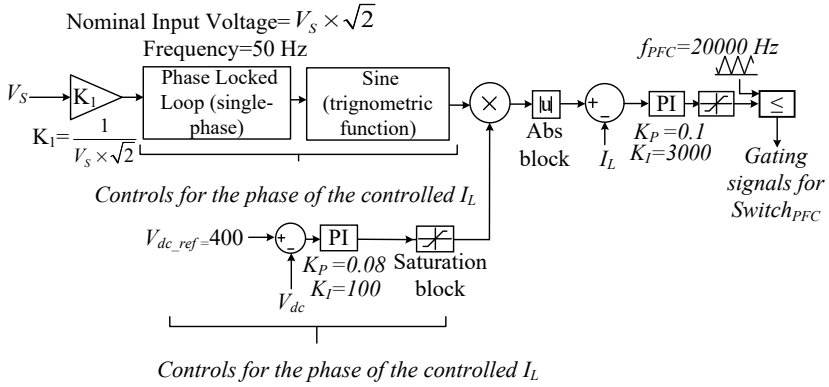


Fig. 3.4: Control algorithm for boost PFC where nominal input voltage of the phase locked loop is given as $V_S \times \sqrt{2}$. (K_P−proportional gain parameter, K_I−integral gain parameter, $K_1 = 1/(V_S \times \sqrt{2})$) [**J1**].

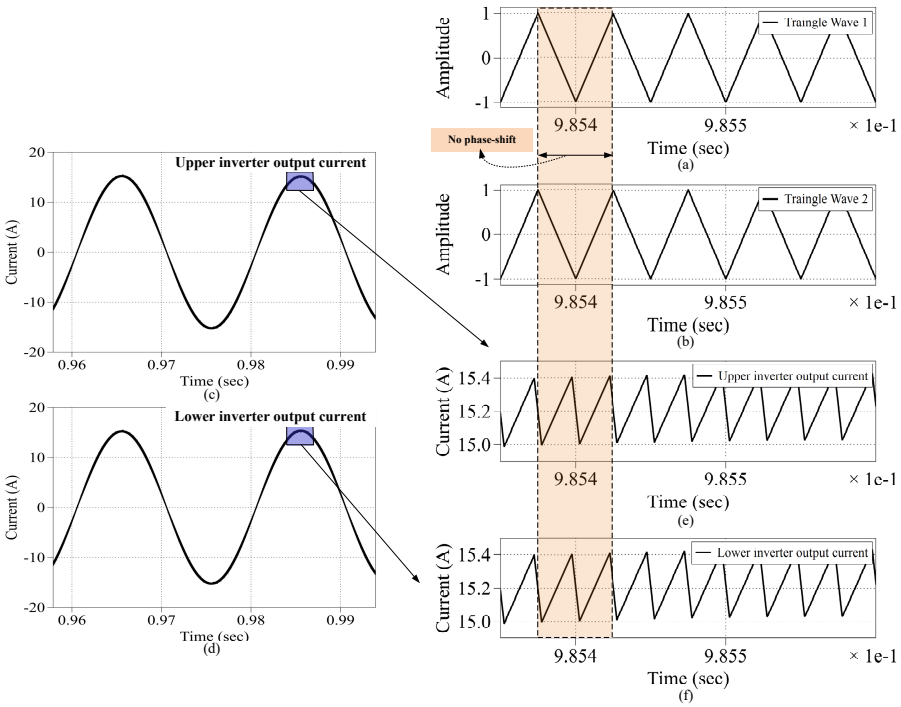


Fig. 3.5: Parallel-connected system waves using the conventional method: (**a**) upper-inverter carrier wave, (**b**) lower-inverter carrier wave, (**c**) upper-inverter output current wave, (**d**) lower-inverter output current wave, (**e**) output current ripples of upper-inverter, and (**f**) output current ripples of the lower-inverter [**J1**].

3.3 Conventional Method without any Phase-Shift

This section explains the conventional method mentioned throughout this chapter. First, the multidrive system seen in Fig. 3.3 is analyzed, assuming that both inverter units draw the same output current, as both of them have the same loading conditions [**J1**]. For the conventional multidrive system used in this case study, output current ripples and carrier-waves (Triangle Wave 1 depicts upper-inverter and Triangle Wave 2 depicts lower-inverter) appear as shown in Fig. 3.5 [**J1**]. These output current ripples from each of the inverter sum up to produce higher DC-link capacitor-current ripples, which might decrease the DC-link capacitor lifetime. Therefore, to improve lifetime of the DC-link capacitors in an in multidrive systems, the DC-link harmonics needs to be reduced [**J1**].

3.4 Proposed Method with an Optimal Carrier Phase-Shift Angle

The proposed method to mitigate DC-link harmonic for both the topologies in this chapter are as follows: Firstly, the multidrive system is simulated for various carrier phase-shift angles of the lower-inverter (θ_{fsw_2}) using the equations (3.1)-(3.9) [**J1**]. Secondly, the total DC- capacitor-current of the harmonic spectrum are evaluated to find the optimum carrier phase-shift angle $\theta_{fsw\_optimal}$ which provides the maximum DC-link harmonics cancellation and thereby the minimum DC-link capacitor current. In this chapter, the upper-inverter carrier signal phase angle, $\theta_{fsw1} = 0°$ and the lower-inverter carrier phase angle θ_{fsw2}=$\theta_{fsw\_optimal}$. The results of applying the proposed method to both the converter topologies in Figs. 3.2 and 3.3 are depicted in Figs. 3.6, 3.7, 3.8 and 3.9 [**J1**].

$$V_{o\_1} = M_A V_{dc} \sin(\omega_{o1} t + \theta_{o1}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o1} t + \theta_{o1}) + m(\omega_{c1} t + \theta_{fsw1})) \tag{3.1}$$

$$I_{o\_1} = I_{o\_peak\_1} \sin(\omega_{o1} t + \theta_{o1}) \tag{3.2}$$

$$I_{dc\_1} = I_{o\_1} \times \underbrace{(\frac{V_{o\_1}}{V_{dc}})}_{SwitchingFunction} \tag{3.3}$$

$$I_{capbank\_1} = I_{dc\_1} - I_{dc\_avg\_1} \tag{3.4}$$

$$V_{o\_2} = M_A V_{dc} \sin(\omega_{o2} t + \theta_{o2}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o2} t + \theta_{o2}) + m(\omega_{c2} t + \theta_{fsw2})) \tag{3.5}$$

$$I_{o\_2} = I_{o\_peak\_2} \sin(\omega_{o2} t + \theta_{o2}) \tag{3.6}$$

$$I_{dc\_2} = I_{o\_2} \times \underbrace{(\frac{V_{o\_2}}{V_{dc}})}_{SwitchingFunction} \tag{3.7}$$

$$I_{capbank\_2} = I_{dc\_2} - I_{dc\_avg\_2} \tag{3.8}$$

$$I_{capbank} = I_{capbank\_1} + I_{capbank\_2}. \tag{3.9}$$

"In the above equations (3.1)-(3.9), $V_{o\_1}, V_{o\_2}, I_{o\_1}, I_{o\_2}$,, present upper and lower-inverter output voltages and output currents. $I_{o\_peak\_1}$, and $I_{o\_peak\_2}$ represents the peak value of the output currents of upper, and lower-inverters. I_{dc_1} and I_{dc_2} are the source DC-current of its upper and lower-inverters $I_{dc\_avg\_1}$ and $I_{dc\_avg\_2}$ are the average value of its upper and lower-inverters. The capacitor-bank currents for upper and lower-inverters are denoted by $I_{capbank\_1}, I_{capbank\_2}$ respectively. The fundamental-frequency and switching-frequency of the upper-inverter are symbolized by, ω_{o1}, ω_{c1}, and that of the lower-inverter is designated by ω_{o2}, ω_{c2}. Finally, the total DC-link capacitor bank is represented by $I_{capbank}$ [**J1**]."

The harmonic spectrum for DC-link capacitor-bank showing the switching-frequency harmonic component $f_{sw\_harmonic} = 40$ kHz, for various phase-shift angles (θ_{fsw_2}) is illustrated in Fig. 3.6 for the multidrive system with a common DC-bank, and in Fig. 3.7 the multidrive system with individual DC-banks. At $\theta_{fsw\_2} = 0°$ (violet colour bar) [**J1**] in Figs. 3.6 and 3.7, there is no phase-shift applied, and this is considered as the conventional case for both the multidrive system topologies. Also, it can be observed that the DC-link capacitor current harmonic is at a minimum when $\theta_{fsw\_2} = 90°$, denoted by the red colour bar in Fig. 3.6, and the green colour in Fig. 3.7. From Figs. 3.6 and 3.7, it could be concluded for that both topologies (shown in Figs. 3.2 and 3.3) when there is a 90° phase-shift angle between carrier-waves in the particular considered case, the main switching-frequency harmonic component ($f_{sw\_harmonic} = 40$ kHz) has minimum value [**J1**]. This is also confirmed from the time-waveforms in Figs. 3.8 and 3.9,] where the maximum of the DC-capacitor current ripple cancellation is at 90° the carrier phase-shift angle shown by the red dotted lines. Finally, the lifetime of the El-caps can be estimated as previously explained in section 2.4 of Chapter 2.

3.5 Experimental Validation of the Proposed DC-link Harmonic Mitigation Strategy

3.5.1 Experimental Validation with Scaled-Downed Parameters

An experimental platform is built to validate the proposed DC-link harmonic mitigation strategy for the topologies, shown in Figs. 3.2 and 3.3. The operating conditions and the parameters are detailed in Table 3.3. As shown in the experimental setup in Fig. 3.10, resistors are used as loads, like in the simulation analysis. The operating conditions (provided in Table 3.4) for both the inverters are kept the same throughout the experiments [**J1**].

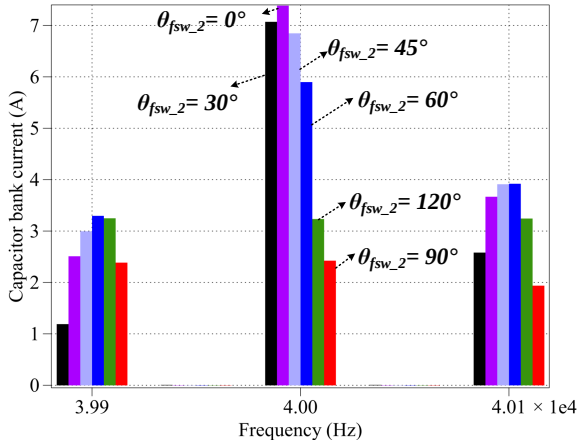


Fig. 3.6: The $f_{sw\_harmonic} = 40$ kHz harmonic spectrum of capacitor bank current for various θ_{fsw_2} for the multidrive system with common DC-bank both at rated operating conditions [**J1**].

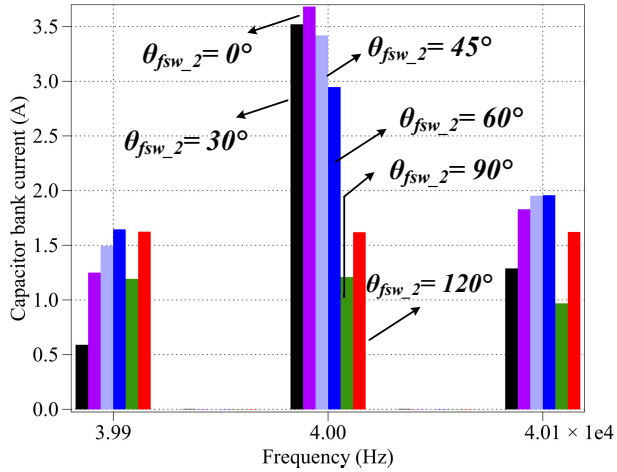


Fig. 3.7: The $f_{sw\_harmonic} = 40$ kHz harmonic spectrum of capacitor bank current for various θ_{fsw_2} for the multidrive system with individual DC-banks both at rated operating conditions [**J1**].

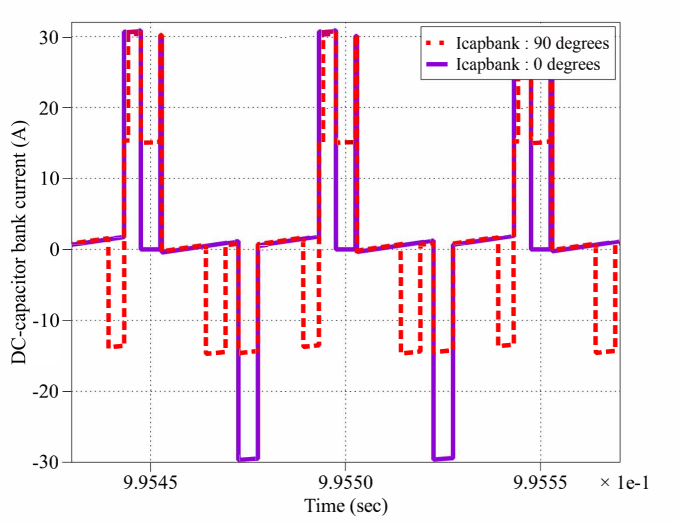


Fig. 3.8: DC-capacitor bank current ripple reduction at $\theta_{fsw\_2} = 0°$ (violet line), and $\theta_{fsw\_2} = 90°$ (red dotted lines) for the multidrive system with a common DC-bank [**J1**].

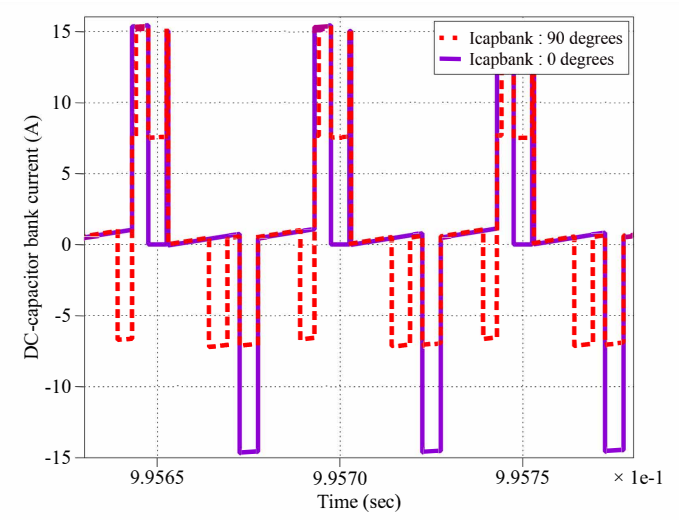


Fig. 3.9: DC-capacitor bank current ripple reduction at $\theta_{fsw\_2} = 0°$ (violet line), and $\theta_{fsw\_2} = 90°$ (red dotted lines) for the multidrive system with individual DC-banks [**J1**].

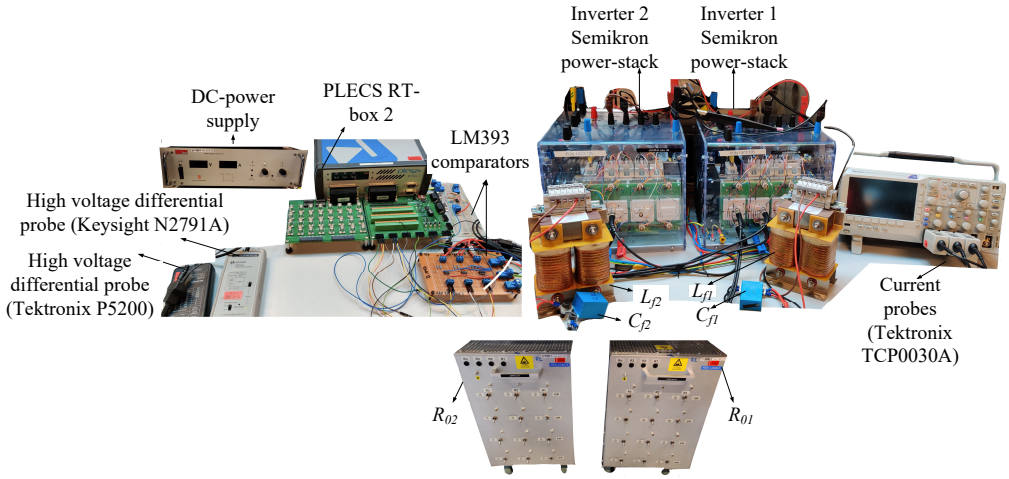


Fig. 3.10: Experimental setup of the multidrive system [**J1**].

Table 3.3: Experimental system specifications [**J1**].

Module	Part Number/Parameter	Symbol
SEMITEACH IGBT module stack	SEMIKRON 08753450	-
AC-filter inductors	4mH, 20A rated current	L_{f1},L_{f2}
AC-filter capacitors	1μF, 1600V, 19.1A @ 40°C	C_{f1},C_{f2}
Voltage comparators	LM393	-
PLECS controller box	RT-box 2	-
Resistor Banks	10 Ω–80 Ω	R_{01},R_{02}

Table 3.4: Operating conditions (scaled-down) for the experimental analysis [**J1**].

Parameter	Symbol	Value
Rated power of each inverter (W)	P_o	80
Load (Ω)	R_L	20
Rated RMS load voltage (V)	$V_{sine-ref}$	40
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	50
Switching frequency (kHz)	f_{sw}	5
Modulation amplitude index	M_A	0.8

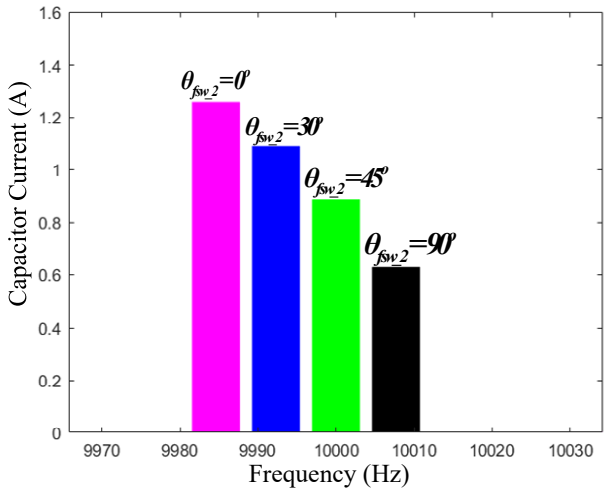


Fig. 3.11: Experimental data plotted in MATLAB showing the $f_{sw\_harmonic} = 10$ kHz harmonic spectrum of DC-link current for various θ_{fsw_2} for the multidrive system with **a common DC-bank**-scaled down operating conditions, as given in Table 3.4 [**J1**].

The proposed harmonic mitigation strategy is applied to both the multidrive systems and the obtained results are illustrated in Figs. 3.11 and 3.12 respectively. It can be understood from the results that the switching-frequency harmonics (at 10 kHz) is minimum when $\theta_{fsw\_2} = 90°$, for the proposed two multidrive systems. Hence, these results agree with the proposed DC-link harmonic mitigation method explained in Section 3.4 [**J1**]. For completeness, the Figs. 3.13 and 3.14 depicting the output waveforms as $\theta_{fsw\_2} = 0°, 90°$, captured in the oscilloscopes are provided.

3.5.2 DC-Harmonic Analysis Using Optimal Carrier Phase-Shift Angle - Simulation

The optimal carrier phase-shift angles are applied to both the topologies (in Figs. 3.2 and 3.3), and simulated. Both the topologies have the same rated output power of 2.5 kW and same operating conditions. The results are illustrated in Fig. 3.15 and Fig. 3.16 respectively [**J1**]. It can be seen that the switching harmonic components in the DC-capacitor current is reduced when the proposed method is applied. Consequently, the electro-thermal stress for each capacitor reduces, which helps to increase its life expectancy. The power-loss and lifetime, calculated using (2.1)–(2.3), is shown in Table 3.5 to prove that the proposed method helps to reduce power-loss of DC-capacitor and thereby improve its lifetime [**J1**].

However, from a practical application it is necessary to take into consideration that,

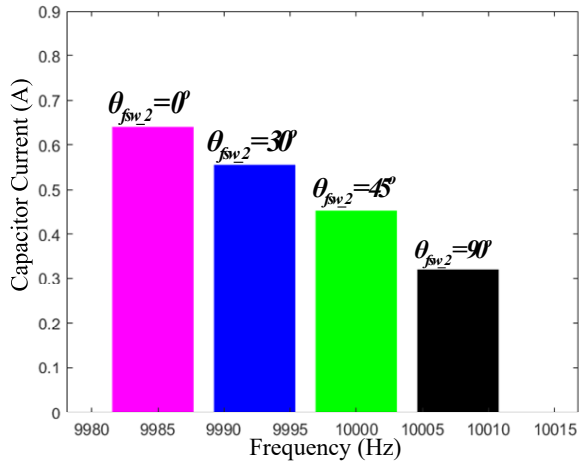


Fig. 3.12: Experimental data plotted in MATLAB showing the $f_{sw\_harmonic} = 10$ kHz harmonic spectrum of DC-link current for various θ_{fsw_2} for the multidrive system with **individual DC-banks**-both under scaled down operating conditions, as given in Table 3.4 [**J1**].

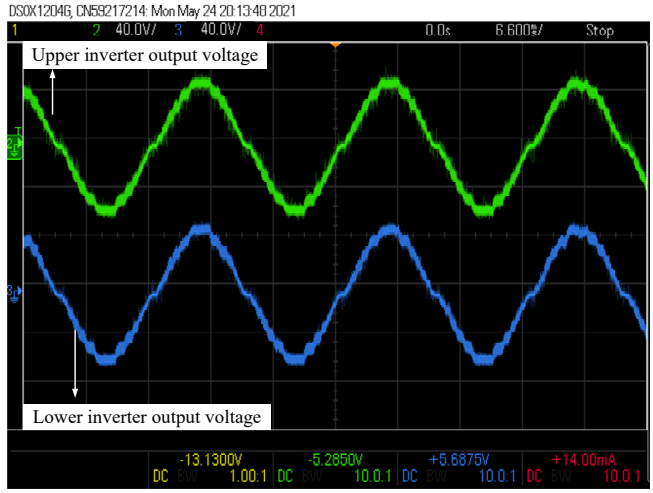


Fig. 3.13: Measured output voltage waveform (with voltage on y-axis and time on x-axis) of the multidrive system with a common DC-bank output -two inverter units interleaved at $\theta_{fsw\_2} = 0°$, and $\theta_{fsw\_2} = 90°$, using the parameters given in Table 3.4 [**J1**].

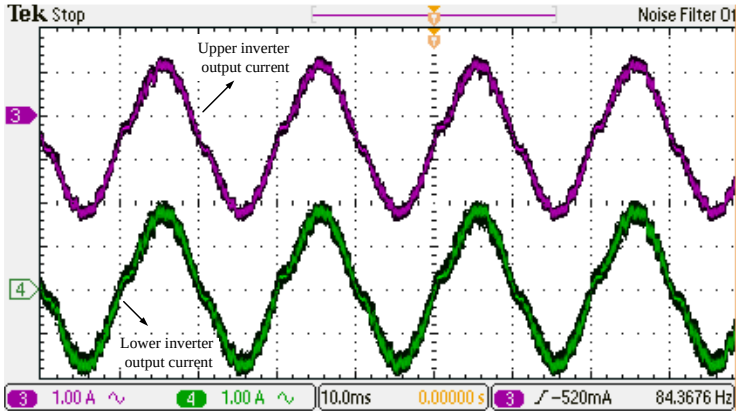


Fig. 3.14: Measured output current waveforms (with current on y-axis and time on x-axis) of the multidrive system with a common DC-bank output currents-two inverter units interleaved at $\theta_{fsw\_2} = 0°$, and $\theta_{fsw\_2} = 90°$, using parameters in Table 3.4 [**J1**].

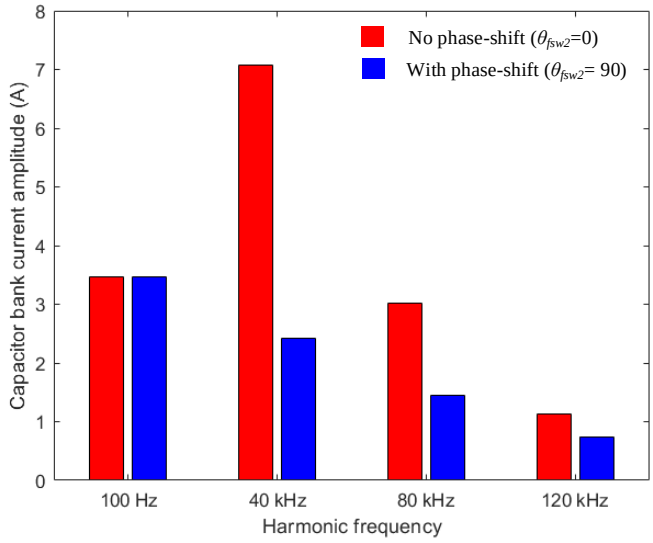


Fig. 3.15: Effect of the optimal shift in the DC-capacitor bank current harmonics for the multidrive system with **a common DC-bank** - operating conditions given in Table 2.1 [**J1**].

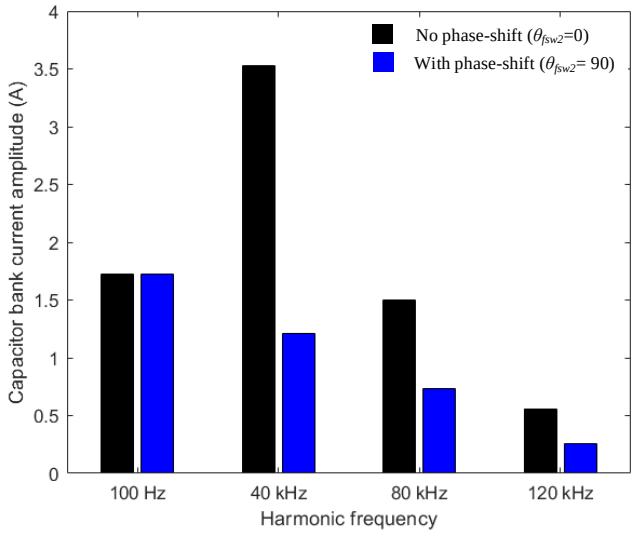


Fig. 3.16: The effect of the optimal shift in the DC-capacitor bank current harmonics for the multidrive system with **individual DC-banks** - operating conditions, are given in Table 2.1[**J1**].

two parallel inverters do not necessarily always operate at a rated loading conditions. Accordingly, for the multidrive topologies depicted in Figs. 3.2 and 3.3, the upper-inverter is operated at a rated output power of 2500 W, while the output load of the lower-inverter is varied between 0 W and 2500 W (rated power) [**J1**]. The switching frequency harmonics are observed in each case, when $\theta_{fsw\_2} = 0°$ (without applying any phase-shift) and $\theta_{fsw\_2} = 90°$ (proposed method) and the results are demonstrated in Fig. 3.17 and 3.18. It is seen that, as the output power increases, the switching-frequency harmonic component amplitude reduces as observed from Fig. 3.17 and Fig. 3.18 [**J1**]. When both two inverters has the same output power, the DC-link capacitor-current ripples will be equal and opposite (due to $\theta_{fsw\_2} = 90°$), resulting in maximum DC-link capacitor current harmonic cancellation [**J1**].

3.6 Summary

In this chapter, a carrier-based DC-link harmonic mitigation strategy is presented for the proposed multidrive systems having a centralized rectifier. Experimental and simulation results show that the maximum switching-frequency harmonic ripple cancellation occurs when the carrier-waves of the two inverters are phase-shifted by a 90° angle,

Table 3.5: Power-loss, and life-expectancy of the DC-link capacitor bank calculated using the experimental results [**J1**].

Multidrive Topology With	$P_{loss}(Watts)$ $\theta_{fsw\_2} = 0°$	$L_x(hours)$ $\theta_{fsw\_2} = 0°$ $\times 10^5$	$P_{loss}(Watts)$ $\theta_{fsw\_2} = 90°$	$L_x(hours)$ $\theta_{fsw\_2} = 90°$ $\times 10^5$
Common DC-bank	1.27	1.35	0.41	1.70
Individual DC-bank	0.33	1.73	0.12	1.85

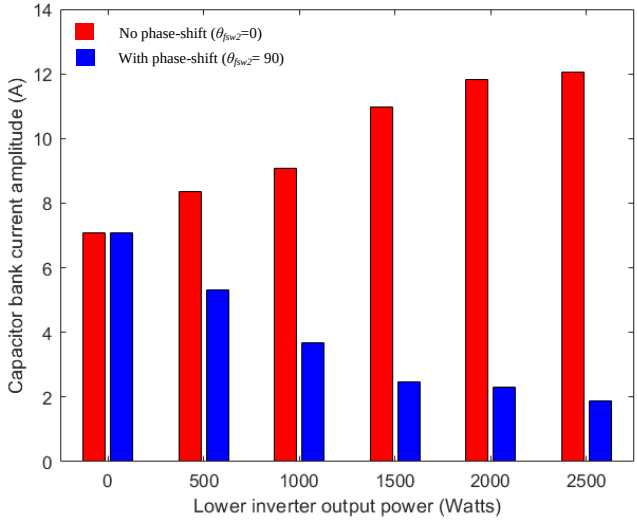


Fig. 3.17: Effect of optimal shift in the DC-capacitor bank current (**RMS**) for varying lower inverter loading in a multidrive system with **a common DC-bank** for $f_{sw\_harmonic}$ = 40 kHz [**J1**] (upper-inverter is operated at 2.5 kW)

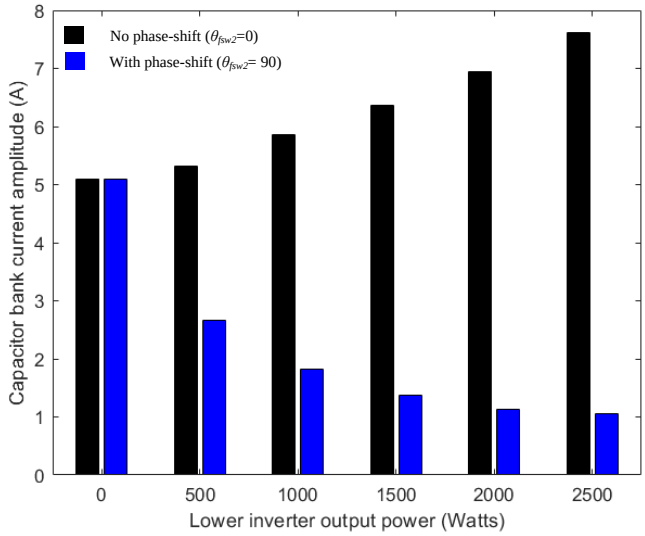


Fig. 3.18: Effect of optimal shift in the DC-capacitor bank current for varying lower inverter loading in a multidrive system with **individual DC-banks for $f_{sw\_harmonic}$ = 40 kHz** (upper-inverter is operated at 2.5 kW) [**J1**].

which reduces the overall RMS value of the DC-link capacitor-current by almost 50% in the case the two inverters have the same load [**J1**]. However. a cancellation effect is also seen in the cases when the loads are not the same.

Publications in Peer-Reviewed Journal

[**J1**] **S. Baburajan**, H. Wang, D. Kumar, Q. Wang, and F. Blaabjerg, "DC-link Current Harmonic Mitigation via Phase-shifting of Carrier-waves in Paralleled Inverter Systems," *Energies*, vol. 14, no. 14, pp. 1–16, 2021.

Chapter 4

Design of DC-Link Capacitor in a Multiple-Drive System

4.1 Background

In the previous chapter, we have seen that the topology with common DC-bus results in higher DC-link capacitor current compared to having individual DC-bus for each inverter. So, in this chapter, we are trying to improve the DC-link harmonic mitigation in that topology and reduced DC-link capacitor current. Then, a design approach for the DC-link capacitor design method is discussed.

4.2 Overview of the Multidrive System

The multidrive system used in this chapter is shown in Fig. 4.1. The specifications of these proposed parallel-inverters are given in Table 4.1 [**J2**]. $C_{DC-bank}$ represents the DC-capacitor bank and C_{dc} represents individual capacitors. The total DC-link capacitor ripple current is depicted by, $I_{capbank}$ and the ripple current flowing through an individual capacitor is denoted by I_{cap} [**J2**]. In this study, as mentioned in the Introduction chapter, El-caps are used as DC-link capacitors. $I_{DC-source}$ denotes the DC-source current and I_{dc} denotes the total DC-current [**J2**]. Unipolar SPWM technique is used to control the four switches of the VSI units of the proposed multidrive system. The specifications of the output filter of each inverter are given in Table 4.2. Each inverter unit's output voltage is maintained at a rated value of 230 V (RMS) using a PR controller (designed according to [27, 32]). The Fig. 4.2 gives the control algorithm of the

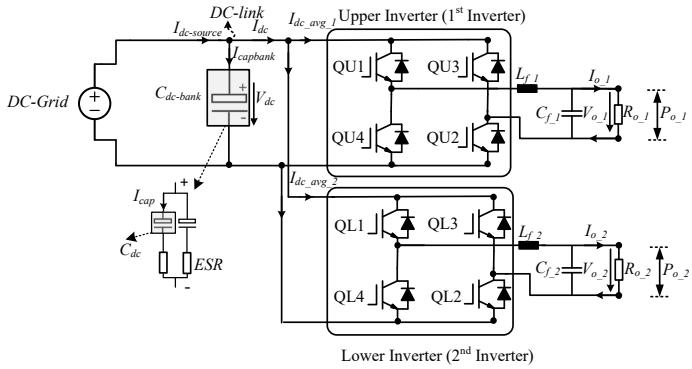


Fig. 4.1: Schematic of the proposed multidrive system [**J2**].

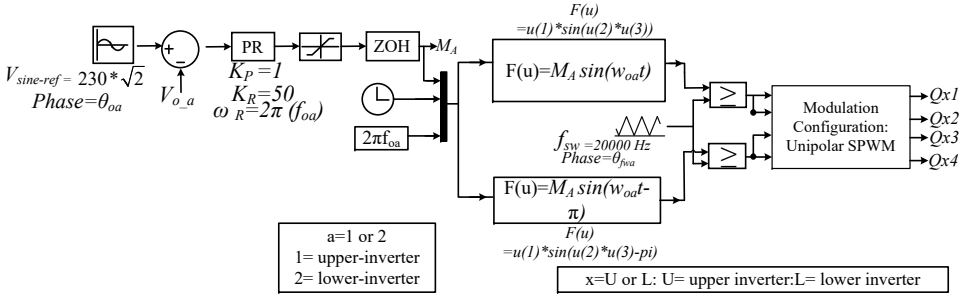


Fig. 4.2: Control algorithm for inverter unit (K_P−proportional parameter, K_I−integral parameter, K_R−resonant coefficient, ω_R- angular resonant frequency, ω_{oa}=2πf$_{oa}$) [**J2**].

inverter. Table 4.3 shows the design criteria of the DC-capacitor and Table 3.2 shows the chosen capacitor's data [34] [**J2**].

4.3 Proposed Method to Reduce the DC-link Capacitor-Current in a Multidrive System

The proposed method to reduce the DC-link Capacitor-Current is summarized in the flowchart given in Fig. 4.3 and further explained in the subsections below.

Table 4.1: Specifications of the multidrive system shown in Fig. 4.1 [**J2**].

Parameter	Symbol	Value
Rated power (kW)	P_{o_1}, P_{o_2}	2.5
Load (Ω)	R_{o_1}, R_{o_2}	20
Rated RMS load voltage (V)	$V_{sine-ref}$	230
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	400
Switching frequency (kHz)	f_{sw}	20
Modulation amplitude index	M_A	0.8

Table 4.2: Specifications of the inverter output filter [**J2**].

Parameter	Symbol	Value
Inductor-filter ripple current limit	I_{f_ripple}	20%
Inductor (mH)	L_{f_1}, L_{f_2}	2
Filter cutoff frequency (kHz)	f_{cutoff} (f_{cutoff}<f_{sw}/10)	2
Filter capacitor (μF)	C_{f_1}, C_{f_2}	6

Table 4.3: Design criteria for DC-link capacitor [**J2**].

Parameter	Symbol	Value
Ripple DC-link voltage peak to peak (p−p) value (V)	V_{p-p}	20
Hold-up time (ms)	$t_{hold}(= 1/f_o)$	20
Minimum required capacitor value (mF)	C_{min}	3.3

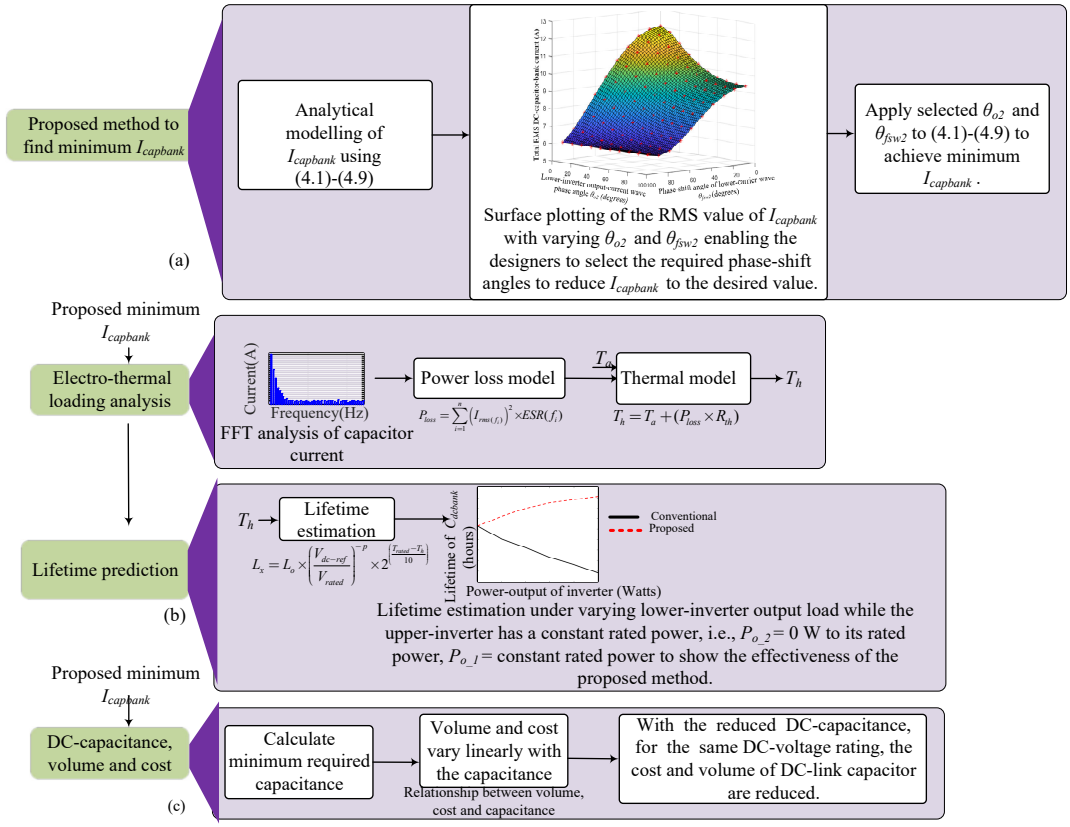


Fig. 4.3: (a) Flowchart of the proposed method to obtain minimum DC-link capacitor current in a multidrive system, (b) lifetime prediction method using the proposed minimum $I_{capbank}$, and (c) DC-capacitance, cost and volume estimation procedure using the proposed minimum $I_{capbank}$ [**J2**].

4.3.1 Analytical Modelling of DC-link Capacitor-Current

The DC-capacitor-current harmonic contribution in the multidrive system, shown in Fig. 4.1 is analyzed using (4.1)-(4.9). The upper-inverter capacitor-bank current is found using (4.1)-(4.4), while equations (4.5)-(4.8) are used to find the lower-inverter unit's DC-link capacitor current, expressed by $I_{capbank\_2}$ [**J2**].

$$V_{o\_1} = M_A V_{dc} \sin(\omega_{o1} t + \boldsymbol{\theta_{o1}}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \left(\frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o1} t + \boldsymbol{\theta_{o1}}) + m(\omega_{c1} t + \boldsymbol{\theta_{fsw1}})) \right) \quad (4.1)$$

$$I_{o\_1} = I_{o\_peak\_1} \times \sin(\omega_{o1} t + \boldsymbol{\theta_{o1}}) \quad (4.2)$$

$$I_{dc\_1} = I_{o\_1} \times \underbrace{(\frac{V_{o\_1}}{V_{dc}})}_{SwitchingFunction} \quad (4.3)$$

$$I_{capbank\_1} = I_{dc\_1} - I_{dc\_avg\_1} \quad (4.4)$$

$$V_{o\_2} = M_A V_{dc} \sin(\omega_{o2} t + \boldsymbol{\theta_{o2}}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \left(\frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o2} t + \boldsymbol{\theta_{o2}}) + m(\omega_{c2} t + \boldsymbol{\theta_{fsw2}})) \right) \quad (4.5)$$

$$I_{o\_2} = I_{o\_peak\_2} \times \sin(\omega_{o2} t + \boldsymbol{\theta_{o2}}) \quad (4.6)$$

$$I_{dc\_2} = I_{o\_2} \times \underbrace{(\frac{V_{o\_2}}{V_{dc}})}_{SwitchingFunction} \quad (4.7)$$

$$I_{capbank\_2} = I_{dc\_2} - I_{dc\_avg\_2} \quad (4.8)$$

In the above equations, θ_{o1} is the upper-inverter fundamental-output current the phase-angle, and θ_{fsw1} represents the upper-inverter carrier-wave phase-angle. [**J2**]. θ_{o2} depicts the lower-inverter fundamental-output current phase angle and θ_{fsw2} represents the lower-inverter carrier-wave phase angle. "$V_{o\_1}, V_{o\_2}, I_{o\_1}, I_{o\_2}$,, denote the

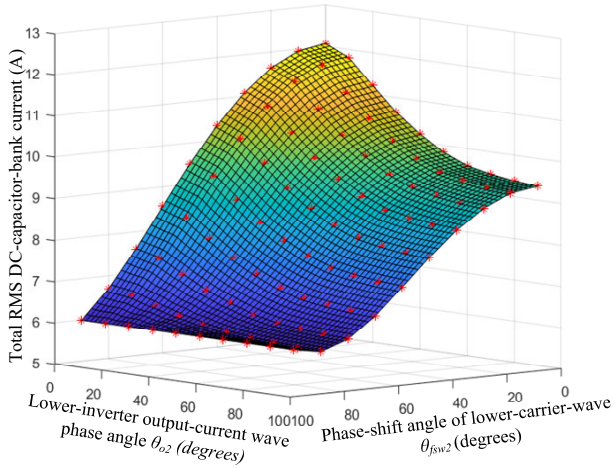


Fig. 4.4: Surface plotting of the total DC-link capacitor-current with varying θ_{o2}, and θ_{fsw2} for the multidrive system shown in Fig. 4.1 and specified in Table 4.1 [**J2**].

upper-inverter and lower-inverter output voltages, and output currents. The peak values of the output currents of upper and lower inverters are represented by $I_{o\_peak\_1}$ and $I_{o\_peak\_2}$. $I_{dc\_1}, I_{dc\_2}, I_{dc\_avg\_1}, I_{dc\_avg\_2}$ represent the individual DC-current drawn by the upper and lower inverters, and their average value " [**J1, J2**]. The fundamental angular-frequency, and angular-switching-frequency of the upper-inverter are symbolized by ω_{o1}, and ω_{c1}, whereas, for the lower-inverter are represented by ω_{o2}, ω_{c2} [**J2**].

The total DC-link capacitor-current is analyzed using

$$I_{capbank} = I_{capbank\_1} + I_{capbank\_2} \tag{4.9}$$

From (4.9), it could be understood that there is a possibility to cancel the switching-frequency harmonic components of the total DC-link capacitor-current as well as the double-fundamental harmonic components, if the two inverters' output currents and carrier waves are phase-shifted by the optimal angle [**J2**].

4.3.2 Surface Plotting to Find the Minimum Capacitor Current

Using the (4.1)-(4.9), the surface plot of the $I_{capbank}$ is plotted by varying θ_{o2} and θ_{fsw2}. This plot helps to select the required phase-shift angles to reduce $I_{capbank}$ to the desired value [**J2**]. As an example, for the system shown in Fig. 4.1, a surface plot is obtained using its analytical equations derived by (4.1)-(4.9) and it is shown in Fig. 4.4. In this

chapter, the desired value of the DC-capacitor bank current is the minimum value of the DC-capacitor bank current. Now, using this minimum DC-capacitor bank current, the DC-capacitor is designed as explained below.

4.4 Design of DC-Link Capacitor in a Multidrive System Based on the Proposed Minimum DC-link capacitor-current

4.4.1 Design Criteria: Lifetime of DC-link capacitor

Using the minimum $I_{capbank}$, the expected lifetime of the DC-link capacitor can be analyzed using the (2.1)-(2.2) as previously explained in Section 2.4 of Chapter 2 [**J2**].

4.4.2 Design Criteria: DC-link Capacitance, Volume and Cost

The DC-link capacitor $C_{DC-bank}$ can be designed using (4.10)-(4.12). Equation (4.10) is used to ensure that the designed DC-link capacitor meets the required hold-up time (t_{hold}). Hold-up time is defined as the time period for which the output voltage will be maintained within a specific range and the power converter can normally function, after the failure of the AC power supply [**J2**]. The hold-up time depends upon the value of DC-link capacitor value. Typically, for a 50 Hz fundamental frequency systems, the hold-up time is minimum 20 ms (= 1/50) and for a 60 Hz fundamental frequency systems, the hold-up time minimum is 16 ms (= 1/60) [**J2**].

On the other hand, equation (4.11) is used to make sure that the designed DC-link capacitor keeps the voltage ripple within the required limits. Now, "to meet the hold-up time (t_{hold}) and voltage ripple requirements, the capacitor is selected to have the largest value of (4.10) and (4.11) given below "[**J2**].

$$C_{DC-bank1} \geq \frac{2 \times P_{o-total} \times t_{hold}}{V_{dc-ref}^2 - V_{dc-ref-min}^2} \tag{4.10}$$

$$C_{DC-bank2} \geq \frac{P_{o-total}}{2\pi f_o \times V_{p-p} \times V_{dc-ref}} \tag{4.11}$$

$$C_{DC-bank} = max(C_{DC-bank1}, C_{DC-bank2}) \tag{4.12}$$

where $P_{o-total} = P_{o\_1} + P_{o\_2}$, is the total output power of the multidrive system [**J2**]. To make sure that, the output power remains stable in the case of a disruption in the power supply for an t_{hold} amount of time, a minimum amount of DC-link voltage $V_{dc-ref-min} \cong 90\% \times V_{dc-ref}$ is considered[**J2**].

Table 4.4: Scaled-down operating conditions for experimental analysis [**J2**].

Parameter	Symbol	Value
Rated power (W)	P_{o_1}, P_{o_2}	50
Upper-inverter load (Ω)	R_{o_1}	20
Lower-inverter load (Ω)	R_{o_2},	20, 35, 52
Rated RMS load voltage (V)	$V_{sine-ref}$	32
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	50
Switching frequency (kHz)	f_{sw}	5
Modulation amplitude index	M_A	0.8

4.5 Experimental Validation of the proposed method

A down scaled experimental platform with resistor banks as the loads (referring to Fig. 4.1) is built, as also shown in Fig. 3.10. The operating conditions (scaled-down) are listed in Table 3.3, and the main system specifications are listed in Table 4.4 [**J2**].

4.5.1 Verification of the Proposed DC-link Capacitor Current Reduction Method

4.5.1.1 Case 1: Multidrive System with Same Output Power and Same Load Frequency [J2]

To verify the proposed DC-link capacitor current reduction method, the multidrive system shown in Fig. 4.1 is analyzed using (4.1)-(4.9), and first the Fig. 4.4 is plotted. Then the optimum phase angles producing minimum value of RMS DC-link capacitor current is selected. For this case study, $\theta_{o2} = \theta_{fsw2} = 90°$ [**J2**]. Next, these interleaving angles are applied in (4.1)-(4.9), and the obtained $I_{capbank}$ harmonic spectrum is plotted in Fig. 4.5(a-e). The frequency spectrum proves that by using the proposed method, the DC-link harmonics can be cancelled [**J2**]. To further observe the effect of the proposed method, the time-domain waves also are plotted in Fig. 4.6. It is observed that the $I_{capbank}$ ripple is reduced by almost 50% (red colour) by implementing the proposed technique, compared to the conventional case (black colour) when no interleaving is applied [**J2**]. Thereby, it is validated the proposed method helps to achieve the minimum value of $I_{capbank}$.

To further prove the effectiveness of the proposed method, the Fig. 4.7(a-b) is plotted. It shows that the proposed method can reduce the RMS value of $I_{capbank}$ by more than 50% compared to that of the conventional method, even when both drives are operating at the highest power [**J2**]. Moreover, the plots in Fig. 4.8 highlights that, for example, when both drives are operated at the same loading condition, the

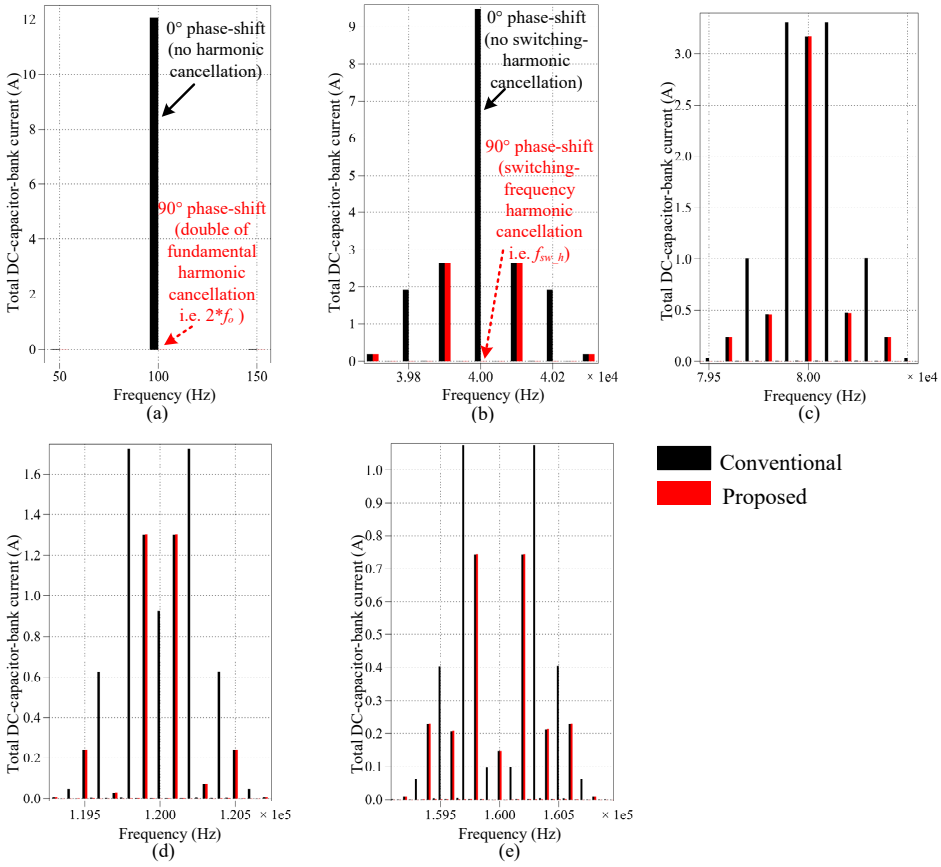


Fig. 4.5: Harmonic characteristics of the total DC-link capacitor-current for the multidrive system, (illustrated in Fig. 4.1) presenting the following harmonic components: (a) $2 \times f_o$, i.e. 100 Hz (as the f_o for the considered multidrive system is $50Hz$), (b) first switching-frequency harmonic component $f_{sw\_h} = 40$ kHz (c) second $f_{sw\_h} = 80$ kHz, (d) third $f_{sw\_h} = 120$ kHz, (e) fourth $f_{sw\_h} = 160$ kHz. (Since a unipolar SPWM is implemented with $f_{sw\_h} = 20$ kHz, f_{sw_h} will appear at multiples of two times the switching frequency) [**J2**].

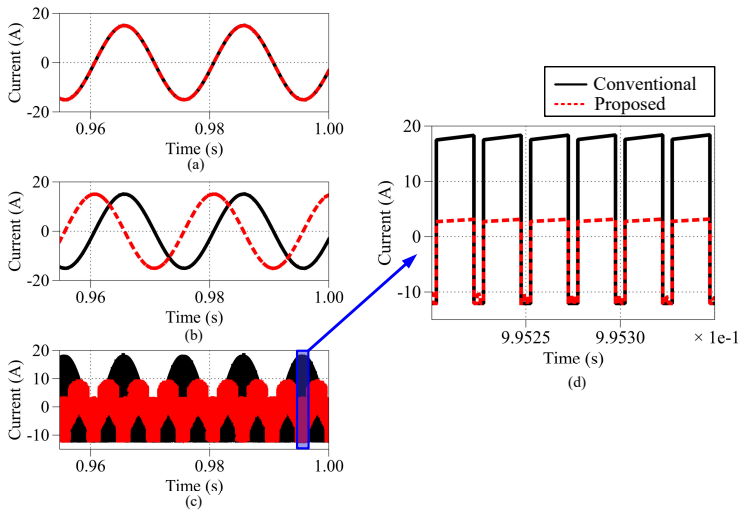


Fig. 4.6: Time-domain waveforms (red lines indicating the proposed method with optimal phase-shift, and black lines indicating system without any phase-shift) of: (a) upper-inverter output current wave, (b) lower-inverter output current wave, (c) total DC-link capacitor current waveform, (d) zoomed in version showing $I_{capbank}$ ripples [**J2**].

power-loss is reduced to more than 80% when the proposed method is applied [**J2**]. The DC-link capacitor lifetime, on the other hand, as can be observed from Fig. 4.8 improves by using that the proposed method. Thus, it could be concluded that the proposed method helps to reduce DC-link capacitor current harmonic content, thereby improving its lifetime [**J2**].

For experimentally validating the proposed method, the phase-shift angle of the lower inverter unit are varied, and the DC-link capacitor harmonic spectrum components ($2 \times f_o = 100$ Hz and $f_{sw\_h} = 10$ kHz) are observed [**J2**]. It is seen that the $2 \times f_o = 100$ Hz and $f_{sw\_h} = 10$ kHz is completely cancelled and the total DC-link capacitor current is reduced by more than 50% when the proposed method is applied to the multidrive system. This means that required DC-link capacitance is reduced [**J2**]. Additionally, the output waveforms of the multidrive system at $\theta_{o2} = \theta_{fsw2} = 0°$, and $\theta_{o2} = \theta_{fsw2} = 90°$, are shown in Fig. 4.10.

An additional experiment is conducted using Table 3.3 and Table 4.4 to further verify the proposed method is effective even for multidrive systems having parallel-inverters with different loading conditions, and with different output frequencies [**J2**].

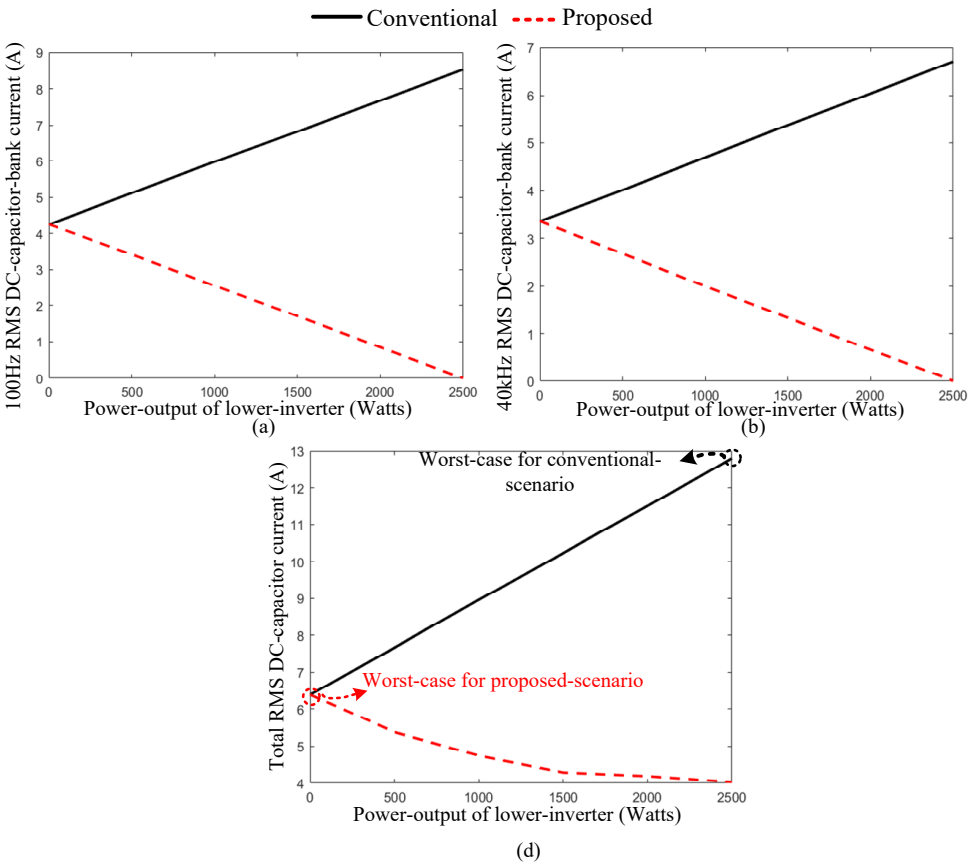


Fig. 4.7: Plots of the harmonic components of $I_{capbank}$, and the total DC-link capacitor-bank current, when P_{o_2} is varied between 0 W to 2500 W (rated power), while P_{o1} has a constant rated power of 2500 W, and $\theta_{o2} = \theta_{fsw2} = 0°$ (conventional method shown in black colour line), and $\theta_{o2} = \theta_{fsw2} = 90°$ (proposed method in red colour line) showing: (a) $2 \times f_o = 100$ Hz, (b) $f_{sw\_h} = 40$ kHz, (c) $I_{capbank}$ [**J2**].

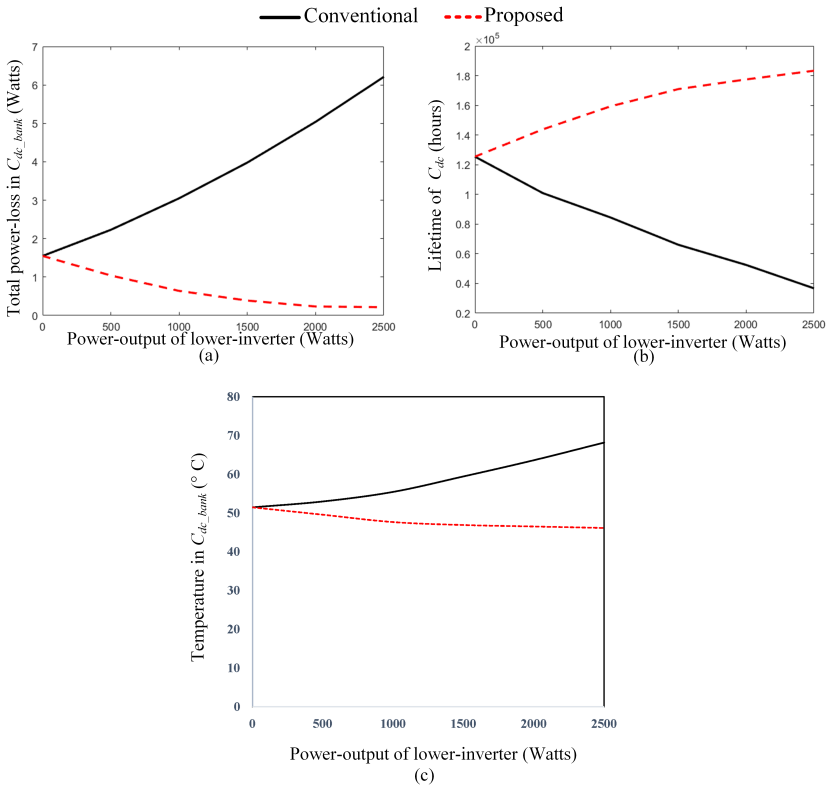


Fig. 4.8: Plots showing the impact of the proposed method (red color) compared to the conventional method (black color) in the (a) total power-loss in DC-link capacitor, (b) lifetime of DC-link capacitor (calculated as per [35]) and (c) DC-link capacitor temperature-with varying lower-inverter having output power (0 W - 2500 W), and $P_{o\_1} = 2500$ W [**J2**].

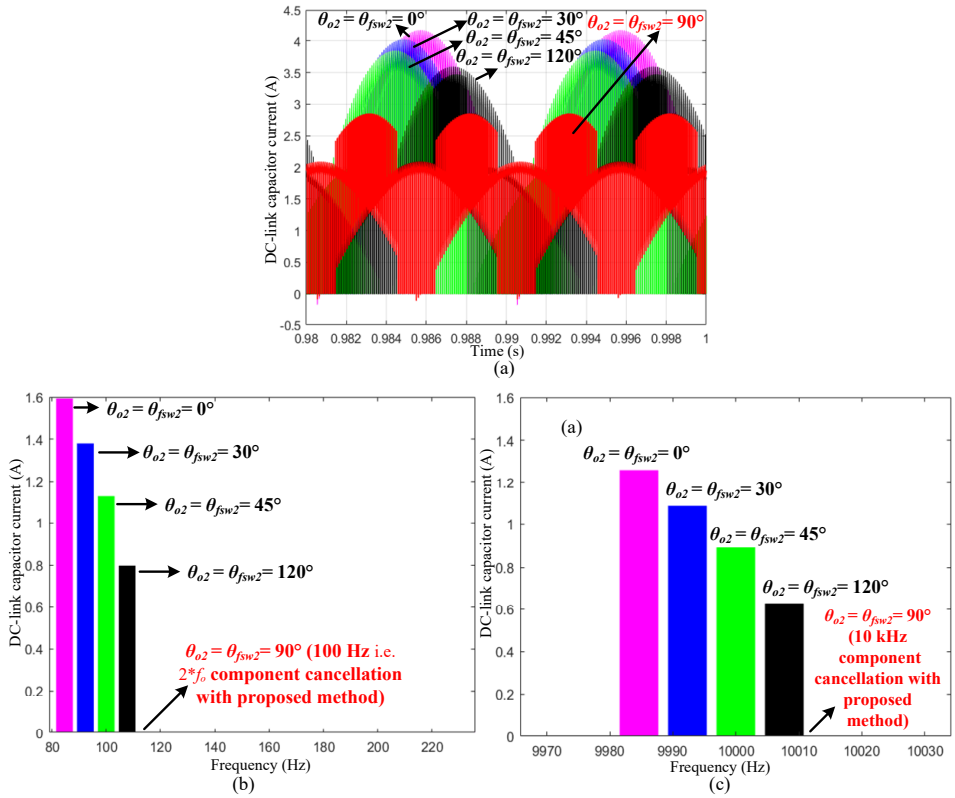


Fig. 4.9: Experimental data (using the scaled-down operating conditions, given in Table 4.4) of **Case 1** plotted in MATLAB showing: (a) the time-domain waveforms when various phase-shift angles are applied, and the corresponding harmonic spectrum components, (b) $2 \times f_o = 100$ Hz, and $\theta_{fsw2} = 10$ kHz: demonstrating the effectiveness of the proposed method in the cancellation of the main harmonic components of $I_{capbank}$ [**J2**]. The upper-inverter output power is $P_{o\_1} = 50$ W, $R_{o\_1} = 20\ \Omega$, and the lower-inverter has output power $P_{o\_2} = 50$ W, $R_{o\_2} = 20\ \Omega$. Both inverters have the same fundamental frequency of 50 Hz. [**J2**]

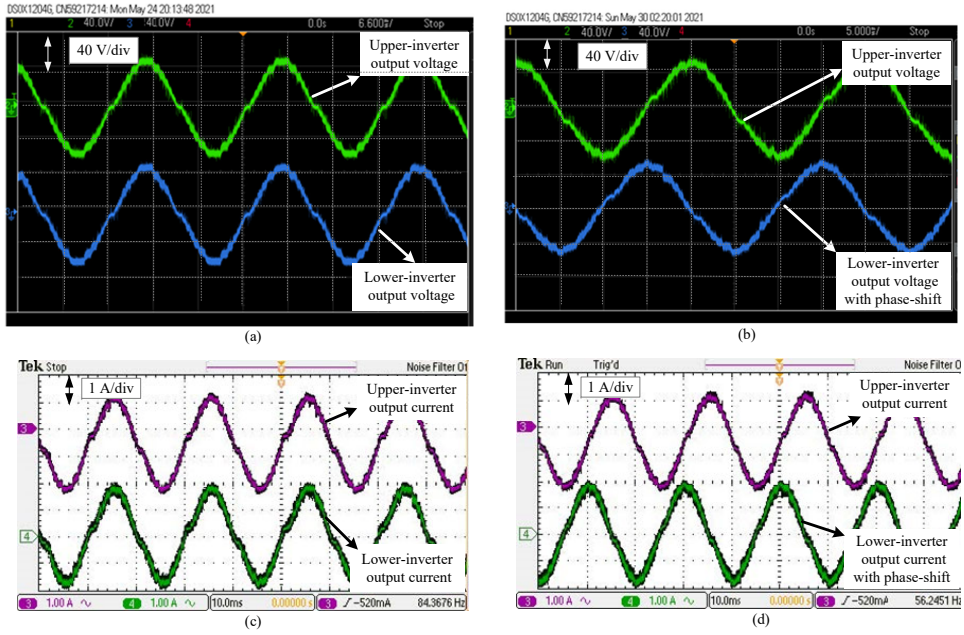


Fig. 4.10: Measured waveforms of the multidrive system (using the parameters in Table. 4.4) for **Case 1** showing: (a) output voltages with no interleaving, (b) output voltages with $\theta_{o2} = \theta_{fsw2} = 90°$, (c) output currents with no interleaving, and (d) output currents with $\theta_{fsw2} = 90°$ [**J2**]. The upper-inverter output power is $P_{o\_1} = 50$ W, $R_{o\_1} = 20\ \Omega$, and the lower-inverter has output power $P_{o\_2} = 50$ W, $R_{o\_2} = 20\ \Omega$. Both inverters have same fundamental frequency of 50 Hz [**J2**]

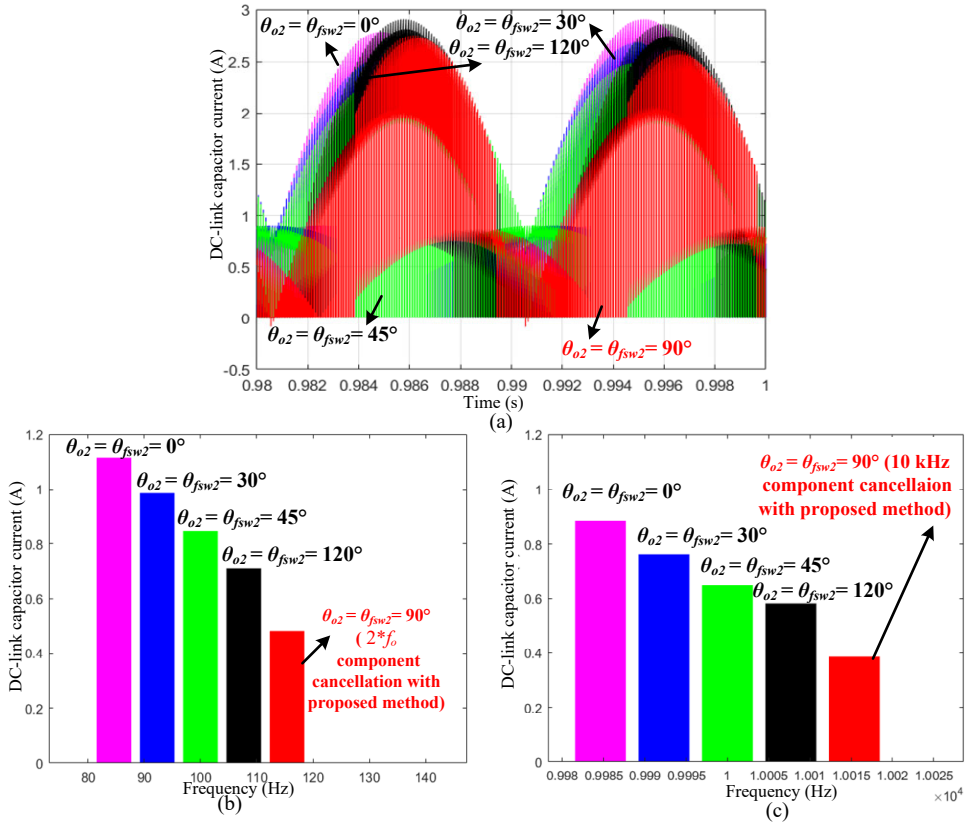


Fig. 4.11: Experimental data of $I_{capbank}$ for **Case 2** plotted in MATLAB showing: (a) the time-domain waveforms when various phase-shift angles are applied, and the corresponding harmonic spectrum components, (b) $2 \times f_o$, and $\theta_{fsw2} = 10$ kHz: demonstrating the effectiveness of the proposed method in cancellation of the main harmonic components of $I_{capbank}$ [**J2**]. The upper-inverter has an output fundamental frequency $f_{o\_1} = 45$ Hz, output power $P_{o\_1} = 50$ W while the lower-inverter has an output fundamental frequency $f_{o\_2} = 50$ Hz, and output power $P_{o\_2} = 20$ W. The upper-inverter has $R_{o\_1} = 20\ \Omega$, and the lower-inverter has $R_{o\_2} = 52\ \Omega$ [**J2**]

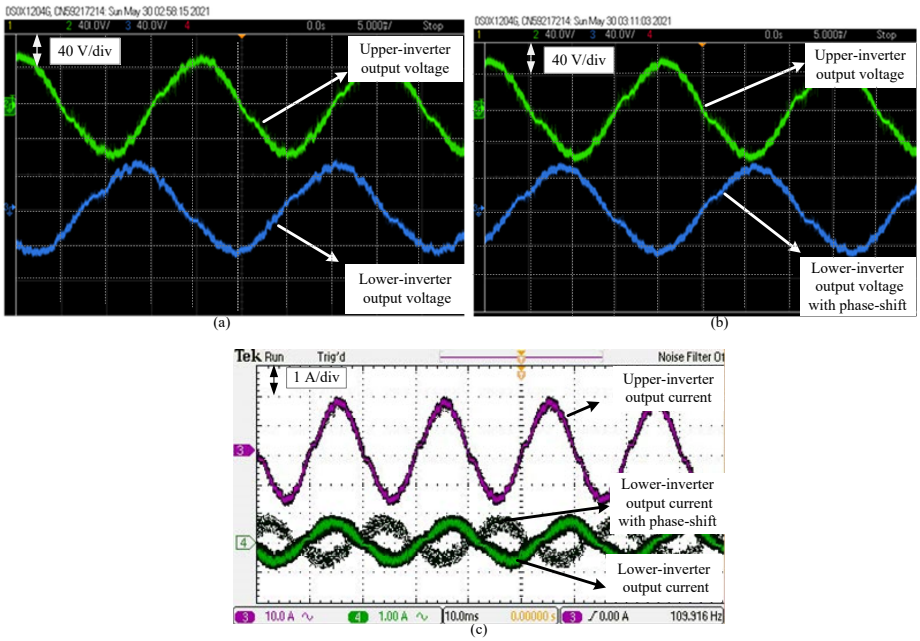


Fig. 4.12: Measured waveforms of the multidrive system for **Case 2** showing: (a) output voltages with no interleaving, (b) output voltages with $\theta_{o2} = \theta_{fsw2} = 90°$, (c) output currents with no interleaving, and output currents with $\theta_{fsw2} = 90°$ [**J2**]. The upper-inverter has an output fundamental frequency $f_{o\_1} = 45$ Hz, output power $P_{o\_1} = 50$ W while the lower-inverter has an output fundamental frequency $f_{o\_2} = 50$ Hz, and output power $P_{o\_2} = 20$ W. The upper-inverter has $R_{o\_1} = 20\ \Omega$, and the lower-inverter has $R_{o\_2} = 52\ \Omega$ [**J2**].

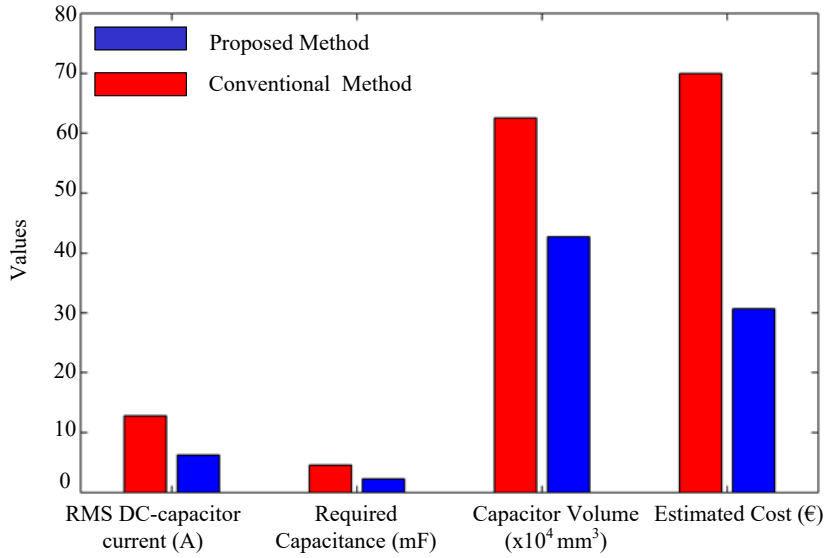


Fig. 4.13: Comparison of the DC-link capacitor design using conventional and proposed design method given in Fig. 4.3 [**J2**]. The lifetime comparison using the proposed method and using the conventional method is shown graphically in Fig. 4.8 [**J2**].

4.5.1.2 Case 2: Multidrive System with Different Output Power and Output Load Frequency

The output fundamental frequency of upper-inverter is considered to be $f_{o\_1} = 45$ Hz and output power $P_{o\_1} = 50$ W. For the lower-inverter, the output fundamental frequency $f_{o\_2} = 50$ Hz, and output power $P_{o\_2} = 20$ W. The loading of the upper-inverter is $R_{o\_1} = 20\ \Omega$, and that for the lower-inverter is $R_{o\_2} = 52\ \Omega$ [**J2**]. The phase-shift angles of the lower-inverter of the experimental setup are varied and the $I_{capbank}$ data is observed. The results are shown in Figs. 4.11 and 4.12. Unlike the previous case study result, the DC-link harmonic components are not completely reduced, but some cancellations can be seen [**J2**]. So, it is fair to say that the proposed method helps to reduce the DC-link current compared to when there is no phase-shift applied even when the multidrive system is operating with different output power and output load frequency [**J2**].

4.5.2 Verification of the Design of DC-link capacitor Based on the Proposed Capacitor Current Reduction Method

In this section, a DC-link capacitor is designed for Case 1, using the minimum $I_{capbank}$ and conventional method and then a comparison is made in terms of the minimum required capacitance value, its volume, and cost (shown Fig. 4.13) [**J2**]. " It can be seen that when the proposed method is applied to a multidrive system: (1) the overall $I_{capbank}$ RMS value decreases (for the Case 1, $I_{capbank}$ can be reduced by 50%), (2) consequently lowering the required DC-link capacitance value (only half the value of the DC-link capacitor is needed in Case-1), which means that the overall capacitor volume, and cost reduces (by half in this example case 1) " [**J2**].

From the above experimental results, it could be concluded that the proposed method is a feasible option to reduce the DC-link current, reduce the size of the DC-link capacitor and eventually increase the DC-link capacitor lifetime in a multidrive system in a low-cost manner [**J2**].

4.6 Conclusion

In this chapter, a low cost DC-link capacitor-current reduction and low cost DC-link capacitor design method is discussed for a multidrive system. This is achieved through optimal interleaving of the fundamental-output currents in addition to the phase-shifting of the carrier-waves of the parallel-connected inverters [**C1, J1, J2**]. The effectiveness of the proposed method is experimentally verified using different case studies.

Publication in Peer-Reviewed Journal

[**J2**] **S. Baburajan**, H. Wang, F. Mandrile, B. Yao, Q. Wang, D. Kumar, and F. Blaabjerg, "Design of Common DC-Link Capacitor in Multiple-Drive System Based on Reduced DC-Link Current Harmonics Modulation," *IEEE Transactions on Power Electronics*, Status: *Accepted (Early Access)*.

Chapter 5

Conclusions

5.1 Summary

In this Ph.D. project, the key focus is to increase a multidrive system reliability by mitigating the DC-link harmonics and, thereby, improving the lifetime of DC-link capacitor. The main contributions and concluding remarks of this Ph.D. research along with its future research perspectives are summarized in this chapter [**C1, J1, J2**].

Chapter 1 gives the background of the research topic, existing state-of-art, project motivation, and research questions in detail. Also, multiple sub-objectives are formulated from the research questions to clearly define objectives and outcomes for this research project. Also, the project limitations are identified, and the thesis outline is explained. The following Chapter 2 explores the impact of unipolar and bipolar SPWM modulation techniques on the lifetime of the DC-link capacitor in a multidrive system having a common DC-bus [**C1**]. The DC-link harmonics are analyzed using PLECS and the lifetime of DC-link capacitors are modelled and estimated using MATLAB. The obtained results indicate that unipolar SPWM produces lesser DC-link current harmonics than bipolar SPWM, thereby gives the longest lifetime for DC-link capacitors in the multidrive topology. The results from this chapter are used in the following chapters to further develop DC-link current harmonic mitigation strategies [**C1**].

In Chapter 3, a DC-link current harmonics mitigation method using a carrier-based phase-shifting scheme in multidrive systems that have a centralized rectifier is discussed. Using analytically developed mathematical equations, an optimal phase-shift angle for the carrier signal is investigated, which provides a maximum DC-link capacitor-current harmonics cancellation and thereby improving the DC-link capacitor lifetime [**J1**].

In Chapter 4, another low-cost DC-link harmonic mitigation is discussed to reduced DC-link capacitor current. In this method, both the output currents and the carrier

signals of the parallel inverter units in a multidrive system are interleaved at the optimally angles [**J2**]. These optimal angles are decided from the surface diagram, plotted using the developed analytical equations. Using the reduced DC-link capacitor current, a low cost DC-capacitor design is suggested.

Based on the results from the above chapters, it can be concluded that three DC-link harmonics mitigation strategies for a multidrive based drivetrain system has been identified: first one is to use unipolar SPWM in multidrive units [**C1**], second is to implement interleaving of the carrier signals [**J1**], and final one is to use the surface plot diagram and developed analytical DC-link capacitor current model to select the required phase-shift angle between switching frequencies and fundamental frequencies of the multidrive units [**J2**]. Also, using these three methods, it is observed that the DC-link capacitor lifetime is improved. Thereby, the two main goals of this Ph.D. study has been accomplished.

5.2 Main Contributions of this Ph.D. Research

The main contributions of this PhD project are summarized below [**C1, J1, J2**]:

1. Proposed two multidrive topologies with centralized rectifier having a common DC.
2. Analyzed and concluded that unipolar SPWM is producing the least amount of DC-link harmonics, and thereby it will result in the longest DC-link capacitor lifetime in a multidrive topology having a centralized rectifier having a common DC [**C1**].
3. Developed the analytical modelling of the DC-link capacitor current in a multidrive topology with centralized rectifier. Based on the analytical model, two DC-link capacitor current mitigation strategies are proposed. The first method is through optimal interleaving of carrier waves [**J1**]. The second method is through optimal interleaving of the fundamental-output currents in addition to the phase-shifting of the carrier-waves of the parallel-connected inverters [**J2**]. By reducing the overall DC-link capacitor current, the power-loss and hot-spot temperature are reduced, which eventually improves the reliability of the DC-link capacitor.
4. Also, using the proposed reduced DC-link capacitor current, a low-cost capacitor sizing/design method is proposed [**J2**].

5.3 Future Work

There are several research possibilities for the future development of the outcomes and proposed solutions of this PhD project. A few of the future works include the following:

1. This research study can be extended to analyze the impact of the proposed harmonic mitigation and DC-link capacitor lifetime extending methods in a multidrive system with three-phase motor drive systems or a mixture of single-phase and three-phase loads.

2. Furthermore, it is worth looking into the lifetime impact of hybrid DC-link capacitor-bank having both film and electrolytic capacitors.

3. The study could also be extended to multidrive systems with more than two drives.

4. Another important future work is to study how to optimize the phase-shift angles and developing a design approach to size the DC-link capacitor when two inverters have different switching-frequencies.

5. Experimental validation of the lifetime calculations.

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Part II

Publications

"I am grateful for all experiences at Aalborg University, which made me stronger and helped me realize what I want to achieve in the long run in my life….I have happily moved to the industry now….

…I also learnt a very important lesson that there will be many people who try to pull you down as you progress in your career but if you trust yourself, give in your best efforts and move ahead with 100% confidence, no one can stop you.."

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