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***Abstract*—New semiconductor devices based on wide bandgap materials are emerging in medium voltage power electronic converter applications, presenting new opportunities to the industry relying on semiconductor devices. SiC MOSFETs with blocking voltages of 10 kV (and above) is a promising technology, however, their fast switching transitions result in increased output voltage slew rate (dv/dt), which poses challenges to the applicability of the SiC MOSFET technology. This paper examines the impact of the increased dv/dt on the applicability of an off-the-shelf closed loop hall-effect current sensor when utilized in a medium voltage SiC MOSFET based power electronics converter. Analysis of the capacitive couplings in the current sensor is presented along with an experimental determination of the parasitic capacitance between its primary conductor and secondary winding. Experimental measurements have identified two distinct noise components in the current sensor measurement path due to: 1) capacitive coupling between the primary conductor and secondary winding, and 2) an inferred capacitive coupling into the active circuitry of the current sensor.**

***Index Terms*—SiC, MOSFET, Medium Voltage, Current Sensor, Capacitive Coupling, Parasitics**

I. Introduction

At present days, extensive research is being carried out to exploit the emerging silicon-carbide (SiC) MOSFETs as an enabling technology in future medium voltage (MV) power electronic converter (PEC) applications [1], [2]. The SiC technology offers higher breakdown voltage, lower switching and conduction losses, and increased operating temperature compared to the traditional and mature silicon technology [3], [4]. However, the recent technological progress uncovers new challenges, for instance, new requirements for the design of power electronic devices due to the increased electrical field stresses, higher switching frequencies, and increased voltage slew rates (dv/dt) [2].

The increased dv/dt of the SiC MOSFET output voltage can cause capacitive displacement currents within the system, which leads to higher switching losses and EMI issues [5], [6], therefore, research in this field is currently focused on reducing the parasitic capacitive couplings within the system, e.g. in the power module packaging [7], the gate drivers [8], [9], and the filter inductors [6], [10], [11]. A critical parasitic capacitance within the system is the output capacitance as it highly influences the switching performance of the SiC MOSFET due to the charging or discharging of the output capacitance during each switching transition [12], [13]. The output capacitance comprises the internal output capacitance of the power module and the parasitic capacitance of whichever equipment being connected to the output terminal of the power module that experiences the dv/dt (i.e. filter inductors, sensors, etc.).

In [14], the measured high frequency current component overlaying the fundamental current component is reported to be caused by the parasitic capacitance of the filter inductor. The high frequency current component has a significant magnitude compared to the fundamental component, approaching a signal-to-noise ratio (SNR) of unity, which could prove critical for the integrity of the current measurement when utilized for control and protective purposes.

Research pertaining to the challenges arising within current sensing and sampling for closed loop feedback of MV PEC applications is lacking. Therefore, this paper aims at analyzing the impact of the parasitic capacitive couplings in the current sensor and the integrity of current measurements taken with an off-the-shelf closed loop hall-effect current sensor.

II. Evaluated Current Sensor

Current sensing is required in a wide range of applications covering many different voltage and current levels, and there-

fore, each application has specific requirements for the current sensor regarding size, cost, accuracy, range, bandwidth, and insulation [15]. A presumably current sensing technology for MV PEC applications to meet the above requirements is the mature closed loop hall-effect current sensor technology based on Faraday's law of induction and magnetic field sensing. Closed loop hall-effect sensors have been widely used in low voltage PEC applications, however, their applicability in MV PEC applications has not yet been explored. In this paper, the closed loop hall-effect current sensor LA 55-P from LEM [16] has been chosen as a candidate solution to evaluate its performance when utilized in a MV PEC application.

When the current sensor is placed directly at the output terminal of the half-bridge power module, the voltage at the primary conductor of the current sensor experiences the same dv/dt as the output terminal of the half-bridge power module during each switching transition, which gives rise to concerns regarding parasitic couplings from the primary conductor to the current sensor. Parasitic couplings can, in principle, occur to all parts of the current sensor, however, the parasitic capacitance from its primary conductor to secondary winding is of special concern in this analysis, as the presence of the parasitic capacitance could cause noise current to couple directly into the measurement path of the current sensor. The analytically expected peak magnitude of the noise current due to the parasitic capacitance is directly proportional to the parasitic capacitance, C, and the voltage slew rate across the capacitor, dv/dt, given by the general equation in (1).

$$i = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{1}$$

The slew rate of the power module output voltage has been measured to be as high as 30 kV/μs [17], mainly limited by the MOSFET gate resistor and the output capacitance. Even a small parasitic capacitance in the range of a few picofarads could cause hundreds of milliamperes of noise current coupling into the secondary winding of the current sensor, and therefore, directly into its measurement path.

Another important aspect that needs to be considered when working with current sensing of MV PEC applications is the turns ratio of the current sensor. Even a small displacement current in the secondary winding of the current sensor may correspond to a relatively large current in the primary conductor when taking the turns ratio of the current sensor into account.

III. Parasitic Capacitance Extraction

The need for determining the parasitic capacitance has been emphasized in the last section, and therefore, this section covers an experimental determination of the parasitic capacitance of this certain current sensor.

A. Low Voltage, High Frequency Sweep

The experimental determination of the parasitic capacitance has been done by performing a low voltage, high frequency sweep of the voltage at the primary conductor and measuring the resulting output voltage across the measuring resistor, v_{R}.

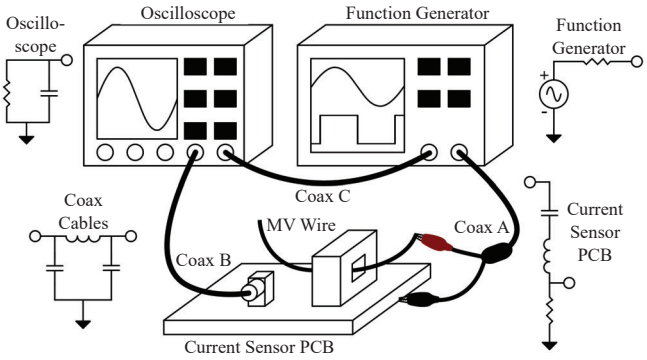


Fig. 1: Configuration of the laboratory setup for experimental determination of parasitic capacitance together with equivalent circuit representations.

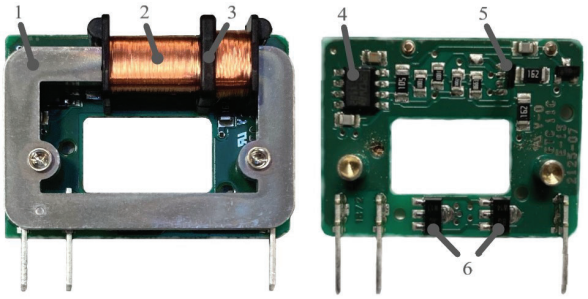


Fig. 2: Internal structure of the LEM LA 55-P with its outer casing removed. 1) Iron core, 2) Secondary winding which spans the air gap, 3) Air gap, 4) Op Amp, 5) Hall-effect element, and 6) Push-pull transistors.

The frequency sweep is performed with a sinusoidal input voltage of $\pm$10 V in the frequency range from 1 to 50 MHz using a Tektronix AFG31000 arbitrary function generator. Due to the nature of the high frequency extraction method, the importance of considering the parasitic circuit elements introduced by cables as well as input and output impedance of connected laboratory equipment is needed. The laboratory configuration is illustrated in Fig. 1 along with schematics of the equivalent circuit representations used to model the experimental setup in LTspice.

From the low voltage, high frequency sweep, the parasitic capacitance is found to be highly dependent on the placement of the primary conductor inside the current sensor opening due to its internal structure and layout, and a parasitic capacitance of 0.31 pF is taken as the worst-case with the primary conductor placed in close proximity to the secondary winding of the current sensor (upper right corner as shown in Fig. 2).

The experimental determination of the parasitic capacitance is further carried out for three primary turns, defined as the practical upper limit considering the cross-sectional area of the MV wire and the opening of the current sensor, to investigate the influence of adding additional primary turns on the parasitic capacitance. The measurements show that an increase in primary turns with a factor of three increases the

parasitic capacitance to 0.65 pF, which is slightly above a factor of two. Hence, in cases where the rated current range of the current sensor allows for additional primary turns, it could prove possible to achieve a comparative lower parasitic capacitance and a lower SNR by increasing the number of primary turns.

IV. Equivalent Impedance Network for Noise Modeling

With the parasitic capacitance from the primary conductor to secondary winding of the current sensor experimentally determined, an equivalent impedance network has been developed in LTspice. The equivalent impedance network aims to model the behavior of the noise current coupling into the measurement path of the current sensor and to predict its frequency as well as magnitude during a switching transition of the SiC MOSFET. The equivalent impedance network is shown in Fig. 3 in which the equivalent circuit representations indicated on Fig. 1 are used in the modeling.

The analysis of the parasitic capacitance between the primary conductor and secondary winding of the current sensor in Section II suggested that the noise current coupling directly into the measurement path of the current sensor could be modeled as a single capacitance. This simplification of utilizing a simple single-stage model implies that only the first harmonic component is represented by the equivalent impedance network, which needs to be considered when utilizing the model to predict the behavior of the noise current.

Even though the capacitive coupling is relatively small compared to other capacitive couplings within the system, it can cause displacement currents of more than 9 mA in the secondary winding, corresponding to 9 A in the primary conductor when taking into account the turns ratio of the current sensor. The magnitude of the displacement currents has been calculated using (1) at a dv/dt of 30 kV/μs for a 10 kV SiC MOSFET half-bridge power module [17].

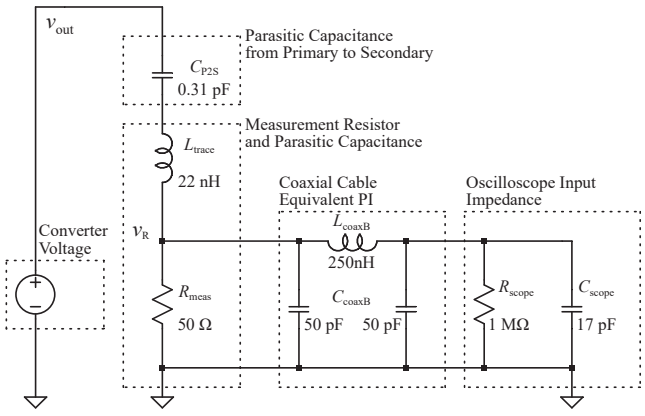


Fig. 3: Equivalent impedance network for noise modeling in LTspice. The converter voltage used as input is the experimentally measured output voltage, v_{out}, from the SiC MOSFET half-bridge power module.

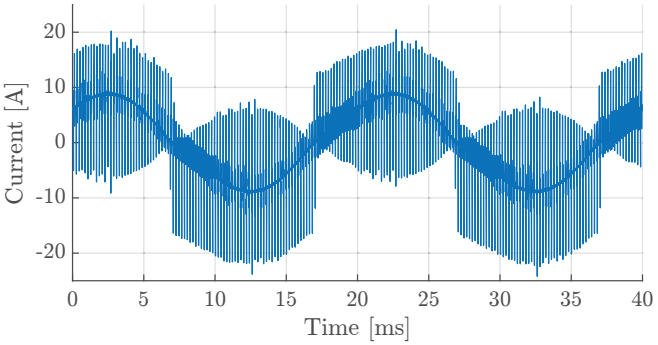


Fig. 4: Continuous current measurement with current sensor, LEM LA 55-P, at 6 kV DC-link voltage and a RMS load current of approx. 7 A.

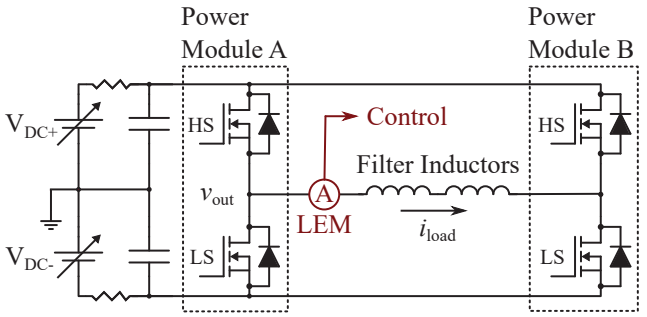
V. Noise Current Evaluation

The actual noise present in the current sensor has been measured during open loop operation of a PEC comprising 10 kV, 20 A, 350 mΩ SiC MOSFET 3rd gen. dies populated in a single-chip half-bridge power modules engineered and manufactured in-house at AAU Energy. A continuous current measurement is shown in Fig. 4, which shows a similar high frequency current component overlaying the fundamental component as the one reported in [14]. These tests have been performed on a single phase test setup shown in Fig. 5 with two half-bridge 10 kV SiC MOSFET power modules connected back-to-back through a shared DC-link and with the half-bridge outputs connected through two series connected 30 mH MV filter inductors to circulate the power. The filter inductors used are designed with a relatively low capacitive coupling of 50 pF terminal to terminal [10].

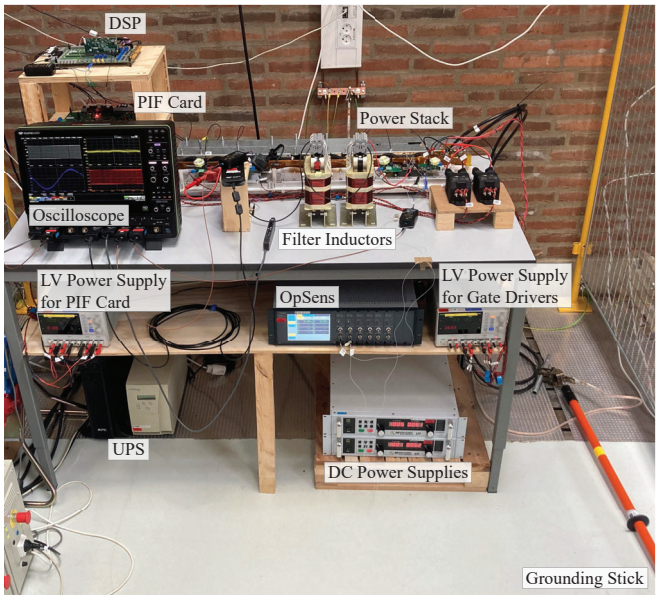
The experimental measurements have identified two distinct noise current components instead of only one as the initial analysis suggested, and therefore, only included in the equivalent impedance network. The first noise component is caused by the direct capacitive coupling, C_{P2S}, into the measurement path of the current sensor as indicated with a red current path in Fig. 6. The second one is inferred to be caused by capacitive coupling, C_{P2H}, into the hall-effect element resulting in noise currents disturbing the active push-pull amplifier circuit of the current sensor as indicated with a purple current path in Fig. 6.

A. First Noise Component

The measurement of the first noise component was made without an auxiliary power supply to the current sensor and the results are shown in Fig. 7 for a turn-on switching transition of the high-side (HS) MOSFET for varying DC-link voltages. The measurements are performed at zero load current corresponding to the highest dv/dt for a switching transition. The upper plot shows the measured output voltage, v_{out}, of power module A. In the lower plot, the solid lines indicate the measured noise current, whereas the dashed lines indicate the corresponding results from the equivalent impedance network in LTspice with the measured output voltage used as converter



(a) Electrical schematic.



(b) Photograph from the laboratory.

Fig. 5: Single phase test setup used to analyze the impact of switching noise in the current sensor when utilized in a medium voltage power conversion application.

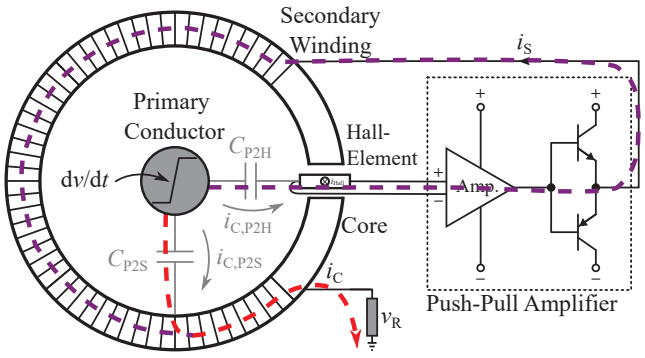


Fig. 6: Schematic of the closed loop hall-effect current sensor with its key parasitic capacitances indicated. The red current path indicates the first noise component and the purple current path indicates the second noise component.

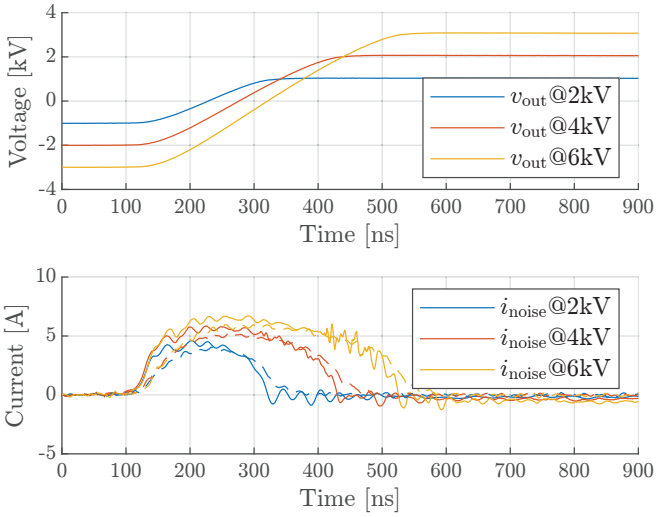


Fig. 7: Measurement of first noise component without an auxiliary power supply to the current sensor. Solid lines are measured values and dashed lines are simulated values from the equivalent impedance network in LTspice shown in Fig. 3 using the measured output voltages as input.

voltage, v_{out}. A high degree of agreement in both magnitude and frequency can be seen between the measured and simulated noise current in Fig. 7 when the current sensor has no auxiliary power supply.

B. Second Noise Component

The measurement of the second noise component was made with an auxiliary power supply to the current sensor and the results are shown in Fig. 8 for a turn-on switching transition of the HS MOSFET at zero load current for varying DC-link voltages. It can be noticed that turning on the current sensor reveals some slower acting response in the noise picked up by the current sensor. The first noise component is presented in a nanosecond timescale, and even though still largest in magnitude, now only covers a fraction of the microsecond timescale associated with the additional noise introduced when the auxiliary power supply is on.

Even though the second noise component is smaller in magnitude compared to the first noise component, it is much more critical for the current sensing and sampling due to its longer duration as will be discussed in the subsequent section.

VI. Proposed Sampling Scheme

The identified noise components can negatively impact the integrity of the current sampling if a conventional sampling scheme is adopted as the second noise component takes more than 20 μs to decay to a sufficient level. Therefore, an alternative sampling scheme is proposed to reduce this negative impact by ensuring that the switching noise has had time to decay. The proposed sampling scheme is based on a double sample, single update principle such that samples are taken on the ZERO and PERIOD counter compare events.

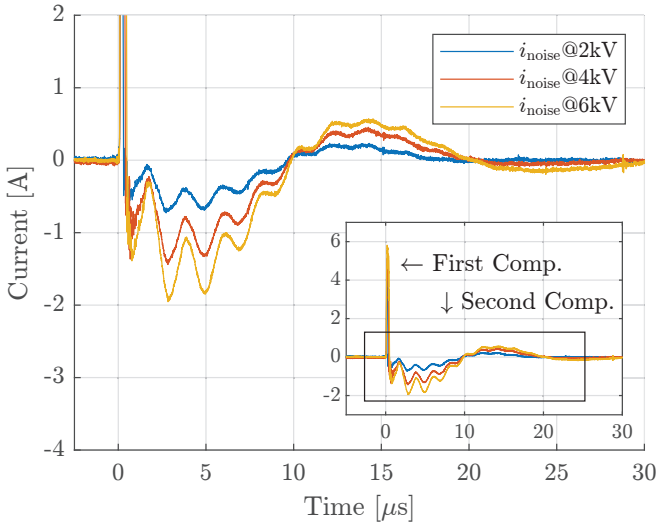


Fig. 8: Measurement of second noise component with an auxiliary power supply to the current sensor. All values are measured experimentally.

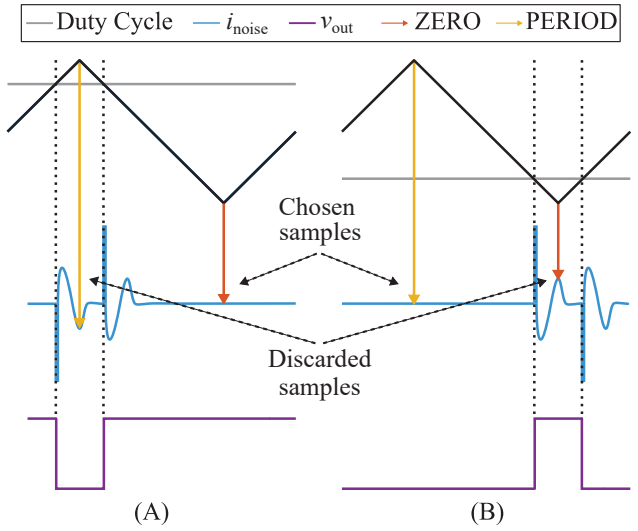


Fig. 9: Illustration of proposed sampling scheme at a (A) high duty cycle and (B) low duty cycle.

Based on the previously calculated duty cycle, one of the current samples is stored/chosen for further computation and the other discarded as shown in Fig. 9. Currents sampled on the ZERO counter compare event are stored for duty cycles above 50%, whereas currents sampled on the PERIOD counter compare event are stored for duty cycles below 50% to ensure that the switching noise has had time to decay.

The proposed sampling scheme has been experimentally evaluated in the setup shown in Fig. 5 at a DC-link voltage of 6 kV and a RMS load current of 7 A. The evaluation compares the sampled currents (ZERO, PERIOD, and chosen) with the voltage across the measuring resistor, v_R, of the current sensor converted into its corresponding noise current as shown in

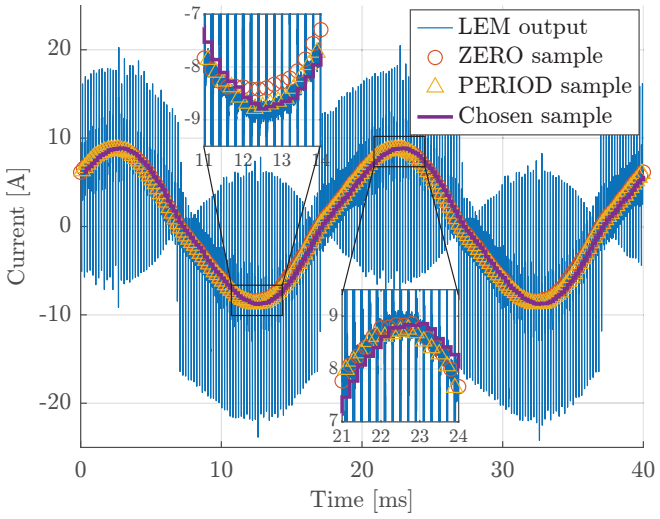


Fig. 10: Sampled currents compared to the measurement output of the current sensor, LEM LA 55-P, converted into its corresponding current.

Fig. 10. The effectiveness of the sampling scheme is most distinct at low or high duty cycles as the noise components are disturbing the sampled current.

It should be noticed that since the converter is operated in open loop without an active dead time compensation, the current waveforms are to be expected to have some distortion around its zero crossings due to converter non-linearities such as dead time voltage error and system parasitics.

VII. Conclusion

This paper analyzes the impact of the increased dv/dt of the MV SiC MOSFETs on the applicability of an off-the-shelf current sensor when utilized in a MV PEC application. The paper presents an analysis of the capacitive couplings introduced by the current sensor and an experimental determination of the parasitic capacitance between its primary conductor and secondary winding of 0.31 pF.

An equivalent impedance network has been proposed to predict the behavior of the noise current coupling into the measurement path of the current sensor during a switching transition of the SiC MOSFETs. An experimental comparison is carried out to validate the equivalent impedance network with a high degree of accuracy.

The experimental measurements have identified two distinct noise components in the measurement path of the current sensor, which negatively impacts the integrity of the current sampling if a conventional sampling scheme is adopted.

Therefore, an alternative sampling scheme is proposed and experimentally validated to reduce the negative impact of the switching noise on the integrity of the current sampling.

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