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Discovery of Loss Imbalance in SiC Half-Bridge Power Modules – Analysis and Validations

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***Abstract*—It is commonly assumed that power semiconductor switching losses are the same for high-side and low-side devices in a half-bridge power module. However, this paper reveal that the high-side SiC MOSFET in a medium voltage power module exhibits over 40 % higher switching energy compared to the low-side SiC MOSFET. The loss imbalance is attributed to the parasitic high-side gate capacitance in the power module, which contributes to the equivalent high-side Miller capacitance. A physics-based switching energy dissipation model is therefore proposed, distinguishing between low-side and high-side switching energy dissipation. Double pulse testing demonstrates that high-side switching energy dissipation increases by 5 mJ per 2.5 pF increment in equivalent Miller capacitance, aligning closely with the analytically calculated increase of 6 mJ per 2.5 pF. Continuous power module testing shows a 10 °C increase in high-side junction temperature. The findings from this paper offer crucial insights into research, design, and manufacturing of half-bridge modules enabled by SiC MOSFETs.**

***Index Terms*—Capacitive couplings, Double pulse testing, Medium voltage SiC MOSFETs, Half-bridge switching dynamics, Miller capacitance, Switching losses, Power module modelling**

I. Introduction

SEMICONDUCTOR power losses are of main concern in the design and engineering of Power Electronic Converter (PEC) systems, due to 1) the power level of the PEC system being constrained by the capability of the power module packaging structure and cooling system to remove heat from the power semiconductor device [2], [3] and 2) thermal stresses causing premature end-of-life and in worst case catastrophic failures within the PEC system [4], [5].

For a half-bridge power module semiconductor configuration, the switching losses are commonly described as in (1)–(2) [6].

$$E_{\text{sw}}^{n} = \underbrace{\int_{t_{\text{on}}} v_{\text{ds}}^{n}(t) \cdot i_{\text{d}}^{n}(t)\ \text{d}t}_{E_{\text{on}}^{n}} + \underbrace{\int_{t_{\text{off}}} v_{\text{ds}}^{n}(t) \cdot i_{\text{d}}^{n}(t)\ \text{d}t}_{E_{\text{off}}^{n}} \tag{1}$$

$$P_{\text{sw}} = \sum_{n=1}^{t_{\text{sum}}/T_{\text{sw}}} \frac{E_{\text{sw}}^{n}(T_{\text{j}}, C_{\text{para}}, ...)}{t_{\text{sum}}} \tag{2}$$

Where E_{on} and E_{off} are the turn-on and turn-off volt-ampere integral switching energy losses, t_{on} and t_{off} are the turn-on and turn-off switching transition times given for an arbitrary switching period T_{sw}^{n}, P_{loss} is the total semiconductor switching losses, E_{sw} is the combined switching energy dissipation per switching period as function of external parameters, e.g. junction temperature T_{j} and parasitic capacitances here denoted C_{para}, n is the n^{th} switching period from 1 to $t_{\text{sum}}/T_{\text{sw}}$, where T_{sw} is the switching period and t_{sum} is the summation time interval.

Modelling of the semiconductor switching losses have been studied extensively in the literature. Different representative mathematical computation methods for evaluating the switching power loss of power semiconductor devices has been proposed in the literature [7]–[15], with increasing complexity and precision. Common for these methods is that switching losses are determined using a black box approach, thus not considering the physical switching dynamics of the power semiconductor device, eg. inductive and capacitive parasitic couplings within and around the PEC system, which is why these methods, even with increasing complexity and precision, will only asymptotically approach the actual losses of the power semiconductor devices.

Recent research within SiC MOSFET applications, have gained increased interest in the capacitive couplings of the PEC system due to the faster switching speeds and increased operating voltage levels compared to the prevalent silicon based power semiconductor technologies [16]–[18]. One of the major impacts of the capacitive couplings is the increase in semiconductor switching losses [19].

The intrinsic power semiconductor capacitive couplings, their modelling methods and their impact on device transient switching performance, including the Miller region switching dynamics, have been studied in great detail in [20]–[26]. Similarly, the power module layout parasitic capacitive couplings and their impact on the semiconductor switching performance have been studied in [27]–[31]. As these capacitive couplings

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are often present in the switching power loop of the SiC semiconductor devices, the capacitive displacement currents will be discharging/charging the parasitic capacitances through the channel of the power semiconductor devices, which causes additional joule heating of the devices from; 1) A effective reduction in device switching speed which results in surplus switching losses from the increase of the Volt-Ampere integral [32] and 2) the displacement currents through the channel of the semiconductors, will increase the switched current amplitude and thus result in increased switching and conduction losses [33]. However, the effects of the capacitive couplings on the switching energy dissipation have not been analytically modelled to an extent where it is applicable in system level design considerations.

Common for all of the previous modelling methods proposed by both industry and academia, both the Silicon-based and WBG-based power semiconductor switching losses are assumed identical for the high-side (HS) and low-side (LS) devices in the half-bridge configured power module. Therefore, the existence of a loss imbalance between LS and HS devices can lead to significant error in the loss estimations of these methods. Limited research are available on loss imbalance between HS and LS. In [34] thermal cycling of SiC MOSFET half-bridge shows elevated junction temperatures on the HS devices compared to the LS devices, insinuating either a loss imbalance or a difference in thermal network from junction-to-case between HS and LS devices. Additionally, the loss imbalance phenomenon is described in [1] where the physics based simulations shows increased switching losses on the HS device compared to the LS device. However, the loss imbalance phenomenon has not been analyzed in detail or experimentally validated. To address these research gaps, this paper will experimentally demonstrate that the HS and LS power semiconductor switching losses are not identical and in fact significantly different in a $10\,\mathrm{kV}$ SiC half-bridge power module. The underlying cause will be derived and an analytical physics based modelling method of the increase in Miller region losses will be proposed and validated experimentally.

The paper is organized as follows. In Sec. II the problem of loss imbalance between HS and LS device of a half-bridge configured power module is defined. In Sec. III the parasitic capacitive couplings of MOSFET and power module packaging will be modelled, the contributions of different relevant parasitic capacitive couplings on the SiC MOSFET switching dynamics will be illustrated and the impact of the defined equivalent Miller capacitance on the MOSFET switching speed will be analytically derived. A physics based model of the turn-on switching energy dissipation is presented in Sec. IV, with the addition of the proposed method for approximating the increase in HS Miller region turn-on energy dissipation. Through an experimental case study of the $10\,\mathrm{kV}$ SiC MOSFET power module in Section V, the turn-on energy increase is related to the increase in the equivalent HS Miller capacitance by sweeping the high-side gate capacitance, thus validating the proposed analytical model. Section VII concludes and highlights the contributions of this work.

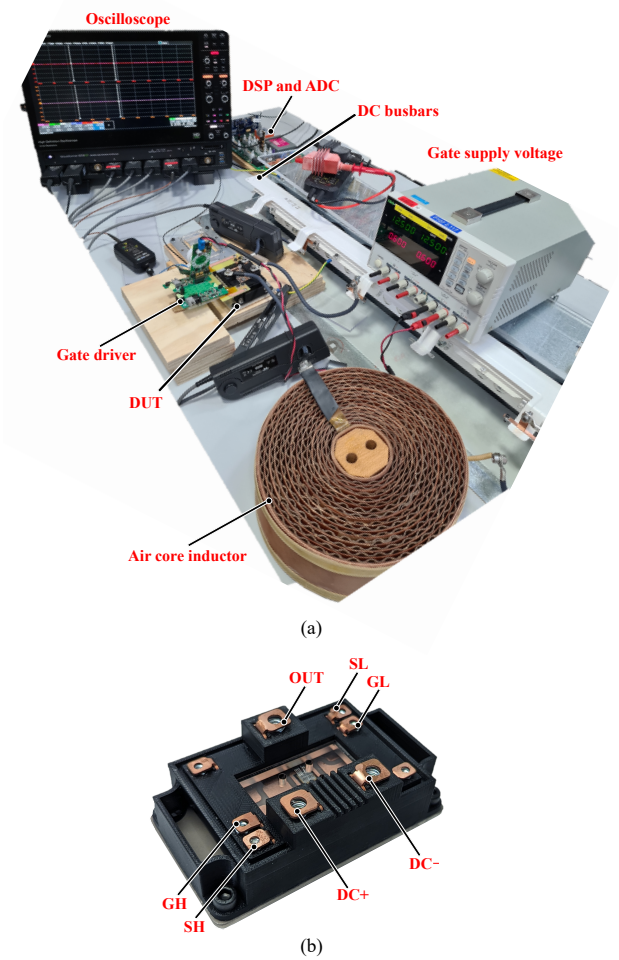

Fig. 1. (a) Experimental double pulse test setup, (b) Custom manufactured medium voltage half-bridge power module [30].

II. Problem Formulation

This paper addresses the significant imbalance in switching energy dissipation between HS and LS SiC MOSFET device in a half-bridge power module. This challenge was presented in [1], where it was derived that the imbalance was due to the increase in equivalent Miller capacitance for the HS MOSFET, where simulation results were presented to demonstrate the impact. Hence, to showcase the challenge in practice, an experimental demonstration of the switching loss imbalance will be provided using a Double Pulse Test (DPT) setup.

The Device Under Test (DUT) is the medium voltage power module shown in Fig. 1(b), populated with $350\,\mathrm{m\Omega}$ $10\,\mathrm{kV}$ SiC MOSFET dies without anti parallel junction barrier schottky diodes, thus the third quadrant operation is through the MOSFET body diodes.

The Double Pulse Test (DPT) setup used for the experimental demonstration is shown in Fig. 1(a) and the schematics for the HS and LS DPT setup are shown in Fig. 2. The experimental test bench is rated for $\pm\,3.6\,\mathrm{kV}$ DC-link voltage. The DC-link busbars are configured in a custom made 3-layer laminated structure with DC+, DC- and DC midpoint terminals, where the DC-midpoint is grounded [42]. The DC-link consists of a series connection of $3.6\,\mathrm{kV}$ DC-link

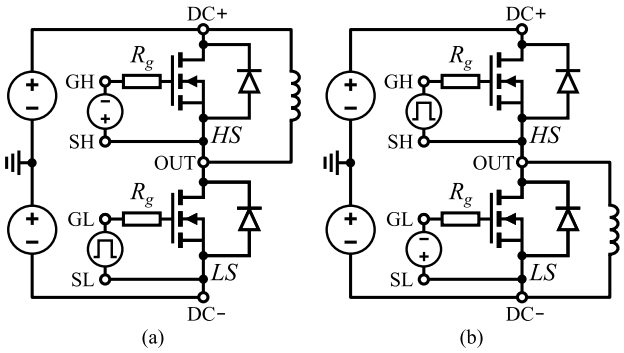

Fig. 2. Double pulse test circuits (a) Low-side (b) High-side.

TABLE I
EQUIPMENT AND COMPONENTS FOR THE EXPERIMENTAL TEST SETUP.

Equipment/Component	Key Parameters
DC-link capacitors [35]	40 µF / 3.6 kV
Magna Power supply [36]	10 kV
Air core inductor	47 mH / ≤12 pF
Isolated gate driver [37]	+20 V / -5 V / ≤2.6 pF
LeCroy CP150 [38]	150 A / 10 MHz
LeCroy HVD3605A [39]	6 kV / 100 MHz / ≤5 pF
LeCroy HVFO103 [40]	60 MHz
LeCroy WaveRunner 8058HD [41]	500 MHz

capacitors with 5 parallel connected 40 µF per pole, yielding a total pole-to-pole DC-link capacitance of 100 µF and a maximum pole-to-pole voltage of 7.2 kV. The DC-link voltage is supplied with ± 10 kV Magna Power Supplies. The load inductor used in the setup is a 47 mH air core inductor. The gate voltage is supplied using a single active bridge topology based isolated gate driver with active Miller clamp [37]. The gate voltage is measured using the optic isolated HVFO103 voltage probe, the drain-source voltage is measured using the HVD3605A differential voltage probe, the drain current is measured by insertion of short connector cables and using the CP150 clamp-on current probe. The measured signals are recorded using a WaveRunner 8058HD oscilloscope. The key parameters of equipment and components used for the setup are summarized in Table I.

The switching waveforms for the LS and HS SiC MOSFET devices are shown in Fig. 3, using a 44 Ω gate resistance. The instantaneous power loss is computed as the product of the time continuous drain current and drain-source voltage and the turn-on energy is calculated from numeric integration as given from (1). From Fig. 3 it can be observed that the HS device exhibits significantly higher turn-on time, compared to the LS device, which causes higher turn-on energy loss. The absolute increase in turn-on time is measured to be approx. 600 ns and the increase in turn-on energy is calculated to be 43 mJ corresponding to a percentage increase of 48 % higher turn-on energy dissipation on the HS compared to the LS, during this specific switching transition.

To understand the cause of this increase in turn-on time and thus the increase in turn-on energy dissipation for the HS device in comparison to the LS device, an analytical model will be derived in the following section.

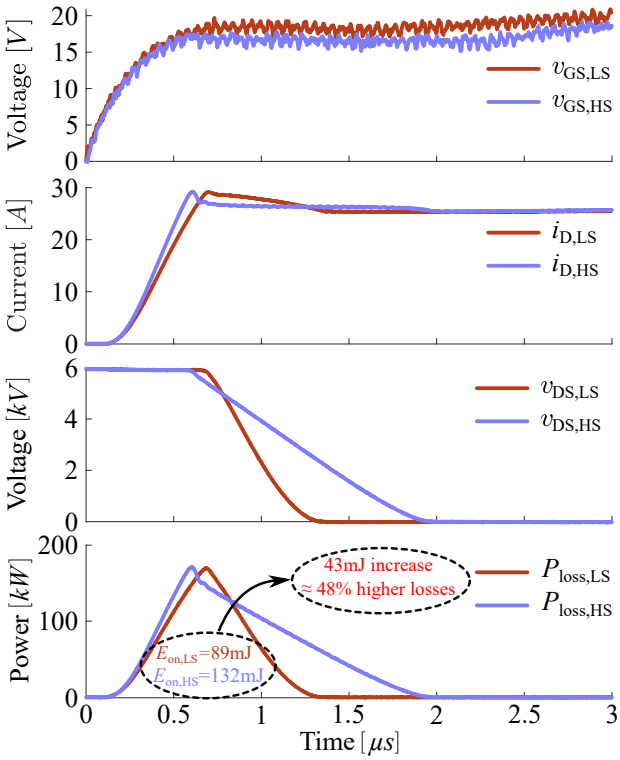

Fig. 3. Turn-on switching transient at 6 kV, 26 A for LS and HS using a 44 Ω gate resistance, showing gate-source voltage v_{GS}, drain current i_D, drain-source voltage v_{DS} and instantaneous semiconductor power loss P_{loss}.

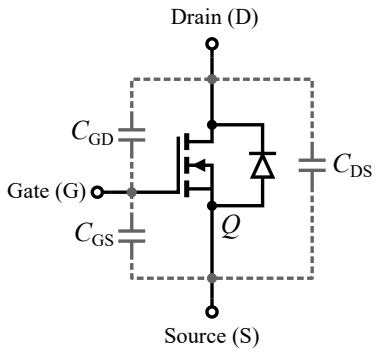

Fig. 4. MOSFET intrinsic capacitances [25].

III. HALF-BRIDGE SIC MOSFET POWER MODULE MODELLING

To obtain the necessary understanding of the MOSFET based half-bridge power module switching transitions, firstly a detailed model of intrinsic and stray capacitive parasitic couplings present within and around the MOSFET based half-bridge power module will be provided.

A. Power MOSFET Modelling

The capacitive couplings of a power MOSFET can be modelled using the intrinsic capacitance model, as illustrated in Fig. 4. Where the capacitances C_{GD} and C_{DS} are typically modelled as being voltage dependent and C_{GS} can be assumed constant [43]. These capacitances are also sometimes referred to as output capacitance C_{OSS}, input capacitance C_{ISS}

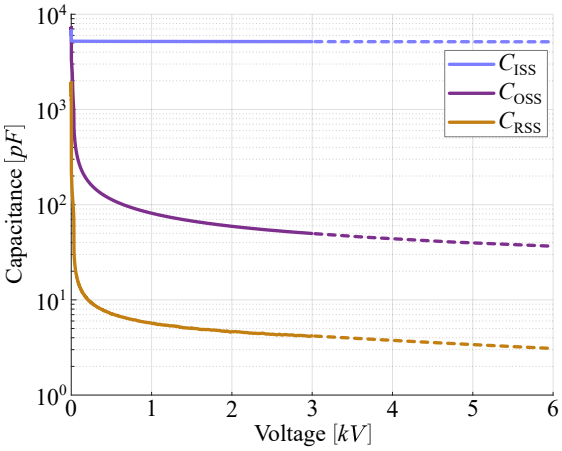

Fig. 5. Intrinsic capacitances of the 10 kV 350 mΩ MOSFET. Solid lines are Keysight B1506 curve tracer measurements up to 3 kV at room temperature, and dashed lines are extrapolated data from exponential curve fitting up to 6 kV.

and reverse transfer capacitance or Miller capacitance C_{RSS}. The definitions of intrinsic MOSFET capacitances are given from (3), where C_{J} is the junction capacitance of the optional external anti-parallel diode.

$$\begin{aligned} C_{\text{OSS}} &= C_{\text{DS}} + C_{\text{GD}} + (C_{\text{J}}) \\ C_{\text{ISS}} &= C_{\text{GS}} + C_{\text{GD}} \\ C_{\text{RSS}} &= C_{\text{GD}} \end{aligned} \tag{3}$$

For the 10 kV rated SiC MOSFET used in the DUT, the intrinsic capacitances as shown as a function of drain-source voltage in Fig. 5. The capacitances are measured using the Keysight B1506 curve tracer at room temperature (22 °C). Due to the curve tracer having a maximum output voltage limitation of 3 kV, the capacitance curves are extrapolated to 6 kV using exponential curve fitting.

The charging dynamics of the MOSFET is governed by these three capacitances. For illustration purposes the MOSFET turn-on characteristics of a half-bridge configuration are depicted in Fig. 6. A brief summary of the MOSFET switching dynamics are given as follows [20], [23], [45]:

$\boldsymbol{t_0 - t_1}$ **:** From time t_0 the gate bias supply voltage is shifted from -5 V to 20 V and the gate-source voltage v_{GS} starts rising with the charging of the gate-source capacitance C_{GS}.

$\boldsymbol{t_1 - t_2}$ **:** At time t_1 the MOSFET gate-source threshold voltage $V_{\text{GS,th}}$ is reached and the drain current i_{D} starts rising. The drain-source voltage V_{DS} is still clamped to the DC voltage level due to the forward voltage drop of the conducting complimentary MOSFET body diode of the half-bridge. When the drain current reaches the load current level i_{OUT} at time t_2 the current is fully commutated from the body diode of the complimentary MOSFET of the half-bridge configuration, thus allowing the body diode to enter the reverse recovery state.

$\boldsymbol{t_2 - t_3}$ **:** At t_2 the stored charge of the body diode of the complimentary MOSFET of the half-bridge is removed during the reverse recovery state of the diode. At time t_3 the peak reverse recovery current of the body diode is reached restoring the reverse blocking capability of the diode, which allows the drain-source voltage v_{DS} to drop as illustrated from Fig. 6.

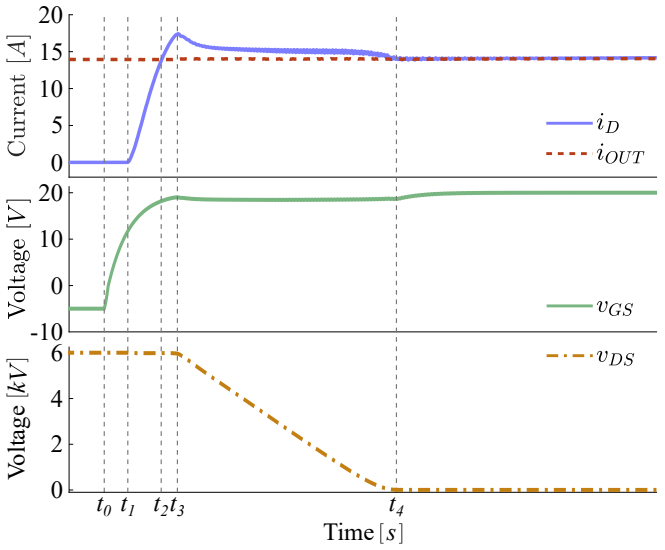

Fig. 6. Medium Voltage SiC MOSFET turn-on switching waveforms, shown for illustration purposes [44].

$\boldsymbol{t_3 - t_4}$ **:** From time t_3 the Miller region is entered with the MOSFET charging dynamics being governed by the charging of the gate-drain capacitance which is often referred to as the Miller capacitance.

In the Miller region a stationary condition is reached where the gate-source voltage is clamped to the Miller voltage level V_{mil} and the Miller capacitance is charged through the gate. The gate current i_{G} is thus limited by the gate resistance R_{G} and the voltage difference caused by the supply voltage V_{G} and the Miller voltage, yielding a constant gate current as illustrated from (4).

$$I_{\text{G}} = \frac{V_{\text{G}} - V_{\text{mil}}}{R_{\text{G}}} \tag{4}$$

During the Miller region C_{GD} and C_{DS} are considered in parallel and thus Kirchhoff's current law dictates that the charging of the drain-source capacitance is forced to follow the charging of the gate-drain capacitance yielding an approximately constant dv/dt on the drain-source voltage until the on-state forward voltage is reached [20].

just as the parasitic capacitive couplings of the MOSFET governs the switching dynamics of the power semiconductor device, the parasitic capacitive couplings of the power module packaging will likewise impact the switching dynamics of the power semiconductor device and will therefore be modelled in the proceeding section.

B. Half-bridge Power Module Modelling

In a typical half-bridge power module the isolating ceramic substrate of the Direct Bonded Copper (DBC) results in parasitic capacitive couplings between the baseplate and the top copper islands, DC+, DC-, OUT, gate-high (GH) and Gate-Low (GL), as depicted by the cross-sectional view in Fig. 7. The circuit representation of the power module capacitive couplings is given in Fig. 8, where the baseplate is assumed grounded, as is the case in most practical setups. The inclusion

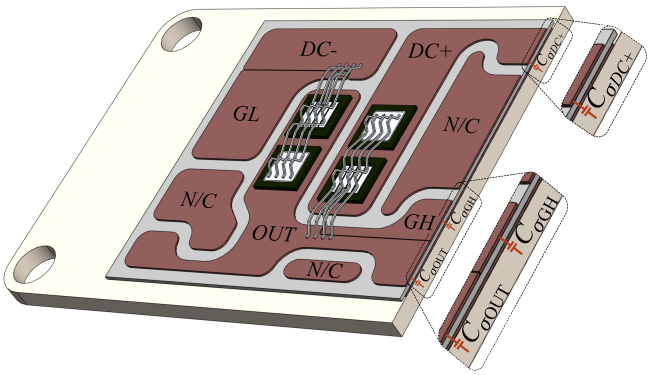

Fig. 7. SiC MOSFET power module layout illustrating the DBC islands, the layering of the DBC and the baseplate including a cross-sectional view of the layering illustrating the OUT, DC+ and gate-high (GH) parasitic capacitive couplings to the baseplate.

TABLE II
VALUES OF PARASITIC CAPACITANCES OBTAINED FROM ANSYS Q3D FOR THE DUT HALF-BRIDGE SiC MOSFET POWER MODULE [33].

$C_{\sigma\mathrm{DC+}}$	$C_{\sigma\mathrm{DC-}}$	$C_{\sigma\mathrm{GH}}$	$C_{\sigma\mathrm{GL}}$	$C_{\sigma\mathrm{OUT}}$	
68.1	32.7	12.4	35.6	81.4	[pF]

of grounding impedance is considered out of scope for this paper, however for the interested reader the impact of grounding impedance is well documented in [33], [46]. In the case

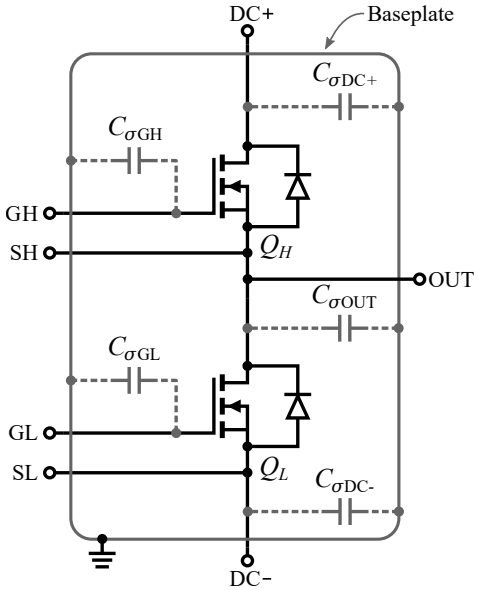

Fig. 8. Parasitic capacitive couplings of the investigated half-bridge power module [30], [33].

of the DUT, the 10 kV SiC MOSFET bare dies are soldered on the top copper of a DBC substrate with 0.63 mm thick AlN isolating ceramic, which is supported by a 5 mm AlSiC baseplate. The parasitic power module capacitive couplings are extracted using Ansys Q3D finite element analysis, under the assumptions of constant AlN permittivity and an equipotential grounded baseplate, yielding the capacitance values in Table II.

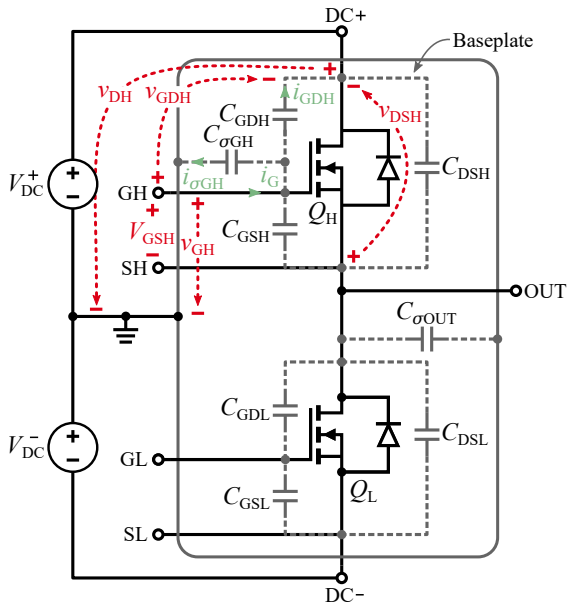

Fig. 9. Equivalent MOSFET half-bridge capacitive coupling model considering MOSFET and power module capacitive parasitic couplings.

The capacitances $C_{\sigma\mathrm{DC+}}$, $C_{\sigma\mathrm{DC-}}$ and $C_{\sigma\mathrm{GL}}$ are referred between two approximately constant potentials during the switching transitions and can thus be analyzed as being fully charged yielding an open-circuit connection in a DC analysis. In contrast the capacitances $C_{\sigma\mathrm{GH}}$ and $C_{\sigma\mathrm{OUT}}$ will be subject to a high dv/dt during switching transitions as the potential of the half-bridge output terminal is changing between DC- and DC+ during each switching commutation [33].

C. Miller Capacitance Modelling

As the majority of the power module parasitic capacitive couplings are referred between constant potentials, the model in Fig. 8 can be simplified and combined with the MOSFET model from Fig. 4 yielding the equivalent MOSFET and power module parasitic capacitive couplings of a half-bridge configuration, in Fig. 9. Here, a difference can be observed in capacitive couplings between the HS gate and LS gate terminals due to the inclusion of the HS gate power module parasitic capacitance $C_{\sigma\mathrm{GH}}$ on the HS MOSFET. The gate voltage V_{GH} to ground will govern the capacitive displacement current of the HS gate capacitance $C_{\sigma\mathrm{GH}}$. As for the HS MOSFET gate-drain capacitance C_{GDH} the voltage governing the capacitive displacement current will be the gate-drain voltage v_{GDH}.

Using Kirchoff's Voltage Law (KVL) the expressions for the HS gate voltage v_{GH}, referred to the grounded DC-midpoint, and HS gate-drain voltage v_{GDH} are derived under the assumption that the gate-source voltage bias is negligible. The respective voltages are given in (5) and (6) and are defined in Fig. 9, which also depicts the polarity conventions used in the derivation. The derivation is based on the HS MOSFET turn-on event, and thus for convenience the polarity of the

drain-source voltage is defined for the negative rate of change of voltage $\mathrm{d}v/\mathrm{d}t$ across the device during turn-on.

$$v_{\mathrm{GH}} = V_{\mathrm{GSH}} + v_{\mathrm{DSH}} + v_{\mathrm{DH}} \approx v_{\mathrm{DSH}} + V_{\mathrm{DC}}^{+} \tag{5}$$

$$v_{\mathrm{GDH}} = v_{\mathrm{GH}} - v_{\mathrm{DH}} = V_{\mathrm{GSH}} + v_{\mathrm{DSH}} + v_{\mathrm{DH}} - v_{\mathrm{DH}} \approx v_{\mathrm{DSH}} \tag{6}$$

The difference between the defined voltages in (5) and (6) is then identified as the DC+ bias on the voltage of the HS gate capacitance $C_{\sigma\mathrm{GH}}$. With V_{DC}^{+} being a constant voltage, only the dv/dt of the drain-source voltage v_{DSH} is governing the capacitive displacement currents of both of the capacitances $C_{\sigma\mathrm{GH}}$ and C_{GDH} as derived in (7) and (8).

$$i_{\sigma\mathrm{GH}} = C_{\sigma\mathrm{GH}} \left(\frac{\mathrm{d}v_{\mathrm{DSH}}}{\mathrm{d}t} + \frac{\mathrm{d}V_{\mathrm{DC}}^{+}}{\mathrm{d}t} \right) = C_{\sigma\mathrm{GH}} \frac{\mathrm{d}v_{\mathrm{DSH}}}{\mathrm{d}t} \tag{7}$$

$$i_{\mathrm{GDH}} = C_{\mathrm{GDH}} \frac{\mathrm{d}v_{\mathrm{DSH}}}{\mathrm{d}t} \tag{8}$$

$$i_{\mathrm{G}} = (i_{\sigma\mathrm{GH}} + i_{\mathrm{GDH}}) = (C_{\sigma\mathrm{GH}} + C_{\mathrm{GDH}}) \frac{\mathrm{d}v_{\mathrm{DSH}}}{\mathrm{d}t} \tag{9}$$

From Kirchoff's Current Law (KCL) the gate current i_{G} is defined as the sum of the two capacitive currents $i_{\sigma\mathrm{GH}}$ and i_{GDH}, thus yielding the expression in (9), clarifying that the HS gate parasitic capacitance $C_{\sigma\mathrm{GH}}$ should be analyzed as being in parallel to the HS gate-drain capacitance C_{GDH}. Effectively this will impact the Miller region of the HS MOSFET Q_{H} compared to the LS MOSFET Q_{L}, which is why the equivalent Miller capacitance $C_{\mathrm{eqmil,H}}$ is introduced. The equivalent Miller capacitance of the HS is defined as the parallel connection of the HS gate capacitance $C_{\sigma\mathrm{GH}}$ and the gate-drain capacitances C_{GDH}, whereas the LS Miller capacitance is defined as the conventional C_{GD}, as shown in (10), under the assumption that the gate-drain capacitances for the LS and HS are identical ($C_{\mathrm{GDH}} = C_{\mathrm{GDL}} = C_{\mathrm{GD}}$).

$$C_{\mathrm{eqmil,H}} = C_{\sigma\mathrm{GH}} + C_{\mathrm{GD}} \;>\; C_{\mathrm{mil,L}} = C_{\mathrm{GD}} \tag{10}$$

$$\left.\begin{aligned} I_{\mathrm{G}} &= C_{\mathrm{eqmil,H}} \cdot \tfrac{V_{\mathrm{DC}}}{\Delta t_{\mathrm{mil,H}}} \\ I_{\mathrm{G}} &= C_{\mathrm{mil,L}} \cdot \tfrac{V_{\mathrm{DC}}}{\Delta t_{\mathrm{mil,L}}} \end{aligned}\right\} \; \Delta t_{\mathrm{mil,H}} \;>\; \Delta t_{\mathrm{mil,L}} \tag{11}$$

As was shown in (4), the charging current of the Miller capacitance during the Miller region is limited by the gate resistor. Thus with a fixed gate current amplitude and a fixed DC voltage yielding a fixed change in drain-source voltage ($\Delta v_{\mathrm{DS}} = V_{\mathrm{DC}}$), the increase in equivalent Miller capacitance will directly impact the duration of the Miller region ($\Delta t_{\mathrm{mil}} = t_4 - t_3$). Thus, changing the slope of the drain-source voltage, as given in (11). This explains the imbalance in the switching dynamics of the two MOSFETs presented in the measurements in Fig. 3 with the HS MOSFET Q_{H} turning on slower than Q_{L} and thus incurring additional losses on the HS device which can impact life-time and reliability of the half-bridge power module.

In (11), the inequality is constrained by the assumption of constant and equal gate current between HS and LS MOSFET during the Miller region. However, from Fig. 3 the Miller voltage levels are observed to be $16.5\,\mathrm{V}$ and $18\,\mathrm{V}$ respectively for the HS and LS, thus implying a difference in constant gate current between HS and LS. The impact on the Miller region time, caused by the deviation between HS and LS gate current is evaluated by combining (4) and (11), as given from (12) and (13).

$$\begin{aligned} \Delta t_{\mathrm{mil,H,\ approx}} &= C_{\mathrm{eqmil,H}} \cdot \frac{V_{\mathrm{DC}} \cdot R_{\mathrm{G}}}{V_{\mathrm{G}} - V_{\mathrm{mil,H}}} \\ &= [1246 \;\; 1364 \;\; 1506]\,\mathrm{ns} \end{aligned} \tag{12}$$

$$\begin{aligned} \Delta t_{\mathrm{mil,L,approx}} &= C_{\mathrm{mil,L}} \cdot \frac{V_{\mathrm{DC}} \cdot R_{\mathrm{G}}}{V_{\mathrm{G}} - V_{\mathrm{mil,L}}} \\ &= [636 \;\; 750 \;\; 915]\,\mathrm{ns} \end{aligned} \tag{13}$$

Where, the gate-drain capacitance is approximated as a constant value by calculating the charge equivalent numeric integral, using the voltage dependent capacitance curve from Fig. 5, as shown from (14).

$$C_{\mathrm{GD,approx}} = \frac{\int_0^{V_{\mathrm{DC}}} C_{\mathrm{GD}}(v)\,\mathrm{d}v}{V_{\mathrm{DC}}} = 5.68\,\mathrm{pF} \tag{14}$$

It should be noted here that the expressions for the Miller region duration in (12) and (13) are highly sensitive to the measured value of the Miller plateau voltage. Thus the measurement error introduced by the voltage probe should be considered in order to evaluate the accuracy of the analytical expression. The LeCroy HVFO103 optical isolated differential probe used to measure the gate-source voltage has a rated accuracy of $\pm 2\,\%$ [40]. Thus by introducing this margin of error of $\pm 2\,\%$ on the measured Miller plateau voltages of $16.5\,\mathrm{V}$ and $18\,\mathrm{V}$, the analytical calculations of the Miller region duration are expressed as confidence intervals, with the middle value being the calculated value without considering the probe accuracy.

From the analytical expressions, the difference in Miller region duration between HS and LS was found to be $600\,\mathrm{ns} \pm 130\,\mathrm{ns}$, which corresponds very well with the measurements in Fig. 3.

IV. TURN-ON SWITCHING ENERGY MODELLING

This section will derive an analytical model of the Miller region turn-on losses, by dissection the turn-on energy dissipation into different loss contributions.

In [33] the impact of parasitic capacitive couplings on the LS MOSFET turn-on switching dynamics during a Double Pulse Test (DPT) is demonstrated by dissecting the switching energy dissipation of an identical $10\,\mathrm{kV}$ SiC MOSFET half-bridge power module. However, the difference between HS and LS switching energy dissipation is not considered. Hence, this section will provide necessary theory to analytically evaluate the difference in HS and LS turn-on switching energy.

The definitions of different contributions of switching energy impacting the combined turn-on switching energy dissipation is clarified from Fig. 10. Here it can be observed how the turn-on energy dissipation can be defined by individual contributions of switching energy during different periods,

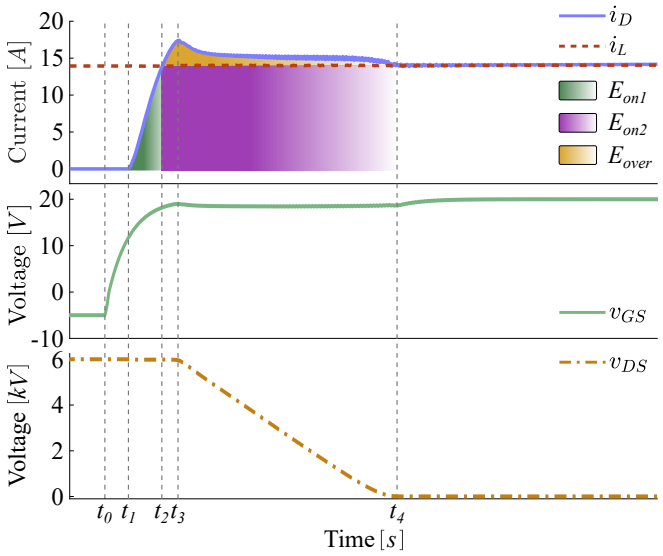

Fig. 10. MOSFET turn-on switching loss energy dissipation [33].

yielding the total energy switching dissipation given in (15)–(18).

$$E_{\text{on}} = E_{\text{on1}} + E_{\text{on2}} + E_{\text{over}} \tag{15}$$

$$E_{\text{on1}} = \int_{t_1}^{t_2} i_{\text{D}} \cdot v_{\text{DS}} \, \mathrm{d}t \tag{16}$$

$$E_{\text{on2}} = \int_{t_2}^{t_4} i_{\text{L}} \cdot v_{\text{DS}} \, \mathrm{d}t \tag{17}$$

$$E_{\text{over}} = E_{\text{QOSS}} + E_{\text{QRR}} + E_{\sigma\text{C}} \tag{18}$$

A. E_{over} Energy Description:

The overshoot energy E_{over} in (18) is the overshoot energy consisting of a combination switching energy contributions; E_{QOSS} is the energy related to the stored charge of the output capacitance and junction capacitance of the MOSFET, body diode and anti-parallel diode of the complementary switching device of the half-bridge, and is given from (19) [33], [47], [48].

$$\begin{aligned} E_{\text{QOSS}} &= \int_0^{V_{\text{DC}}} \left(V_{\text{DC}} - v_{\text{DS}}\right) \cdot C_{\text{OSS}} \, \mathrm{d}v_{\text{DS}} \\ &= \underbrace{V_{\text{DC}} \int_0^{V_{\text{DC}}} C_{\text{OSS}} \, \mathrm{d}v_{\text{DS}}}_{Q_{\text{OSS}} \cdot V_{\text{DC}}} - \underbrace{\int_0^{V_{\text{DC}}} v_{\text{DS}} \cdot C_{\text{OSS}} \, \mathrm{d}v_{\text{DS}}}_{E_{\text{OSS}}} \end{aligned} \tag{19}$$

Where C_{OSS} is the voltage dependent static output capacitance of the MOSFET semiconductor device, defined from (3), Q_{OSS} is the cumulative stored charge of the output capacitance, and E_{OSS} is the related stored energy on the output capacitance for the specified drain-source voltage interval, and v_{DS} is the drain-source voltage of the complimentary switching device.

E_{QRR} is the energy dissipation related to the reverse recovery of the complimentary switching device body diode and optional external anti-parallel diode. The reverse recovery energy is defined by the reverse recovery charge Q_{RR}, which is the charge representing the portion of the excess carries of the diode drift region that is swept out by the reverse current [6], [49]. The energy dissipated during the turn-on of the device is the related to the reverse recovery of the complimentary switching device body diode and/or anti-parallel diode, as derived in (20).

$$\begin{aligned} E_{\text{QRR}} &= \int_{t_2}^{t_4} i_{\text{RR}} \cdot \left(V_{\text{DC}} - v_{\text{DS}}\right) \mathrm{d}t \\ &= \underbrace{V_{\text{DC}} \int_{t_2}^{t_4} i_{\text{RR}} \, \mathrm{d}t}_{Q_{\text{RR}} \cdot V_{\text{DC}}} - \underbrace{\int_{t_2}^{t_4} i_{\text{RR}} \cdot v_{\text{DS}} \, \mathrm{d}t}_{E_{\text{RR}}} \end{aligned} \tag{20}$$

Where i_{RR} and v_{DS} respectively are the reverse recovery current and drain-source voltage of the complimentary switching device. The reverse energy E_{RR} of the complimentary device can be estimated using the triangular approximation of the reverse recovery current transient [6], however in practice for SiC devices with very low reverse recovery energy [50], [51], this will bring a not insignificant overestimation of the diode reverse recovery energy. To the best of the authors' knowledge, no valid analytical model of the reverse recovery energy exists for the medium voltage SiC devices. Additionally, the rated reverse recovery charge of the body diode and/or anti-parallel diode is not provided in the data sheet of the research samples for the medium voltage SiC devices. Hence, the energy related to the diode reverse recovery energy will be neglected in the following derivations. This will entail a margin of error by underestimating the total MOSFET turn-on switching energy dissipation, which should be evaluated in the further validation of the proposed analytical model.

The energy contribution $E_{\sigma\text{C}}$ is a combination of the parasitic capacitive couplings of power module and load inductor equivalent parallel capacitance. The parasitic capacitive couplings contributing to the switching loss energy, differs between HS and LS, as shown from (21)–(22).

$$E_{\sigma\text{C,H}} = \frac{1}{2} \cdot \left(C_{\sigma\text{OUT}} + C_{\sigma\text{L}}\right) \cdot V_{\text{DC}}^2 \tag{21}$$

$$E_{\sigma\text{C,L}} = \frac{1}{2} \cdot \left(C_{\sigma\text{OUT}} + C_{\sigma\text{GH}} + C_{\sigma\text{L}}\right) \cdot V_{\text{DC}}^2 \tag{22}$$

The parasitic power module and inductor capacitances $C_{\sigma\text{OUT}}$, $C_{\sigma\text{GH}}$ and $C_{\sigma\text{L}}$ are constant based on geometry and material properties. It should be noted that the HS gate capacitance $C_{\sigma GH}$ is included in the total capacitance of the LS device being subjected to the $\mathrm{d}v/\mathrm{d}t$ of the OUT terminal, whereas it is not included in the HS device total capacitance. This is the case as the HS gate capacitance will be discharging through the channel of the LS MOSFET during the LS MOSFET turn-on event, thus incurring additional losses caused by displacement current. This should not be mistaken for the impact of the HS gate capacitance on the turn-on switching dynamics of the HS MOSFET where the HS gate capacitance is charged through the gate, impacting the charging time of the combined Miller capacitance.

Thus, by combining the contributions from (19)–(22) the total overshoot energy E_{over} contribution from t_2 to t_4, can be

summarized as (23)–(24).

$$E_{\text{over,H}} = \frac{1}{2} \cdot C_{\text{tot,H}} \cdot V_{\text{DC}}^2 + Q_{\text{tot}} \cdot V_{\text{DC}} - E_{\text{OSS}} \quad (23)$$

$$E_{\text{over,L}} = \frac{1}{2} \cdot C_{\text{tot,L}} \cdot V_{\text{DC}}^2 + Q_{\text{tot}} \cdot V_{\text{DC}} - E_{\text{OSS}} \quad (24)$$

$$C_{tot,H} = C_{\sigma\text{OUT}} + C_{\text{L}} \quad (25)$$

$$C_{tot,L} = C_{\sigma\text{OUT}} + C_{\sigma\text{GH}} + C_{\text{L}} \quad (26)$$

$$Q_{tot} = Q_{\text{OSS}} + Q_{\text{RR}} \quad (27)$$

B. E_{on2} Energy Description:

As was described previously the MOSFET Miller region is defined from t_3 to t_4 during turn-on. The Miller region switching energy dissipation are incorporated into E_{on2} as depicted from (28)–(29), which shows how E_{on2} can be split into two contributions; $E_{\text{on2,RR}}$, from t_2 to t_3, which is being governed by the diode reverse recovery time and $E_{\text{on2,mil}}$, from t_3 to t_4, which is governed by the Miller capacitance charging time.

This may be further simplified by approximating i_{L} and v_{DS} as constant from t_2 to t_3, and approximating constant $\mathrm{d}v_{\text{DS}}/\mathrm{d}t$ from t_3 to t_4. Thus, allowing the Volt-Ampere integral to be simplified using a triangular approximation, yielding (28) and (29).

$$E_{\text{on2}} = \underbrace{\int_{t_2}^{t_3} i_{\text{L}} \cdot v_{\text{DS}}\,\mathrm{d}t}_{E_{\text{on2,RR}}} + \underbrace{\int_{t_3}^{t_4} i_{\text{L}} \cdot v_{\text{DS}}\,\mathrm{d}t}_{E_{\text{on2,mil}}}$$

$$E_{\text{on2,H}} = I_{\text{L}} \cdot V_{\text{DC}} \cdot (t_3 - t_2) + \underbrace{0.5 \cdot (I_{\text{L}} \cdot V_{\text{DC}} \cdot \Delta t_{\text{mil,H}})}_{E_{\text{on2,mil,approx,H}}} \quad (28)$$

$$E_{\text{on2,L}} = I_{\text{L}} \cdot V_{\text{DC}} \cdot (t_3 - t_2) + \underbrace{0.5 \cdot (I_{\text{L}} \cdot V_{\text{DC}} \cdot \Delta t_{\text{mil,L}})}_{E_{\text{on2,mil,approx,L}}} \quad (29)$$

By combining (15)–(16), (23)–(24), and (28)–(29) an indirect expression for the Miller region turn-on losses, as a function of the experimentally determined losses, can be derived as in (30) and (31).

$$E_{\text{on2,mil,H}} = E_{\text{on,H}} - E_{\text{on1}} - E_{\text{on2,RR}} - E_{\text{over,H}} \quad (30)$$

$$E_{\text{on2,mil,L}} = E_{\text{on,L}} - E_{\text{on1}} - E_{\text{on2,RR}} - E_{\text{over,L}} \quad (31)$$

The expressions in (30) and (31) are evaluating the Miller region losses based on the combined experimental data and knowledge of the power module and semiconductor parasitic capacitive couplings. These expressions can then be used to evaluate the accuracy of the simplified approximated analytical Miller region losses described by (32) and (33).

$$E_{\text{on2,mil,H,approx}} = 0.5 \cdot (I_{\text{L}} \cdot V_{\text{DC}} \cdot \Delta t_{\text{mil,H}}) \quad (32)$$

$$E_{\text{on2,mil,L,approx}} = 0.5 \cdot (I_{\text{L}} \cdot V_{\text{DC}} \cdot \Delta t_{\text{mil,L}}) \quad (33)$$

To validate the proposed analytical model, the following two sections will evaluate the increase in HS turn-on switching energy dissipation from both double pulse and continuous test experimental results.

V. Experimental Case Study 1: Double Pulse Testing

To investigate the impact of increase in equivalent Miller capacitance, a sensitivity analysis is conducted where the HS gate capacitance $C_{\sigma\text{GH}}$ is increased incrementally during double pulse testing.

A. Equivalent Miller Capacitance Sweep

In the experimental case study, the equivalent Miller capacitance is artificially increased by inserting ceramic lead capacitance $C_{\text{GH,ext}}$ between HS gate terminal and baseplate, external to the power module, as shown in Fig. 11 and illustrated by the schematic in Fig. 12.

By series connecting two of the $6\,\text{kV}$, $5\,\text{pF}$ rated ceramic capacitances [52], the external capacitance is increased in steps of approximately $2.5\,\text{pF}$. Thus, the total equivalent Miller capacitance $C_{\text{eqmil,H}}$ is given from (34), under the assumption of negligible impact from lead inductance.

$$C_{\text{eqmil,H}} = C_{\sigma\text{GH}} + C_{\text{GD}} + C_{\text{GH,ext}} \quad (34)$$

Hence, by referring the size of the gate-drain capacitance from (14) and the size of the power module HS gate capacitance from Table II, each increment of external added capacitance is approximately equal to $14\,\%$ increase in equivalent Miller capacitance.

Details of the experimental DPT setup is described thoroughly in Section II. Experimental waveforms with $2.5\,\text{pF}$ increments in external $C_{\text{GH,ext}}$ are shown in Fig. 13, demonstrating the increase in HS turn-on energy dissipation with the increase in external HS gate capacitance. As is depicted in Fig. 13, the switching transition instances t_1 $=62\,\text{ns}$, t_2 $=213\,\text{ns}$ and t_3 $=259\,\text{ns}$ are identical for all values of external HS gate capacitance. Thus, only Δt_{mil} is increased. The Miller plateau voltage level is similar and approximately constant at $16.8\,\text{V}$ for all cases. Therefore, as the Miller voltage level is constant, Fig. 13 demonstrates the increased HS turn-on energy loss due to longer Δt_{mil} caused by increased HS capacitance, as was predicted from (12). As shown from Fig. 13, the total turn-on switching energy dissipation is observed to increase by $4\,\text{mJ}$–$6\,\text{mJ}$ between each increment of $2.5\,\text{pF}$ of external HS gate capacitance, which is deemed a significant increase. Analysis and comparison between the experimentally obtained values and the calculated values from theoretical predictions will be presented in the proceeding sections.

Additionally, as the external HS gate capacitance increases, oscillations with increasing amplitude can be observed on gate-source voltage, drain current, and drain-source voltage. In [53], a hypothesis is proposed that these oscillations are caused by a positive feedback forming when the HS gate-to-baseplate capacitance provides the path of least impedance, seen by the gate-source capacitance. This corresponds well with the observed trend, that the oscillations seems to increase in amplitude as the external gate-to-baseplate capacitance is increased. Further investigations of this positive feedback oscillations phenomenon is considered outside the scope of this work, however the authors would like to encourage future research on this phenomenon.

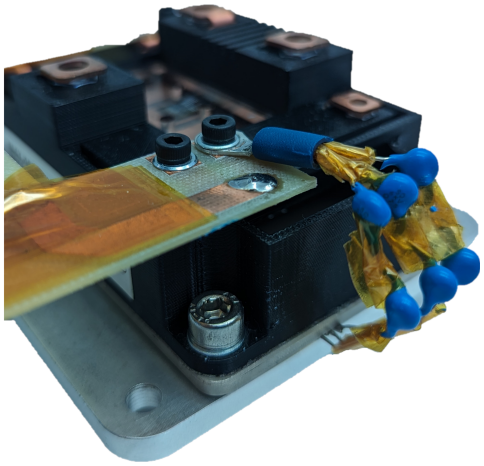

Fig. 11. Ceramic lead capacitances inserted externally between power module HS gate terminal and baseplate/heatsink.

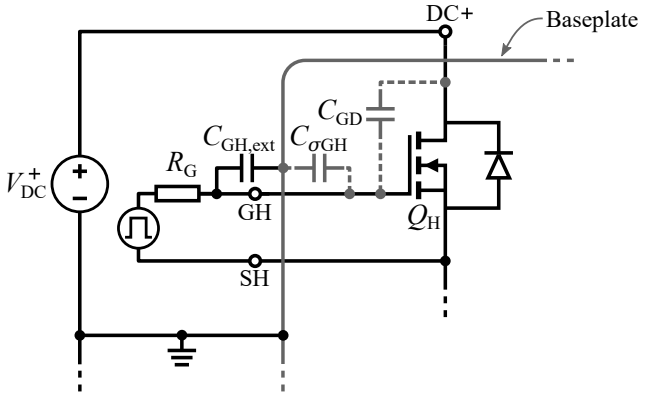

Fig. 12. Simplified schematic illustrating the three capacitances contributing to the total equivalent high-side MOSFET Miller capacitance; $C_{\sigma GH}$, C_{GD}, and $C_{GH,ext}$.

B. Validation of Analytical Model

In Section IV two expression for the the Miller region turn-on switching energy dissipation was derived, the direct approximation in (32) and the analytical approximation in (12). The analytical method of calculating the Miller region turn-on energy is based on the triangular approximation of the drain-source voltage. Hence, it is chosen to investigate the impact of this analytical approximation, by comparing to the experimentally acquired results as is shown in Fig. 14. As can be seen the triangular approximation of the drain-source voltage will introduce a significant deviation between the calculated and the measured Miller region duration. This deviation is caused by the voltage dependent non-linearity of the gate-drain capacitance, which causes the gate-drain capacitance to change dramatically at low voltage levels as shown from Fig. 5, thus impacting the slope of the drain-source voltage at low voltage levels. These dynamics are not included in the approximated model due to the charge equivalent average gate-drain capacitance approximation from (14), and thus the analytical approximation of the Miller region duration is expected to be different from the experimentally measured Miller region duration.

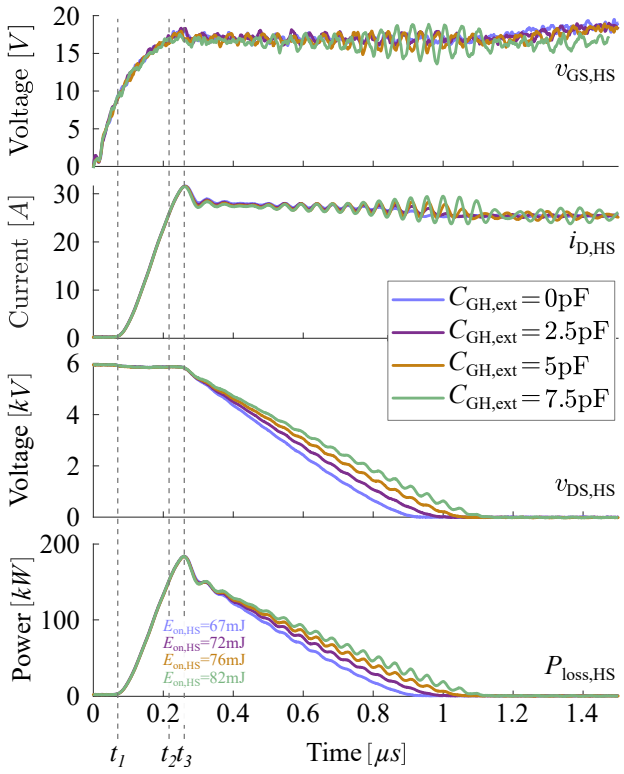

Fig. 13. Experimental turn-on switching transient at 6 kV, 26 A for HS using a 15 Ω external gate resistance, showing gate-source voltage v_{GS}, drain current i_D, drain-source voltage v_{DS} and instantaneous semiconductor power loss P_{loss} at 2.5 pF increments in external HS gate capacitance.

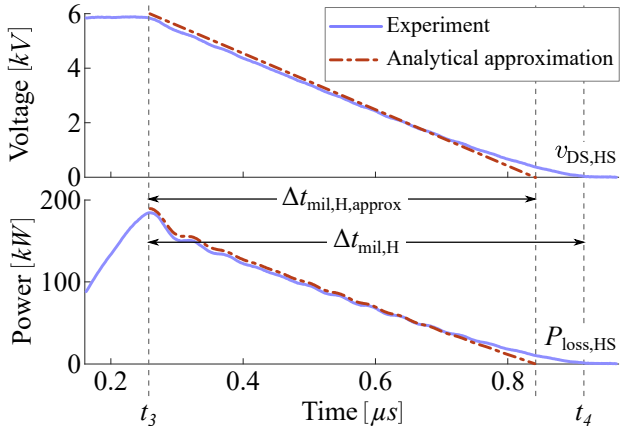

Fig. 14. Graphical illustration depicting the impact of the triangular approximation of the drain-source voltage.

To establish a base for comparison between experimental and analytically approximated Miller region turn-on energy dissipation, the indirect method of calculating the Miller region turn-on switching energy dissipation based on the already acquired experimental data was proposed as seen in (30).

Table III summarizes the calculated turn-on energy dissipation and turn-on times from both the experimental sensitivity analysis and analytical calculations with increments in external HS gate capacitance. From the experimental data in Table III the absolute increase in turn-on energy dissipation is observed to vary from 4.8 mJ–5.4 mJ between each increment in ex-

TABLE III
SUMMARIZED TURN-ON ENERGY DISSIPATION AND TURN-ON TIMES FOR HS SIC MOSFET WITH VARIED EXTERNAL HS GATE CAPACITANCE, FOR 6 kV, 26 A DPT.

$C_{\text{GH,ext}}$	0	2.5	5	7.5	[pF]
$E_{\text{on,H}}$	67	72	76	82	[mJ]
$t_{\text{on,H}}$	871	948	1,004	1,080	[ns]
$\Delta t_{\text{mil,H}}$	674	751	806	883	[ns]
$E_{\text{on2,mil,H}}$: Eq. (30)	46	51	56	61	[mJ]
$\Delta t_{\text{mil,H,approx}}$: Eq. (12)	581	662	742	822	[ns]
$E_{\text{on2,mil,H,approx}}$: Eq. (32)	45	52	58	64	[mJ]

ternal HS gate capacitance, and the increase in Miller region duration between each increment differs from $55\,\text{ns}$–$78\,\text{ns}$.

From the indirect method in (30), the absolute increase in turn-on energy dissipation is calculated to be between $4.8\,\text{mJ}$–$5.4\,\text{mJ}$ for each increment in external HS gate capacitance, which is identical to the experimental increase. This is to expected, as the as the indirect method is based on subtracting the analytical energy contributions from the experimental data, and the terms E_{on1}, $E_{\text{on2,RR}}$ and $E_{\text{over,H}}$, in (30), are constant and independent of Miller region switching dynamics.

The Miller region duration is calculated from (12) yielding an increase between each increment of HS gate capacitance of $80\,\text{ns}$, using a constant Miller plateau voltage of $17.2\,\text{V}$. By utilizing the calculated Miller region duration for the approximation of the Miller region turn-on losses in (32), the increase in energy dissipation is calculated to be $6.3\,\text{mJ}$ between each increment of HS gate capacitance, yielding an overestimated increase of $1\,\text{mJ}$-$1.5\,\text{mJ}$ calculated turn-on Miller region losses between each increment, compared to the total turn-on energy dissipation E_{on} and the indirect calculated Miller region turn-on energy dissipation $E_{\text{on2,mil,H}}$.

By considering the measurement accuracy of the voltage and current probes of the experimental setup, which is summarized in Table IV, the deviation between the indirect and approximated method of calculating the Miller region turn-on energy dissipation from (30) and (32) respectively, is expressed as confidence intervals rather than exact values, as shown in Fig. 15. Here, it is observed how the measurement error introduced by the accuracy of the probes causes the analytically approximated Miller region turn-on energy $E_{\text{on2,mil,approx,H}}$ to overlap with the Miller region turn-on losses calculated from the combination of the derive analytical model and the experimental data $E_{\text{on2,mil,H}}$. These results implies that the deviation between approximated Miller region turn-on energy dissipation and the Miller region turn-on energy calculated from the indirect method in (30) is within the experimental voltage measurement accuracy. The magnitude on the error bars on the approximated Miller region turn-on energy dissipation shows deviation from $5\,\text{mJ}$–$9\,\text{mJ}$ dependent on the size of the external HS gate capacitance, which demonstrates how the calculation of the Miller region duration from (12) is highly sensitive to the accuracy of the measured Miller plateau voltage level.

However, as is observed from Table III, the exact values obtained with the analytically method of deriving the Miller region turn-on energy dissipation is within $5\,\%$ deviation of the

TABLE IV
MEASUREMENT ACCURACY OF THE EXPERIMENTALLY USED VOLTAGE AND CURRENT PROBES.

LeCroy HVFO103 [40]	$\pm 2\,\%$
LeCroy HVD3605A [39]	$\pm 1\,\%$
LeCroy CP150 [38]	$\pm 1\,\%$

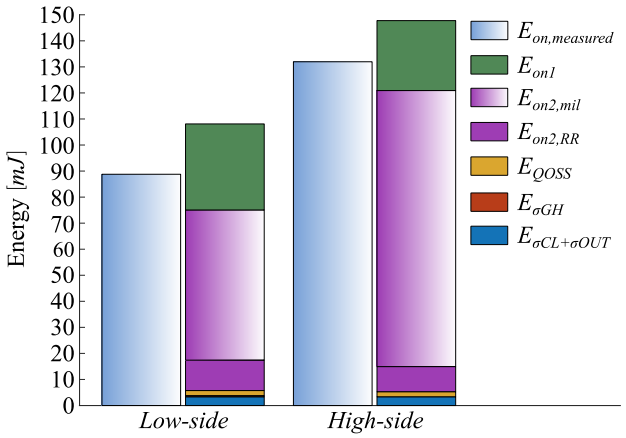

Fig. 15. Turn-on switching energy dissipation as function of increase in equivalent high-side Miller capacitance. The measurement accuracy of current and voltage probes impacting the results for the Miller region turn-on energy dissipation are evaluated, with the error bars showing the interval of accuracy.

combined experimental and analytically derived Miller region turn-on energy. This is deemed as a good agreement between experiment data and analytical model. Furthermore, it should be noted that the intend of the proposed analytical model is to demonstrate the loss mechanism behind the increase in HS energy, caused by the increase in HS gate capacitance, which is clearly shown from the results in both Table III and Fig. 15. Thus the proposed method is able to capture the loss mechanism related to the increase in module parasitic HS gate capacitance to a satisfactory extent.

Having validated the proposed analytical model, the expression from (11) and (32) are now combined into the expression in (35).

$$E_{\text{on2,mil,H,approx}} = \underbrace{0.5 \cdot C_{\text{eqmil,H}} \cdot V_{\text{DC}}^2}_{\text{stored capacitive energy}} \cdot \underbrace{\frac{I_{\text{L}}}{I_{\text{G}}}}_{\text{current gain}} \tag{35}$$

The switching energy dissipation contributed during the Miller region duration can thus, according to (35), be described by two parts; 1) the stored energy on the equivalent Miller capacitance, multiplied by, 2) the MOSFET current amplification gain. It should although be noted that this is only valid during the Miller region duration where the gate current is constant, yielding a constant MOSFET current amplification gain.

C. Switching Energy Dissection

The accuracy of the proposed analytical model has been discussed in previous section. This section will analyze the imbalance in switching energy dissipation, demonstrated in Fig. 3, by providing a dissection of the individual switching energy contributions using the proposed analytical model.

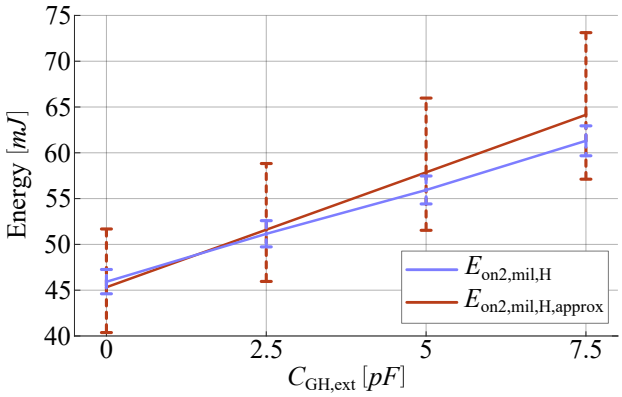

Fig. 16. Turn-on switching energy dissection for low-side and high-side SiC MOSFET during 6 kV, 26 A DPT using a 44 Ω gate resistance.

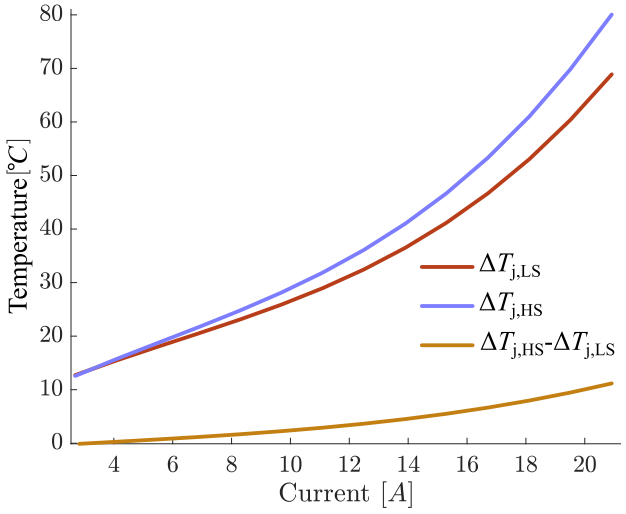

Fig. 17. Loss imbalance between high-side and low-side demonstrated from a comparison of junction temperature increase between high-side and low-side SiC MOSFET during continuous operation with 5 kHz pulse width modulation and 6 kV DC-link voltage.

Figure 16 shows a bar plot of the switching energy dissipation for the LS and HS SiC MOSFET power semiconductor device during double pulse testing at 6 kV, 26 A using a 44 Ω gate resistance. From here it is illustrated how the proposed analytical method yields a 40 mJ increase in switching energy dissipation between HS and LS, with 108 mJ calculated for LS and 148 mJ for HS. The total experimental measured switching energy dissipation from the Volt-Ampere integral are found to be 89 mJ and 132 mJ for the LS and HS respectively, yielding a difference of 43 mJ. This depicts how the analytical model can accurately predict the relative difference between HS and LS switching energy dissipation, however the analytical method over estimates both LS and HS energy by approx. 20 mJ. This over estimation is attributed to the measurement accuracy on the Miller plateau voltage reading as was also addressed in (12)–(13).

From the individual switching energy contributions, it is observed how the extra switching energy dissipation on the HS compared to the LS is primarily contributed by the extended Miller region duration with an increase in $E_{on2,mil}$ from 58 mJ on LS to 106 mJ on HS, thus highlighting the impact of the equivalent HS Miller capacitance. The E_{on1} contribution is reduced from 33 mJ on LS to 27 mJ on HS, which is attributed to the positive shift in Miller plateu voltage voltage seen on the LS compared to the HS in Fig. 3, thus extending the duration of the time interval from t_1–t_2. The shift in Miller plateau voltage similarly causes extended duration for the commutation of the current between diode and MOSFET, thus reducing the $E_{on2,RR}$ contribution from 12 mJ on the LS compared to 10 mJ on the HS. The contributions of E_{QOSS}, $E_{\sigma\text{L}}$ and $E_{\sigma\text{OUT}}$ are constant of 4 mJ and identical between HS and LS, whereas the contribution of $E_{\sigma\text{GH}}$ is only present on the LS and contributes 0.2 mJ.

Although the proposed method overestimates both the HS and LS losses by approx. 20 mJ, the method can predict with high accuracy the relative increase in switching energy on the HS compared to the LS. If methods from existing literature were used for evaluating the switching energy dissipation, only the LS would be considered and the HS losses would be assumed to be identical, leading to significant underestimation of the HS switching energy dissipation.

VI. Experimental Case Study 2: Continuous Testing

To showcase the direct impact of the extra switching energy dissipation caused by increased equivalent Miller capacitance on the HS compared to the LS, the junction temperatures for both HS and LS SiC MOSFET are measured under continuous operation.

A. Continuous Test Results

The DUT 10 kV power module used for double pulse testing in previous sections is utilized in this section for pulse width modulated continuous power circulation testing. The SiC MOSFETs are operated at 5 kHz, 6 kV DC voltage, and the load current is incrementally increased up to 21 A peak (15 A RMS). The junction temperatures for HS and LS are measured using Opsens fiber optic sensors [54] and shown in Fig. 17, with the junction temperature increase ΔT_{j} being defined as the difference between the absolute measured junction and liquid temperature as shown in (36).

$$\Delta T_{\text{j}} = T_{\text{junction,measured}} - T_{\text{liquid,measured}} \tag{36}$$

From Fig. 17 a maximum increase of 10 °C in junction temperature is observed, corresponding to a 16.4 % increase from LS to HS. This increase in temperature is directly caused by the increased switching energy dissipation of the HS compared to the LS. Similarly, it can be noticed how the trend curves shows an increasing difference in junction temperature between HS and LS as the load current increases. Due to the positive temperature coefficient of the on-state resistance, the increase in HS temperature from the extra switching losses causes increased on-state resistance. The increased on-resistance causes more conduction losses, which further increases the temperature difference between HS and LS. This increase in HS junction temperature demonstrates the impact of the equivalent high-side Miller capacitance and

further emphasizes the importance of considering the loss imbalance in SiC half-bridge power modules.

B. Impact of Loss Imbalance

Previous sections of this paper have clearly demonstrated a significant turn-on switching energy imbalance between HS and LS SiC MOSFET device, which from continuous test results have been validated to cause significant junction temperature difference between HS and LS devices.

As the state-of-the-art methods for estimating converter losses are based on the assumption of identical losses between HS and LS, many converter designs will be evaluated based on only the LS device switching losses. Thus, as the capacity of the cooling system will be dimensioned for the LS losses under nominal operation, being unaware of the increased HS device switching losses can lead to severe overestimation of the power handling capability of the PEC system. The unexpected increased thermal stresses on the HS device will impact the estimated life-time reliability, which can cause premature end-of-life thus hindering predictive maintenance, and in in worst case cause catastrophic failures within the PEC system. Additionally, this will directly impact the converter efficiency estimates by overestimating the converter efficiency. Therefore, if a designer is unaware of the increase in HS device switching losses, the errors introduced to both estimated efficiency and reliability of the PEC system could severely impact the operation expenditures of the PEC system which could be detrimental to the expected revenue of the product.

C. Perspectives and Solutions

To address the loss imbalance between HS and LS, some possible mitigation strategies are shared from the authors' perspectives.

1) Binning of power semiconductor dies offers the possibility of matching the power semiconductor losses between HS and LS, by e.g. choosing the dies with the lowest R_{dson} for the HS, thus the conduction losses for the HS will be lower than that of the LS, thereby accounting for the increased switching losses on the HS. Alternatively, the dies with the lowest threshold voltage could be chosen for the HS devices to reduce the relative difference in switching speed between HS and LS, and thus eliminate the imbalance in switching losses.

2) Optimized package layout solutions targeting reduction in the size of the power module parasitic high-side gate capacitance could reduce the impact of the loss imbalance between HS and LS. This includes methods such as reducing the top copper area of the high-side gate plane [30], or by using double DBC to effectively half the parasitic power module capacitance [55]. State-of-the-art research demonstrates a liquid cooled ceramic baseplate-less power module assembly with no backside copper for complete elimination of the parasitic power module capacitances [56], thus ideally achieving balanced losses between HS and LS. However, this has not been proven from experimental results, and the performance of the proposed power module design has not been fully validated under continuous operation, and therefore more research is needed to prove this as a suitable mitigation strategy.

3) Introducing different turn-on gate resistances for HS and LS semiconductor devices, could potentially force the switching speed of the two devices to be identical, thus achieving balanced switching losses.

VII. Conclusion

In this work the discovery of difference in high-side and low-side turn-on switching energy dissipation is presented by experimental demonstration of a conventional half-bridge power module enabled by $10\,\mathrm{kV}$ SiC MOSFET devices. From double pulse test results a $48\,\%$ increase in high-side turn-on energy is demonstrated. Through modelling of the intrinsic and stray capacitances of the MOSFET and power module capacitances, the different in switching speed between high-side and low-side is found to be caused by the high-side power module layout parasitic capacitance. Physics based analytical derivations of the semiconductor switching dynamics and switching energy dissipation supports the findings of increased high-side switching energy, showing only $5\,\%$ deviation to the experimental results. The results are validated under continuous operation, showing $10\,^{\circ}\mathrm{C}$ $(16.4\,\%)$ junction temperature increase on the high-side device compared to the low-side device. The findings of this paper provide new insight for further research in design and optimization strategies in SiC half-bridge power modules, and additionally highlights the need to evaluate both high-side and low-side switching losses for future designs of SiC MOSFET power electronic converter systems.

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