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Comparative Analysis of Bond Wire Degradation in Power Modules during DC and AC Power Cycling

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***Abstract*—This study assesses bond wire degradation differences between DC and AC power cycling tests in IGBT power modules. With existing experimental data, an empirical lifetime model has been developed for both methods. With the bond wire lift-off being the main failure mechanism, physical modeling approach is applied using a simplified thermo-mechanical finite element model to examine the temperature evolution, stress and strain development at the bond wire-chip interface. Factors including heating time, temperature gradient, and current density are addressed and discussed to explain the number of cycles to failure difference between the two power cycling test methods.**

***Index Terms*—accelerated power cycling test, reliability, on-line monitoring, IGBT, power module, lifetime prediction**

I. Introduction

Reliability concerns related to power semiconductor components have received substantial attention across various applications, including renewable energy systems and traction. The power cycling (PC) test, a widely recognized methodology, plays a crucial role in evaluating the reliability of power semiconductors, with a specific focus on packaging. This accelerated test method induces aging mechanisms by subjecting the devices under test (DUT) to heightened thermal stresses [1]. To date, the DC PC test has been extensively adopted in various reliability standards [2] - [5]. In contrast, the AC PC test, which more closely approximates real operating conditions, has gained increasing attention in recent years [6] - [8]. Comparing these two accelerated testing methods in terms of their effectiveness for lifetime estimation is of natural interest. Studies in references [9] and [10] have compared the experimental results and thermal stress distribution under both methods, confirming no differences in failure modes and only slight differences in the number of cycles to failure. As this comparative analysis between these two test methods is relatively nascent in the literature, further research and additional confirmation are necessary.

Interconnection failures, particularly bond wire lift-off, are the prevalent failures in power modules during PC tests. Comparing bond wire degradation across different PC test methods can be effectively achieved using physical modeling, which allows for a direct description and assessment of the deformation mechanisms involved, numerous studies have utilized the method for estimating bond wire lifetime [11] - [16]. Physical modeling provides deeper insights into the physical processes leading to failure and can also be used to validate the extrapolation of existing empirical models [17]. This makes it particularly suitable for analyzing bond wire degradation across different power cycling tests.

The purpose of this paper is to present the differences in power cycling test results for an IGBT power module under DC and AC conditions and to analyze bond wire degradation using physical modeling. A simplified thermo-mechanical model has been developed to assess temperature distribution, stress, and strain under accelerated conditions, providing explanations for the observed differences in experimental results. Additionally, the effects of heating time, temperature gradient, and current density are explored, with a discussion on their impacts on lifetime prediction, which requires further investigation.

II. Methodology

DC and AC PC tests are conducted using a versatile power cycling tester under different temperature swings. The operating principles and a detailed description of the setup can be found in [18]. Bond wire lift-off is identified as the primary failure mechanism. Subsequently, a simple Coffin-Manson model is developed to correlate the number of cycles to failure, N_f, with the temperature swing, ΔT (=T_{max}-T_{min}).

$$N_f = A \cdot (\Delta T)^{-m} \tag{1}$$

where A and m are empirical constants within the model. With limited experimental results available, the AC PC tests exhibit an evident larger N_f at both ΔT=80K and ΔT=100K conditions compared to the DC PC tests.

A 3D thermo-mechanical finite element model (FEM) simulation is conducted to offer a more comprehensive physical description of the observed failure mechanism and to validate the lifetime model. Firstly, an electrical circuit model is developed to simulate the operating conditions of each PC test. By maintaining consistent values for ΔT, T_{max}, t_{on} and t_{off}, the estimated power losses of the DUT are imported into the FEM model for thermal modeling. The temperature profiles generated in the thermal model serve as inputs for the mechanical simulation. This approach estimates the stress-strain development at the bond wire-chip interface, which can serve as an indicator of the number of cycles to failure.

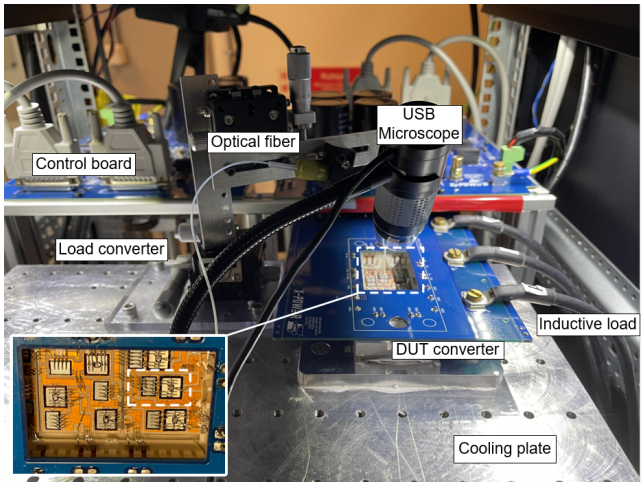


Fig. 1. DUT instrumented with optical fiber for power cycling.

III. Experimental Results

IGBT power module FP50R12KT4 (1200V-50A) from Infineon has been chosen to perform both DC and AC PC tests. In both tests, the failure criterion is set as a 5% increase of the on-state voltage as the primary failure mechanism identified is the bond wire lift-off. During the power cycling, the junction temperature is directly measured using optical fiber at a sampling frequency of 1kHz. Both DC and AC PC tests are conducted on the same setup (shown in Fig. 1), ensuring consistency in the junction temperature measurement method.

The testing conditions for the PC tests are outlined as follows:

TABLE I
DC PC TEST PARAMETER SPECIFICATIONS

Parameter	Value
Gate Voltage	12 V
Load Current	40/48/57 A
Fundamental Frequency	0.25 Hz
Duty Cycle	0.5
Maximum Junction Temperature	150 °C
Temperature Swing	60/80/100 K

TABLE II
AC PC TEST PARAMETER SPECIFICATIONS

Parameter	Value
Bus Voltage	400 V
Gate Voltage	15 V
Inductor Current (peak)	34 A
Inductive Load	0.42 mH
Gate Resistance	33 Ω
Switching Frequency	13/15 kHz
Fundamental Frequency	0.25 Hz
Duty Cycle	0.5
Power Factor	-1
Maximum Junction Temperature	150 °C
Temperature Swing	80/100 K

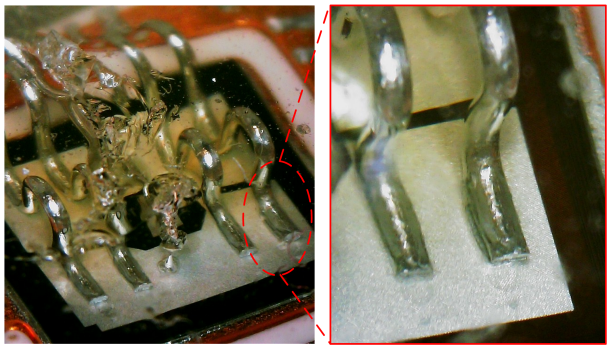


Fig. 2. Main failure mechanism under DC and AC PC tests: bond wire lift-off.

Several modules underwent visual inspection using a digital microscope for failure analysis. For DUT subjected to DC power cycling, only bond-wire lift-off is observed. In another DUT that failed during the AC power cycling test, a gate-emitter short occurred due to a local hotspot around the non-lifted bond wires. Both burnout and bond wire lift-off are identified. To facilitate post-failure analysis, the test will be stopped for both DC and AC PC when a 5% increase in V_{CE} is reached.

The Weibull percentile plots for samples tested under DC and AC PC are depicted in Fig. 3 and Fig. 4, respectively. Within a 60% confidence interval, for DC PC tests, under both ΔT=80K and ΔT=100K conditions, the bounds of the upper and lower percentiles remain relatively narrow, while for the AC PC, with a limited number of tested samples, the scattering of cycles to failure is still no more than 25% around the mean value. The statistical assessment of the power cycling results is conducted by fitting the failure data to Weibull statistics using the maximum likelihood estimation method, implemented in Minitab 21 Statistical Software.

With consistent T_{max}, t_{on} and t_{off}, the correlation between the number of cycles to failure N_f and ΔT =80K and 100K is depicted in the Coffin-Manson plot in Fig. 5. One DC PC test with a temperature swing of 60K was also conducted, and

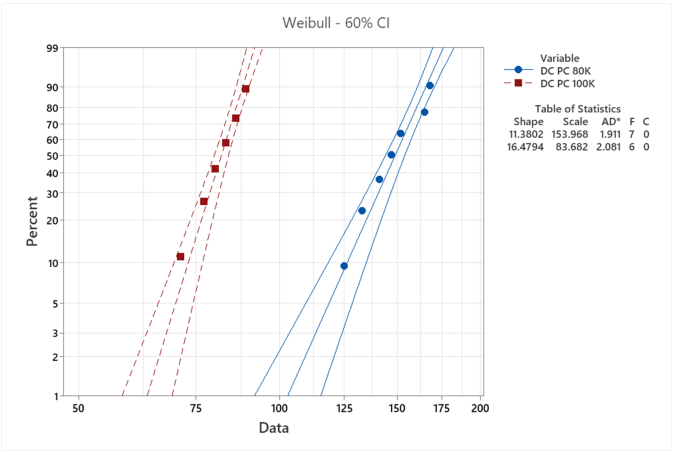


Fig. 3. Weibull plot for DC PC test results.

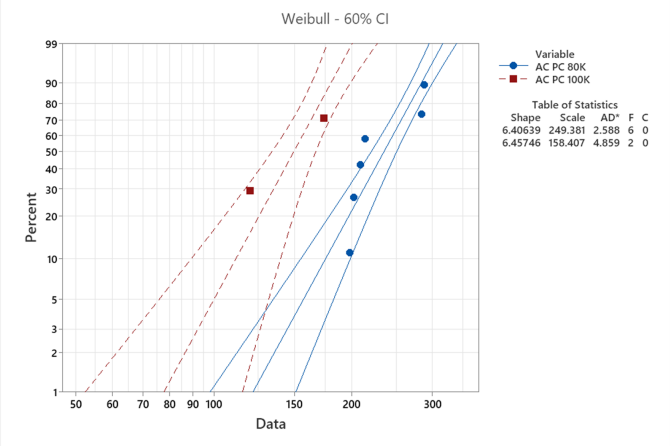


Fig. 4. Weibull plot for AC PC test results.

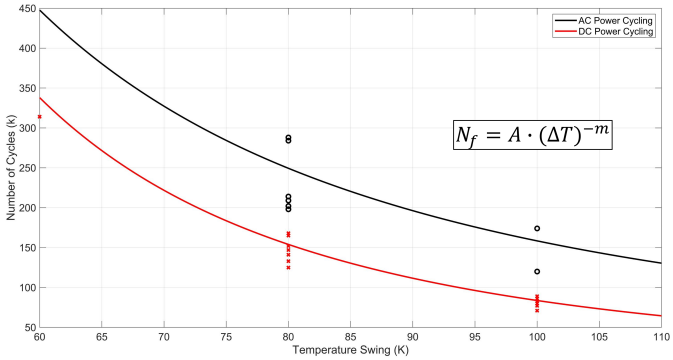


Fig. 5. Coffin-Manson plot for DC and AC PC tests.

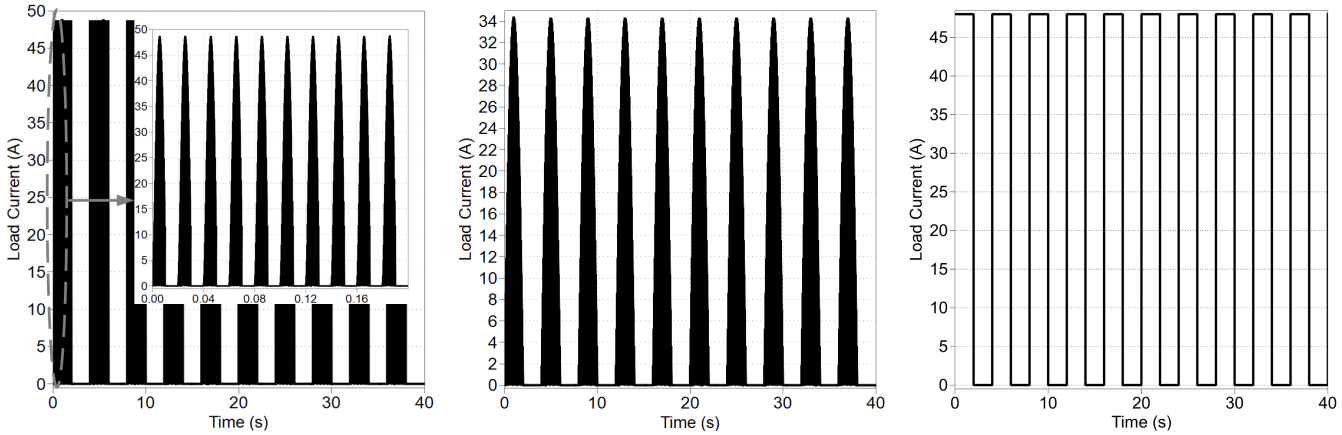
its N_f aligns with the expected lifetime plot for DC PC tests. It is also noted that as ΔT increases from 80K to 100K, the difference between the N_f correspondingly enlarges.

IV. Simulation Results

The power cycling simulation begins with using the Piecewise Linear Electrical Circuit Simulation (PLECS) to estimate power losses under the testing conditions outlined in the previous experimental section. One more condition (AC PC, f_0=50Hz) is added up to showcase the difference within the AC PC test methods. Under the condition of ΔT = 80K, T_{max} =150°C, t_{on}=t_{off}=2s, the load currents and the corresponding temperature swings are depicted in Fig. 6 and Fig. 7, respectively. It is clear that for both DC PC (f_0=0.25Hz) and AC PC (f_0=50Hz), when current is injected, the chip's junction temperature rises rapidly and reaches the T_{max} at the end of the on period. Conversely, for AC PC at a lower frequency (f_0=0.25Hz), the junction temperature increases more slowly and reaches T_{max} before the end of the on period. Consequently, it is naturally of interest to evaluate the differences in the degree of cyclic damage incurred in the aluminum associated with these varied temperature profiles.

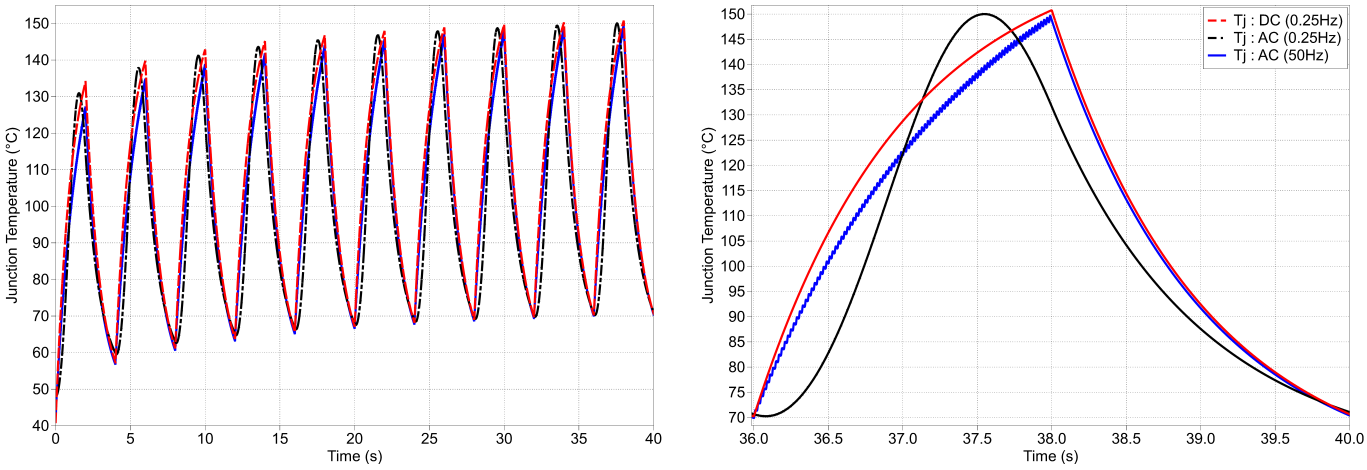
The commercial multiphysics FEM software, COMSOL, has been used for the simulations. Power losses estimated from the PLECS model are applied to the IGBT chips under two loading conditions: DC PC and AC PC with f_0=0.25Hz. Since the simulation primarily aims to validate the differences in bond wire degradation between DC and AC PC tests, the model has been simplified to include only thermo-mechanical aspects. The effects of Joule heating of the bond wire are omitted, and the power module is not modeled at full scale. Focusing on bond wire degradation, which experiences stress under cyclic loading due to coefficient of thermal expansion (CTE) mismatch, the aluminum bond wire is modeled as an elasto-plastic material with isotropic hardening. The material properties used in the simulation is obtained from [13].

The investigation of stress and strain at the bond wire-chip interface is crucial, as experimental evidence suggests that delamination often occurs just above the interface to the bond pad [19]. In Fig. 9, the von Mises stress and the equivalent plastic strain are plotted over time at the most stressed point



(a) AC PC, f_0=50Hz. (b) AC PC, f_0=0.25Hz. (c) DC PC, f_0=0.25Hz.

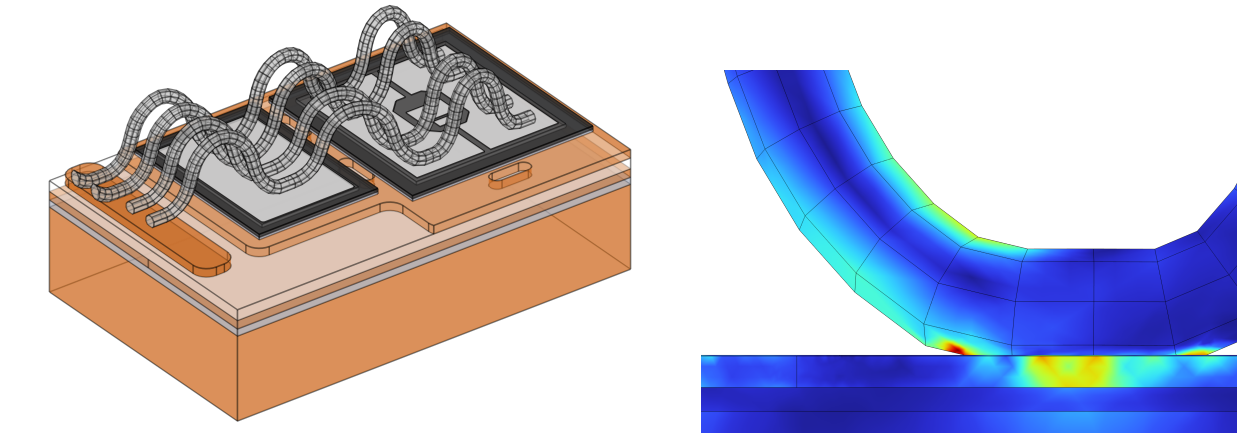
Fig. 6. Applied load currents at varied fundamental frequencies for PC tests (dT=80K).



(a) Thermal equilibrium reached after ten cycles.

(b) Temperature evolution within one cycle.

Fig. 7. Temperature swings at varied fundamental frequencies during DC and AC PC tests.



(a) A section of the IGBT power module featuring 400μm diameter bond wires.

(b) The most stressed point on the bond wire-chip interface was chosen for stress and strain evaluation.

Fig. 8. Thermo-mechanical FEM modeling.

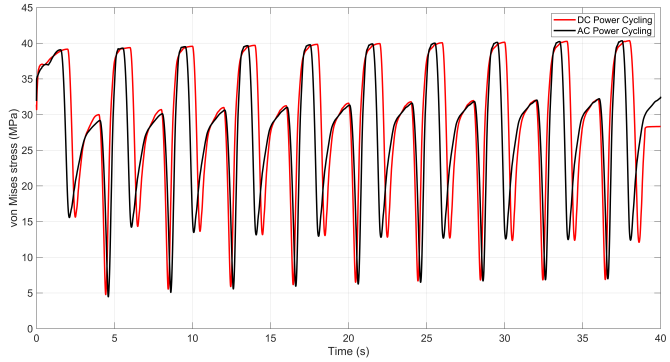
on the bond wire-chip interface. Given that equivalent plastic strain is widely used as a key parameter for reliability analysis, Fig. 9(b) clearly shows that there is a higher degree of deformation under DC PC compared to AC methods. The bond wire under AC PC exhibits less overall plastic strain. In terms of reliability analysis, this difference could indicate an advantage in the number of cycles to failure, potentially validating the experimental results. However, a precise quantitative analysis of N_f under both methods using the equivalent plastic strain requires accurate material properties, comprehensive power module modeling (including thermal coupling effects), bond wire Joule heating effects, etc, which exceeds the scope of this paper and is reserved for future work.

V. Discussion

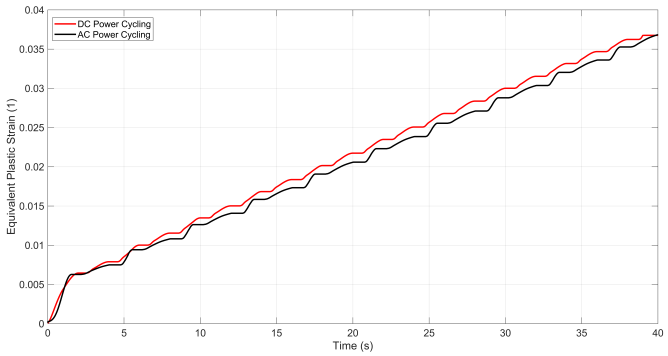
The FEM simulation results have confirmed the difference in bond wire degradation under DC and AC power cycling. However, the underlying causes of the varying lifetimes observed with these two testing methods still warrant further discussion. The factors to consider include:

A. Heating Time

In many standards like AQG 324 [5], t_{on} is defined as the on-time of the load current, or the period during which power losses are generated in the device. However, for AC PC tests with a low fundamental frequency (e.g., 0.25Hz), the heating time (steady junction temperature rise) is observed to be shorter than t_{on}. From a physical modeling perspective, longer stress duration (heating time) results in greater deformations per cycle, leading to shorter lifetimes. This mechanism may



(a) Maximum von Mises stress development on the bond wire-chip interface.



(b) Equivalent plastic strain around the stress maximum on the bond wire-chip interface.

Fig. 9. Thermo-mechanical FEM simulation results under DC and AC PC.

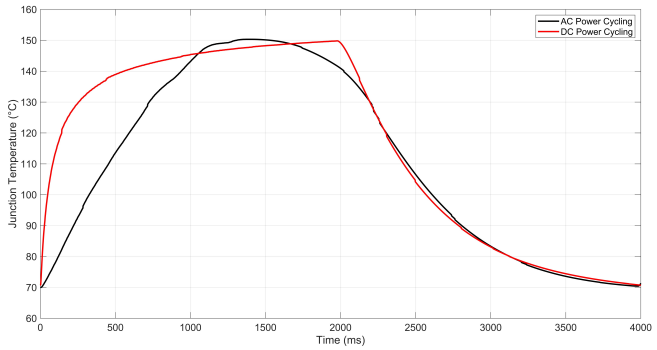


Fig. 10. Temperature evolution on the chip surface measured by optical fiber during DC and AC PC tests (sampling frequency=1kHz).

explain why AC PC tests tend to last longer than DC PC tests under the same temperature swing. In [20], N_f has been given as a function of t_{on} (0.1s<t_{on}<60s), which has been used for N_f compensation. However, given that the actual t_{on} for AC PC is considered to be 1.5s, the compensated N_f remains larger than the results from DC PC.

B. Junction Temperature Gradient

As shown in Fig. 10, the temperature gradient differs between DC PC and AC PC tests. In [21], a thermographic method is utilized to record the temperature rise in the specimen caused by hysteresis heating during fatigue tests. The findings indicate that the initial temperature increase rate over time could be used to predict fatigue life.

C. Current Density

As shown in Fig.6.a and b, the same temperature swing could be achieved under different load currents/current densities. In [22], a strong correlation was found between the power loss density in the bond loop and the tested lifetime across a wide range of load currents.

VI. Conclusions

This study examined the differences in bond wire degradation between DC and AC power cycling tests in IGBT power modules, utilizing a simplified thermo-mechanical model. Variations in equivalent plastic strain confirm the empirical lifetime model discrepancies under DC and AC conditions. Key factors such as heating duration, temperature gradient, and current density, which may contribute to these lifetime differences, are discussed and highlighted for future research.

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