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Secondary Control for Compensation of Voltage Harmonics and Unbalance in Microgrids

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***Abstract*—In this paper, a hierarchical control scheme is proposed for enhancement of Sensitive Load Bus (SLB) voltage quality in microgrids. The control structure consists of primary and secondary levels. The primary control level comprises Distributed Generators (DGs) local controllers. Each of these controllers includes a selective virtual impedance loop which is considered to improve sharing of fundamental and harmonic components of load current among the DG units. The sharing improvement is provided at the expense of increasing voltage unbalance and harmonic distortion. Thus, the secondary control level is applied to manage the compensation of SLB voltage unbalance and harmonics by sending proper control signals to the primary level. DGs compensation efforts are controlled locally at the primary level. The system design procedure for selecting proper control parameters is discussed. Simulation results are provided in order to demonstrate the effectiveness of the proposed control scheme.**

***Index Terms*—Distributed Generator (DG), microgrid, voltage harmonics, voltage unbalance.**

I. Introduction

DISTRIBUTED Generators (DGs) are often connected to the utility grid or microgrid through a power-electronic interface converter. Microgrid is a local grid consisting of DGs, energy storage systems and dispersed loads which may operate in grid-connected or islanded mode [1].

Recently, some control approaches are proposed to control the DG interface converter aiming to compensate power quality problems. A single-phase DG which injects harmonic current to compensate voltage harmonics is presented in [2]. However, in the case of sever harmonic distortion, a large amount of the interface converter capacity is used for compensation and it may interfere with the power supply by the DG.

Harmonic compensation approaches of [3]-[5] are based on making the DG units of a power distribution system emulate a resistance at harmonic frequencies. Moreover, a method for compensation of voltage harmonics in an islanded microgrid has been presented in [6]. This method is also based on the resistance emulation and applies a harmonic power droop characteristic in order to share the compensation effort among DGs.

The approach presented in [7] is based on controlling each DG unit of a microgrid as a negative sequence conductance to compensate voltage unbalance. The conductance reference is determined by applying a droop characteristic which uses negative sequence reactive power to provide the compensation effort sharing. The control system of [7] is implemented in *dq* (synchronous) reference frame while [8] addresses the voltage unbalance compensation using $\alpha\beta$ (stationary) frame control.

The control method presented in [9] is based on using a two-inverter interface converter (one connected in shunt and the other in series with the grid) in order to control power flow and also to compensate the voltage unbalance. This two-inverter structure can be unattractive considering the cost and volume of the DG interface converter.

In addition, it should be noted that the methods presented in [3]-[8] are designed to enhance voltage quality at the DG terminal while the power quality at the "Sensitive Load Bus (SLB)" is an important concern in microgrids.

Furthermore, if the voltage distortion is compensated locally, it may be amplified in the other buses of the electrical system including the SLB. This phenomenon is called "whack-a-mole" in the case of harmonic distortion [10].

As the first step to address these concerns, the authors proposed a hierarchical control scheme for direct compensation of fundamental voltage unbalance at SLB of a microgrid where the unbalance was originated from linear unbalanced loads [11]. In the present paper, this scheme is extended considering unbalanced harmonic distortion caused by nonlinear unbalanced loads. In this case, the negative sequence of fundamental component (which creates SLB fundamental voltage unbalance) as well as positive and negative sequences of SLB voltage main harmonics should be compensated.

In the applied hierarchical structure, the central secondary control level manages the compensation by sending proper control signals to the primary level. The sharing of compensation effort among the DGs is controlled locally at the primary level. By sharing the compensation effort, the load current will not necessarily be shared properly, especially, in the microgrids which are noticeably asymmetrical in terms of the line impedances and/or loads distribution. Thus, a selective virtual impedance loop is proposed for each DG unit to improve the load sharing.

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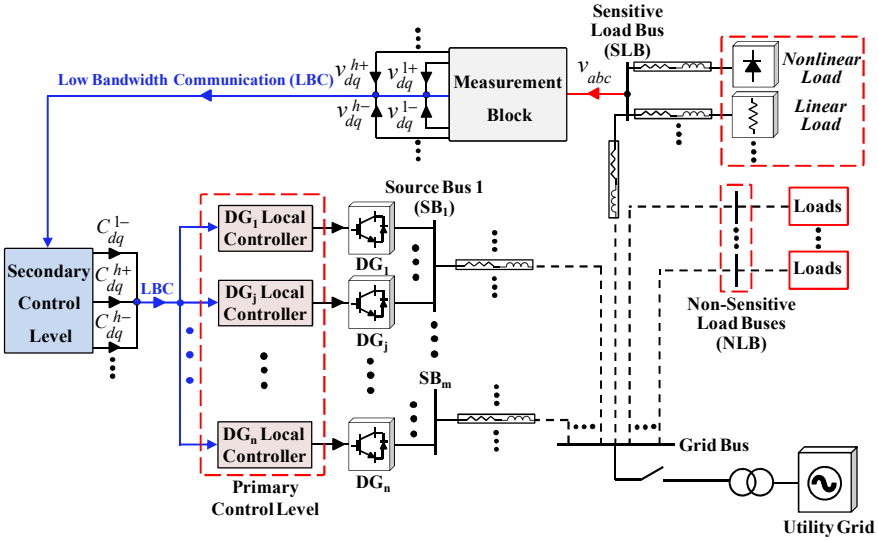

Fig. 1. Hierarchical control scheme for a general microgrid.

II. Microgrid Hierarchical Control Scheme

Fig. 1 shows application of the proposed hierarchical control scheme to a general microgrid which includes a number of electronically-interfaced DGs connected to the Source Buses (SB). Each DG unit may consist of power generators and/or energy storage systems. Furthermore, some dispersed loads including balanced/unbalanced linear and nonlinear loads are connected to the Load Buses including SLB and Non-Sensitive Load Buses (NLB). The hierarchical scheme consists of two control levels. The primary level comprises DG local controllers and the secondary level is a central controller which sends proper reference signals to each of the DGs in order to reduce the voltage unbalance and harmonic distortion at the microgrid SLB to the required level.

The secondary controller can be far from DGs and SLB. Thus, as shown in Fig. 1, SLB voltage information is sent to this controller by means of low bandwidth communication (LBC). Low bandwidth is applied to avoid dependence on the availability of a high bandwidth which may endanger the system reliability. In order to ensure LBC adequacy, positive and negative sequences of SLB voltage fundamental and main harmonic components are extracted in *dq* frame and the resultant dc values are transmitted to the secondary controller. In Fig. 1, superscripts "+", "–", "1" and "*h*" represent positive sequence, negative sequence, fundamental component and h^{th} harmonic component, respectively. For instance, v_{dq}^{h+} is the positive sequence of h^{th} harmonic voltage in *dq* frame. The details of voltage components extraction are depicted in "*Measurement Block*" of Fig. 2. As seen, in order to extract v_{dq}^{1+}, v_{dq}^{1-}, v_{dq}^{h+} and v_{dq}^{h-}, at first, the measured three-phase voltage of SLB (v_{abc}) is transformed to *dq* reference frames rotating at ω, $-\omega$, $h\omega$ and $-h\omega$, respectively. ω is the system angular frequency estimated by a phase-locked loop (*PLL*) [12]. Afterwards, three second-order 5Hz low pass filters (*LPF*) are applied. The second-order filters are used since the first-order ones were not able to provide acceptable performance.

On the other hand, as shown in Figs 1 and 2, compensation references for fundamental component unbalance and h^{th} harmonic positive and negative sequences (C_{dq}^{1-}, C_{dq}^{h+}, and C_{dq}^{h-}, respectively) which are also in *dq* frame are generated by the secondary controller and sent to the DGs local controllers using LBC. As shown in Fig. 2, these references are fed to "*Compensation Effort Controller*" block of each DG local controller and the outputs ($C_{dq,j}^{1-}$, $C_{dq,j}^{h+}$ and $C_{dq,j}^{h-}$ as the compensation references for DG_j) are transformed to $\alpha\beta$ frame, added together and injected as a reference for the DG voltage controller. The rotation angles of transformations are set to $-\phi^*$, $h\phi^*$ and $-h\phi^*$ for the compensation references of voltage unbalance and positive and negative sequences of h^{th} voltage harmonic, respectively. ϕ^* is the DG voltage reference phase angle generated by the active power controller [11].

It should be noted that the harmonic and also unbalance variations in the practical grids are usually slow [13]. Thus, it is not necessary to provide a very fast control action. This fact confirms the sufficiency of LBC for the proposed compensation approach. On the other hand, low communication bandwidth can be provided at a relatively low cost.

The total time needed to transmit the measured and control signals between control levels and to perform the required control actions depends on the data size, bandwidth and delay of communication and also the processing time of the measurement and control devices [14].

Fig.1 is depicted assuming one SLB in the microgrid. However, in the case of multiple SLBs, the microgrid can be divided to some control regions that each has a dedicated secondary controller and includes one SLB. Each secondary controller manages the voltage quality enhancement at the corresponding SLB by sending control signal to the DG units of the region.

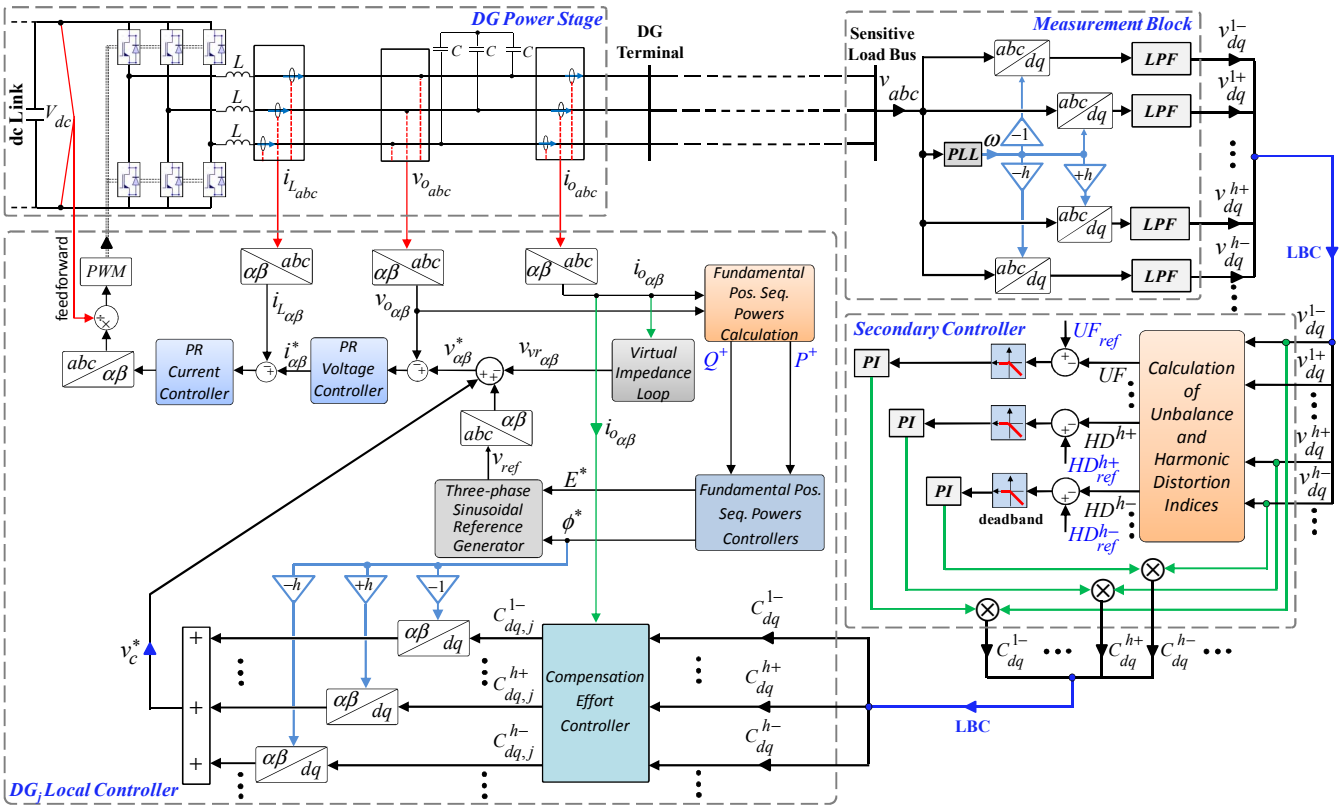

Fig. 2. Detailed block diagram of the control system.

It is also noteworthy that the proposed control approach is applicable for voltage quality enhancement in both grid-connected and islanded modes of microgrid operation. It is only necessary to make the necessary changes to the power controllers of DG units depending on the operation mode.

III. DG Local Control System

The structure of each DG power stage and local controller is shown in Fig. 2. As it can be seen, a feedforward loop may be included to consider small variations of dc link voltage (V_{dc}).

The local control of DGs is performed in $\alpha\beta$ reference frame. As shown in "*DG$_j$ local controller*" block, the reference of the DG output voltage in $\alpha\beta$ frame ($v^*_{\alpha\beta}$) is provided by power controllers, virtual impedance loop and compensation effort controller. Then, according to $v^*_{\alpha\beta}$ and the instantaneous measured output voltage ($v_{o_{\alpha\beta}}$), the reference current ($i^*_{\alpha\beta}$) is generated. On the other hand, LC filter inductor current is measured, transformed to $\alpha\beta$ frame ($i_{L_{\alpha\beta}}$) and controlled by the current controller to provide voltage reference for pulse width modulator (*PWM*).

A. Fundamental Positive Sequence Powers Controllers

Control of the active and reactive powers is performed assuming a mainly inductive microgrid. The power controllers determine the reference values of DGs output voltage phase angle and amplitude (ϕ^* and E^*, respectively) considering the operation mode of microgrid, i.e. islanded or grid connected. Design of the power controllers is sufficiently studied in the literature (e.g., [15],[16]) and will not be discussed.

B. Voltage and Current Controllers

The following proportional-resonant (PR) voltage and current controllers are applied in this paper.

$$G_V(s) = k_{pV} + \sum_{k=1,3,5,7} \frac{2k_{rVk}\cdot\omega_{cV}\cdot s}{s^2 + 2\cdot\omega_{cV}\cdot s + \left(k\cdot\omega_0\right)^2} \quad (1)$$

$$G_I(s) = k_{pI} + \sum_{k=1,3,5,7} \frac{2k_{rIk}\cdot\omega_{cI}\cdot s}{s^2 + 2\cdot\omega_{cI}\cdot s + \left(k\cdot\omega_0\right)^2} \quad (2)$$

where k_{pV} (k_{pI}) and k_{rVk} (k_{rIk}) are the proportional and k^{th} harmonic (including fundamental component as the first harmonic) resonant coefficients of the voltage (current) controller, respectively. ω_{cV} and ω_{cI} represent voltage and current controllers cut-off frequencies, respectively.

In order to design these controllers, the closed-loop transfer function of local control system is extracted [8]. Bode diagram of this transfer function using the power stage and local controller parameters (Tables I and II) is depicted in Fig. 3. As seen, the gain and phase angle at the resonant frequencies are fixed at unity and zero, respectively. Thus, proper tracking of the voltage reference is ensured.

The output impedance of the interface inverter can be expressed as $Z_o(s) = Z'_o(s) + Z_{vr}(s)$ where $Z_{vr}(s)$ represents the virtual impedance and $Z'_o(s)$ is the inverter output

impedance without addition of the virtual impedance [8]. Fig. 4 shows $Z'_o(s)$ magnitude plot of DG units. It can be observed that the magnitude is approximately zero at fundamental and 3rd, 5th and 7th harmonic frequencies.

C. Virtual Impedance Loop

The block diagram of the virtual impedance is depicted in Fig. 5 where R_{vr}^{1+}, R_{vr}^{1-} and R_{vr}^{h} represent the virtual resistance for fundamental positive sequence, fundamental negative sequence and h^{th} harmonic (both positive and negative sequences) components of DG output current, respectively. L_{vr} and ω_0 are respectively the virtual inductance against fundamental positive sequence current and the rated frequency. In order to provide proper control of fundamental positive sequence powers, the microgrid is made more inductive by including L_{vr}. However, a small R_{vr}^{1+} is added to damp the system oscillations [15],[17].

The basic structure of the fundamental frequency virtual impedance has been proposed in [18]. Moreover, it is demonstrated in [17], [19] and [20] that the virtual impedance can improve the sharing of nonlinear (harmonic) load among parallel converters. Hence, the basic structure is extended by including virtual resistances for the fundamental negative sequence (R_{vr}^{1-}) and the main harmonic components (R_{vr}^{h}, h=3, 5 and 7) of the DG output current in order to improve the sharing of these current components. Output current components are extracted according to [21] and [22].

The sharing improvement is achieved at the expense of distorting DGs output voltage as a result of voltage drop on the virtual resistances. Thus, for selection of virtual resistance values, a trade-off should be considered between the amount of output voltage distortion and sharing accuracy. Furthermore, considering double rating of DG_1 in the studied microgrid, its virtual impedances at fundamental and harmonic frequencies are set at half value to improve the current sharing (see Table II).

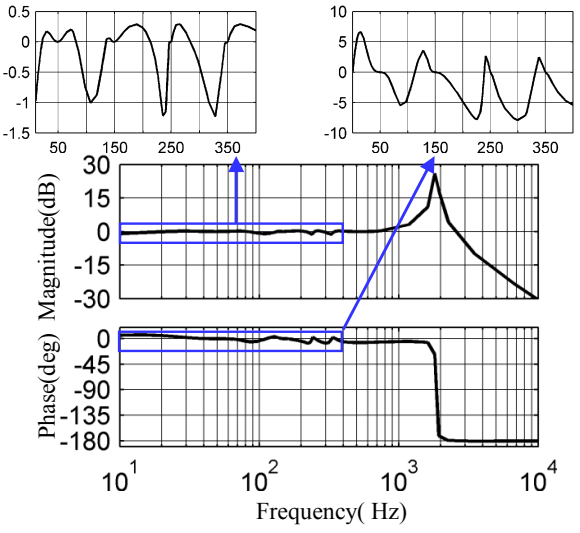

Fig. 3. Bode diagram of closed loop transfer function.

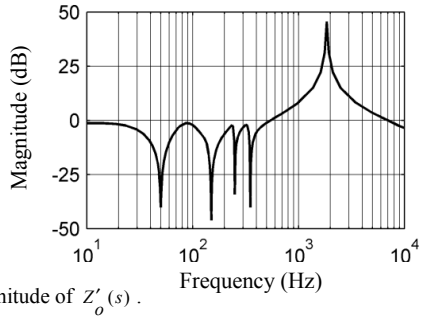

Fig. 4. Magnitude of $Z'_o(s)$.

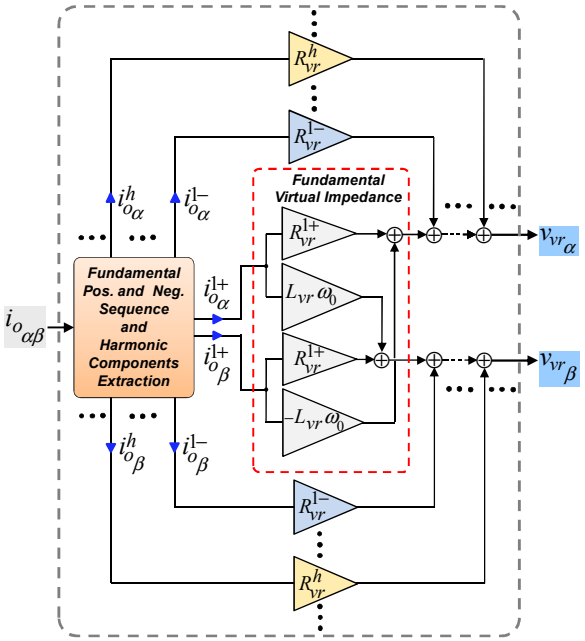

Fig. 5. Block diagram of selective virtual impedance.

D. Compensation Effort Controller

The compensation effort controller manages the sharing of compensation workload among the microgrid DGs. The block diagram of DG_j effort controller is shown in Fig. 6. As seen, DG unit output current in $\alpha\beta$ frame ($i_{o\,\alpha\beta}$) is fed to this controller and positive and negative sequences of its α-axis fundamental component ($i_{o_\alpha}^{1+}$ and $i_{o_\alpha}^{1-}$) and h^{th} harmonic component ($i_{o_\alpha}^{h+}$ and $i_{o_\alpha}^{h-}$) are extracted. Then, $i_{o_\alpha}^{1+}$, $i_{o_\alpha}^{1-}$, $i_{o_\alpha}^{h+}$ and $i_{o_\alpha}^{h-}$ are applied to calculate current unbalance factor (UF_I) and harmonic distortion indices of h^{th} harmonic positive and negative sequences (HD_I^{h+} and HD_I^{h-}, respectively). UF_I, HD_I^{h+} and HD_I^{h-} are calculated as the ratio of $i_{o_\alpha}^{1-}$, $i_{o_\alpha}^{h+}$ and $i_{o_\alpha}^{h-}$ *rms* values ($I_{o_\alpha}^{1-}$, $I_{o_\alpha}^{h+}$ and $I_{o_\alpha}^{h-}$, respectively) to *rms* value of $i_{o_\alpha}^{1+}$ ($I_{o_\alpha}^{1+}$), respectively. Note that using β-components for calculation of unbalance and harmonic distortion indices leads to the same results because the magnitude of α- and β-components is equal for both positive and negative sequences of fundamental and harmonic components.

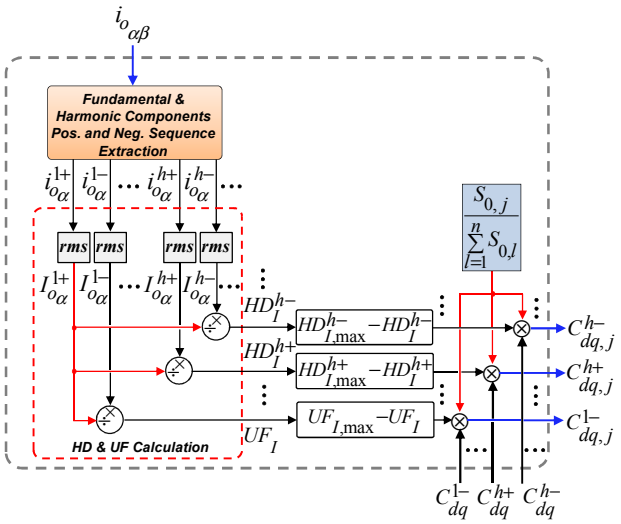

Fig. 6. Block diagram of compensation effort controller of DG_j.

Finally, the references for compensation of fundamental unbalance and h^{th} harmonic positive and negative sequences by DG_j ($C_{dq,j}^{1-}$, $C_{dq,j}^{h+}$ and $C_{dq,j}^{h-}$, respectively) are calculated as shown in Fig. 6 where $S_{0,j}$ is the rated capacity of DG_j and subscript "max" represent the maximum value. By multiplying the ratio of DG_j rated capacity ($S_{0,j}$) to the total capacity of the microgrid DGs ($\sum_{l=1}^{n} S_{0,l}$), compensation effort of each DG will be proportional to its rated capacity.

UF_I, HD_I^{h+} and HD_I^{h-} can be considered as the indices of compensation effort because as shown in the simulation results, compensation of SLB voltage unbalance and h^{th} harmonic positive and negative sequences is achieved through injecting corresponding current components by the DGs. Thus, the terms $\left(UF_{I,\max}-UF_I\right)$, $\left(HD_{I,\max}^{h+}-HD_I^{h+}\right)$ and $\left(HD_{I,\max}^{h-}-HD_I^{h-}\right)$ in Fig. 6 contribute towards sharing of compensation effort. In fact, increase of each component compensation effort leads to the increase of corresponding index. Consequently, $\left(UF_{I,\max}-UF_I\right)$, $\left(HD_{I,\max}^{h+}-HD_I^{h+}\right)$ or $\left(HD_{I,\max}^{h-}-HD_I^{h-}\right)$ decrease and it leads to compensation effort decrease. So, inherent negative feedbacks exist in the effort controller. It is assumed that the maximum values of unbalance factor and harmonic distortion indices are unity. This assumption is valid for most of the practical cases; however, larger constants can be used as the maximum values.

IV. Secondary Controller

The block diagram of the secondary controller is also shown in Fig. 2. As seen, *dq* components of SLB voltage fundamental positive and negative sequences (v_{dq}^{1+} and v_{dq}^{1-}) and h^{th} harmonic positive and negative sequences (v_{dq}^{h+} and v_{dq}^{h-}) are used to calculate voltage unbalance factor (UF) and h^{th} harmonic positive and negative sequence distortion indices (HD^{h+} and HD^{h-}, respectively). Calculation block is similar to "*HD&UF Calculation*" block of Fig. 6. Then, UF, HD^{h+} and HD^{h-} are compared with the reference values (UF_{ref}, HD_{ref}^{h+} and HD_{ref}^{h-}, respectively) and the errors are fed to proportional-integral (PI) controllers. Afterwards, the outputs of these controllers are multiplied by v_{dq}^{1-}, v_{dq}^{h+} and v_{dq}^{h-} to generate C_{dq}^{1-}, C_{dq}^{h+} and C_{dq}^{h-}, respectively. If the unbalance factor or any of the harmonic distortion indices are less than the reference value, the respective deadband block prevents the increase of the distortion by the PI controller.

It is well known that with the increase of proportional coefficient of PI controllers, the response time is reduced, but, the control system becomes more prone to instability. On the other hand, in order to minimize the effect of PI controllers phase lag on the compensation performance, the corner angular frequency of these controllers which can be calculated as the ratio of integral to proportional coefficients, should be set at one decade or more below the frequency of under-compensation component [13]. Harmonic and unbalance variations are usually slow; thus, it is not necessary to apply high bandwidth PI controllers.

Here, secondary level comprises PI controllers for compensation of SLB voltage fundamental negative sequence and 3rd, 5th and 7th harmonic components. The parameters of PI controllers are listed in Table III.

V. Simulation Results

Fig. 7 shows the simulation test system which is a two-DG islanded microgrid comprising two source buses, one sensitive load bus and one non-sensitive load bus. A diode rectifier and a star-connected linear load are connected to SLB. It is assumed that one phase of nonlinear load is disconnected to create unbalanced voltage distortion. Furthermore, a balanced nonlinear load is connected to NLB. Switching frequency of the DGs inverters is 10 kHz. The test system parameters are listed in Table I. Note that in this Table, the impedances of linear load and lines are presented in terms of resistance (Ω) and inductance (mH). Simulations are performed using *MATLAB/Simulink*. Three simulation steps are considered:

- Step 1 ($0 \le t < 2s$)
  DGs operate only with fundamental positive sequence virtual impedance and secondary control is not acting.
- Step 2 ($2 \le t < 4s$)
  Virtual resistances for fundamental negative sequence and harmonic components are added.
- Step 3 ($4 \le t < 7s$)
  Secondary control is activated. The reference values of unbalance factor and harmonic distortion indices are 0.2%.

As seen in Table IV, before activating the virtual resistances for fundamental negative sequence and harmonic com-

ponents, DGs output voltages are approximately free of distortion. This fact can also be observed in Fig. 8 as the low values of UF and HD^{3-} before t=2s. It demonstrates the effectiveness of local controllers in tracking the voltage reference. But, as shown in Table IV and Fig. 8, SLB voltage is distorted noticeably due to voltage drops on distribution lines. It should be noted that in order to avoid excessive length, simulation results of other distortion indices are not included.

Table V shows negative sequence single-phase waveforms at fundamental and 3rd harmonic frequencies as well as three-phase waveforms of DGs output current in different simulation steps. Considering double rating of DG_1, it can be noticed from Table V that the load current is not properly shared in the first simulation step. In fact, all components of the load current except fundamental positive sequence one are shared according to the test system topology and before adding R_{vr}^{1-}, R_{vr}^{3}, R_{vr}^{5} and R_{vr}^{7}, DG_2 will supply larger portions of the fundamental negative sequence and the harmonic currents. As mentioned before, fundamental positive sequence component of the load is shared by using droop controllers. Fig. 9 demonstrates the proper sharing of P^+ and Q^+ between DGs throughout the under-study interval. It demonstrates the effectiveness of the droop controllers.

In simulation Step 2, virtual resistances for fundamental negative sequence and harmonic components are added. As seen in Table V, the current sharing is improved noticeably; however, still is not in proportion to the DGs rated powers. The sharing improvement is achieved at the expense of voltage distortion increase at DGs terminals and consequently at SLB, as can be observed in Table IV and Fig. 8. On the other hand, it can be seen in Fig. 9 that the addition of these virtual resistances leads to the change of fundamental positive sequence powers. In fact, due to nonlinear nature of the diode rectifiers, fundamental positive sequence component cannot be considered completely decoupled from the other components.

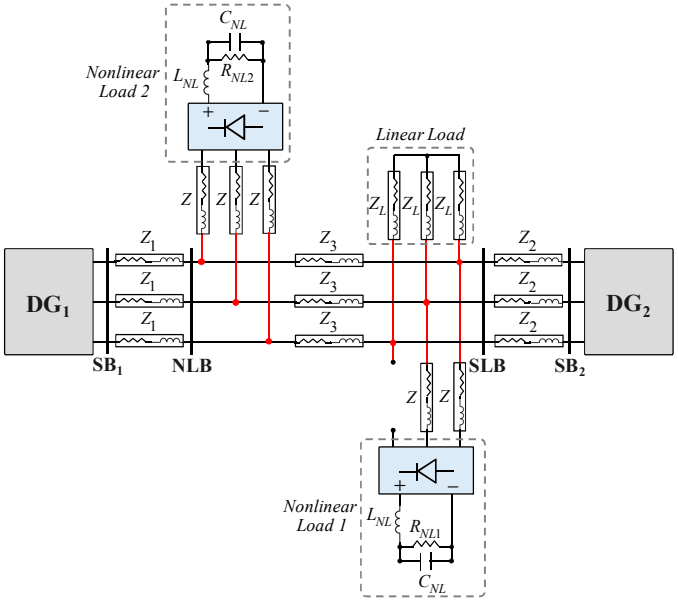

Fig. 7. Test system for simulation studies.

In the last simulation step, selective compensation of SLB voltage main harmonics and fundamental negative sequence component is activated at t=4s. As seen in Fig. 8, UF and HD^{3-} track the reference values properly. The other harmonic components which are not shown in this paper show the same behavior. Consequently, SLB voltage quality is significantly improved as seen in Table IV.

TABLE I
POWER STAGE PARAMETERS

dc link voltage	LC Filter Inductance	LC Filter Capacitance	Nonlinear Loads Tie Lines
V_{dc} (V)	L (mH)	C (μF)	Z (Ω,mH)
650	1.8	25	0.1, 1.8
Distribution Lines	Nonlinear Loads		Linear Load
Z_1,Z_2,Z_3 (Ω,mH)	$C_{NL}/R_{NL1},R_{NL2}/L_{NL}$ (μF)/(Ω)/(mH)		Z_L (Ω,mH)
0.1,1.8	235/50,200/0.084		50,20

TABLE II
DGS LOCAL CONTROLLER PARAMETERS

Power Controllers (DG_1/DG_2) [11]					
m_D (rad/W)		m_P (rad/W.s)		n_P (V/VAr)	
$0.6\times10^{-5}/1.2\times10^{-5}$		$0.6\times10^{-4}/1.2\times10^{-4}$		$1.4\times10^{-1}/2.8\times10^{-1}$	
Virtual Impedance (DG_1/DG_2)					
R_{vr}^{1+} (Ω)	L_{vr} (mH)	R_{vr}^{1-} (Ω)	R_{vr}^{3} (Ω)	R_{vr}^{5} (Ω)	R_{vr}^{7} (Ω)
0.3/0.6	2.5/5	1.5/3	2/4	4/8	4/8
Voltage/Current Controller					
k_{pV}/k_{pI}	k_{rV1}/k_{rI1}	k_{rV3}/k_{rI3}	k_{rV5}/k_{rI5}	k_{rV7}/k_{rI7}	ω_{cV}/ω_{cI} (rad/s)
1/5	100/1000	200/400	50/100	100/100	2/2

TABLE III
SECONDARY PI CONTROLLERS PARAMETERS

Fundamental Negative Sequence		3rd Harmonic Positive and Negative Sequences	
proportional	integral	proportional	integral
3	90	1.25	110
5th Harmonic Positive and Negative Sequences		7th Harmonic Positive and Negative Sequences	
proportional	integral	proportional	integral
1	150	0.95	200

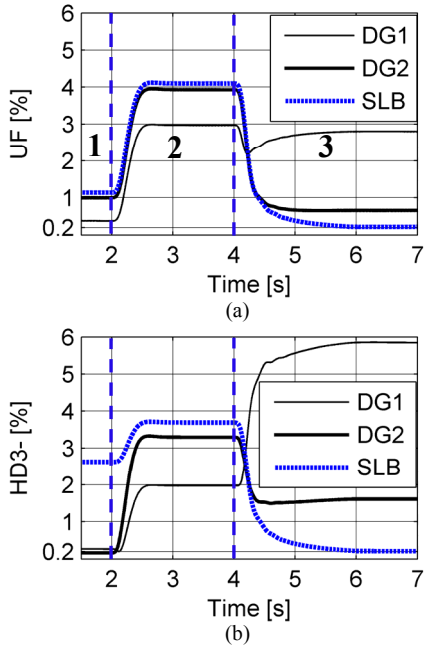

Fig. 8. (a) DGs and SLB voltage unbalance factor, (b) DGs and SLB voltage distortion index for 3rd harmonic negative sequence.

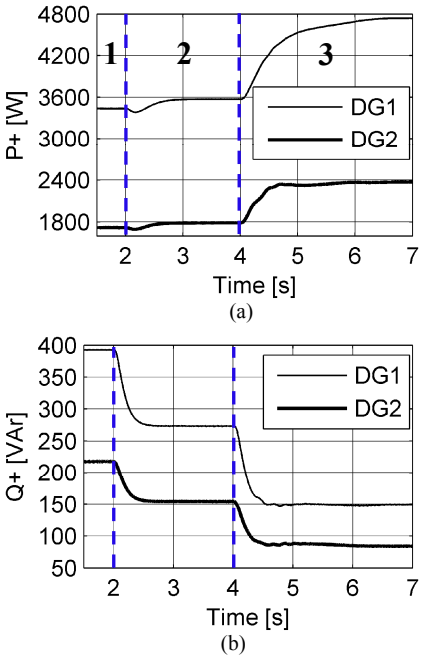

Fig. 9. DGs positive sequence output powers: (a) P^+, (b) Q^+.

Moreover, as observed in Table V, fundamental negative sequence and 3rd harmonic negative sequence of DGs output current increase to provide compensation. The same behavior has been achieved for other harmonic components. The increase of these current components leads to the increase of DGs output current as shown in Table V. However, due to double capacity, the increase of DG_1 current is significantly higher. In addition, it can be observed that the current sharing is noticeably improved after compensation activation. This fact reveals the effectiveness of the proposed compensation effort controller and virtual impedance loop.

Furthermore, it can be observed in Table IV that the compensation is achieved by the increase of DG_1 output voltage distortion. Note that the impedance of the distribution line between SB_1 and SLB is relatively high; also, the fundamental negative sequence and harmonic components of the load which are supplied by this DG are approximately twice of the amounts of DG_2. Thus, in order to compensate the voltage drops on the lines and the virtual resistances and provide approximately sinusoidal voltage at SLB, DG_1 output voltage becomes noticeably distorted. On the other hand, due to low value of the line impedance between SB_2 and SLB and also lower load portion of DG_2, the distortions of SLB and DG_2 voltages change with a similar behavior.

Moreover, it can be seen in Fig. 9 that active and reactive powers change as a result of compensation. As mentioned before, it is originated from coupling between fundamental positive sequence and other components.

VI. Conclusions

A hierarchical control structure consisting of primary and secondary levels is proposed for microgrids. The secondary level controls selective compensation of SLB voltage fundamental negative sequence and positive and negative sequences of main harmonics by sending proper control signals to the primary level. A new method for sharing of harmonic compensation effort is presented. Moreover, a selective virtual impedance scheme is proposed to improve load sharing among the microgrid DGs. The control system design is discussed in detail. Simulation results show that the SLB voltage quality is enhanced significantly by using the proposed compensation method while the load current is shared properly.

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TABLE IV
VOLTAGE WAVEFORMS AT DIFFERENT SIMULATION STEPS

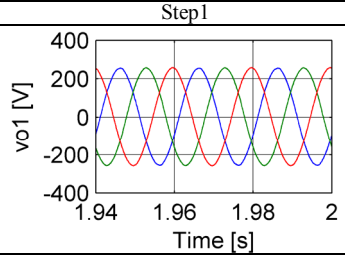
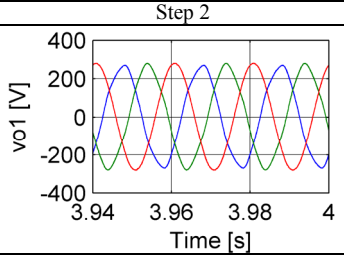
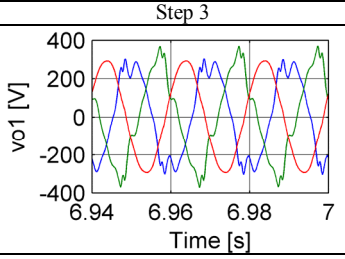
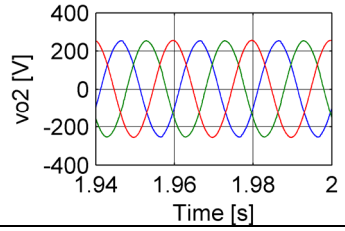
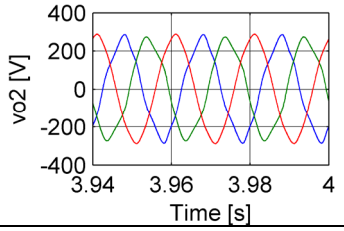
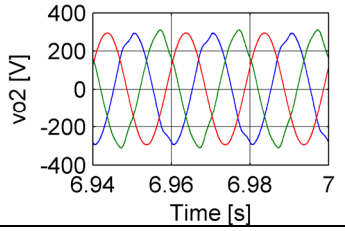
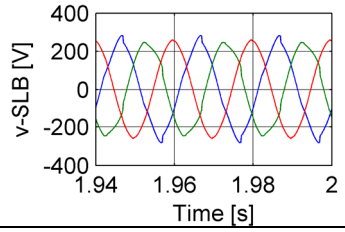
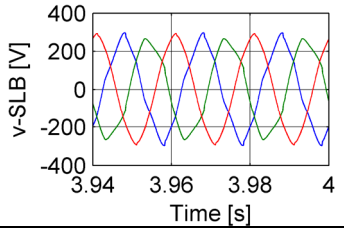
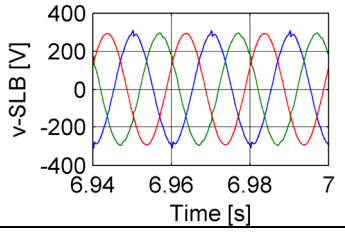
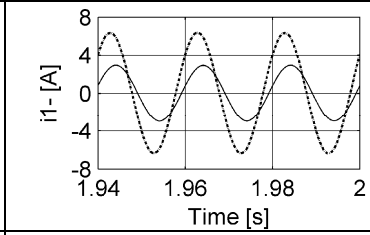
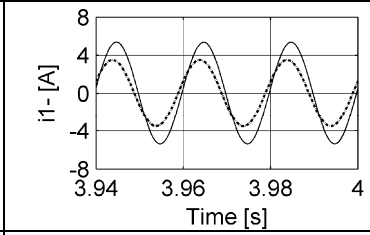
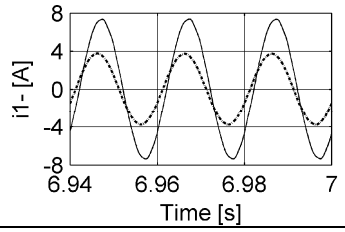
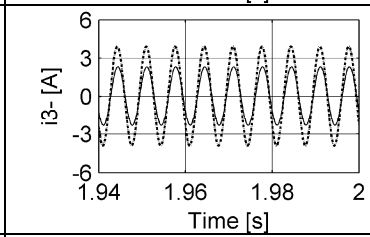
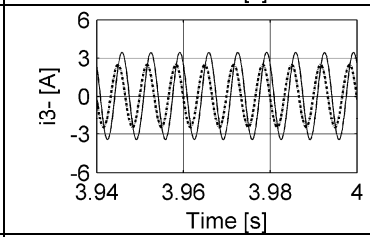
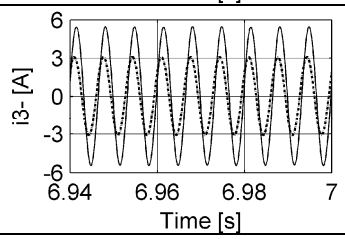
	Step1	Step 2	Step 3
SB_1			
SB_2			
SLB			

TABLE V
DGS OUTPUT CURRENT WAVEFORMS AT DIFFERENT SIMULATION STEPS

	Step1	Step 2	Step 3
fundamental negative sequence (DG1: solid DG2: dashed)			
3rd harmonic negative sequence (DG1: solid DG2: dashed)			
total output current (DG1: solid DG2: dashed)