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Morten Rahr Nielsen, Mathias Kirkeby, Hongbo Zhao, Jannick Kjær Jørgensen,
Michael Møller Bech, and Stig Munk-Nielsen
DEPARTMENT OF ENERGY / AALBORG UNIVERSITY
Pontoppidanstræde 111, Aalborg, Denmark
E-mail: mrni@energy.aau.dk

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***Index Terms*—Silicon Carbide (SiC), MOSFET, Wide bandgap, Medium voltage, Dead time, Compensation.**

***Abstract*—This paper highlights the increased importance of volt-second compensating converter nonlinearities such as dead time for wide bandgap semiconductor devices utilized in medium voltage converters. The increasing voltage level of medium voltage converters impose a penalty to the volt-second compensation required to compensate for the voltage error caused by dead time. A thorough analysis and experimental results of switching events are utilized to present the required volt-second compensation for a 10 kV silicon-carbide MOSFET power module.**

I. INTRODUCTION

The silicon-carbide (SiC) market of semiconductor devices is prospected to exceed $6 billion by 2027 and the major actors in the SiC market invest billions of dollars to expand their market share. The silicon (Si) technology is still the most dominant in today's semiconductor market with more than 90% market share, however, the SiC technology is prospected to increase from 5% in 2021 to 20% in 2027 [1], [2]. The SiC semiconductor market is dominated by a few major actors [3] with some of the most predominant being Wolfspeed, Infineon Technologies, STMicroelectronics, and onsemi, which achieved a combined yearly revenue of almost $1 billion in 2021 on SiC semiconductor devices. Further, they all reached a year-to-year growth of 40% or more from 2020 to 2021 in their SiC revenue [2]. Their portfolios include SiC MOSFETs of up to 1.7 kV, however, SiC MOSFETs with rated voltages above 1.7 kV have started to become commercially available.

The automotive market of electric vehicles, including hybrid-electric vehicles and plug-in hybrid-electric vehicles, has been one of the strongest markets during the last several years due to the green transition and the increased political and economical interest [2], [4]. Of the previously mentioned yearly revenue of almost $1 billion in 2021 among the four major actors, the automotive sector alone accounted for an impressive 63% of the revenue [2]. This has led to a rapid expansion of available 1.2 and 1.7 kV SiC MOSFETs to support the increased demand from the automotive market.

The SiC technology presents many well-known advantages compared to their Si-counterpart [5], [6] with one of these being their ability to withstand higher electric field strengths, which exploits the opportunity to manufacture MOSFETs with increased breakdown voltage. With the current trend of increasing the voltage to lower the conversion and transmission losses, the utilization of wide bandgap (WBG) semiconductor devices is unavoidable.

A common low-level control strategy to avoid shoot-through of the DC-link is to apply a dead time (also known as blanking time) between the switching events of the low-side (LS) and the high-side (HS) semiconductor devices of the half-bridge, however, this comes with the penalty of distorting the voltage and current. Dead time has been known for several decades and is well described in the literature for low voltage (LV) converters [7]–[11], however, no research has been presented pertaining the emerging medium voltage (MV) converters utilizing SiC MOSFETs with voltage ratings above 3.3 kV. The increasing voltage level inevitably penalizes the voltage error caused by dead time, which needs to be compensated to achieve accurate controlability of voltage and

current. With the voltage error being proportional to the DC-link voltage, the implications of compensating the voltage error when increasing the DC-link voltage needs to be investigated. These implications have not been studied in the existing literature, which leaves a potential research gap. Therefore, this paper tries to close this research gap by revisiting the well-known theory behind dead time from a WBG perspective together with a thorough analysis of the voltage transients during turn-on and turn-off switching events of the MOSFET. The theory is followed by experimental measurements on a 10 kV SiC MOSFET half-bridge power module utilizing a modified double-pulse test (DPT) setup to be able to determine the required volt-second compensation to compensate for the error introduced by the converter non-linearities.

II. Revisiting Dead Time - A WBG Perspective

The analysis of dead time is based on the half-bridge configuration with MOSFETs as shown in Fig. 1. The HS and the LS gate signals are shown in green and blue, respectively. The half-bridge consists of a HS and a LS semiconductor device, which are ideally being controlled in complementary. However, due to finite switching speeds of the semiconductor devices, a dead time period, t_d, is implemented between the turn-off and the subsequent turn-on of the complementary as shown in Fig. 2. The dead time period is implemented to avoid a shoot-through of the DC-link and cross-conduction currents [8], [9], but it will inevitably introduce a voltage error compared to the commanded output voltage of the half-bridge. From the literature [7], the voltage error is derived for ideal voltage transients of the semiconductor devices as in (1) and Fig. 2.

$$\Delta V = \begin{cases} +t_\mathrm{d} \cdot f_\mathrm{sw} \cdot V_\mathrm{DC}, & i_\mathrm{out} > 0 \\ -t_\mathrm{d} \cdot f_\mathrm{sw} \cdot V_\mathrm{DC}, & i_\mathrm{out} < 0 \end{cases} \tag{1}$$

where ΔV is the voltage error, t_d is the dead time, f_sw is the switching frequency, V_DC is the DC-link voltage, and i_out is the output current of the half-bridge. This derivation from ideal voltage transients can be seen to constitute a constant term with its sign changing based on the polarity of the current.

The voltage error caused by dead time is the predominant converter non-linearity as it has the most distinct impact on the shape of the output current of the half-bridge. In case the dead time voltage error is not being compensated, the output current will be distorted with increased harmonic components. Other converter non-linearities worth mentioning are the finite voltage drop

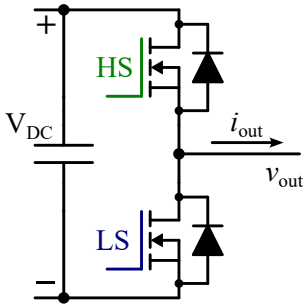


Fig. 1: The half-bridge configuration.

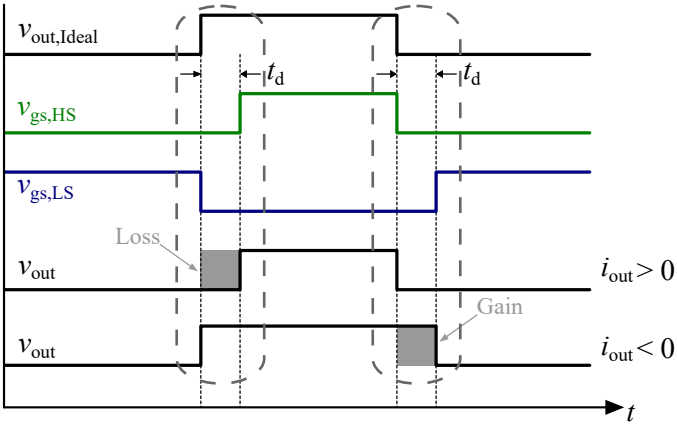


Fig. 2: Impact of dead time on the output voltage of the half-bridge [7].

across the semiconductor device and the device parasitics of the power module [8].

The device parasitics, which need to be charged or discharged during a switching event, make the voltage transients non-ideal by limiting the rate of change in the output voltage (dv/dt) [12], which gives the semiconductor devices their finite switching speeds. The finite switching speeds of the semiconductor devices give rise to finite switching times defined as the period in which the drain-source voltage increases or decreases across the semiconductor device. With reference to Fig. 2 and the assumption of a negative output current, the turn-on switching event of a HS MOSFET achieves what is commonly known as soft switching or zero voltage switching (ZVS), however, the subsequent turn-on switching event of a LS MOSFET is being switched at the full DC-link voltage, commonly known as hard switching. The soft switching of the HS MOSFET and the hard switching of the LS MOSFET are illustrated in black in Fig. 3. However, the finite switching times of the semiconductor devices are also known to be dependent on the magnitude of the output current [8], [12] with the

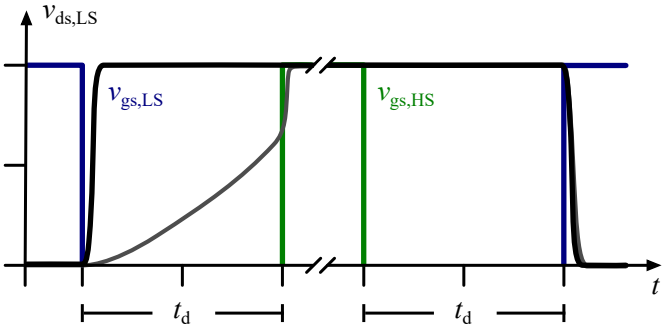


Fig. 3: Illustration of the transient behavior of the drain-source voltage during switching events at a negative output current. The black line represents a high output current and the gray line represents a low output current.

dependency being non-linear and inversely proportional. Therefore, in case of a low negative output current, the finite switching time of the LS MOSFET may exceed the dead time due to a low dv/dt in the output voltage [12], which results in the HS MOSFET being turned on at some voltage known as partial hard switching [13]. The partial hard switching of the HS MOSFET is illustrated in gray in Fig. 3. The opposite applies to a positive output current where the LS MOSFET experiences either soft or partial hard switching and the HS MOSFET experiences only hard switching. This evidently impacts the voltage that needs to be compensated, and therefore, a thorough analysis of the MOSFET voltage transient during switching events is given in Section III.

However, the voltage error caused by dead time is not only proportional to the DC-link voltage but also the switching frequency as shown in (1). Therefore, with the utilization of SiC MOSFETs, the DC-link voltage and switching frequency are both expected to be increased with several factors compared to Si IGBTs, which evidently increases the magnitude of the voltage that needs to be compensated with multiple factors.

III. MOSFET Voltage Transient

The voltage transient of a MOSFET depends on a variety of factors with the main factors being the I/V characteristic of the MOSFET, its gate driving circuitry, and the parasitic device capacitances of the MOSFET and the circuitry in which it is deployed. This analysis has its main focus on the necessary charging and discharging of the parasitic device capacitances and the resulting internal displacement current paths during a switching event. As it has been shown in Section II, the voltage transient during a turn-on and turn-off switching event of a MOSFET differs significantly as it depends on the polarity and the magnitude of the output current.

The analysis of the MOSFET switching characteristics considers the turn-on and turn-off switching event of the LS MOSFET of the half-bridge shown in Fig. 1. The analysis assumes a negative output current, however, the same theory applies to the HS MOSFET for a positive output current. Throughout the analysis, the output current is assumed to be constant during the complete switching event.

A. Turn-on Switching Event of LS MOSFET

The analysis of the turn-on switching event assumes a negative output current, and with both MOSFETs initially turned off, the total output current is being conducted through the HS diode, hence the LS MOSFET has the full DC-link voltage across it. The voltage across the HS MOSFET needs to increase while it simultaneously decreases across the LS MOSFET during the turn-on switching event of the LS MOSFET. The switching time is highly dependent on the parasitic device capacitances as these need to be charged or discharged, which gives rise to internal displacement currents as shown in Fig. 4. All of the displacement currents are sourced through the channel of the LS MOSFET or the gate driving circuitry, hence the charging and discharging of parasitic device capacitances are independent of the output current.

B. Turn-off Switching Event of LS MOSFET

The turn-off switching event of the LS MOSFET is very different compared to the turn-on switching event of the LS MOSFET as the current needed to charge or discharge the parasitic device capacitances depends on the magnitude of the output current of the half-bridge. The analysis of the turn-off switching event also assumes a negative output current, and with the HS MOSFET initially turned off and the LS MOSFET initially turned on, the total output current is being conducted through the LS MOSFET, hence the HS MOSFET has the full DC-link voltage across it. The internal displacement currents during a turn-off switching event of the LS MOSFET are as shown in Fig. 5. Here, it can be seen that all of the displacement currents, except the current needed to discharge the gate-source capacitance of the LS MOSFET, are depending on the output current, hence the charging and discharging of parasitic device capacitances are highly dependent on the magnitude of the output current. Thus, at lower magnitudes of output currents, the charging and discharging process of the capacitances extends, which results in a lower dv/dt of the output voltage as explained in Section II.

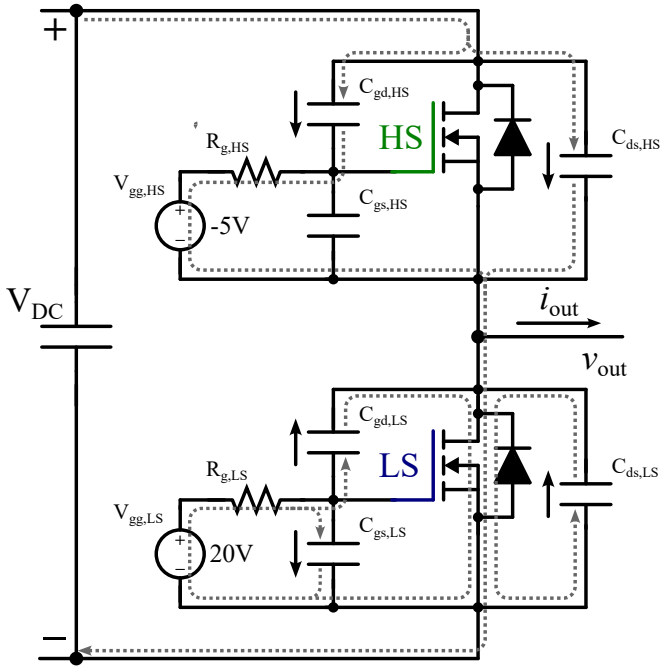


Fig. 4: Internal displacement current paths during a turn-on switching event of the LS MOSFET.

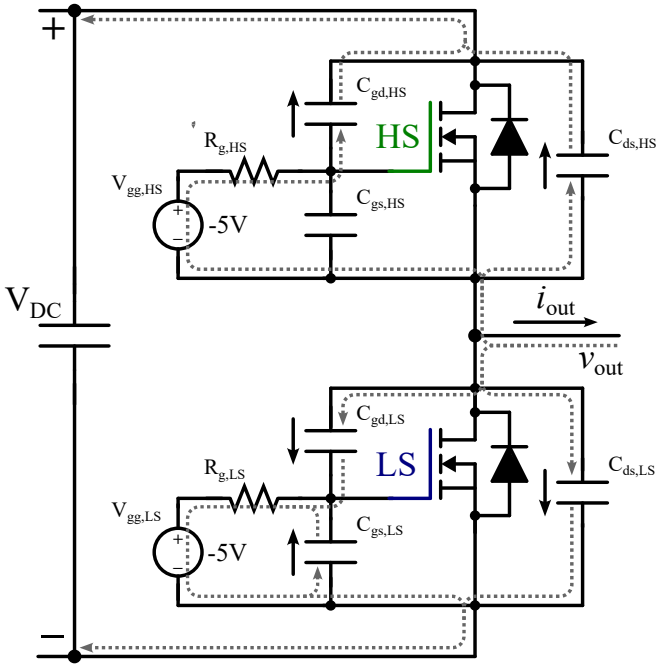


Fig. 5: Internal displacement current paths during a turn-off switching event of the LS MOSFET.

In the case where the charging and discharging process exceeds the dead time, the turn-on of the HS MOSFET causes the voltage to change rapidly as the HS MOSFET experiences a partial hard switching, which allows the displacement currents to be sourced through the channel of the HS MOSFET.

IV. Modified Double-Pulse Test

The above-described turn-on and turn-off voltage transients of the MOSFET cannot be replicated using a DPT setup, where the HS of the half-bridge only consists of a passive diode and an uncontrolled MOSFET. The voltage transients can be shown during continuous operation of a single- or three-phase configuration, however, a simple modification of the standard DPT setup by controlling the HS MOSFET to achieve a half-bridge configuration allows for replicating the voltage transients. The modified DPT setup is shown in Fig. 6 with the respective gate-source voltages indicated.

To perform the experimental DPT, a power module with engineering samples of 10 kV, 20 A, 350 mΩ SiC MOSFET dies from Wolfspeed/Cree [14] and a custom made gate driving circuitry is available [15]. The gate driver operates at -5/+20 V and applies a dead time of 2 μs. Further, a MV inductor designed with an inductance of 28.5 mH and a relatively low parasitic capacitance of 50 pF from terminal to terminal is utilized [16]. However, to perform the DPT in simulations, a detailed LTspice model of the 10 kV SiC MOSFET and its power module, including internal parasitic device capacitances and inductances, is utilized.

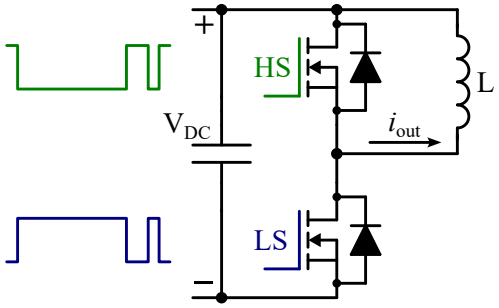


Fig. 6: Schematic of modified double-pulse test setup.

A. LTspice Simulation Model

A model of the modified DPT setup has been made in LTspice to investigate the turn-on and turn-off switching events of the MOSFET in simulations. The LTspice model includes the detailed LTspice model of the 10 kV SiC MOSFET, the power module, and all the relevant device parasitics of the circuitry in which it is applied, including the busbars, the heatsink, the inductor, the current/voltage probes as well as the gate resistors. A schematic of the modified DPT setup from LTspice is shown in Fig. 7.

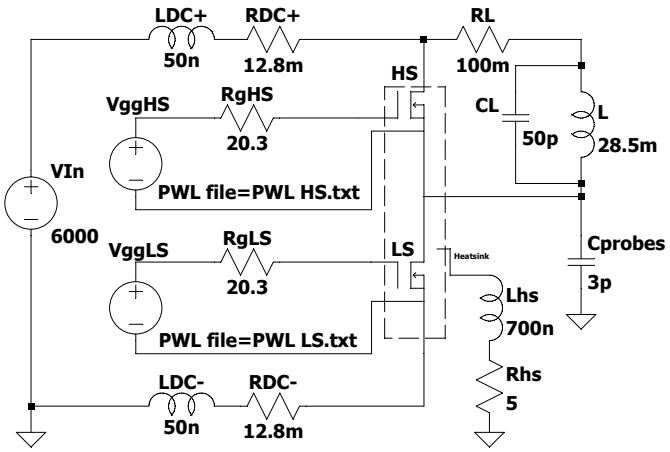


Fig. 7: Schematic of the LTspice simulation model.

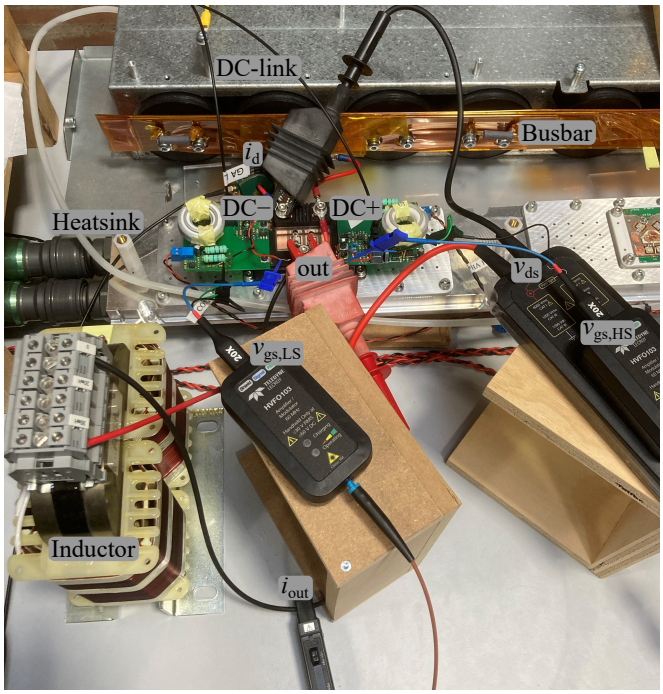


Fig. 8: Photograph of experimental double-pulse test.

B. Experimental Setup

The experimental validation is performed in an experimental DPT setup as the one shown in Fig. 8. The current and voltage measurements are captured on a LeCroy WaveRunner 8058HD oscilloscope with the measuring equipment listed in Table I.

V. Results

The experimental results for the turn-on and turn-off switching events of the LS MOSFET are presented throughout this section. According to the presented theory in Section II and III, it is highly relevant to compare the voltage transient at low and high magnitudes of output currents, and therefore, results at -1 and -8 A are presented. Similar measurements of the voltage transient has been captured for several magnitudes of output currents to illustrate the non-linear relation between the voltage error caused by dead time and the magnitude of the output current. At last, this section presents the required volt-second compensation as a function of the output current for this particular 10 kV SiC MOSFET power module.

TABLE I: List of measuring equipment.

Measurement equipment		
Probe	***Measurement***	
LeCroy HVD3605A	Drain-source voltage	v_{ds}
LeCroy HVFO103-x20	Gate-source voltage	v_{gs}
Pearson CT 2878	Drain current	i_d
LeCroy CP030	Output current	i_{out}

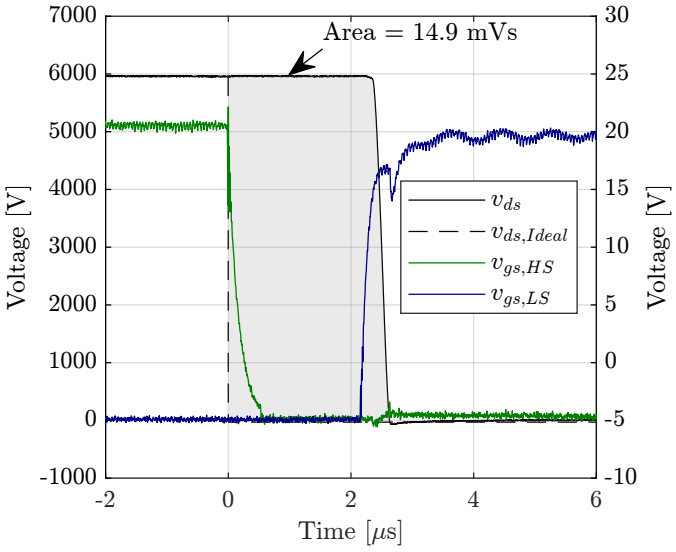
In this section, the required compensation is referred to as volt-second compensation for two reasons: 1) the measured voltage error is not only accounting for the voltage error caused by dead time, but also the other converter non-linearities introduced in Section II and 2) the volt-second compensation is more general, which makes the required compensation independent of switching frequency.

A. Turn-on Switching Event of LS MOSFET

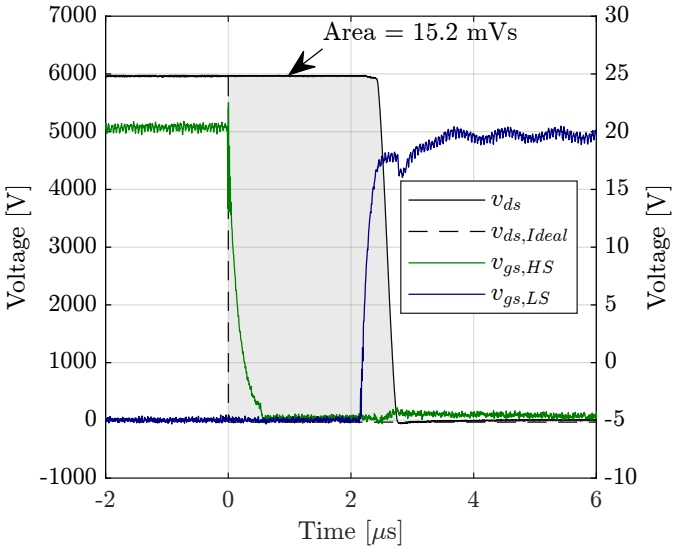
The turn-on switching event of the LS MOSFET at an output current of -1 and -8 A are shown in Fig. 9, whereas the turn-on switching event of the LS MOSFET for several magnitudes of output current is shown in Fig. 10. These results emphasize the independence between the switching time and the magnitude of the output current as the voltage transients are approximately equal. Only a slight increase in the switching time can be seen in the zoomed view.

B. Turn-off Switching Event of LS MOSFET

The turn-off switching event of the LS MOSFET at an output current of -1 and -8 A are shown in Fig. 11, whereas the turn-off switching event of the LS MOSFET for several magnitudes of output current is shown in Fig. 12. These results emphasize the dependence between the switching time and the magnitude of the output current as the switching time reduces significantly with increased magnitudes of output current.



(a)



(b)

Fig. 9: Experimental measurement results for turn-on switching events of the LS MOSFET at an output current of (a) -1 A and (b) -8 A.

C. Volt-Second Compensation

The required volt-second compensation can be estimated by comparing the ideal drain-source voltages with the measured drain-source voltages presented in Fig. 9 and 11. However, in a more sophisticated way, the volt-second gain during a turn-on switching event of the LS MOSFET and the volt-second loss during a turn-off switching event of the LS MOSFET can be calculated as the difference in area between the ideal and measured drain-source voltages. In the case of a negative output current, the constant volt-second gain, which can

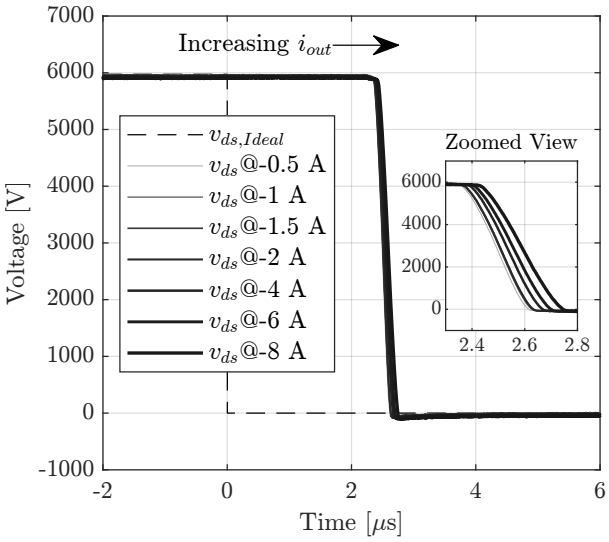
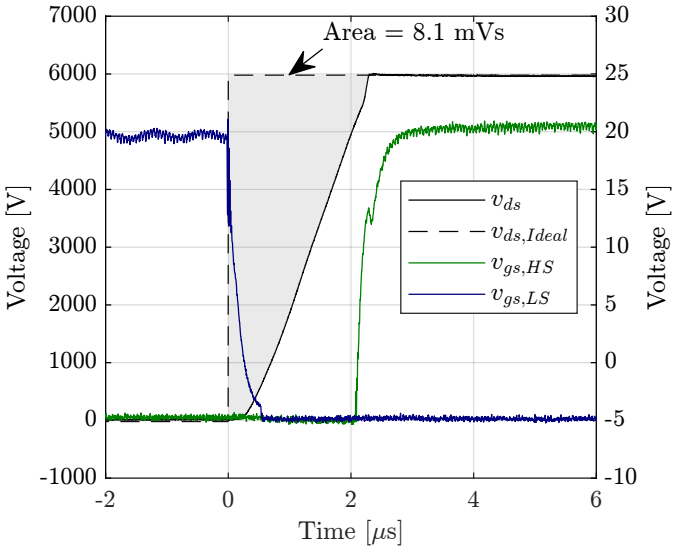


Fig. 10: Experimental measurement results for turn-on switching events of the LS MOSFET for several magnitudes of output current.

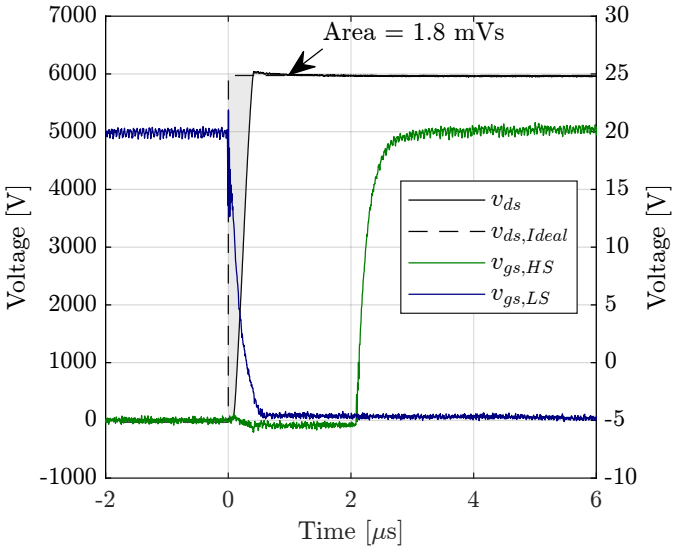
be estimated with (1) by leaving out the switching frequency, is compensated by the increased volt-second loss at lower magnitudes of output currents, which therefore reduces the required volt-second compensation around low magnitudes of output currents as shown in Fig. 13. As in the case of an output current of -1 A, the volt-second gain has been calculated to be 14.9 mVs as shown in Fig. 9a and the volt-second loss has been calculated to be 8.1 mVs as shown in Fig. 11a, which results in a volt-second error of 6.8 mVs, and therefore, a required volt-second compensation of -6.8 mVs. Likewise, in the case of an output current of -8 A, the volt-second gain has been calculated to be 15.2 mVs as shown in Fig. 9b and the volt-second loss has been calculated to be 1.8 mVs as shown in Fig. 11b, which results in a volt-second error of 13.4 mVs and a required volt-second compensation of -13.4 mVs.

The simulation model in LTspice has been used to simulate the required volt-second compensation while sweeping from negative to positive magnitudes of output current, hence simulated values for the required volt-second compensation are also included in Fig. 13.

Both the measured and simulated values for the required volt-second compensation exceed the ideal volt-second compensation at high magnitudes of output current. The cause of this can be found in the calculation of the ideal volt-second compensation from (1) as it only takes into account the volt-second error caused by dead time and not the volt-second error caused by the other converter non-linearities introduced in Section II.



(a)



(b)

Fig. 11: Experimental measurement results for turn-off switching events of the LS MOSFET at an output current of (a) -1 A and (b) -8 A.

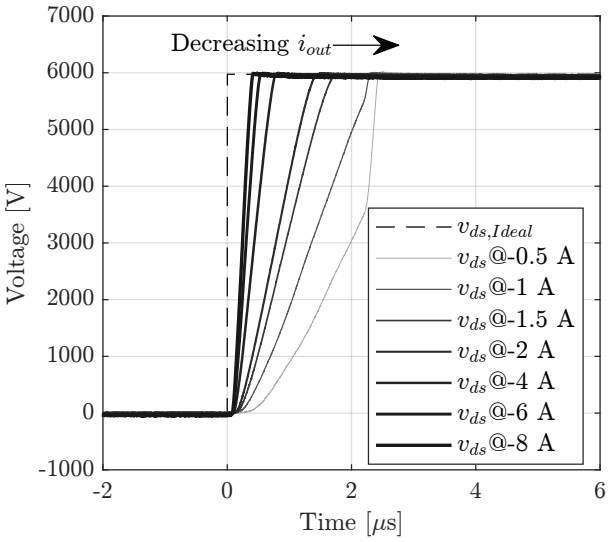


Fig. 12: Experimental measurement results for turn-off switching events of the LS MOSFET for several magnitudes of output current.

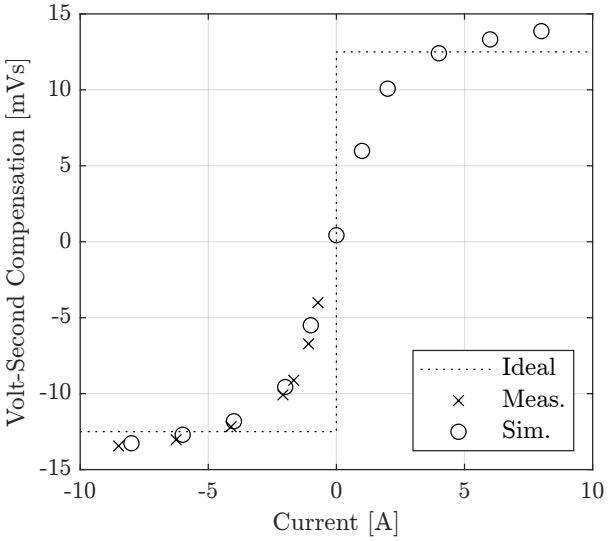


Fig. 13: Required volt-second compensation at 6 kV DC-link voltage and 2 μs dead time for this particular 10 kV SiC MOSFET power module.

VI. Conclusion

The increased importance of compensating converter non-linearities such as dead time for WBG semiconductor devices utilized in MV converters has been highlighted throughout this paper. The well-known theory behind dead time has been revisited from a WBG perspective to quantify the impact of increasing both the DC-link voltage and the switching frequency. Further, a thorough analysis of the voltage transient during turn-on and turn-off switching events of the LS MOSFET is given with the main focus on the necessary charging and discharging of parasitic device capacitances and the resulting internal displacement current paths. A modified DPT setup utilizing a 10 kV SiC MOSFET half-bridge power module has been used to present experimental results for switching events performed at a DC-link voltage of 6 kV with 2 μs dead time. The experimental results together with simulation results are used to present the required volt-second compensation as a function of the magnitude of the output current for this particular 10 kV SiC MOSFET power module.

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