Supporting Development of Energy-Optimised Java Real-Time Systems using TetaSARTS

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Motivation
It is well-known, that the traditional Java run-time is unsuited for use in embedded real-time systems, which is attributed issues such as the lack of high-resolution real-time clocks and timers, insufficient thread semantics, and, most notably, memory management, which is traditionally handled by a garbage collector whose execution is highly unpredictable. However, with emerging standards such as the Real-Time Specification for Java (RTSJ) and the Safety Critical Java (SCJ) profile, these issues have been accounted for, thereby achieving a significant step towards use in embedded real-time systems development.

Having a suitable programming model as introduced by e.g. SCJ and RTSJ is not the only component in making Java a viable technological alternative and competitor to C in the embedded real-time systems domain. Equally important is the complementation of tools and analyses that support the development, and for verification purposes. For real-time systems, the latter comprises functional correctness, but also temporal correctness, which is the focus of this work.

Contributions

TetaSARTS

Fig. 3: TetaSARTS. Fig. 4: Resulting NTA. TetaSARTS is a fully automated tool for conducting timing analyses of SCJ Java Bytecode programs taking into account the execution environment (see Fig. 3 for an overview). It accommodates hardware implementations of the JVM, and traditional execution environments with a software implementation of the JVM including the hosting hardware. It supports both periodic and sporadic real-time tasks, and from these, it generates Timed Automata simulating their control flow. The structure of the model and the communication between the Timed Automata using synchronisation actions is shown in Fig. 4. The analyses are performed using the UPPAAL model checker.

Results

We base the results on analysing two representa- tive examples of real-time systems written in Java: the Real-Time Sorting Machine (RTSM) and the Minepump control system. The systems have been evaluated on the Java Optimized Processor (JOP), and an execution environment consisting of the Hardware Virtual Machine (HVM) on an AVR ATmega2560 microcontroller. The results have been obtained on a system with an Intel Core i7-2620M @ 2.70GHz and 8 GB of memory. The results are shown in Table 1, 2, and 3.

<table>
<thead>
<tr>
<th>System</th>
<th>Clock Freq</th>
<th>Idle</th>
<th>Utilisation</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTSM</td>
<td>100 MHz</td>
<td>4.0 ms</td>
<td>48.5 μs (1.2%)</td>
</tr>
<tr>
<td>RTSM</td>
<td>60 MHz</td>
<td>4.0 ms</td>
<td>80.8 μs (2.0%)</td>
</tr>
<tr>
<td>Minip.</td>
<td>100 MHz</td>
<td>2.0 ms</td>
<td>25.9 μs (1.3%)</td>
</tr>
<tr>
<td>Minip.</td>
<td>10 MHz</td>
<td>11.8 ms</td>
<td>259.0 μs (2.1%)</td>
</tr>
</tbody>
</table>

Table 1: Schedulability of the Minepump when varying the clock frequency.

Future Work
Support other Analyses The Timed Automata model can be used for analysing other interesting properties e.g. worst case blocking time.

Statistical Model Checking[2] Can be used for analysing systems for which probabilistic guarantees of temporal correctness are sufficient. The technique can be used to avoid exhaustive exploration of the state-space of the model.


Case Studies We want to further evaluate the applicability of TetaSARTS by using more complex real-time systems, and possibly other variations of the execution environment.

References